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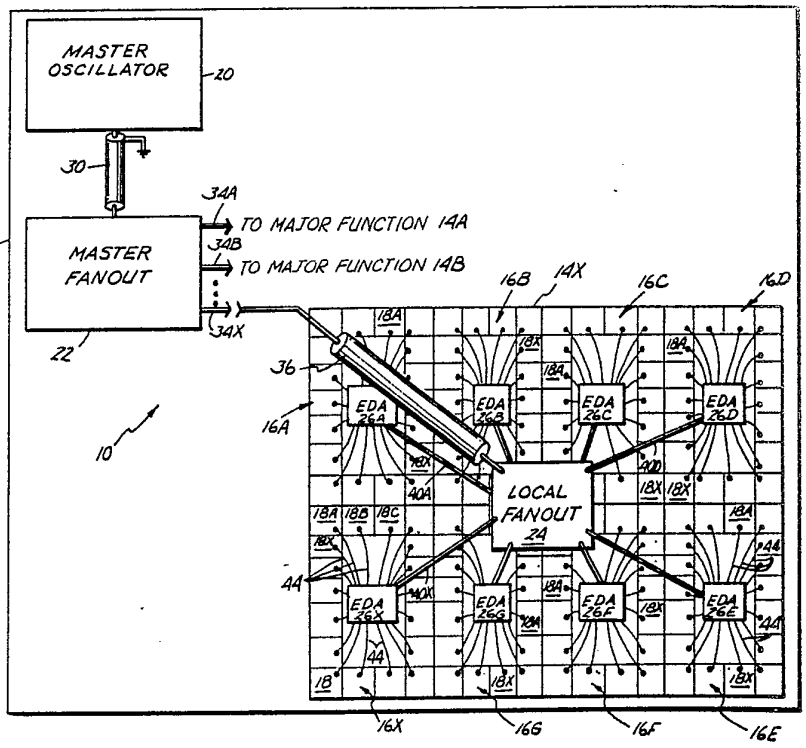
(54) Title: ELECTRONIC CLOCK TUNING SYSTEM

(57) Abstract

An electronic clock tuning system for a digital computer of the type including a plurality of major function circuit boards comprised of a plurality of gate arrays (18 A-X). A clock pulse train is produced by a master oscillator (20), and distributed to each major function circuit board (14 A-X) by a master fanout (22). The clock pulse train is distributed throughout each major function circuit board by a local fanout (24). Each major function circuit board (14 A-X) includes a plurality of electronic delay arrays (26 A-X), each of which distributes the clock pulse train to a group of gate arrays (18 A-X) on the major function board (14 A-X), and delays the clock pulse train supplied to each gate array by one of a plurality of discrete delay periods. Each electronic delay array (26 A-X) includes shift registers for serially receiving digital delay tuning codes and for producing digital delay select signals representative of discrete delay periods. Delay circuits on each electronic delay array are responsibe to one of the shift registers, and delay the clock pulse trains supplied to the gate arrays by discrete delay periods represented by the digital delay select signals.



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ELECTRONIC CLOCK TUNING SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The present invention relates to clock systems used in digital computers. In particular, the present invention is an electronic clock tuning system for tuning the delay of clock pulses distributed throughout the computer.

2. Description of the Prior Art.

Modern digital computers are formed by hundreds of thousands and even millions of logic elements. In computer architectures which are highly integrated, these logic elements are fabricated on very large-scale integrated (VLSI) circuit chips known as gate arrays. The gate arrays themselves are organized onto a plurality of major function circuit boards which are dedicated to the performance of specific tasks. A supercomputer, for example, can include a central processing unit (CPU), memory interface, and input/output (I/O) major function circuit boards. Each of these circuit boards will typically be formed by hundreds of gate arrays.

In order to achieve a high data throughput, operations are distributed throughout the computer, and performed in "parallel." Processed data and microinstructions are communicated between individual gate arrays, and between major function circuit boards. It is extremely important, therefore, that all microinstructions and data transfers executed by the gate arrays be synchronized with those of other gate arrays. To this end, the computer includes a central clock system for driving and or "clocking" operations performed by all gate arrays.

The clock system will include a master oscillator which is the source of clock signals for all gate arrays. A clock pulse train produced by the master oscillator is divided, and replicas thereof distributed to each major function circuit board by a master fanout circuit. On each major function circuit board the clock pulse train is further divided, and distributed to each gate array through a local fanout circuit. Each gate array is, therefore, clocked by a replica of the pulse train produced by the master oscillator. While this technique helps maintain synchronization between gate arrays, it is inadequate for the high degree of performance demanded of modern supercomputers.

Even minute discrepancies between the phases of the clock pulse trains arriving at different gate arrays can have disastrous consequences on computer operation. These discrepancies, or skews, are the product of numerous factors. Variables such as operating temperature, supply voltage, component tolerance variables due to manufacturing processes, and differing path lengths between master oscillator and gate arrays, all contribute to skew between the clock pulse trains. Adding to the problem is the fact that many of these factors cannot be accurately controlled.

Obviously, the higher the frequency of the clock pulse train, the faster the computer can process data. Frequency of the clock pulse train, however, is limited by the uncertainty, or maximum skew, introduced between clock pulse trains supplied to various gate arrays. Simply put, computer performance can be greatly increased by reducing

skews introduced by the clock system.

Currently used techniques for tuning computer clock systems are primarily manual. A technician will measure the time delay in the distribution path between the master oscillator and each and every gate array. A length of coaxial cable in each path is then removed, trimmed, and reinserted. This procedure is repeated until the delay in the clock pulse train at each gate array is within predetermined tolerances. This procedure is obviously very labor intensive. It must be performed for each and every one of the hundreds of gate arrays on the computer. On a supercomputer, this procedure can take several weeks.

There is clearly a continuing need for improved apparatus for tuning clock systems in digital computers. An electronic clock tuning system would be especially desirable. Electronic test equipment could then be used to tune the clock pulse train supplied to each gate array. Computer "setup" time could be greatly reduced by the elimination of tedious and labor intensive tasks. An electronic clock tuning system of this type could also be extremely accurate, and significantly increase computer performance by permitting gate arrays to be clocked at frequencies approaching their specified maximums. The system should, of course, also be relatively simple and inexpensive.

SUMMARY OF THE INVENTION

The present invention is an electronic clock tuning system for delaying a clock pulse train by one of a plurality of discrete delay periods. The electronic clock tuning system includes means for

producing digital delay select signals representative of the discrete delay periods, and means responsive thereto for delaying the clock pulse train by discrete delay periods represented by the delay select signals. Use of this system permits clock pulse trains distributed to individual gate arrays throughout a computer to be tuned so as to have identical phases or skews. This task can be quickly performed by electronic test equipment, thereby significantly reducing computer setup time and expense. The extremely high degree of accuracy obtainable through use of the system permits all gate arrays to be clocked at frequencies approaching the upper limits of their specifications, and still be accurately synchronized with all other gate arrays within the computer. As a result, the clock tuning system is an important contribution to the performance required for demanding supercomputer applications.

In a preferred embodiment, the means for producing the digital delay select signals includes a coarse delay register and a fine delay register. The coarse delay register is adapted to receive coarse delay tuning codes, and produces coarse delay select signals representative of one of a plurality of discrete coarse delay periods. The fine delay register is adapted to receive fine delay tuning codes, and produces fine delay select signals representative of one of a plurality of discrete fine delay periods.

The means for delaying the clock pulse train by discrete delay periods includes a fine delay circuit, and a coarse delay circuit. The coarse

delay circuit is responsive to the coarse delay register, and includes a plurality of first delay elements having an input connected to receive the clock pulse train, and an output. Each coarse delay element is adapted to delay the clock pulse train by one of the plurality of discrete coarse delay periods. The coarse delay circuit also includes a multiplexer which has signal inputs connected to the outputs of the first delay elements to receive the delayed clock pulse trains, a signal output, and a control input responsive to the coarse delay register. The multiplexer supplies to its signal output one of the delayed clock pulse trains, as represented by the coarse delay select signal.

The fine delay circuit is connected to receive the coarse delayed clock pulse train from the multiplexer, and further delays the clock pulse train by one of a plurality of fine delay periods. The fine delay circuit includes a transmission line to which a plurality of binary weighted loads are switchably interconnected by transmission gates. The transmission gates are responsive to the fine delay register, and the fine delay circuit further delays the clock pulse train by one of a plurality of fine delay periods, as represented by the fine delay select signals.

In one preferred embodiment, the coarse delay register is a four bit shift register, and the coarse delay circuit means introduce one of sixteen coarse delay periods which are integer multiples of five hundred picoseconds. The fine delay shift register is also a four bit shift register, and fine delay circuit means further delays the clock pulse

train by one of sixteen fine delay periods which are interger multiples of one hundred picoseconds. Clock pulse trains can thereby be tuned to an accuracy of one hundred picoseconds.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram representation of a computer which includes the electronic clock tuning system of the present invention.

Figure 2 is a block diagram representation of the electronic clock tuning system shown in Figure 1.

Figure 3 is a block diagram representation of an electronic delay array (EDA) shown in Figures 1 and 2.

Figure 4 is a schematic representation of a fine delay circuit element shown in Figure 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A computer 12 which includes electronic clock tuning system 10 of the present invention is illustrated in block diagram form in Figure 1. Computer 12 is highly integrated, and formed by a plurality of major function circuit boards 14A-14X (only 14X is illustrated). Major function circuit boards 14 are subsystems of computer 12, and are dedicated to performing specific operations. In one embodiment, computer 12 is a high speed supercomputer, which includes a central processing unit board, a shared memory interface board, and an input/output interface board.

Each major function circuit board 14 is organized into a plurality of smaller functional units or regions 16A-16X. In one embodiment (not shown), major function boards 14 can include up to

sixteen regions 16. Each region 16 is in turn formed by a plurality of very large-scale integrated (VLSI) circuit elements or gate arrays 18A-18X. Gate arrays 18A-18X can also be characterized as subsystem components of major function boards 14A-14X. Logic elements which perform digital operations are fabricated onto gate arrays 18 during manufacture.

Clock tuning system 10, as shown in Figures 1 and 2, includes master oscillator 20, master fanout circuit 22, a local fanout circuit 24 on each major function board 14, and a plurality of electronic delay arrays (EDA) 26A-26X, one of which is associated with each region 16 of major function board 14. As shown in Figures 2 and 3, a plurality of first or coarse delay elements 56A-56X are associated with each EDA 26A-26X. Delay elements 56A-56X are not shown in Figure 1 for reasons of clarity.

Operation of clock tuning system 10 is perhaps best illustrated with reference to Figure 2. Master oscillator 20 produces a source clock pulse train 28 which is supplied to master fanout circuitry 22 by a transmission line such as coaxial cable 30. As shown, clock pulse train 28 is comprised of a plurality of rectangular pulses which switch between first and second logic states (e.g. logic "0" and logic "1" states) at a master frequency.

Master fanout circuit 22 is connected to receive clock pulse train 28, and produces a plurality of major function clock pulse trains 32A-32X. Clock pulse trains 32A-32X are replicas of clock pulse train 28, and are distributed to one of major function boards 14A-14X on transmission lines

34A-34X, respectively.

On each major function board 14, (board 14X, for example, as shown in Figures 1 and 2) major function clock pulse train (32X in this example) is supplied to a local fanout circuit 24 by a transmission line such as coaxial cable 36. Local fanout circuit 24 divides clock pulse train 32 and produces a plurality of EDA clock pulse trains 38A-38X. EDA clock pulse trains 38A-38X are supplied to electronic delay arrays 26A-26X by transmission lines 40A-40X, respectively, as shown.

From each EDA 26A-26X, the EDA clock pulse train 38 is again divided, and a plurality of tuned clock pulse trains 42A-42X are produced. Each tuned clock pulse train 42A-42X is a replica of EDA clock pulse train 38, and, therefore, source clock pulse train 28. A tuned clock pulse train 42A-42X is supplied to each gate array 18A-18X, respectively, of each region 16A-16X by a transmission line 44.

Having been propagated to the respective gate arrays 18 through transmission lines 30, 34, 36, 40, and 44, fanout circuits 22 and 24, and electronic delay arrays 26A-26X, clock pulse trains 42A-42X will have been delayed due to various factors. Different delays will have been introduced to different clock pulse trains 42A-42X. As a result, some of tuned clock pulse trains 42A-42X will be out of phase, or skewed, with respect to others. Clock pulse trains 42B and 42X, for example, as illustrated in Figure 2, have arrived at gate arrays 18B and 18X, respectively, with no phase difference or skew. As illustrated, their rising edges R and trailing edges T occur at identical times. Clock pulse train 42A,

however, has arrived at gate array 18A with a different delay than that of clock pulse trains 42B and 42X. As shown, rising edges R of clock pulse train 42A are skewed with respect to those of clock pulse trains 42B and 42X by a period S. As a result, the operations being performed by gate array 18A will not be synchronized with those performed by gate arrays 18B and 18X.

Through the use of electronic delay arrays 26A-26X, gate array clock pulse trains 42A-42X can all be electronically tuned so as to have identical delays when they arrive at a test point on their respective gate array 18A-18X. Clock pulse trains 42A-42X will, therefore, have identical phases, and no skew S. In this manner, all microinstruction executions and data transfers of gate arrays 18 can be synchronized with those of all other gate arrays 18. Computer 12 can, therefore, operate at higher speeds, and achieve higher performance levels.

A preferred embodiment of electronic delay array 26A (which is typical of EDA's 26A-26X) is illustrated in Figure 3. Electronic delay array 26A has an input terminal 50 connected to receive an EDA clock pulse train 38A from local fanout circuit 24. EDA 26A includes an EDA fanout 51 which is connected to input terminal 50. EDA fanout 51 divides, and produces a plurality of replicas of EDA clock pulse train 38A, for distribution to delay elements 56A-56X through terminals 53A-53X. Digital tuning codes, preferably in serial format, are received by EDA 26A on tuning code input terminal 52. Tuned gate array clock pulse trains 42A-42X are supplied to gate arrays 18A-18X through pins 54A-54X, respectively.

Associated with EDA 26A are a plurality of discrete delay elements 56A-56X. Delay elements 56A-56X are preferably external to EDA 26A. Each delay element 56A-56X, respectively, has an input terminal 55A-55X connected to terminals 53A-53X, respectively, of EDA fanout 51, and an output terminal 57A-57X. Each delay element 56A-56X delays EDA clock pulse train 38A by one of a plurality of first, or coarse, delay periods. In one preferred embodiment, EDA 26A includes sixteen delay elements 56A-56X, each of which delays the EDA clock pulse train 38A by an integer multiple of five hundred picoseconds. Delay element 56A, for example, delays the received clock pulse train by five hundred picoseconds, while delay element 56B delays the received clock pulse train by one thousand picoseconds, and so on. Although delay elements 56A-56X can take other forms, in one preferred embodiment they are different lengths of printed circuit delay line which closely approximate the desired coarse delay periods.

EDA 26A also includes coarse delay multiplexers 58A-58X, first or coarse delay (C.D.) shift registers 60A-60X, second or fine delay circuits 62A-62X, and second or fine delay (F.D.) shift registers 64A-64X. Together, each coarse delay multiplexer 58A-58X and delay elements 56A-56X form a coarse delay circuit. Each coarse delay multiplexer 58A-58X, coarse delay shift register 60A-60X, fine delay circuit 62A-62X, and fine delay shift register 64A-64X is associated with one of gate arrays 18A-18X for which EDA 26X produces a tuned clock pulse train

42A-42X, respectively.

Coarse and fine delay shift registers 60A-60X and 64A-64X, respectively, are preferably all connected in a series arrangement for the serial transfer of delay tuning codes received on tuning code input pin 52. In the embodiment shown, all shift registers 60A-60X and 64A-64X are four bit shift registers. Coarse delay shift registers 60A-60X serially receive, and store, coarse delay tuning codes, and produce a four bit coarse delay select signal representative of one of sixteen discrete coarse delay periods on busses 61A-61X, respectively. Similarly, each fine delay shift register 64A-64X serially receives, and stores, a fine delay tuning code representative of one of sixteen discrete fine delay periods, and produces four bit fine delay select signals representative thereof on busses 65A-65X, respectively.

In the embodiment shown, each coarse delay multiplexer 58A-58X is a sixteen input multiplexer, and has input terminals A-X connected to output terminals 57A-57X of delay elements 56A-56X, respectively. Each coarse delay multiplexer 58A-58X also has a four bit control terminal connected to bus 61A-61X, respectively, to receive the four bit coarse delay select signal from its respective coarse delay shift register 60A-60X. In response to the particular coarse delay select signal received at its control terminal, coarse delay multiplexers 58A-58X will supply to their output terminal 70 one of the sixteen coarse delayed clock pulse trains from signal input terminals A-X. In this manner, each coarse delay multiplexer 58A-58X delays EDA clock pulse

train 38A by one of sixteen discrete coarse delay periods.

Fine delay circuit elements 62A-62X have input terminals 67A-67X, respectively, connected to receive the coarse delayed EDA clock pulse train from coarse delay multiplexers 58A-58X, respectively, and an output terminal 63A-63X. A four bit control terminal of each fine delay circuit element 62A-62X is connected to bus 65A-65X, respectively, to receive the four bit fine delay select signal from its respective fine delay shift register 64A-64X. In response to the fine delay select signal, fine delay circuit elements 62A-62X further delay the coarse delayed EDA clock pulse train by one of sixteen discrete fine delay periods. These further delayed EDA clock pulse trains are output pins 54A-54X, respectively, as tuned clock pulse trains 42A-42X.

A preferred embodiment of fine delay circuit element 62A (which is typical of elements 62A-62X) is illustrated in Figure 4. Input terminal 67A and output terminal 63A are interconnected by a transmission line 72 which includes a plurality of inverters 74A-74H connected in a series arrangement. Four load elements 76A-76D are adapted to be interconnected to transmission line 72 by electronic transmission gates 78A-78D, respectively. Each transmission gate 78A-78D has a first terminal A connected to transmission line 72, a second terminal B connected to its respective load element 76A-76D, and a control terminal C connected to one of control terminal pins 79A-79D. Control terminal C of each transmission gate 78A-78D, therefore, receives from bus 65A one bit of the fine delay select signal

produced by the fine delay shift register 64A to which it is attached. Each load element 76A-76D is connected between a power supply potential (not shown), ground 80, and terminal B of its respective transmission gate 78A-78D.

Although schematically represented as switches in Figure 4, transmission gates 78A-78D are electronic transmission gates fabricated on EDA 26A. When a first (e.g. a logic "0" state) signal is received at their control terminals C, transmission gates 78A-78D are in their OPEN conduction state, electrically disconnecting load elements 76A-76D from transmission line 72. When the particular bit of a fine delay select signal has a second (e.g. a logic "1") state, the corresponding transmission gate 78A-78D will be in a CLOSED conduction state, and electrically connect its load element 76A-76D to transmission line 72. When one of load elements 76A-76D is connected to transmission line 72, it loads transmission line 72 and thereby further delays propagation of the EDA clock pulse train therethrough.

In a preferred embodiment, load elements 76A-76D are formed by MOS transistors in a manner well known to those skilled in the art. Load elements 76A-76B are also binary weighted so that one of sixteen discrete fine delay periods can be added to the clock pulse train. Gate load 76A preferably has a binary weight of eight, and will further delay the clock pulse train by eight hundred picoseconds when interconnected to transmission line 72 by transmission gate 78A. Gate load 76B has a binary weight of four, and will delay the clock pulse train by four hundred picoseconds. Gate load 76C has a

binary weight of two, and will further delay the clock pulse train by two hundred picoseconds. Gate load 76D has a binary weight of one, and will further delay the clock pulse train by one hundred picoseconds when interconnected to transmission line 72 by transmission gate 78D. The fine delay select signals produced by fine delay shift registers 64 can, therefore, digitally represent one of sixteen fine delay periods, each of which is an integer multiple of one hundred picoseconds.

A preferred method of using clock tuning system 10 is illustrated in Figure 2. Gate arrays 18A-18X preferably include a built-in self-test system having a test data output pin 80A-80X, respectively, from which a copy of the tuned clock pulse train can be monitored. Since the clock pulse train is propagated through portions of gate arrays 18A-18X, delays dependent upon the particular fabrication batch can be compensated for. Electronic test instrument 82 is used to measure the delay introduced to the clock pulse train between master oscillator 20 and test data output pin 80A-80X of each gate array 18A-18X. Delay tuning code generator 84 then produces tuning codes which are applied to tuning code input pin 52 so as to tune the tuned clock pulse train 42 until a predetermined time delay is established. In this manner, all gate arrays 18A-18X of all major functions 14 can be tuned so as to have identically delayed clock pulse trains 42. This procedure can be automated, and quickly performed.

Although the present invention has been described with reference to preferred embodiments,

those skilled in the art will recognize that changes may be made in form and detail without departing from the spirit and scope of the invention.

WHAT IS CLAIMED IS:

1. An electronic clock tuning system for delaying a clock pulse train by one of a plurality of discrete delay periods, comprising:

means for producing digital delay select signals representative of discrete delay periods; and

means responsive to the means for producing the digital delay select signals for delaying the clock pulse train by discrete delay periods represented by the delay select signals.

2. The electronic clock tuning system of claim 1 wherein:

the means for producing the digital delay select signals includes first select means for receiving first digital delay tuning codes and for producing first digital delay select signals representative of discrete first delay periods; and

the means for delaying the clock pulse train includes first delay circuit means responsive to the first select means for delaying the clock pulse train by the discrete first delay periods represented by the first digital delay select signals.

3. The electronic clock tuning system of claim 2 wherein the first select means includes shift register means for serially receiving first digital delay tuning codes and for producing first digital delay select signals.

4. The electronic clock tuning system of claim 2 wherein the first delay circuit means includes:

a plurality of first delay elements having an input connected to receive the clock pulse train, and an output, each delay element adapted to delay the clock pulse train by one of the discrete first delay periods; and

multiplexer means having signal inputs connected to the output of one of the delay elements to receive delayed clock pulse trains, a signal output, and control inputs responsive to the first select means, the multiplexer means supplying to its signal output delayed clock pulse trains represented by the first delay select signals.

5. The electronic clock tuning system of claim 2 wherein:

the means for producing the digital delay select signals further includes second select means for receiving second digital delay tuning codes and for producing

second digital delay select signals representative of discrete second delay periods; and

the means for delaying the clock pulse train further includes second delay circuit means responsive to the first delay circuit means and the second select means for further delaying the clock pulse train by the discrete second delay periods represented by the second digital delay select signals.

6. The electronic clock tuning system of claim 5 wherein the second select means includes shift register means for serially receiving second digital delay tuning codes and for producing second digital delay select signals.

7. The electronic clock tuning system of claim 5 wherein the second delay circuit means includes:

input means responsive to the first delay circuit means for receiving the delayed clock pulse train;

output means for outputting the further delayed clock pulse train from the second delay circuit means;

transmission line means for transmitting the delayed clock pulse train between the input means and the output means;

a plurality of load means for loading the transmission line means and thereby further delaying the clock pulse train by the discrete second delay periods; and

a plurality of transmission gate means, each transmission gate means responsive to the second select means for switchably interconnecting one of the load means to the transmission line means in response to the second digital delay select signals.

8. The electronic clock tuning system of claim 5 wherein:

the first select means is adapted to receive coarse delay tuning codes and to produce coarse delay select signals representative of one of a plurality of discrete coarse delay periods;

the first delay circuit means is a coarse delay circuit for delaying the clock pulse train by the discrete coarse delay periods represented by the coarse delay select signals;

the second select means is adapted to receive fine delay tuning codes and to produce fine delay select signals representative of one of a plurality of discrete fine delay periods;

the second delay circuit means is a fine delay circuit for further delaying the clock pulse train by the discrete fine delay periods represented by the fine delay select signals; and

the discrete coarse delay periods are greater periods than the discrete fine delay periods.

9. The electronic clock tuning system of claim 8 wherein:

the coarse delay circuit introduces one of sixteen coarse delay periods which are multiples of a five hundred picosecond period;

the fine delay circuit introduces one of sixteen fine delay periods which are multiples of a one hundred picosecond period.

10. The electronic clock tuning system of claim 2 wherein the first delay circuit means includes:

input means responsive to the first delay circuit means for receiving the delayed clock pulse train;

output means for outputting the further delayed clock pulse train from the first delay circuit means;

transmission line means for transmitting the delayed clock pulse train between the input means and the output means;

a plurality of load means for loading the transmission line means and thereby further delaying the clock pulse train by the discrete first delay periods; and

a plurality of transmission gate means, each transmission gate means responsive to the first select means for switchably interconnecting one of the load means to the transmission line means in response to the first digital delay select signals.

11. An electronic clock tuning system for a digital computer of the type having plurality of major functions formed by a plurality of subsystem components, including:

master oscillator means for producing a clock pulse train;

master fanout means operatively connected to the master oscillator means for distributing the clock pulse train to each major function;

local fanout means associated with each major function operatively connected to the master fanout means for distributing the clock pulse train throughout the major function; and

a plurality of electronic delay means associated with each major function operatively conected to the local fanout means for

distributing the clock pulse train to each of a group of subsystem components on the major function, and for delaying the clock pulse train supplied to each subsystem component by one of a plurality of discrete delay periods, each electronic delay means comprising:

select means for receiving digital delay tuning codes and for producing digital delay select signals representative of discrete delay periods; and

delay means responsive to the select means for delaying the clock pulse trains supplied to the subsystem components by discrete delay periods represented by the digital delay select signals.

12. The electronic clock tuning system of claim 11 wherein:

the select means of each electronic delay means includes:

a plurality of select means for receiving digital delay tuning codes and for producing digital delay select signals representative of discrete delay periods; and

the delay means of each electronic delay means includes:

electronic delay fanout means operatively connected to the local fanout means for further distributing the clock pulse train;

a plurality of delay elements having an input connected to receive a clock pulse train from the electronic delay fanout means, and an output, each delay element adapted to delay the received clock pulse train by one of the delay periods; and

a plurality of multiplexer means each having signal inputs connected to the output of one of the delay elements, a signal output, and control inputs responsive to one of the select means, each multiplexer means supplying to its signal output a delayed clock pulse train represented by the delay select signal.

13. The electronic clock tuning system of claim 12 wherein the select means include shift register means for serially receiving digital delay tuning codes and for producing digital delay select signals.

14. The electronic clock tuning system of claim 13 wherein the electronic delay fanout means, the shift register means, and the multiplexer means are fabricated on an electronic delay array.

15. The electronic clock tuning system of claim 13 wherein:

each of the shift register means is a four bit shift register which receives a four bit digital delay tuning code and produces a four bit digital delay select signal representative of one of sixteen discrete delay periods;

each electronic delay means includes sixteen delay elements, each delaying the clock pulse train by a different delay period; and

each of the multiplexer means is a sixteen input multiplexer.

16. The electronic clock tuning system of claim 15 wherein each of the sixteen delay periods is a multiple of a five hundred picosecond period.

17. The electronic clock tuning system of claim 11 wherein:

the select means of each electronic delay means includes:

a plurality of select means for receiving digital delay tuning codes and for producing digital delay select signals representative of discrete delay periods; and

the delay means includes a plurality of delay circuit means for delaying the clock pulse trains, each including:

input means operatively connected to the local fanout means to receive the clock pulse train;

output means for outputting the delayed clock pulse train from the delay circuit means;

transmission line means for transmitting the delayed clock pulse train between the input means and the output means;

a plurality of load means for loading the transmission line means and thereby delaying the clock pulse train by the discrete delay periods; and

a plurality of transmission gate means, each transmission gate means responsive to the select means for switchably interconnecting one of the load means to the transmission line means in response to the digital delay select signals.

18. The electronic clock tuning system of claim 17 wherein the select means include shift register means for serially receiving digital delay tuning codes and for producing digital delay select signals.

19. The electronic clock tuning system of claim 18 wherein the shift register means and the delay circuit means are fabricated on an electronic delay array.

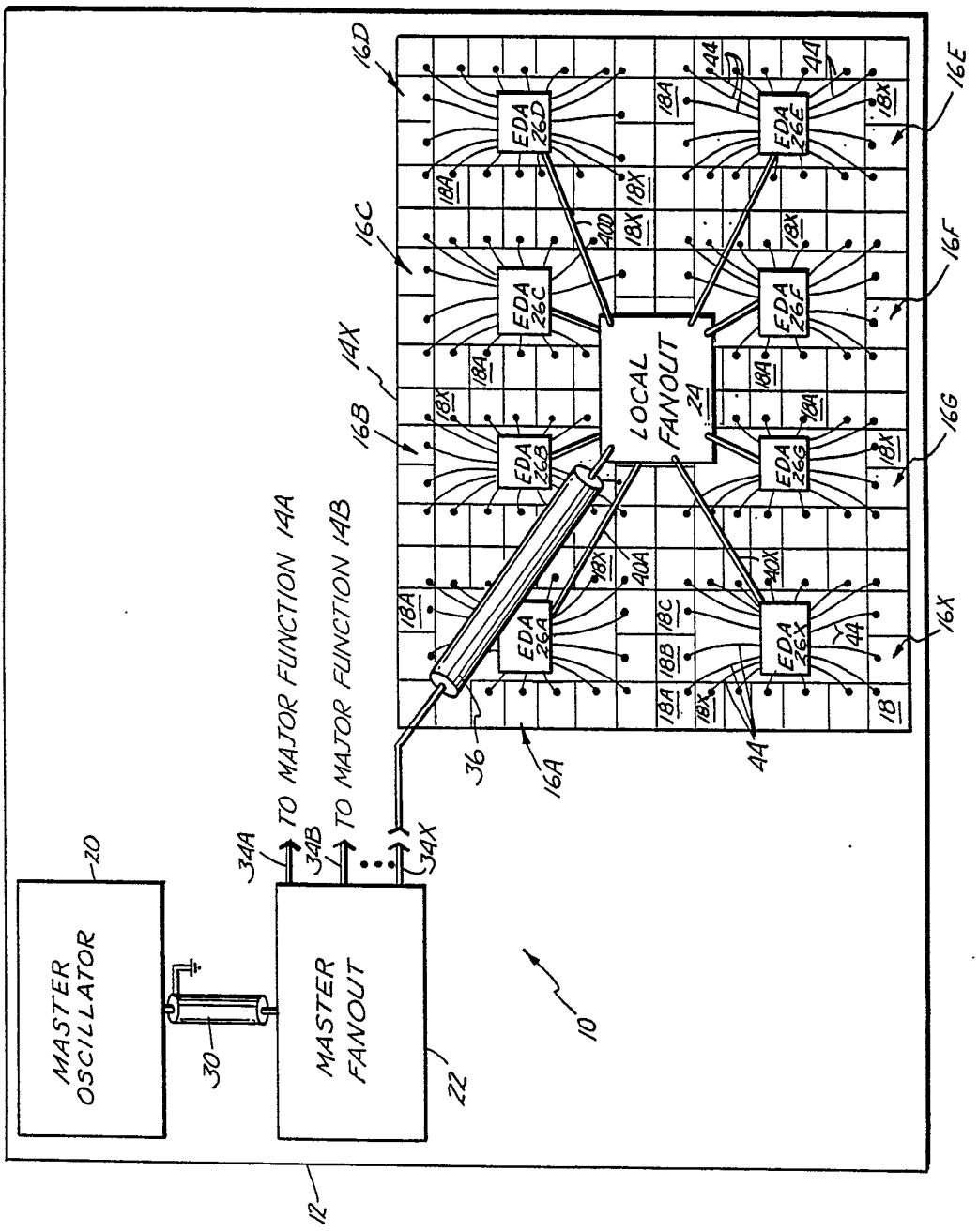
20. The electronic clock tuning system of claim 18 wherein the four load means of each delay circuit means are binary weighted.

21. The electronic clock tuning system of claim 18 wherein:

each of the shift register means is a a four bit shift register which receives a four bit digital delay tuning code and produces a four bit digital delay select signal representative of one of sixteen discrete delay periods;

each of the delay circuit means includes four transmission gate means and four load means, each load means switchably interconnected to the transmission line means by a transmission gate means, wherein each delay circuit means delays the clock pulse train by one of sixteen different delay periods.

22. The electronic clock tuning system of claim 21 wherein each of the sixteen delay periods is a multiple of a one hundred picosecond period.


MASTER OSCILLATOR
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40A
40X
44

Fig. 1

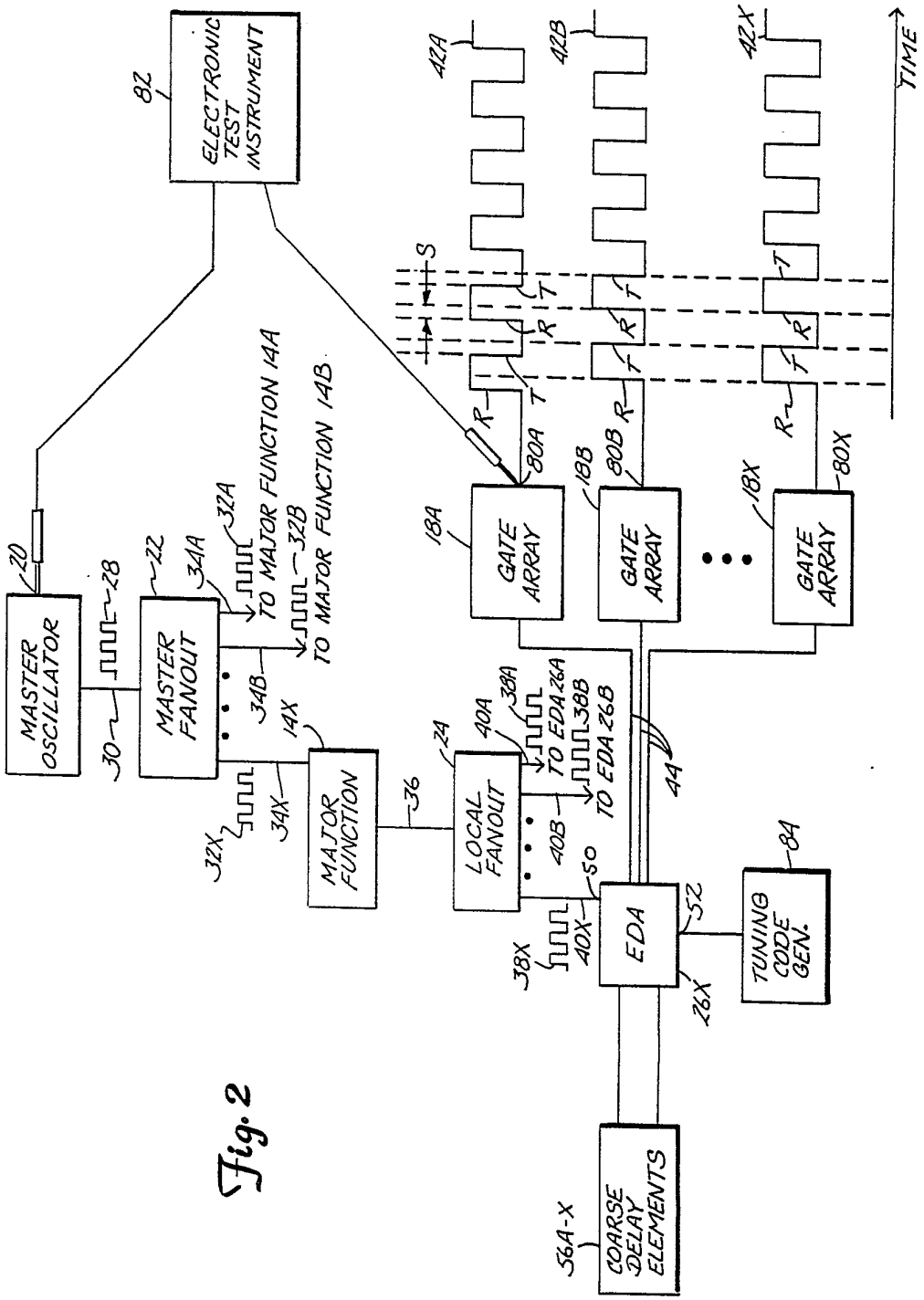
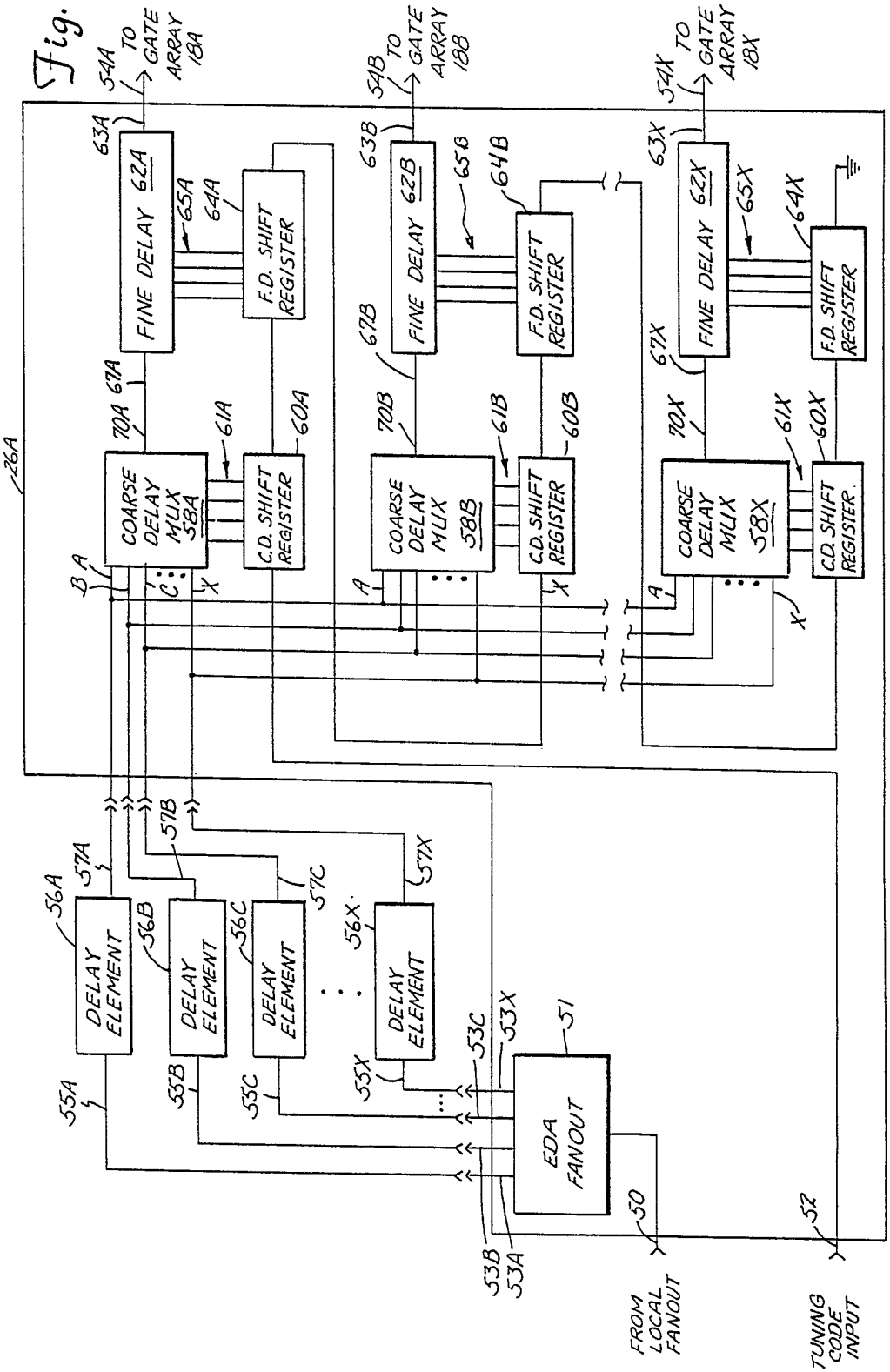

ELECTRONIC TEST INSTRUMENT
82
MASTER OSCILLATOR
20
28
30
MASTER FANOUT
22
34A
34B
34X
32A
32B
32X
TO MAJOR FUNCTION 14A
TO MAJOR FUNCTION 14B
MAJOR FUNCTION
14X
36
LOCAL FANOUT
24
40A
40B
40X
38A
38B
38X
TO EDA 26A
TO EDA 26B
44
50
EDA
52
26X
TUNING CODE GEN.
84
COARSE DELAY ELEMENTS
56A-X
GATE ARRAY
18A
18B
18X
80A
80B
80X
42A
42B
42X
R
T
S
TIME

Fig. 2

Fig. 3


26A
54A TO GATE ARRAY 18A
54B TO GATE ARRAY 18B
54X TO GATE ARRAY 18X
63A
63B
63X
FINE DELAY 62A
FINE DELAY 62B
FINE DELAY 62X
65A
65B
65X
64A
64B
64X
F.D. SHIFT REGISTER
67A
67B
67X
70A
70B
70X
61A
61B
61X
60A
60B
60X
COARSE DELAY MUX 58A
COARSE DELAY MUX 58B
COARSE DELAY MUX 58X
C.D. SHIFT REGISTER
B A
C
X
A
57A
57B
57C
57X
56A
56B
56C
56X
DELAY ELEMENT
55A
55B
55C
55X
53A
53B
53C
53X
EDA FANOUT
51
50
52
FROM LOCAL FANOUT
TUNING CODE INPUT

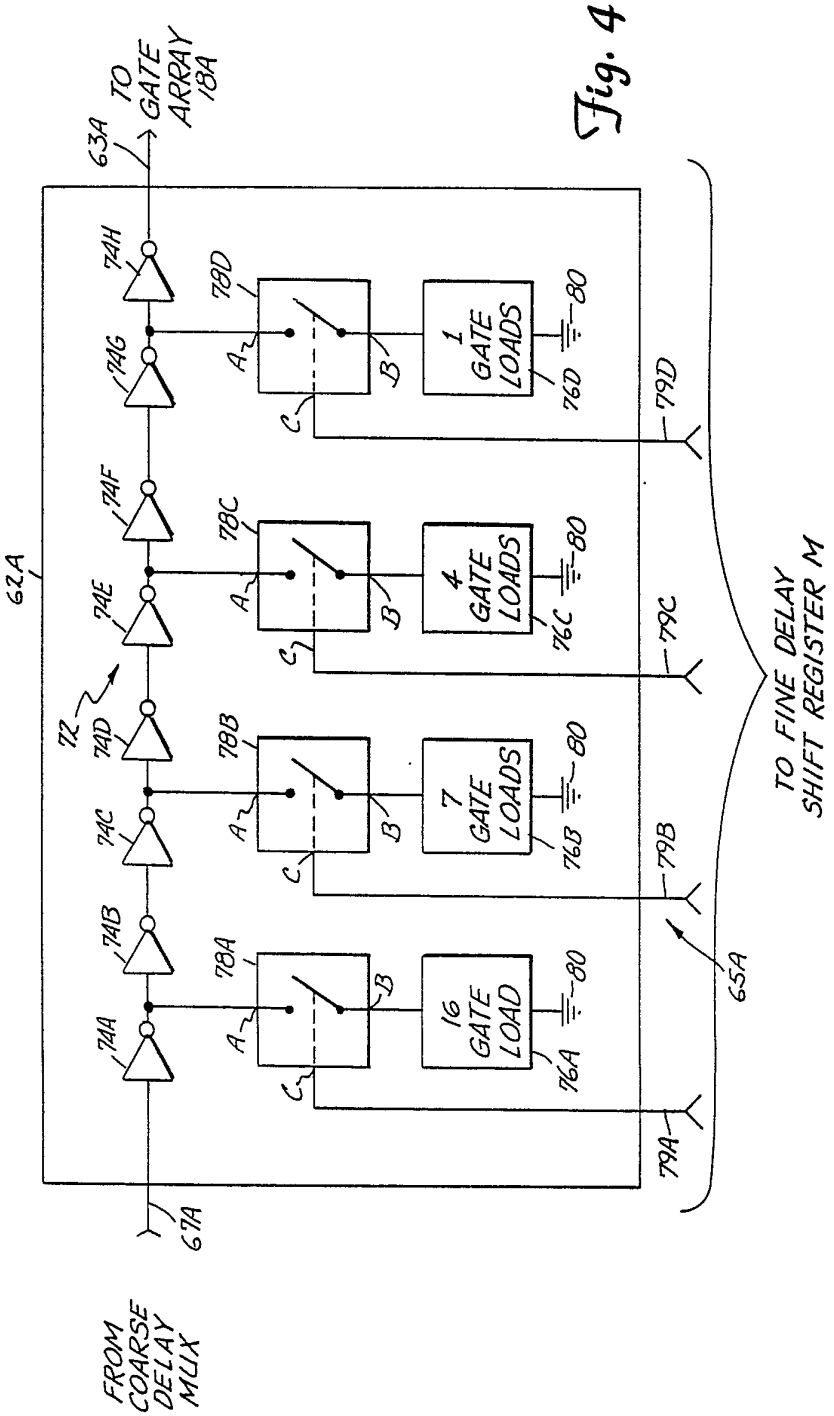

FROM COARSE DELAY MUX
67A
62A
63A
TO GATE ARRAY 18A
72
74A
74B
74C
74D
74E
74F
74G
74H
78A
78B
78C
78D
16 GATE LOAD
7 GATE LOADS
4 GATE LOADS
1 GATE LOADS
76A
76B
76C
76D
80
79A
79B
79C
79D
65A
TO FINE DELAY SHIFT REGISTER M

Fig. 4

INTERNATIONAL SEARCH REPORT

International Application No PCT/US86/02761

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) 3

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[4] H03K 5/13; H04L 7/00
US CL 340/825.200

II. FIELDS SEARCHED

Minimum Documentation Searched 4

Classification System	Classification Symbols
U.S.	340/825.200, 825.610; 307/269, 582, 590, 595, 602, 603, 606, 480; 375/106, 107; 328/55, 63, 72, 155; 370/108

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched 5

III. DOCUMENTS CONSIDERED TO BE RELEVANT 14

Category *	Citation of Document, 16 with indication, where appropriate, of the relevant passages 17	Relevant to Claim No. 18
X, P Y	U.S. A 4626716 (MIKI) 02 December 1986 See Abstract, Figure 3, col. 1 and col. 3, lines 1-30	1-4, 5-8, 10 9; 11-22
X, P Y	US. A 4623805 (Flora et al) 18 November 1986 See Abstract, Figure 4, col. 2 lines 3-30, col. 3, lines 1-45	1-4, 5-8, 10 9; 11-22
X Y	US. A 4503490 (Thompson) 05 March 1985 See Abstract, Figs 1; 7, col. 1, lines 23-54 col. 5, lines 25-58	1-4 9; 11-2
A	U.S. A 4514647 (Shoji) 30 April 1985	
A	U.S. A 4482819 (Oza, et al) 13 November 1984	
A	U.S. A 4488297 (Vaid) 11 December 1984	
A	U.S. A 3675049 (Haven) 04 July 1972	

* Special categories of cited documents: 15

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search 2	Date of Mailing of this International Search Report 2
24 February 1987	06 MAR 1987
International Searching Authority 1	**Signature of Authorized Officer 20**
ISA/US	Donald J. Yusko

Form PCT/ISA/210 (second sheet) (May 1986)