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(54) **Title:** SCRATCH FILTER FOR WAFER INSPECTION

(57) **Abstract:** Methods and systems for filtering scratches from wafer inspection results are provided. One method includes generating a defect candidate map that includes image data for potential defect candidates as a function of position on the wafer and removing noise from the defect candidate map to generate a filtered defect candidate map. The method also includes determining one or more characteristics of the potential defect candidates based on portions of the filtered defect candidate map corresponding to the potential defect candidates. In addition, the method includes determining if each of the potential defect candidates are scratches based on the one or more characteristics determined for each of the potential defect candidates and separating the potential defect candidates determined to be the scratches from other defects in inspection results for the wafer.

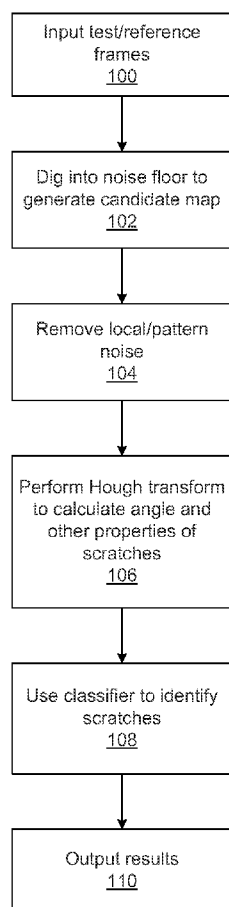


Fig. 1



BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

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## SCRATCH FILTER FOR WAFER INSPECTION

### BACKGROUND OF THE INVENTION

#### 5     1.     Field of the Invention

      This invention generally relates to filtering scratches out of defect detection results of wafer inspection.

#### 10    2.     Description of the Related Art

      The following description and examples are not admitted to be prior art by virtue of their inclusion in this section.

15       Inspection processes are used at various steps during a semiconductor manufacturing process to detect defects on wafers to promote higher yield in the manufacturing process and thus higher profits. Inspection has always been an important part of fabricating semiconductor devices such as ICs. However, as the dimensions of semiconductor devices decrease, inspection becomes even more  
20   important to the successful manufacture of acceptable semiconductor devices because smaller defects can cause the devices to fail.

      Inspection processes generally detect a significant amount of potential defects that are actually nuisance defects on the wafer or noise. Nuisance defects as that  
25   term is generally used in the art can be defined as defects that are detected on the wafer that the user does not care about or events that are detected as defects but are not any kind of actual defects. For instance, in some wafer inspections, defects that are located on layers of the wafer under the layer being inspected can be detected, but those defects on underlying layers may not be of interest for the layer being  
30   inspected. In one such instance, scratches from a chemical mechanical polishing (CMP) layer can appear as optically real defects in inspections of later layers.

However, scratches may not be defects of interest for the layer being inspected.

Therefore, scratches on one layer can cause the nuisance rate of inspection of later layers on a wafer to be higher. As such, detecting such nuisance defects and reporting them as actual defects to a user have a number of disadvantages such as obscuring actual defects that a user cares about and/or affect the device fabrication in a meaningful manner in the inspection results, obstructing process control attempts to correct the actual defects that a user cares about, and causing users to change the wafer inspection process in ways to reduce the detection of nuisance defects that cause fewer defects of interest to be detected.

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Since nuisance defects will be detected by most every inspection process, many inspection processes have been developed in which defect detection is performed and then the detected defects are filtered in some manner to separate defects of interest from nuisance defects. For instance, when there may be previous layer scratches detected in an inspection process, the inspection process may include using size or shape features to filter out relatively large scratches. Such filtering may be effective for some scratches but perhaps not all scratches. For instance, scratches caused by a CMP process include micro-scratches, which can have a substantially faint tail. Regular inspection processes may not detect the relatively faint tail of the micro-scratches. Therefore, only a portion of a micro-scratch having a relatively faint tail can appear in defect detection results thereby causing the micro-scratch to appear to have a shape in an image of the wafer that is different from its actual shape on the wafer. As such, defect filtering that is performed based on the shape of defects may not classify such micro-scratches as scratch defects. Consequently, the wafer inspection results may include a significant number of micro-scratches. In addition, since 60% to 70% of scratches caused by CMP processes can be micro-scratches having relatively faint tails, the wafer inspection results may include a significant percentage of all of the scratches on the wafer.

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Accordingly, it would be advantageous to develop methods and systems for filtering defects detected on wafers that can be used to more effectively reduce the nuisance rate of inspection processes for wafers due to micro-scratches on the wafers.

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### **SUMMARY OF THE INVENTION**

The following description of various embodiments is not to be construed in any way as limiting the subject matter of the appended claims.

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One embodiment relates to a computer-implemented method for filtering scratches from inspection results for a wafer. The method includes generating a defect candidate map for a wafer from images of the wafer generated by a wafer inspection system. The defect candidate map includes image data for potential defect candidates as a function of position on the wafer. The method also includes removing noise from the defect candidate map to generate a filtered defect candidate map. In addition, the method includes determining one or more characteristics of the potential defect candidates based on portions of the filtered defect candidate map corresponding to the potential defect candidates. The method further includes determining if each of the potential defect candidates are scratches based on the one or more characteristics determined for each of the potential defect candidates. The method also includes separating the potential defect candidates determined to be the scratches from other defects in inspection results for the wafer generated by the wafer inspection system. The generating, removing, determining the one or more characteristics, determining if each of the potential defect candidates are scratches, and separating steps are performed by a computer system.

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Each of the steps of the method described above may be performed as described further herein. The method described above may include any other

step(s) of any other method(s) described herein. The method described above may be performed using any of the systems described herein.

Another embodiment relates to a non-transitory computer-readable medium  
5 storing program instructions executable on a computer system for performing a computer-implemented method for filtering scratches from inspection results for a wafer. The computer-implemented method includes the steps of the computer-implemented method described above, which may be performed as described further herein. In addition, the computer-implemented method for which the  
10 program instructions are executable may include any other step(s) of any other method(s) described herein. The non-transitory computer-readable medium may be further configured as described herein.

An additional embodiment relates to a system configured to filter scratches  
15 from inspection results for a wafer. The system includes an optical subsystem configured to direct light to a wafer and detect light from the wafer to thereby generate images for the wafer. The system also includes a computer subsystem configured for performing the generating, removing, determining the one or more characteristics, determining if each of the potential defect candidates are the  
20 scratches, and separating steps described above. The system may be further configured as described herein.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

25 Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Fig. 1 is a flow chart illustrating one embodiment of a computer-implemented  
30 method for filtering scratches from inspection results for a wafer;

**Fig. 2 is a block diagram illustrating one embodiment of a non-transitory computer-readable medium storing program instructions executable on a computer system for performing one or more of the computer-implemented method**  
5 **embodiments described herein; and**

**Fig. 3 is a schematic diagram illustrating a side view of one embodiment of a system configured to filter scratches from inspection results for a wafer.**

10 **While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all**  
15 **modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.**

### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

20 **Turning now to the drawings, it is noted that the figures are not drawn to scale. In particular, the scale of some of the elements of the figures is greatly exaggerated to emphasize characteristics of the elements. It is also noted that the figures are not drawn to the same scale. Elements shown in more than one figure that may be similarly configured have been indicated using the same reference**  
25 **numerals. Unless otherwise noted herein, any of the elements described and shown may include any suitable commercially available elements.**

**One embodiment relates to a computer-implemented method for filtering scratches from inspection results for a wafer. Fig. 1 illustrates one embodiment of**  
30 **such a computer-implemented method. The computer-implemented method may include acquiring the inspection results using the inspection system. For example,**

acquiring the inspection results may include scanning light over the wafer, generating output (e.g., images or image data) responsive to light from the wafer detected by the inspection system during the scanning, detecting defects on the wafer based on the output, and generating the inspection results to include  
5 information about the defects. In this manner, acquiring the inspection results may include scanning the wafer. However, acquiring the inspection results does not necessarily include scanning the wafer. For example, acquiring the inspection results may include acquiring the inspection results from a storage medium in which the inspection results have been stored (e.g., by the inspection system). Acquiring  
10 the inspection results from the storage medium may be performed in any suitable manner, and the storage medium from which the inspection results are acquired may include any of the storage media described herein. Images used in the embodiments described herein may be acquired in similar manners (e.g., by scanning the wafer or from a storage medium in which the images are stored).

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The method includes generating a defect candidate map for a wafer from images of the wafer generated by a wafer inspection system. For example, as shown in step 100 of Fig. 1, the input to the method may include input test/reference (“ref”) frames. The test image frames and the reference image frames may include image  
20 frames for any two dies on the wafer such as two dies that are adjacent to each other on the wafer. However, any other reference and test image frames known in the art may be used in the embodiments described herein (e.g., image frames for cells, fields, etc.). The defect candidate map includes image data for potential defect candidates as a function of position on the wafer. The potential defect candidates  
25 may be detected in the image data generated for the wafer as described further herein. The defect candidate map may have any suitable format. Different defect candidate maps may be generated for different potential defect candidates. For example, each of the defect candidate maps may include a predetermined number of pixels surrounding the location of a detected potential defect candidate.

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In one embodiment, images of the wafer described further herein are generated by the wafer inspection system detecting light from the wafer. The wafer inspection system may be configured as described further herein. In some embodiments, the scratches are caused by a chemical mechanical polishing (CMP) process performed on the wafer. In a further embodiment, the scratches are located under a layer of the wafer for which the inspection results were generated. For example, scratches from a CMP layer usually appear as optically real defects in inspection of later layers formed on a wafer. In other words, the scratches on a layer under the one being inspected can appear in the images of the wafer generated during inspection and can be detected as defects even though they are not located on the layer being inspected. In addition, such scratches are not defects of interest (DOI) for the inspection of those later layers. Therefore, the scratches are nuisance defects (i.e., defects the user does not care about) and, as such, the scratches can increase the nuisance rate of wafer inspection tools. One advantage of the embodiments described herein is that they can better classify scratches and furthermore can filter out scratches without hurting DOI captures.

In one embodiment, generating the defect candidate map includes applying a threshold to the images and determining that portions of the images having values above the threshold are the potential defect candidates. In one such embodiment, the threshold is substantially close to a noise floor in the images. In this manner, as shown in step 102 of Fig. 1, the method may include “digging” into the noise floor to generate a candidate map. The threshold used to generate a candidate map that will be used as described further herein can be lowered into the noise floor level in an attempt to find the faint tail of micro-scratches. “Micro-scratches” as that term is used herein generally refers to scratches caused by CMP processes that have lengths on the order of microns. “Micro-scratches” are also not usually very deep along the entire length of the scratches. In this manner, a “tail” of the scratches may appear substantially faint in images of the wafer compared to the “head” of the scratches. Micro-scratches can also have multiple parts of the tail which are disconnected from

each other but the shape of the outline that connects the multiple parts forms a “scratch line.”

The embodiments described herein can dig into the noise floor trying to find the faint tails of micro-scratches using the threshold described above. Using such a threshold to detect the potential defect candidates is advantageous since 60% to 70% of scratches are micro-scratches with faint tails. Regular inspection will not catch the faint tails of micro-scratches and thus will fail to classify them as scratches (e.g., they would be classified as another type of defect). In some embodiments, a regular inspection can be performed on a wafer with a normal value of a threshold and then only the pixels surrounding defects detected in the regular inspection could be examined using the threshold at or near the noise floor. In this manner, the entire area of the wafer scanned by the wafer inspection system can be inspected for defects, and then only the areas around (e.g., next to or near) the detected defects can be inspected with a threshold near the noise floor in an attempt to see if the defects extend beyond their originally detected pixels. In this manner, previously undetected portions of scratches can be detected with the noise floor level threshold. In another such embodiment, the images of the wafer include gray scale images. In this manner, the candidate map may be formed by thresholding gray scale images.

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The method also includes removing noise from the defect candidate map to generate a filtered defect candidate map. In one embodiment, the noise that is removed from the defect candidate map includes local color noise. In one such embodiment, removing the noise includes applying a local difference filter to the images. In this manner, the local color noise can be mitigated by removing the noise source of local color using a difference filter. “Local color variation” refers to color variation in images or image data for the wafer due to process variations on the wafer. Local color noise in the images may also be filtered as described in U.S. Patent Application Serial No. 14/450,170 by Huang et al. filed August 1, 2014, which is incorporated by reference as if fully set forth herein. In another embodiment, the

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noise that is removed from the defect candidate map includes pattern noise. In one such embodiment, removing the noise includes removing horizontal and vertical pattern noise from the images. In this manner, the pattern noise can be mitigated by removing horizontal and vertical pattern residues. For example, filtering the

5 pattern noise may include suppressing horizontal pattern noise by removing relatively long lines. In addition, the embodiments described herein can be configured to remove both local color and pattern noise. For example, as shown in Fig. 1, the method may include removing local color/pattern noise in step 104. Therefore, the embodiments described herein can mitigate noise sources of local

10 color variation and pattern noise. The embodiments described herein can also or alternatively be configured to remove any other noise sources in the defect candidate map.

In addition, the method includes determining one or more characteristics of

15 the potential defect candidates based on portions of the filtered defect candidate map corresponding to the potential defect candidates. In one embodiment, determining the one or more characteristics includes applying a simplified Hough transform to the portions of the filtered defect candidate map corresponding to the potential defect candidates to thereby determine the one or more characteristics of

20 the potential defect candidates. The simplified Hough transform may include any suitable form of the Hough transform and can be applied to the portions of the filtered defect candidate map corresponding to the potential defect candidates in any suitable manner. The one or more characteristics may, however, be determined using any other suitable algorithm and/or method known in the art. For instance,

25 the one or more characteristics may be determined by using a geometric method to find the scratch head and tail angles.

In one embodiment, the one or more characteristics include angle of orientation of the potential defect candidates on the wafer. For example, as shown

30 in step 106 of Fig. 1, a simplified version of the Hough transform may be used to

calculate the angle and other properties of scratches. In this manner, the embodiments described herein may include calculating any Hough-based features and other features of the defect candidates (e.g., orientation, head magnitude, tail magnitude, size of tail and scratch confidence). In another embodiment, applying the simplified Hough transform includes applying the simplified Hough transform to only the portions of the filtered defect candidate map corresponding to the potential defect candidates. For example, the simplified Hough transform can be used to calculate the Hough transform from only the defective pixels, instead of all pixels.

The embodiments described herein may use a simplified Hough transform and mitigations on local color and pattern noise to increase the ability of micro-scratch classification. For example, the method further includes determining if each of the potential defect candidates are scratches based on the one or more characteristics determined for each of the potential defect candidates. Determining if the potential defect candidates are scratches may be performed using a simple classifier to decide if a detected defect is actually a scratch. A “simple” classifier may be any classifier that can classify scratches using decision rules based on scratch features such as those described further herein. For example, as shown in step 108 of Fig. 1, the method may include using a classifier to identify scratches.

In one embodiment, the scratches include heads that appear stronger in the images than tails of the scratches. In one such embodiment, generating the inspection results for the wafer includes applying a threshold to the images of the wafer generated by the wafer inspection system, and the tails of the scratches have values in the images that are approximately equal to or less than the threshold. In another such embodiment, the one or more characteristics include magnitude of the heads and tails in the images. In an additional such embodiment, the one or more characteristics include angles of orientation of the heads and the tails. In a further such embodiment, the one or more characteristics include number of pixels in the

tails. For example, the simple classifier described above may utilize information of (1) the magnitude of both the head and tail of an inspected defect, (2) the angle formed from the head and tail, (3) how many pixels are in the tail, and (4) the confidence of that head and tail form a scratch.

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In one example, if the maximum magnitude of the head portion is below a certain predetermined threshold (determined based on the wafer and inspection system characteristics), then the head portion may be determined to not be part of a scratch. In another example, if the magnitude of the tail portion of a potential defect candidate is less than a first predetermined threshold or greater than a second predetermined threshold (i.e., not between two predetermined thresholds, which are wafer and inspection system dependent), then the defect candidate that includes the tail portion may be determined to not be a scratch. In addition, if the number of pixels in a potential defect candidate in the main direction of the defect candidate is less than a certain number (e.g., 3), then the defect candidate may be determined to not be a scratch. Furthermore, if the directions of the head portion and tail portion of a potential defect candidate do not agree with each other (i.e., scratch confidence is low), then the potential defect candidate may be determined to not be a scratch. In addition, if the direction of a potential defect candidate is horizontal or vertical, then the potential defect candidate may be determined to not be a scratch. Moreover, if a primary portion of a potential defect candidate is not strong, then the potential defect candidate may be determined to not be a scratch.

In contrast, if the maximum magnitude of the head portion of a potential defect candidate is above the certain predetermined threshold, if the magnitude of the tail portion is between the first and second predetermined thresholds, if the number of pixels in the main direction of the potential defect candidate is equal to or greater than the certain number, if the major and second directions agree with each other, if the direction of the potential defect candidate is not horizontal or vertical, and if the primary portion of the potential defect candidate is strong, then

the potential defect candidate may be determined to be a scratch. Therefore, the classifier described above may be configured to compare the characteristics described above to a number of different benchmarks that separate values of the characteristics that are indicative of scratches and those that are not characteristic of scratches. The characteristics described above may be considered in a different order than that described above. In addition, any other suitable characteristics may be added to those described above if they can be used to separate scratches from non-scratches.

The method also includes separating the potential defect candidates determined to be the scratches from other defects in inspection results for the wafer generated by the wafer inspection system. Separating the potential defect candidates determined to be scratches from other defects may include eliminating the scratches from the inspection results. In this manner, the method may include outputting final results, as shown in step 110 of Fig. 1, that include mostly DOI and almost no scratch and micro-scratch nuisance defects. However, separating the potential defect candidates determined to be scratches from other defects may include separating the scratches into a different classified bin than other current layer defects. In this manner, a user can keep track of both previous layer and current layer defects in one inspection check point.

The embodiments described herein, therefore, can be used as scratch filters and provide a reliable classification solution for micro-scratches for the first time. In contrast, the previously used scratch filters can only classify relatively large scratches and there was no solution for micro-scratch classification. In this manner, the embodiments described herein provide opportunities for enhancement of tool sensitivity (i.e., better sensitivity for wafer inspection tools) by reducing the nuisance rate and providing yield relevant defects to wafer inspection tool users.

The embodiments described herein are different from previously used methods for filtering scratches from inspection results in a number of important ways. For example, the embodiments described herein do not assume the size of the scratch (as many micro-scratches can be substantially small with a relatively faint  
5 tail, but bigger scratches can span over many pixels). In contrast, some previously used methods use size as a requirement for spatial characteristics of potential defect candidates and try to search for scratches with the same size on an image. Also, some previously used methods require the scratches to be wholly included in a sub-image of an entire wafer image, while the embodiments described herein do not  
10 require that.

Generating the defect candidate map, removing noise from the defect candidate map, determining the one or more characteristics, determining which of the potential defect candidates are scratches, and separating the potential defect  
15 candidates determined to be the scratches are performed by a computer system, which may be configured as described further herein.

All of the methods described herein may include storing results of one or more steps of the method embodiments in a computer-readable storage medium.  
20 The results may include any of the results described herein and may be stored in any manner known in the art. The storage medium may include any storage medium described herein or any other suitable storage medium known in the art. After the results have been stored, the results can be accessed in the storage medium and used by any of the method or system embodiments described herein, formatted  
25 for display to a user, used by another software module, method, or system, etc.

Another embodiment relates to a non-transitory computer-readable medium storing program instructions executable on a computer system for performing a computer-implemented method for filtering scratches from inspection results for a  
30 wafer. One such embodiment is shown in Fig. 2. For example, as shown in Fig. 2,

non-transitory computer-readable medium 200 includes program instructions 202 executable on computer system 204 for performing the computer-implemented method for filtering scratches from inspection results for a wafer described above. The computer-implemented method for which the program instructions are  
5 executable may include any other step(s) of any other method(s) described herein.

Program instructions 202 implementing methods such as those described herein may be stored on non-transitory computer-readable medium 200. The computer-readable medium may be a storage medium such as a magnetic or optical  
10 disk, a magnetic tape or any other suitable computer-readable medium known in the art.

The program instructions may be implemented in any of various ways, including procedure-based techniques, component-based techniques, and/or object-oriented techniques, among others. For example, the program instructions may be  
15 implemented using Matlab, Visual Basic, ActiveX controls, C, C++ objects, C#, JavaBeans, Microsoft Foundation Classes ("MFC"), or other technologies or methodologies, as desired.

Computer system 204 may take various forms, including a personal  
20 computer system, mainframe computer system, workstation, system computer, image computer, programmable image computer, parallel processor, or any other device known in the art. In general, the term "computer system" may be broadly defined to encompass any device having one or more processors, which executes  
25 instructions from a memory medium.

An additional embodiment relates to a system configured to filter scratches from inspection results for a wafer. One embodiment of such a system is shown in Fig. 3. As shown in Fig. 3, the system includes optical subsystem 300 and computer  
30 subsystem 302. The optical subsystem is configured to direct light to a wafer and

detect light from the wafer to thereby generate images for the wafer. For example, as shown in Fig. 3, the optical subsystem includes light source 304, which may include any suitable light source known in the art.

5           Light from the light source may be directed to beam splitter 306, which may be configured to direct the light from the light source through lens 308 to wafer 310. The light source may be coupled to any other suitable elements (not shown) such as one or more condensing lenses, collimating lenses, relay lenses, objective lenses, apertures, spectral filters, polarizing components and the like. As shown in Fig. 3, the light may  
10   be directed to the wafer at a normal angle of incidence. However, the light may be directed to the wafer at any suitable angle of incidence including near normal and oblique incidence. In addition, the light or multiple light beams may be directed to the wafer at more than one angle of incidence sequentially or simultaneously. The optical subsystem may be configured to scan the light over the wafer in any suitable  
15   manner.

          Light reflected from wafer 310 may be collected and detected by multiple channels of the optical subsystem during scanning. For example, light specularly reflected from wafer 310 may be collected by lens 308. Lens 308 may include a  
20   refractive optical element as shown in Fig. 3. In addition, lens 308 may include one or more refractive optical elements and/or one or more reflective optical elements. Light collected by lens 308 may be directed through beam splitter 306 to beam splitter 312, which may be configured to separate the light into two different paths, one of which is directed to detector 314 and another of which is directed to detector  
25   316. The beam splitters shown in Fig. 3 may include any suitable beam splitters known in the art. The detectors shown in Fig. 3 may include any suitable detectors known in the art such as charge coupled devices (CCDs) or another type of imaging detectors. Detectors 314 and 316 are configured to generate images that are responsive to the specularly reflected light. Therefore, each of the detectors form  
30   one channel of the optical subsystem.

Since the optical subsystem shown in Fig. 3 is configured to detect light specularly reflected from the wafer, the optical subsystem is configured as a bright field (BF) optical subsystem. Such an optical subsystem may, however, also be configured for other types of wafer inspection. For example, the optical subsystem shown in Fig. 3 may also include one or more other channels (not shown). The other channel(s) may include any of the optical components described herein such as a lens and a detector, configured as a scattered light channel. The lens and the detector may be further configured as described herein. In this manner, the optical subsystem may also be configured for dark field (DF) inspection.

Computer subsystem 302 is configured to acquire the images generated by the optical subsystem. For example, images generated by the detector(s) during scanning may be provided to computer subsystem 302. In particular, the computer subsystem may be coupled to each of the detectors (e.g., by one or more transmission media shown by the dashed lines in Fig. 3, which may include any suitable transmission media known in the art) such that the computer subsystem may receive the images generated by the detector(s).

The computer subsystem is configured for performing the steps of the computer-implemented method described further herein. The computer subsystem may be configured to perform any other step(s) of any method embodiment(s) described herein. The computer subsystem, the optical subsystem, and the system may be further configured as described herein.

It is noted that Fig. 3 is provided herein to generally illustrate one configuration of an optical subsystem that may be included in the system embodiments described herein. Obviously, the optical subsystem configuration described herein may be altered to optimize the performance of the optical subsystem as is normally performed when designing a commercial inspection

system. In addition, the systems described herein may be implemented using an existing inspection system (e.g., by adding functionality described herein to an existing inspection system) such as the 29xx/28xx series of tools that are commercially available from KLA-Tencor. For some such systems, the methods  
5 described herein may be provided as optional functionality of the system (e.g., in addition to other functionality of the system). Alternatively, the system described herein may be designed “from scratch” to provide a completely new system.

Further modifications and alternative embodiments of various aspects of the  
10 invention will be apparent to those skilled in the art in view of this description. For example, methods and systems for filtering scratches from inspection results for a wafer are provided. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the invention. It is to be understood that the forms of the invention  
15 shown and described herein are to be taken as the presently preferred embodiments. Elements and materials may be substituted for those illustrated and described herein, parts and processes may be reversed, and certain features of the invention may be utilized independently, all as would be apparent to one skilled in the art after having the benefit of this description of the invention. Changes may be made  
20 in the elements described herein without departing from the spirit and scope of the invention as described in the following claims.

**WHAT IS CLAIMED IS:**

- 1. A computer-implemented method for filtering scratches from inspection results for a wafer, comprising:**

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**generating a defect candidate map for a wafer from images of the wafer generated by a wafer inspection system, wherein the defect candidate map comprises image data for potential defect candidates as a function of position on the wafer;**

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**removing noise from the defect candidate map to generate a filtered defect candidate map;**

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**determining one or more characteristics of the potential defect candidates based on portions of the filtered defect candidate map corresponding to the potential defect candidates;**

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**determining if each of the potential defect candidates are scratches based on the one or more characteristics determined for each of the potential defect candidates; and**

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**separating the potential defect candidates determined to be the scratches from other defects in inspection results for the wafer generated by the wafer inspection system, wherein the generating, removing, determining the one or more characteristics, determining if each of the potential defect candidates are the scratches, and separating steps are performed by a computer system.**

**2. The method of claim 1, wherein generating the defect candidate map comprises applying a threshold to the images and determining that portions of the images having values above the threshold are the potential defect candidates.**

5 **3. The method of claim 2, wherein the threshold is substantially close to a noise floor of the images.**

**4. The method of claim 2, wherein the images of the wafer comprise gray scale images.**

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**5. The method of claim 1, wherein the noise that is removed from the defect candidate map comprises local color noise.**

15 **6. The method of claim 5, wherein removing the noise comprises applying a local difference filter to the images.**

**7. The method of claim 1, wherein the noise that is removed from the defect candidate map comprises pattern noise.**

20 **8. The method of claim 7, wherein removing the noise comprises removing horizontal and vertical pattern noise from the images.**

**9. The method of claim 1, wherein the one or more characteristics comprise angle of orientation of the potential defect candidates on the wafer.**

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**10. The method of claim 1, wherein determining the one or more characteristics comprises applying a simplified Hough transform to the portions of the filtered defect candidate map corresponding to the potential defect candidates to thereby determine the one or more characteristics of the potential defect candidates.**

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11. The method of claim 10, wherein applying the simplified Hough transform comprises applying the simplified Hough transform to only the portions of the filtered defect candidate map corresponding to the potential defect candidates.

5 12. The method of claim 1, wherein the scratches comprise heads that appear stronger in the images than tails of the scratches.

13. The method of claim 12, wherein generating the inspection results for the wafer comprises applying a threshold to the images of the wafer generated by the  
10 wafer inspection system, and wherein the tails of the scratches have values in the images that are approximately equal to or less than the threshold.

14. The method of claim 12, wherein the one or more characteristics comprise magnitude of the heads and tails in the images.

15

15. The method of claim 12, wherein the one or more characteristics comprise angles of orientation of the heads and the tails.

16. The method of claim 12, wherein the one or more characteristics comprise  
20 number of pixels in the tails.

17. The method of claim 1, wherein the images of the wafer are generated by the wafer inspection system detecting light from the wafer.

25 18. The method of claim 1, wherein the scratches are caused by a chemical mechanical polishing process performed on the wafer.

19. The method of claim 1, wherein the scratches are located under a layer of the wafer for which the inspection results were generated.

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**20. The method of claim 1, wherein the scratches comprise micro-scratches.**

**21. A non-transitory computer-readable medium, storing program instructions executable on a computer system for performing a computer-implemented method for filtering scratches from inspection results for a wafer, wherein the computer-implemented method comprises:**

**generating a defect candidate map for a wafer from images of the wafer generated by a wafer inspection system, wherein the defect candidate map comprises image data for potential defect candidates as a function of position on the wafer;**

**removing noise from the defect candidate map to generate a filtered defect candidate map;**

**determining one or more characteristics of the potential defect candidates based on portions of the filtered defect candidate map corresponding to the potential defect candidates;**

**determining if each of the potential defect candidates are scratches based on the one or more characteristics determined for each of the potential defect candidates; and**

**separating the potential defect candidates determined to be the scratches from other defects in inspection results for the wafer generated by the wafer inspection system.**

**22. A system configured to filter scratches from inspection results for a wafer, comprising:**

**an optical subsystem configured to direct light to a wafer and detect light from the wafer to thereby generate images for the wafer; and**

**a computer subsystem configured for:**

5

**generating a defect candidate map for the wafer from the images, wherein the defect candidate map comprises image data for potential defect candidates as a function of position on the wafer;**

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**removing noise from the defect candidate map to generate a filtered defect candidate map;**

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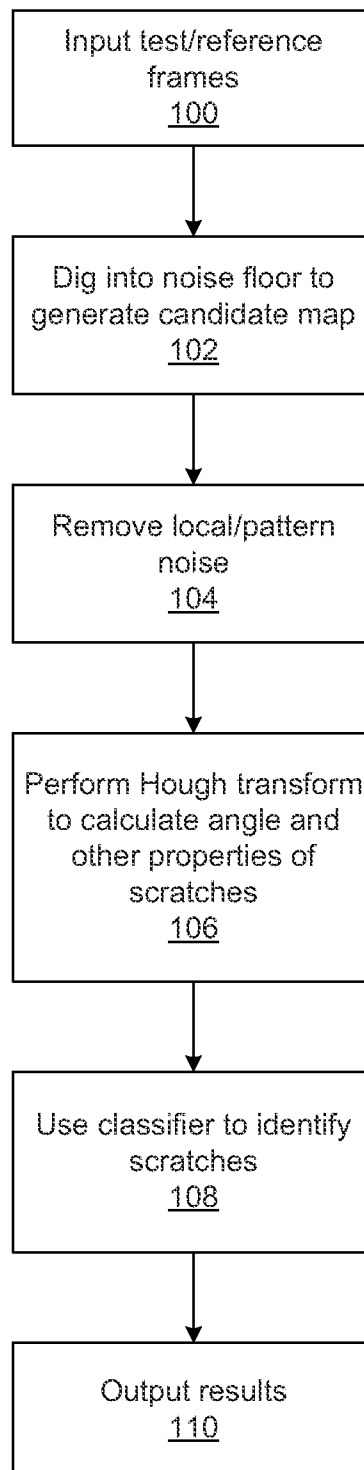
**determining one or more characteristics of the potential defect candidates based on portions of the filtered defect candidate map corresponding to the potential defect candidates;**

20

**determining if each of the potential defect candidates are scratches based on the one or more characteristics determined for each of the potential defect candidates; and**

25

**separating the potential defect candidates determined to be the scratches from other defects in inspection results for the wafer.**

*1/2**Fig. 1*

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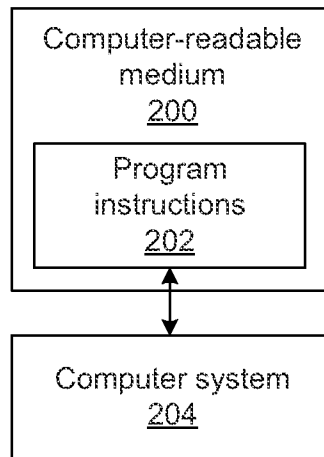


Fig. 2

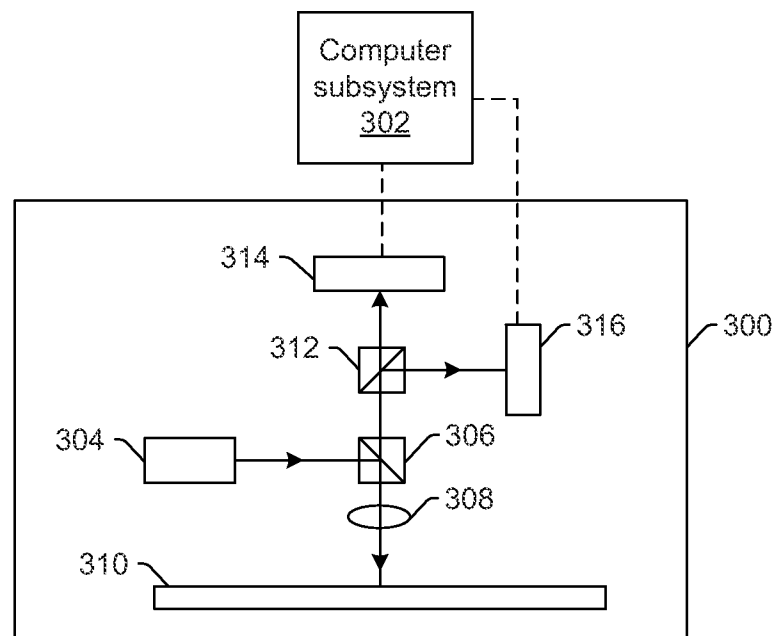


Fig. 3

## INTERNATIONAL SEARCH REPORT

International application No.  
**PCT/US2014/052758****A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/66(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/66; G06F 11/30; G01B 5/28; G06F 19/00; G01N 21/956; G06T 1/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; keywords: wafer inspection, defect, scratch, filter, map

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                  | Relevant to claim No. |
|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| X         | US 7373277 B1 (SEAN WU et al.) 13 May 2008<br>See abstract, column 1, lines 36-48, column 6, line 43 - column 13, line 67, claim 1 and figures 1-3. | 1-22                  |
| A         | US 2004-0064269 A1 (HISAE SHIBUYA et al.) 01 April 2004<br>See abstract, paragraphs [0034]-[0073] and figures 1-12.                                 | 1-22                  |
| A         | US 6493645 B1 (THOMAS HLADSHIK) 10 December 2002<br>See abstract, column 6, line 62 - column 8, line 14 and figures 4-7.                            | 1-22                  |
| A         | US 2004-0220754 A1 (INGO BRASACK et al.) 04 November 2004<br>See abstract, paragraphs [0019]-[0021] and figures 2-3.                                | 1-22                  |
| A         | JP 2001-331784 A (HITACHI LTD.) 30 November 2001<br>See abstract, paragraphs [0010]-[0084] and figures 1-22.                                        | 1-22                  |



Further documents are listed in the continuation of Box C.



See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

09 December 2014 (09.12.2014)

Date of mailing of the international search report

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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2014/052758**

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s) | Publication<br>date |
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