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- (71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).
- (72) Inventors: AVCI, Uygur E.; 3868 NW 139th Place, Portland, Oregon 97229 (US). NIKONOV, Dmitri E.; 16569 SW Whietail Ln., Beaverton, Oregon 97229 (US). YOUNG, Ian A.; 3181 NW 114th Terrace, Portland, Oregon 97229 (US).
- (74) Agent: RICHARDS, II, E.E. "Jack"; Trop, Pruner & Hu, P.C. 1616 S. Voss, Rd., Ste. 750, Houston, Texas 77057-2631 (US).
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(54) Title: REDUCED SCALE RESONANT TUNNELING FIELD EFFECT TRANSISTOR

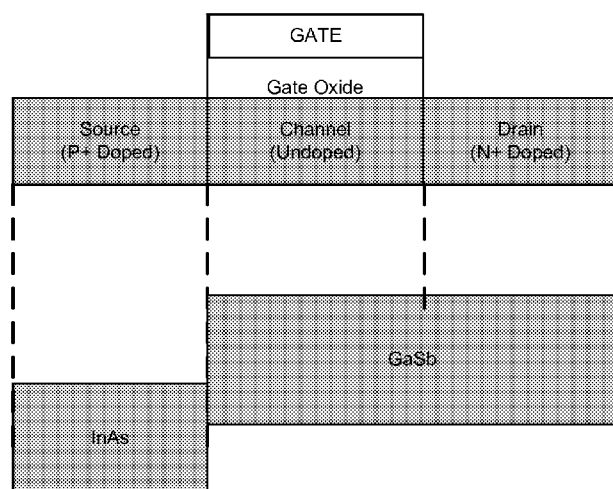


FIG. 4

(57) Abstract: An embodiment includes a hetero-junction tunneling field effect transistor including a source, a channel, and a drain; wherein (a) the channel includes a major axis, corresponding to channel length, and a minor axis that corresponds to channel width and is orthogonal to the major axis; (b) the channel length is less than 10 nm long; (c) the source is doped with a first polarity and has a first conduction band; (d) the drain is doped with a second polarity, which is opposite the first polarity, and the drain has a second conduction band with higher energy than the first conduction band. Other embodiments are described herein.

**Declarations under Rule 4.17:**

- as to the identity of the inventor (Rule 4.17(i))
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

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REDUCED SCALE RESONANT TUNNELING FIELD EFFECT TRANSISTOR

Background

[0001] A Tunnel Field Effect Transistor (TFET) structure is similar to a metal oxide semiconductor field effect transistor (MOSFET) structure and includes a source, a drain, and a channel coupled to a gate. TFETs are available in different forms, such as n type (nTFET) and p type (pTFET) devices. The drain current (I_d) increases with increasing gate voltage (V_g) for an nTFET and increases with decreasing V_g for a pTFET. The nTFET switches on ("on state") for a gate/source voltage (V_g) greater than the threshold voltage, while the pTFET switches on for a V_g less than the threshold voltage. The source in an nTFET is p doped while the drain is n doped and the source in a pTFET is n doped while the drain is p doped. The channel is undoped or less doped, in terms of doping concentration, than the source or drain.

Brief Description Of The Drawings

[0002] Features and advantages of embodiments of the present invention will become apparent from the appended claims, the following detailed description of one or more example embodiments, and the corresponding figures, in which:

Figures 1-2 concern MOSFET, TFET and heterojunction TFET (heTFET) off/on state characteristics.

Figure 3 concerns a conventional heTFET structure.

Figure 4 concerns a reverse heTFET structure in an embodiment.

Figures 5-6 concern MOSFET, heTFET and reverse heTFET off/on state characteristics in an embodiment.

Figures 7-8 concern MOSFET, heTFET and reverse heTFET off/on state characteristics in an embodiment.

Figure 9 concerns a reverse heTFET energy band diagram in an embodiment.

Figures 10(a)-(d) concern density of state (DOS) for an embodiment.

Figure 11 includes a schematic cross section view of an embodiment.

Detailed Description

[0003] In the following description, numerous specific details are set forth but embodiments of the invention may be practiced without these specific details. Well known circuits, structures and techniques have not been shown in detail to avoid obscuring an understanding of this description. "An embodiment", "various embodiments" and the like indicate embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Some embodiments may have some, all, or none of the features described for other embodiments. "First", "second", "third" and the like describe a common object and indicate different instances of like objects are being referred to. Such adjectives do not imply objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner. "Connected" may indicate elements are in direct physical or electrical contact with each other and "coupled" may indicate elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact. Also, while similar or same numbers may be used to designate same or similar parts in different figures, doing so does not mean all figures including similar or same numbers constitute a single or same embodiment.

[0004] A MOSFET's inverse "subthreshold slope", $dV_g/d_{\log(I_d)}$ has a theoretical lower limit of 60 mV/decade ("dec") at room temperature. Subthreshold slope concerns the slope of current-voltage characteristics near the device's "off state" (i.e., where I_d is small, also referred to as I_{off} or "off current"), and the device's "on state" (i.e., where there is substantial I_d , also referred to as I_{on} or "on current"). For a given off current target (which is determined by a standby power requirement for a device that includes the MOSFET) I_d for a MOSFET can only increase at this maximum rate of 60 mV/dec. This limits the on current and, consequently, circuit performance (e.g., speed of transistor switching). For low active power devices, operation at lower supply voltages is desirable because of the strong dependence of active power on supply voltage (proportional to supply voltage to the power of 2). However, due to the MOSFET's limited subthreshold slope, when a MOSFET is operated at low supply voltages the on current is significantly lower because the

MOSFET is operating close to its threshold voltage (which is needed to convert from off state to on state).

[0005] Figure 1 depicts various transistor performance characteristics that show, for example, a TFET (trace 102) may have a sharper turn on behavior (i.e., steeper subthreshold slope) than a MOSFET (trace 101). The conditions for Figure 1 includes an I_{off} of 1 nA/ μm , equivalent oxide thickness (EOT) of 0.8 nm, and gate length (L_g) = 15 nm. This sharpness advantage for the TFET is shown in Figure 1 from V_g of 0.0 to 0.2 V, where MOSFET 101 has a 74 mV/dec slope and TFET 102 has a 41 mV/dec slope in that same range. In other words, the TFET has a steeper and more desirable subthreshold slope. This enables higher on currents than with the MOSFET when the devices are driven at low supply voltages. An heTFET (trace 103) uses a combination of two semiconductor materials (one for the source and another for the channel and drain; hence the term heterojunction) to enable higher tunneling current and better TFET characteristics. The subthreshold slope for heTFET 103 is about 35 mV/dec, better (steeper) than TFET 102 or MOSFET 101.

[0006] However, this advantage of TFET devices over MOSFETs gets smaller at aggressively scaled (shorter) gate lengths. While Figure 1 included data for devices with an L_g of 15 nm, Figure 2 includes data for the same conditions as Figure 1 but for an L_g of only 9 nm. Figure 2 illustrates the subthreshold slopes for 201, 202, 203 are similar for V_g of 0.0 to 0.1 V, in contrast to Figure 1 showing the clear advantage (steeper slopes) in that same range of the TFETs to the MOSFET. The subthreshold slope differential between the three devices decreases as gate length decreases. In other words, traces 202 and 203 (which are both TFETs) have less slope steepness improvement compared to the MOSFET between Figures 1 and 2.

[0007] Figure 3 depicts a conventional heTFET design combining semiconductor material at the source (e.g., gallium antimonide (GaSb)) with a lower conduction band material at the channel and drain (e.g., indium arsenide (InAs)). In contrast, Figure 4 depicts an embodiment of the invention that includes a reverse heTFET where the band material order is switched. In other words, reverse heTFET design of Figure 4 combines semiconductor material at the source (e.g., InAs) with a higher conduction band material at the channel and drain (e.g., GaSb). Still, in Figure 4 the

band discontinuity from the disparate materials works against tunneling current density and makes for a much harder tunneling path.

[0008] Embodiments of the invention are not limited to source/drain combinations such as the above described InAs/GaSb material system. Other embodiments include material combinations that create significant band discontinuity. Other examples comprise materials such as silicon (Si), germanium (Ge), phosphorous (P), and include, but are not limited to, source/drain combinations such as: Si/InAs, Si/SiGe, GaAsSb/InAsSb, and InGaAs/InP.

[0009] This can be seen from the operation characteristics difference between conventional and reverse heTFET devices each with $L_g = 20$ nm, which are illustrated in Figures 5 and 6. In Figures 5 and 6 MOSFET (traces 501, 601), conventional heTFET (source = GaSb, drain = InAs) (traces 503, 603), and reverse heTFET (source = InAs, drain = GaSb) (traces 504, 604) are plotted for off current targets of 1 nA/ μ m (Figure 5, element 505) and 10 pA/ μ m (Figure 6, element 605). These figures show conventional heTFETs have higher on-current than reverse heTFETs for various off-current targets and supply voltages when the devices have $L_g = 20$ nm.

[0010] However, this behavior changes with a very short L_g having confined channel dimensions. For a short L_g a reverse heTFET has a very sharp subthreshold slope. This enables low supply voltage and low off current target operations, which both enable very low power products. For example, an embodiment includes a channel with $L_g = 9$ nm included in a 3 nm wide and 3 nm tall nanowire (a semiconductor nanoscale structure). As seen in Figures 7 and 8, this reverse heTFET embodiment has a very sharp subthreshold slope. MOSFET (traces 701, 801), conventional heTFET (source = GaSb, drain = InAs) (traces 703, 803), and reverse heTFET (source = InAs, drain = GaSb) (traces 704, 804) are respectively plotted for I_{off} targets of 1 nA/ μ m (Figure 7) and 10 pA/ μ m (Figure 8). All devices have $L_g = 9$ nm. Reverse heTFETs show the best subthreshold slope and perform best at both I_{off} targets with low supply voltages. Specifically, for Figure 8 reverse heTFET trace 804 shows a 25 mV/dec subthreshold slope (between 0.0 and 0.1 V_g), whereas heterojunction device trace 803 shows a 47 mV/dec subthreshold

slope, and MOSFET 801 shows a 63 mV/dec subthreshold slope. Thus, this embodiment of a reverse heTFET achieves a better on current than both MOSFETs and conventional heTFETs at low supply voltages.

[0011] An embodiment has improved transistor characteristics due to, for example, the discreet resonant states created by three dimensional confinement of the reverse heTFET channel. For example, an embodiment includes a channel with L_g less than 10 nm, two dimensions are confined by using a nanowire width and height of 3 nm, and a third dimension confined due to the profile of band discontinuity between the source and channel of the embodiment. These resonant states enable a rapid change from I_{off} to I_{on} due to the tight Density of States (DOS) characteristics.

[0012] This rapid change from I_{off} to I_{on} is non-obvious when viewing a classical potential profile. For example, in an embodiment including a reverse heTFET the energy bands do not accurately explain the actual device operation. Figure 9 shows classical band edges for the reverse heTFET at I_{off} (traces 910) and I_{on} (traces 911). Traces 910 correspond to conduction and valence bands at 0.0 eV and traces 911 correspond to conduction and valence bands at 0.3 eV. Tunneling distance 920 is large but even tunneling distance 921 remains large indicating a very low (undesirable) channel current in the on state.

[0013] However, Figures 10(a)-(d) better illustrate operation of an embodiment of the device and why highly confined channel geometry favors reverse heTFETs over non-reverse heTFETs and MOSFETs. Due to the strong channel confinement, the allowed electron energies have peaks around the heterojunction interface region. Specifically, Figures 10(a)-(d) illustrate density of states (DOS) characteristics. DOS equals the density per unit volume and energy of the number of solutions to Schrödinger's equation. Figures 10(a) and (b) correspond to off and on states for a conventional heTFET ($L_g = 9$ nm). Figures 10(c) and (d) correspond to off and on states for a reverse heTFET ($L_g = 9$ nm). Until discrete energy states are aligned with the valence band on the source side (area 1021 for each of Figures 10(a)-(d)), the tunneling current is low due to the low DOS in the region necessary to conduct electrons. Thus, Figure 10(a) shows a conventional heTFET in the off state with a

large tunneling distance 1020. Figure 10(c) shows an embodiment of a reverse heTFET in the off state with large tunneling distance 1030.

[0014] In Figure 10(c) once V_g is increased for the conventional heTFET there is still low DOS (as understood from the shaded contour labels) at source/channel junction 1023. However, in Figure 10(d) once the energy of the discrete levels is brought down to the level of the valence band of the source side 1021 (due to increasing V_g), there is a sharp increase in tunneling current that creates sharp subthreshold slope behavior. In other words, source/channel junction 1033 includes high DOS projection 1034 (which resembles a horizontal “needle” pointing to the left of the graph). High DOS projection 1031 is misaligned with the source valence band 1021 in I_{off} (Figure 10(c)); but projection 1034 is aligned with the source valence band 1021 in Figure 10(d). More generally, Figure 10(d) shows high DOS (darker portions are higher DOS) as a function of energy along the device near the source/channel junction (near the 10 nm mark on X axis). As a result, reverse heTFETs outperform conventional heTFETs at small L_g providing better on current at lower V_g .

[0015] An embodiment is implemented with the same or similar approach as conventional heTFETs (only with the switched semiconductor materials in the source and channel/drain regions as shown in Figure 4). This enables heterogeneous integration of two devices, where, for example, high performance requiring circuits use the conventional heterojunction device and low power requiring circuits use the reverse heTFET on the same substrate.

[0016] Various methods for creating a narrow channel suitable for reverse heTFET are available. Such methods are described in, for example, U.S. Patent No. 6,897,098, assigned to Intel Corporation (Santa Clara, California, U.S.A.) and entitled “Method of fabricating an ultra-narrow channel semiconductor device”. As detailed in U.S. Patent No. 6,897,098, a small scale channel suitable for use in various embodiments of the invention is produced as follows. Nanowire 1106 is deposited on first dielectric layer 1104, which is formed on substrate 1102 (see Figure 11). The nanowire has a first dimension. The nanowire provides first region 1108, second region 1107, and third region 1109. A sacrificial gate stack having a

sacrificial dielectric layer and a sacrificial gate electrode layer is deposited over first region 1108 of the nanowire leaving exposed the second region and the third region of the nanowire. A first spacer is deposited adjacent each side of the sacrificial gate stack. A second dielectric layer is deposited over the first dielectric layer to cover the second region and third region. The sacrificial gate electrode and the sacrificial dielectric layer are removed after the first spacer is deposited. Removing the sacrificial gate electrode and the sacrificial dielectric layer exposes the first region of the nanowire. The first region of the nanowire is thinned by at least one thermal oxidation and oxide removal process. After thinning, the first region has a second dimension that is smaller than the first dimension. Thinning the first region of the nanowire provide the first region of the nanowire with a cross-sectional dimension that is substantially smaller (e.g., ten times or at least two times smaller) than that of the second region and the third region. First region can be middle region 108 of the nanowire and the second and third regions 1107, 1109 can be the side regions of the nanowire. Dielectric layer 1125 and gate electrode layer 1123 may be added.

[0017] In one embodiment, the nanowire has first cross-sectional dimensions that are in the order of nanoscale. The nanowire has length 1130 of about 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, or 15 nm, height 132 of about 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, or 15 nm, and width 134 of about 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, or 15 nm. The height, width, and length can be varied depending on the methods used to form the nanowire. As shown above, some embodiments include a length, width, height combinations of 10, 3, and 3 nm. But other embodiments include, for example and without limitation, length, width, height combinations of 8, 3, and 3 nm; 12, 3, and 3 nm; 8, 2, and 2 nm; and the like.

[0018] In one embodiment, before thinning, the middle region has the same initial thickness or cross-sectional dimension as the rest of the nanowire. After thinning, the middle region will have a cross-sectional dimension that is smaller or substantially smaller than other portions of nanowire 1106. In one embodiment, the thinned middle portion has width and/or height less than about 5 nm or less than about 2-3 nm. In some embodiments there is no thinning of middle portion 1108, which has the same height and width as portions 1107, 1109.

[0019] In one embodiment, the second region and the third region are implanted using conventional methods such as ion implantation to form the source/drain regions for a semiconductor device. For example, for an n heTFET region 1107 may be a p doped source, channel region 1108 may be intrinsic, and region 1109 may be an n doped drain. In another embodiment, for a p heTFET region 1107 may be a p doped drain, channel region 1108 may be intrinsic, and region 1109 may be n doped source. The source and drain may be different materials in terms of doping concentration, material concentrations (e.g., $\text{In}_x\text{Ga}_{1-x}\text{As}$ and $\text{In}_y\text{Ga}_{1-y}\text{As}$, where x is not equal to y), and materials (e.g., InAs and GaSb).

[0020] A silicide layer can be formed over each of the second region and the third region after the implantation to facilitate contacts to the source/drain regions. The silicide layer provides a low contact resistance to the source/drain regions formed in the second region and the third region. The silicide layer can be formed of a metal such as cobalt, nickel, and the like. The silicide layer can be formed using conventional methods that deposit the metal over the second region and the third region. After the metal is deposited, heat is applied to these regions to allow the silicon in these regions to react with the metals to form silicide.

[0021] Thus, as indicated above, an embodiment includes an heTFET including a source, a channel, and a drain; wherein the channel includes a major axis, corresponding to channel length, and a minor axis that corresponds to channel width and is orthogonal to the major axis. In an embodiment the channel length is less than 10 nm long; but in other embodiments the length is longer (e.g., 10 or 15 nm) or shorter (e.g., 3 or nm). In one embodiment the channel width is less than 5 nm wide, but in other embodiments the width is wider (e.g., 7 or 9 nm) or narrower (e.g., 2 or 3). In one embodiment the channel height is less than 5 nm wide, but in other embodiments the height is taller (e.g., 7 or 9 nm) or shorter (e.g., 2 or 3). For a p heTFET the source is doped with a first polarity (n) and has a first conduction band; and the drain is doped with a second polarity (p), and the drain has a second conduction band that is higher than the first conduction band. The doping polarity is opposite for an n heTFET. In one embodiment the off current is less than 3 nA and may extend down to, for example, 1 pA, but in other embodiments the off current may be 1 or 2 nA or 4, 5, 6, 7, 8, 9 or more nA. In one embodiment the subthreshold

gate voltage to logarithm of drain current ratio (the subthreshold slope), which occurs between transition from off state to on state, is less than 30 mV/dec but in other embodiments the slope is 15, 20, 25, 35, or 40 mV/dec.

[0022] An embodiment includes an apparatus comprising: a heterojunction tunneling field effect transistor including a source, a channel, and a drain; wherein (a) the channel includes a major axis, corresponding to channel length, and a minor axis that corresponds to channel width and is orthogonal to the major axis; (b) the channel length is less than 10 nm long; (c) the source is doped with a first polarity and has a first conduction band; (d) the drain is doped with a second polarity, which is opposite the first polarity, and the drain has a second conduction band that has higher energy than the first conduction band. In an embodiment the first polarity is positive. In an embodiment the source includes InAs. In an embodiment the drain includes GaSb. In an embodiment the channel width is less than 4 nm wide. In an embodiment the channel includes a nanowire. In an embodiment the off current is less than 3 nA. In an embodiment the subthreshold gate voltage to drain current ratio, which occurs between the transition from off state to on state, is less than 30 mV/dec. In an embodiment the DOS at a junction between the source and channel includes a triangular projection misaligned with a valance band for the source in an "off state" and aligned with the valance band in an "on state". In an embodiment allowed electron energy states have a peak at a junction between the source and channel in an on state. In an embodiment the heTFET is a reverse heterojunction TFET, the apparatus comprising a non-reverse heterojunction TFET (i.e., heterojunction TFET) in a substrate that also includes the reverse heterojunction TFET.

[0023] An embodiment includes an apparatus comprising: a heterojunction tunneling field effect transistor including a source, a channel, and a drain; wherein the channel length is less than 10 nm long; the drain has conduction band with higher energy than a conduction band of the source; and the transistor includes a subthreshold gate voltage to drain current ratio, which occurs between transition from "off state" to "on state", less than 30 mV/dec. In an embodiment the DOS at a junction between the source and channel includes a triangular projection misaligned with a valance band for the source in an "off state" and aligned with the valance band

in an “on state”. In an embodiment allowed electron energy states have a peak at a junction between the source and channel in an on state.

[0024] An embodiment includes an apparatus comprising: a substrate; a first heTFET including a first source, a first channel, and a first drain; wherein the first channel length is less than 10 nm long, the first drain has conduction band with higher energy than a conduction band of the first source, and the heTFET is formed on the substrate; and a second heTFET including a second source, a second channel, and a second drain; wherein the second drain has conduction band with lower energy than a conduction band of the second source, and the second heTFET is formed on the substrate. In an embodiment the first heTFET includes a subthreshold gate voltage to drain current slope, which occurs between transition from “off state” to “on state”, less than 30 mV/dec. In an embodiment the first channel width is less than 4 nm wide. In an embodiment off current for the first heTFET is less than 3 nA.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

- 1 1. An apparatus comprising:
2 a heterojunction tunneling field effect transistor including a source, a channel, and a
3 drain;
4 wherein (a) the channel includes a major axis, corresponding to channel
5 length, and a minor axis that corresponds to channel width and is orthogonal to the
6 major axis; (b) the channel length is less than 10 nm long; (c) the source is doped
7 with a first polarity and has a first conduction band; (d) the drain is doped with a
8 second polarity, which is opposite the first polarity, and the drain has a second
9 conduction band with higher energy than the first conduction band.
- 1 2. The apparatus of claim 1 wherein the first polarity is positive.
- 1 3. The apparatus of claim 1 wherein the source includes InAs.
- 1 4. The apparatus of claim 3 wherein the drain includes GaSb.
- 1 5. The apparatus of claim 1 wherein the channel width is less than 4 nm wide.
- 1 6. The apparatus of claim 1 wherein the channel includes a nanowire.
- 1 7. The apparatus of claim 1 wherein off current for the transistor is less than 3 nA.
- 1 8. The apparatus of claim 1 wherein the transistor includes a subthreshold gate voltage
2 to drain current ratio, which occurs between transition from off state to on state, less than
3 30 mV/dec.
- 1 9. The apparatus of claim 1 wherein the source and the drain respectively
2 include one of InAs and GaSb; Si and InAs; Si and SiGe; GaAsSb and InAsSb; and
3 InGaAs and InP.

- 1 10. The apparatus of claim 1 wherein the density of states (DOS) at a junction between
2 the source and channel includes a triangular projection misaligned with a valance band for
3 the source in an off state and aligned with the valance band in an on state
- 1 11. The apparatus of claim 1 wherein allowed electron energy states have a peak at a
2 junction between the source and channel in an on state.
- 1 12. The apparatus of claim 1, wherein the heterojunction tunneling field effect
2 transistor (heTFET) is a reverse heTFET, the apparatus comprising a non-reverse
3 heTFET in a substrate that also includes the reverse heTFET.
- 1 13. An apparatus comprising:
2 a heterojunction tunneling field effect transistor including a source, a channel, and a
3 drain;
4 wherein the channel length is less than 10 nm long; the drain has conduction band with
5 higher energy than a conduction band of the source; and the transistor includes a
6 subthreshold gate voltage to drain current ratio, which occurs between transition from off
7 state to on state, less than 30 mV/dec.
- 1 14. The apparatus of claim 13 wherein the source and the drain respectively
2 include one of InAs and GaSb; Si and InAs; Si and SiGe; GaAsSb and InAsSb; and
3 InGaAs and InP.
- 1 15. The apparatus of claim 13 wherein the density of states (DOS) at a junction between
2 the source and channel includes a triangular projection misaligned with a valance band for
3 the source in an off state and aligned with the valance band in an on state.
- 1 16. The apparatus of claim 13 wherein allowed electron energy states have a peak at a
2 junction between the source and channel in an on state.
- 1 17. An apparatus comprising:
2 a substrate;

3 a first heterojunction tunneling field effect transistor (heTFET) including a first
4 source, a first channel, and a first drain; wherein the first channel length is less than 10 nm
5 long, the first drain has conduction band with higher energy than a conduction band of the
6 first source, and the heTFET is formed on the substrate; and

7 a second heTFET including a second source, a second channel, and a
8 second drain; wherein the second drain has conduction band with lower energy than
9 a conduction band of the second source, and the second heTFET is formed on the
10 substrate.

1 18. The apparatus of claim 17 wherein the first heTFET includes a subthreshold
2 gate voltage to drain current ratio, which occurs between transition from off state to
3 on state, less than 30 mV/dec.

1 19. The apparatus of claim 17 wherein the first channel width is less than 4 nm
2 wide.

1 20. The apparatus of claim 19 wherein off current for the first heTFET is less than
2 3 nA.

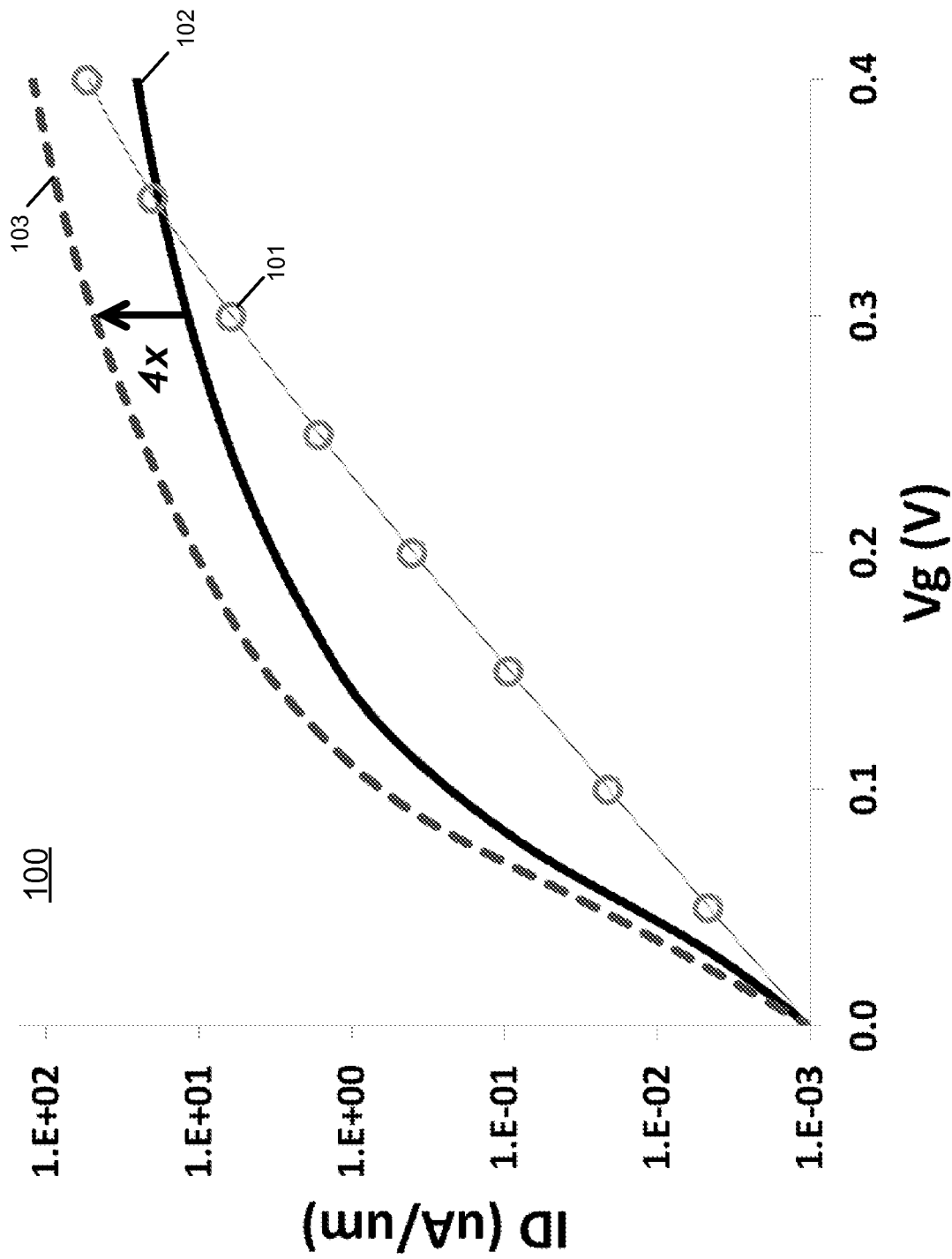


FIG. 1

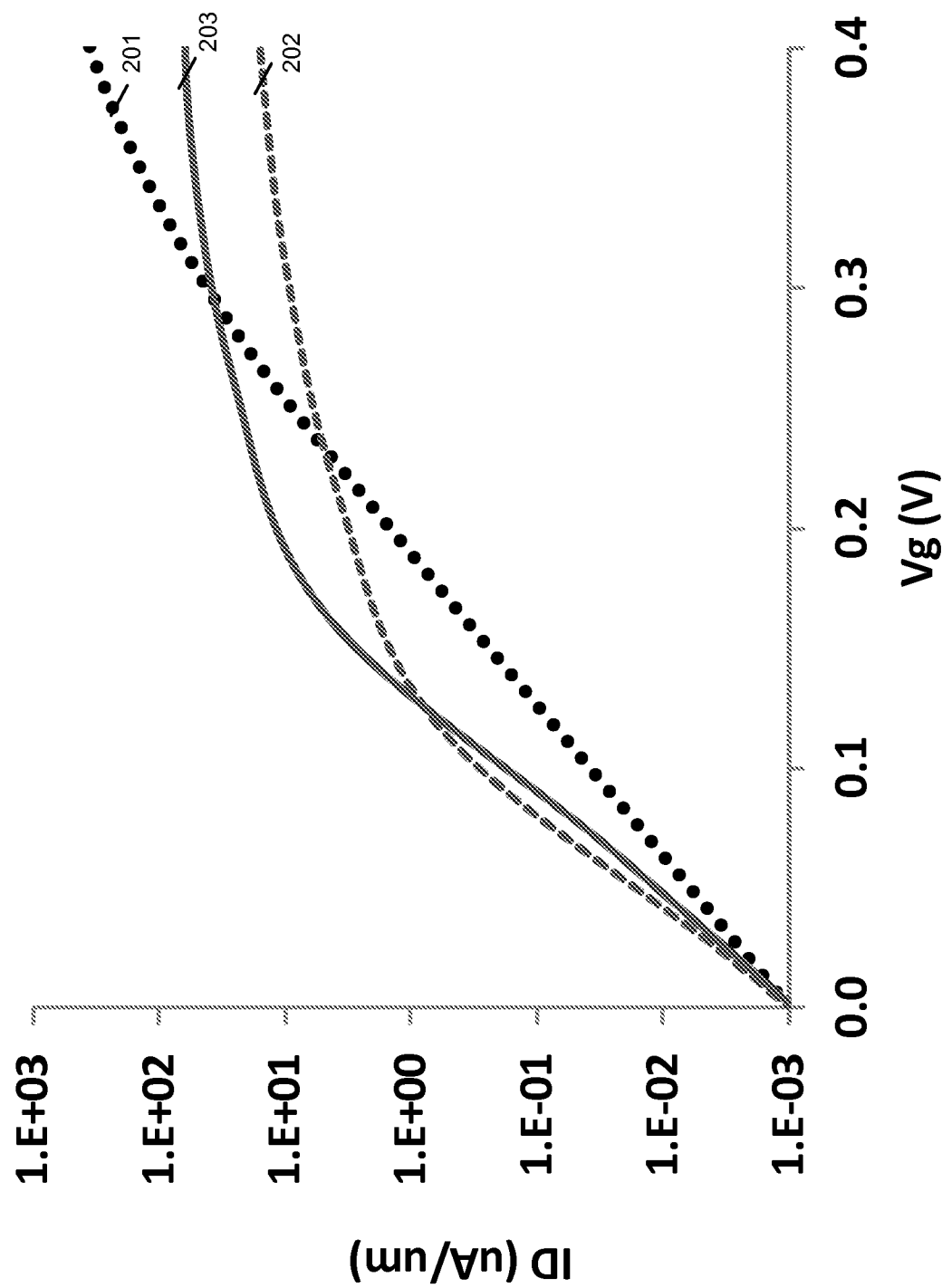


FIG. 2

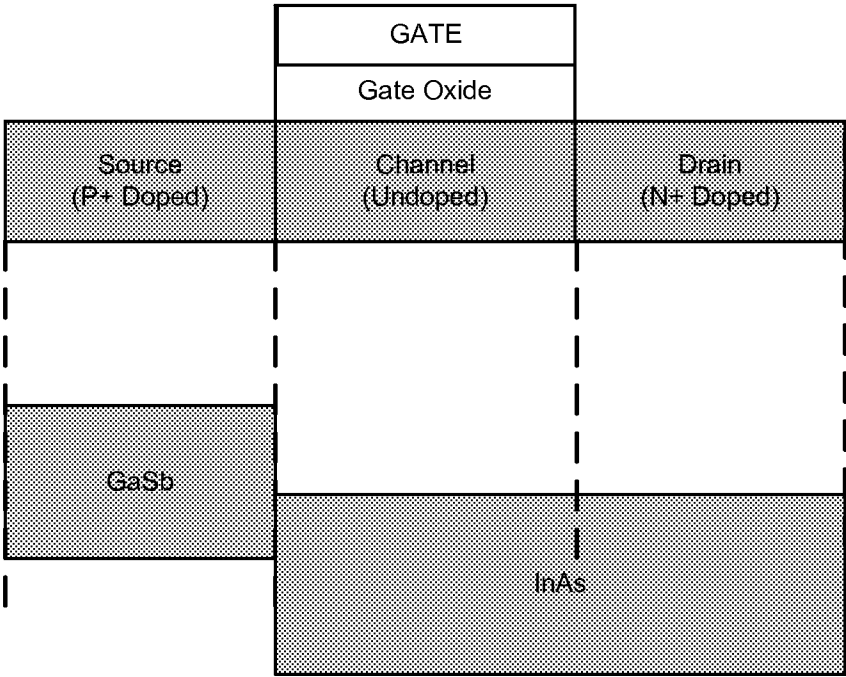


FIG. 3

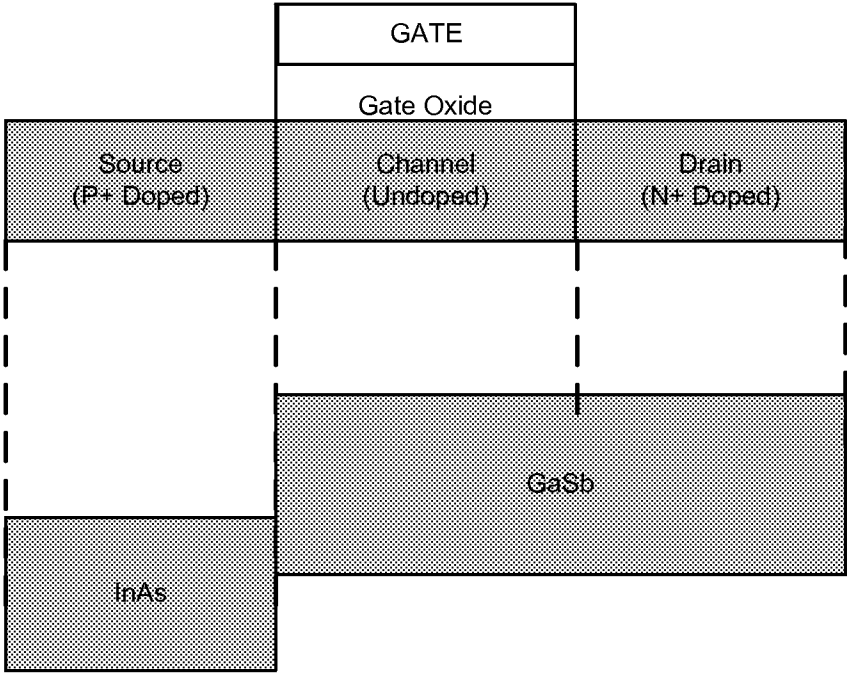


FIG. 4

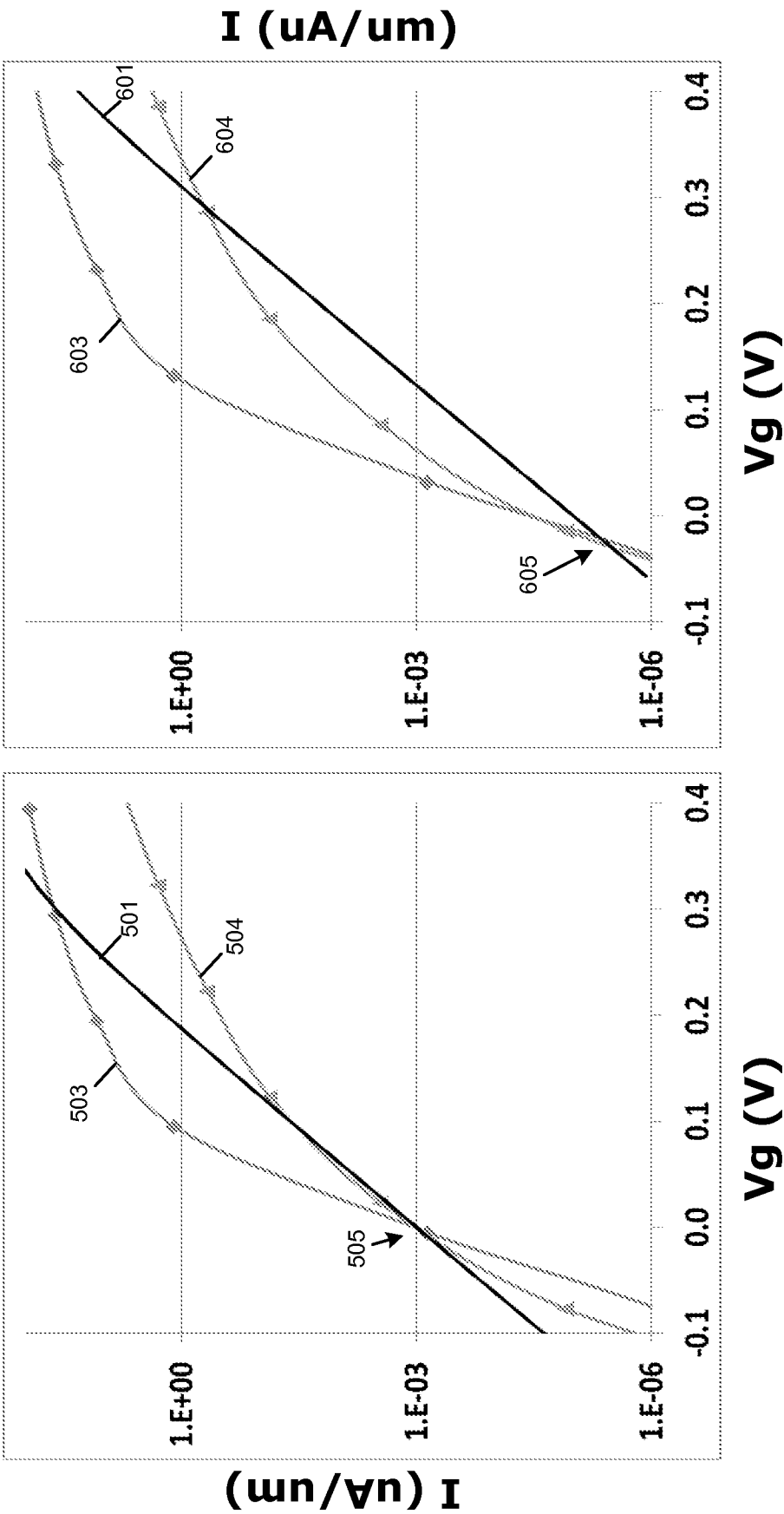


FIG. 5

FIG. 6

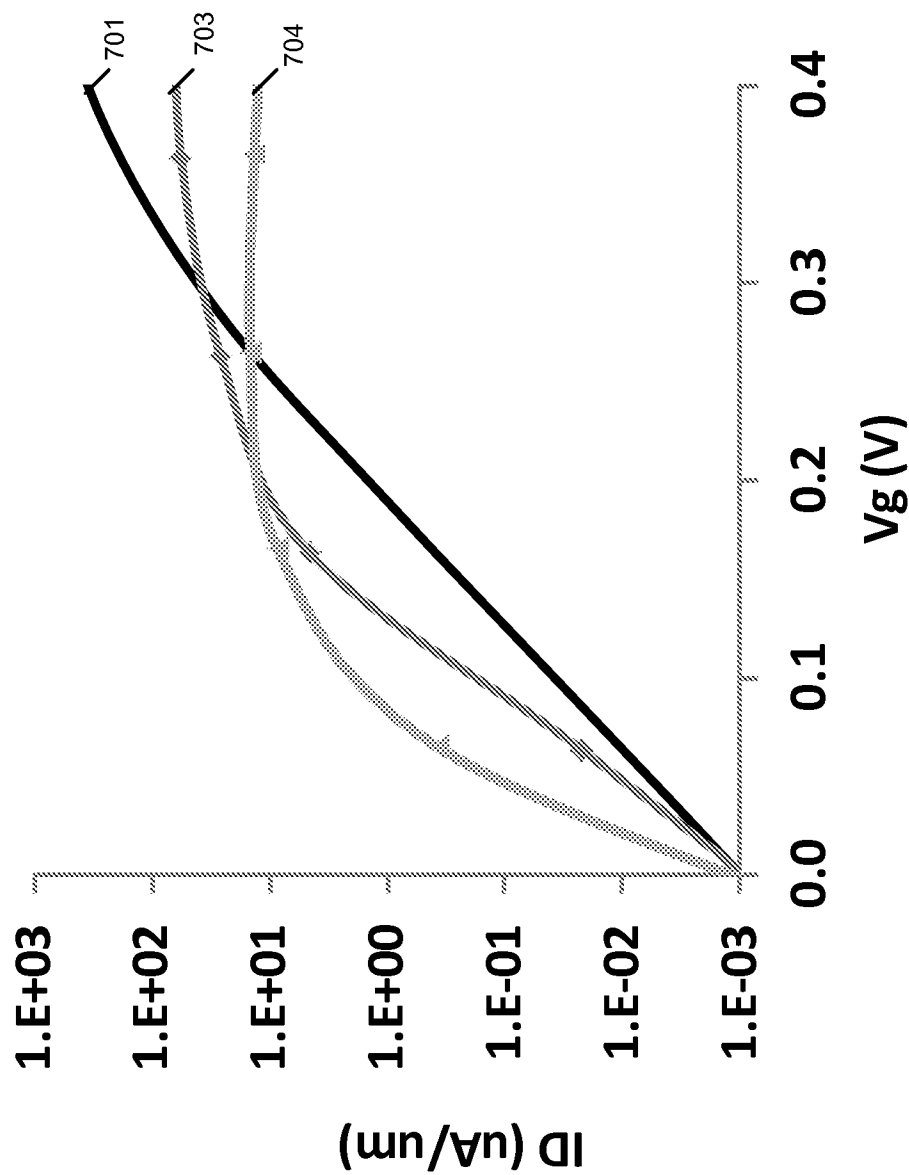


FIG. 7

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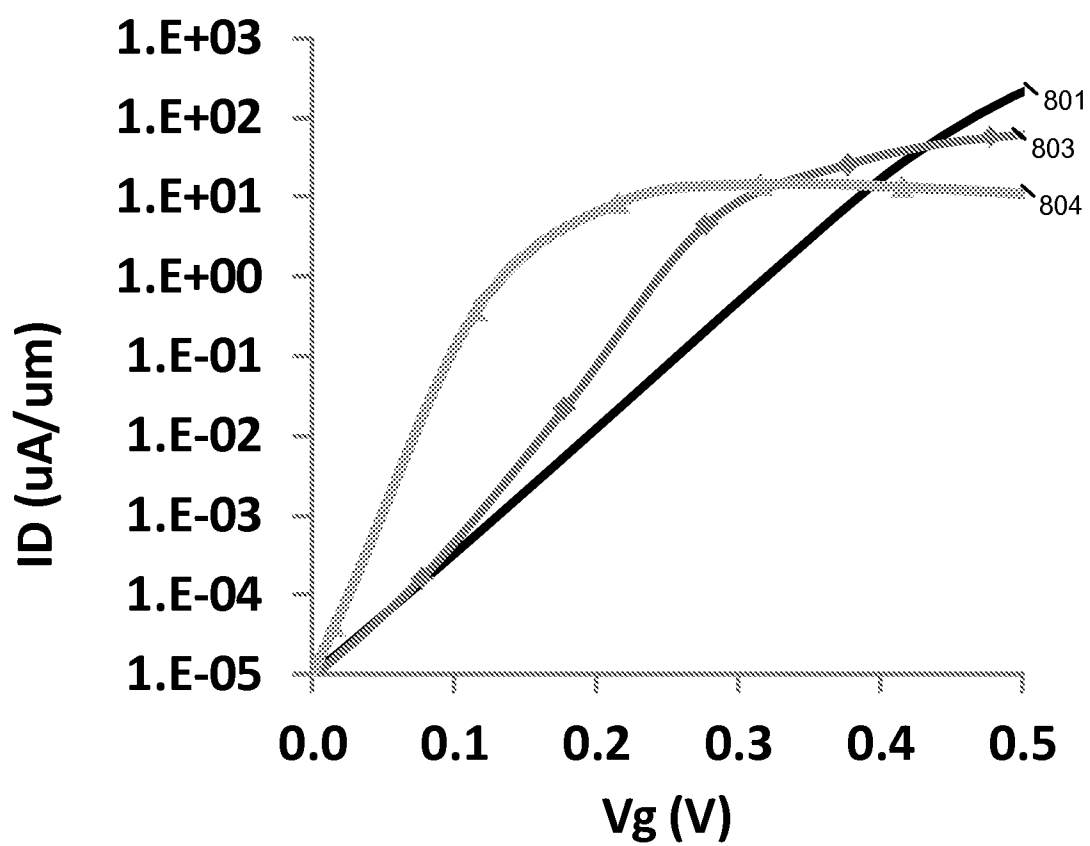


FIG. 8

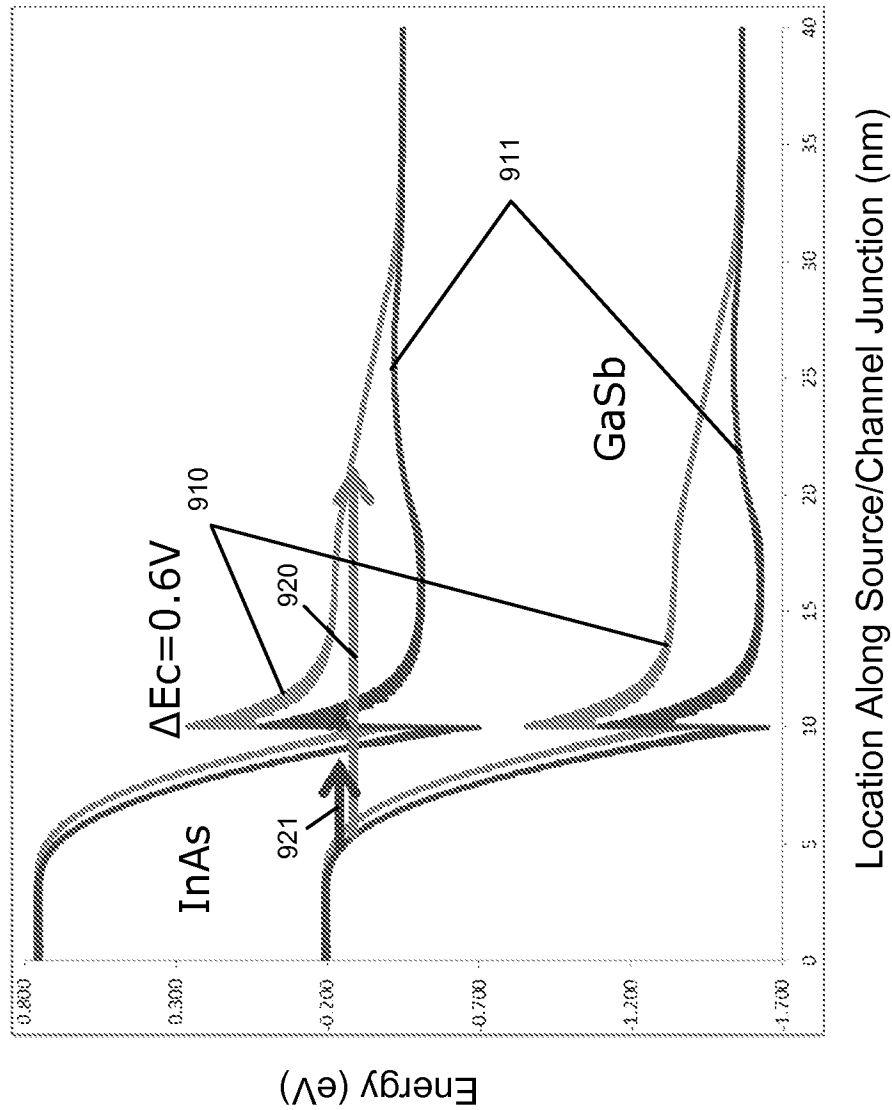


FIG. 9

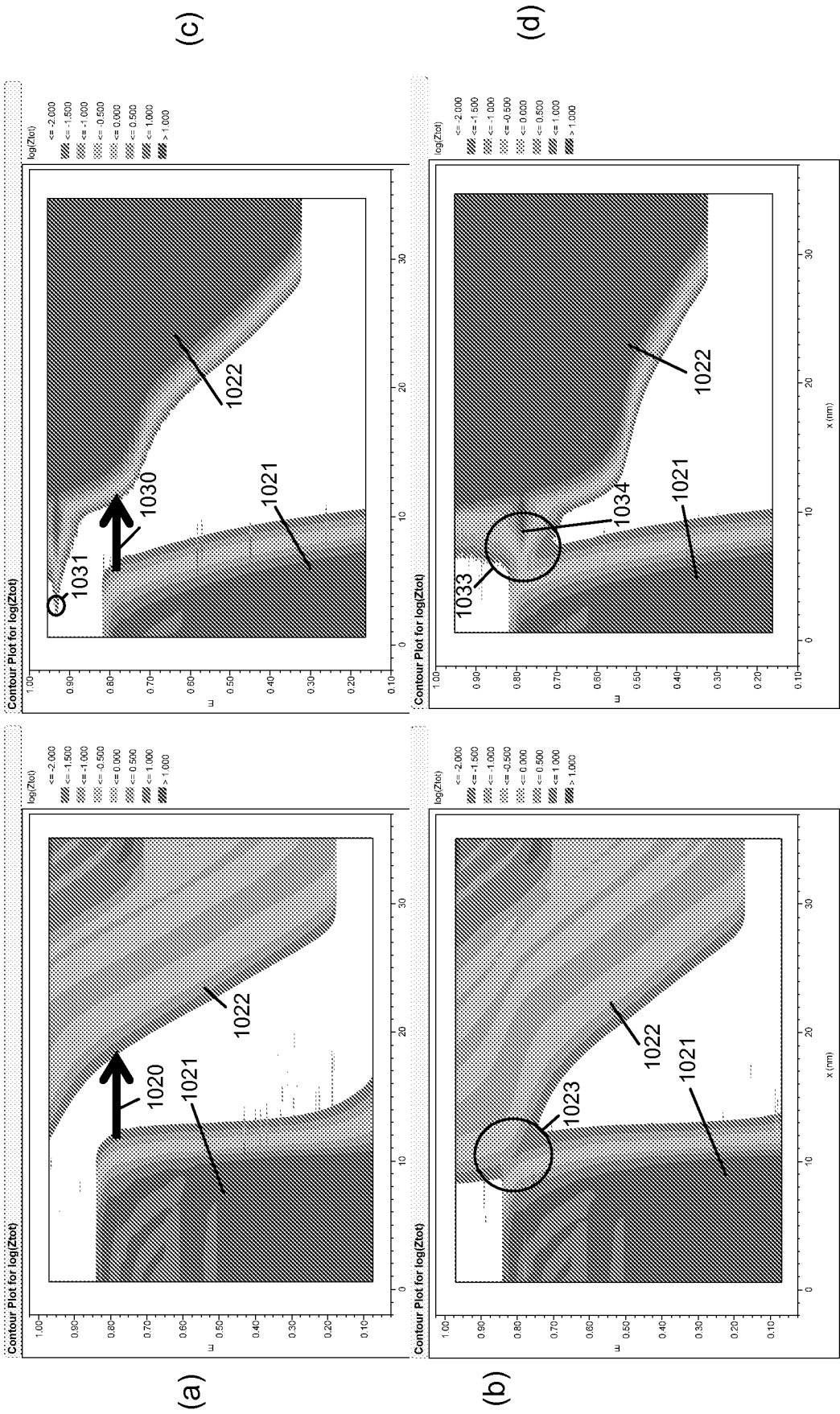


FIG. 10

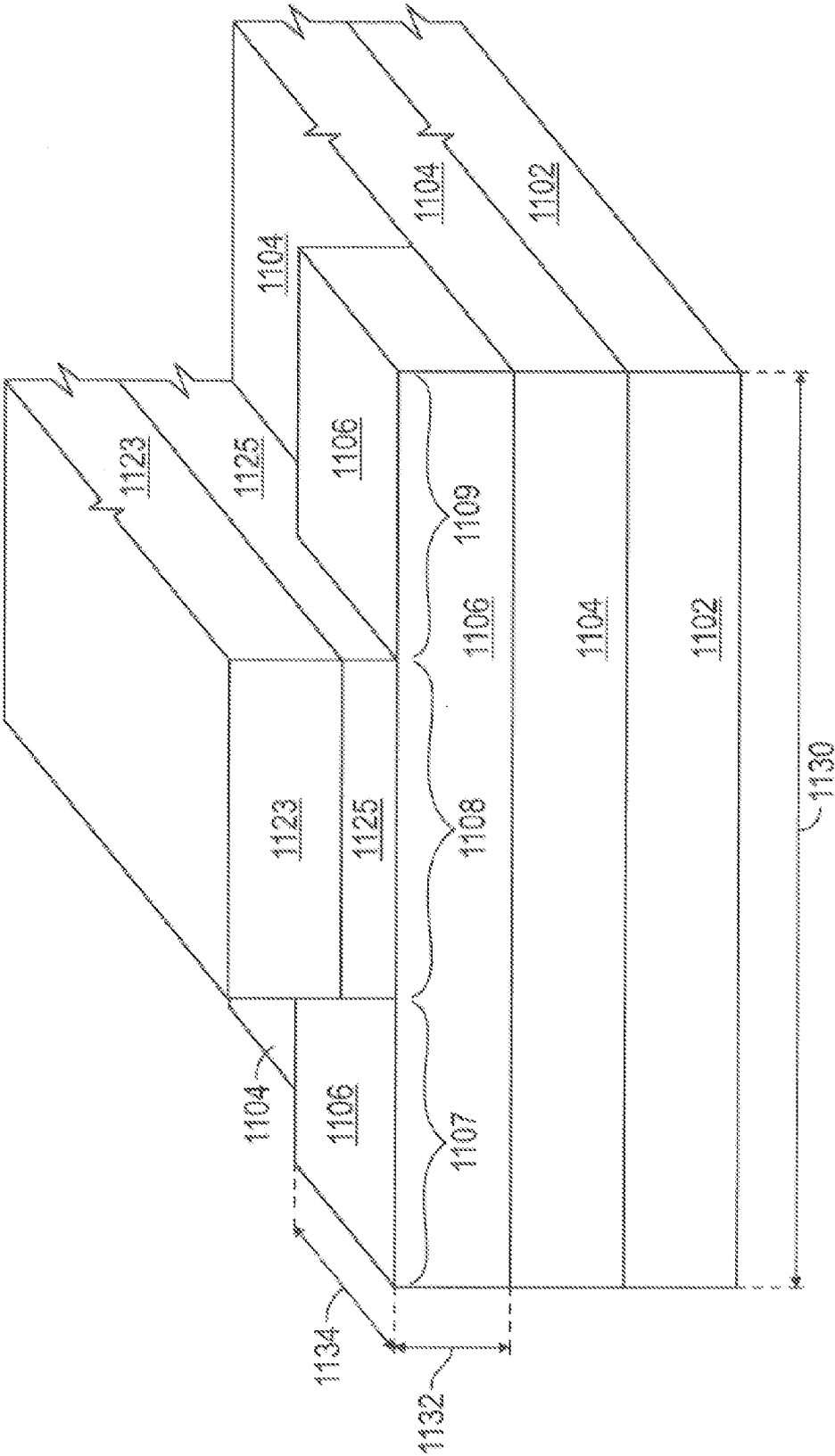


FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/048236**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/78(2006.01)i, H01L 21/336(2006.01)j**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
H01L 29/78; H01L 21/336; H01L 31/0352; H01S 5/00; H01L 29/15Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: TFET, reverse, hetero-junction, length, conduction band and sub-threshold**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	VINAY SARIPALLI et al. `An energy-efficient heterogeneous CMP based on hybrid TFET-CMOS cores` In: Design Automation Conference (DAC), 2011 48th ACM/EDAC/IEEE. New York: IEEE, 2011, ISBN 978-1-4503-0636-2, pages 729-734. See page 731, col. 1, lines 1 - 30, page 734, col. 1, lines 24-32, figures A(A)-(D).	1,3-7,9,12,17,19-20
A		2,8,10-11,13-16,18
Y	US 2008-0224224 A1 (WILLIAM G. VANDENDERGHE et al.) 18 September 2008 See abstract, paragraph [0121], claim 1 and figures 8A-8B.	1,3-7,9,12,17,19-20
A	US 2008-0050881 A1 (XIANGDONG CHEN et al.) 28 February 2008 See abstract, paragraphs [0074]-[0075], claim 1 and figure 6F.	1-20
A	US 2009-0224228 A1 (RAZEGHI MANIJEH) 10 September 2009 See abstract, paragraphs [0028]-[0031], claim 1 and figure 4.	1-20
A	KR 10-2008-0053094 A (ELECTRONICS AND TELECOMMUNICATIONS RESEARCH INSTITUTE) 12 June 2008 See abstract, paragraphs [0050]-[0052], claim 1 and figure 2b.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search
20 January 2014 (20.01.2014)Date of mailing of the international search report
20 January 2014 (20.01.2014)Name and mailing address of the ISA/KR
 Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City,
302-701, Republic of Korea
Facsimile No. +82-42-472-7140Authorized officer
KIM, Tae Hoon
Telephone No. +82-42-481-8407

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/048236

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