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[72] Inventor **Richard S. Sharp**
Sierra Madre, Calif.

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[73] Assignee **Burroughs Corporation**
Detroit, Mich.

[54] **FLIP-FLOP DISPLAY AND MANUAL CONTROL FOR BUS ORGANIZED COMPUTER**
14 Claims, 1 Drawing Fig.

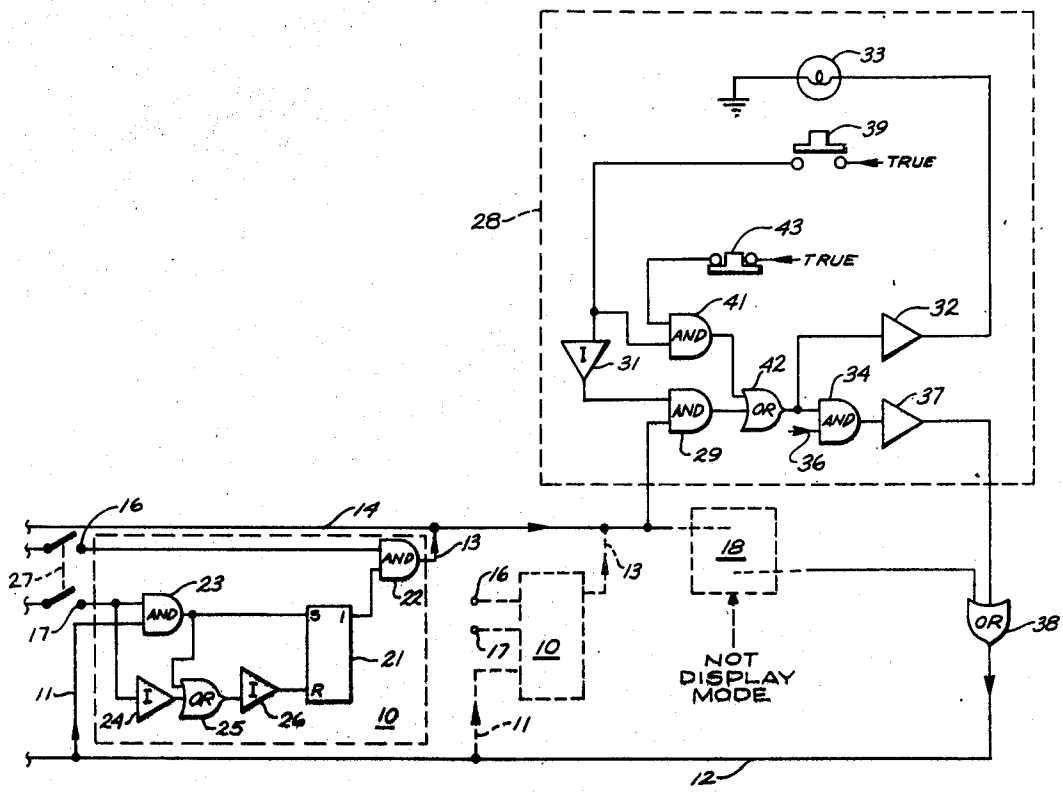
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[50] **Field of Search** 340/166

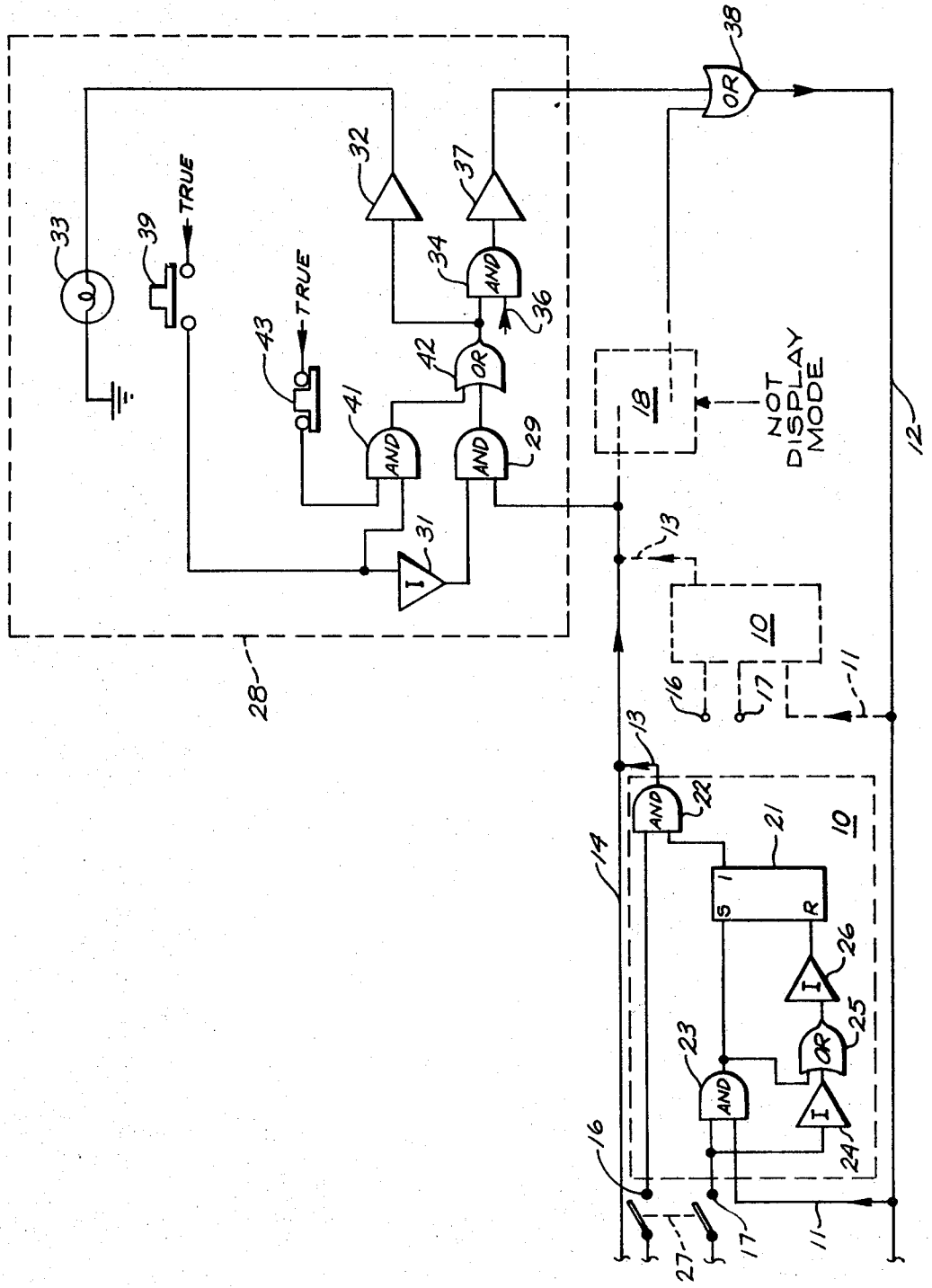
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Primary Examiner—Harold I. Pitts
Attorney—Christie, Parker and Hale

ABSTRACT: In a computer a plurality of flip-flops are connected to a common source bus and to a common destination bus. A combined display and manual control circuit is connected to the source bus and the destination bus in such a manner that the state of one of the flip-flops can be displayed and manually controlled as selected by an addressing means. In particular, means are provided for displaying a selected flip-flop and maintaining the state of that flip-flop, with logical provisions for manually over-riding the existing state and either setting or clearing the selected flip-flop, all with only a pair of leads between the combined circuit and the matrix of flip-flops.





INVENTOR.
RICHARD S. SHARP

BY

Christie Parker & Hale
ATTORNEYS

FLIP-FLOP DISPLAY AND MANUAL CONTROL FOR BUS ORGANIZED COMPUTER

BACKGROUND OF THE INVENTION

This invention is in the field of digital computers, registers and the like and in particular in a logical arrangement for selectively displaying and controlling individual flip-flops in a matrix.

In electronic data-processing units or computers it is often desirable to display the state of selected flip-flops in the computer and it is often desirable to provide a means for manual control in order to set or clear selected flip-flops. Although the display and manual control functions are not employed during the normal high-speed operation of the computer, the flip-flop display and manual control are of significant importance in debugging and testing computer operation.

It has been the practice to employ separate flip-flop display indicators and manual control push buttons for each flip-flop so that special separate connections are needed to the flip-flops in addition to the connections normally employed during operation of the computer. Thus, for example, the flip-flops may have an indicator or display output terminal and a manual control input terminal, with one assembly of an indicator and manual control push button employed for each individual flip-flop. In some cases, separate terminals for display and manual control are not available and conventional logical connections are employed.

When a large number of flip-flops are mounted on printed circuit boards, the requirement for separate display and manual control connections for each of the flip-flops depletes the number of available terminal connections on the board, so that there may not remain enough for other operating functions. Thus it becomes desirable to provide a combined display and manual control unit for a plurality of flip-flops. This not only permits a single unit to be employed with consequent saving of expense, but also reduces the number of leads required and hence the number of connections that must be made.

SUMMARY OF THE INVENTION

Thus in the practice of this invention according to a preferred embodiment there is provided a matrix of flip-flops having a common source bus connected to the several outputs of a number of flip-flops and a common destination bus connected to the several inputs of the same flip-flops. In such an arrangement a connection is provided for selectively addressing a particular flip-flop and operatively connecting its input and output terminals to the common busses. A display circuit is provided for displaying the state of the selected flip-flop and maintaining or restoring that state upon display. Combined with the display circuit is a logical circuit for selectively manually setting or clearing the selected flip-flop regardless of its original state.

DRAWING

Objects and many of the advantages of this invention will be readily appreciated as the same become better understood by reference to the following detailed description and considered in connection with the accompanying drawing which shows the logical diagram for a combined display and manual control selectively connectable to any of a plurality of commonly bussed flip-flops.

DESCRIPTION OF THE INVENTION

The drawing illustrates schematically a portion of a computer or other data processor or memory array constructed according to principles of this invention. As illustrated in this embodiment, a plurality of flip-flop circuits **10** are arranged in a matrix. As illustrated in this drawing only one of the flip-flop circuits is shown in detail and another is shown only schematically to indicate the presence of a series of such flip-flop circuits in a row of the matrix. A plurality of rows are involved in the entire organization of the computer.

An input lead **11** to each of the flip-flop circuits **10** is connected from a common destination bus **12**. Likewise, the output lead **13** from each of the flip-flop circuits **10** is connected to a common source bus **14**. A source address lead **16** is provided for each flip-flop circuit for selectively applying the state of a given flip-flop circuit **10** to the source bus **14**. Likewise, a destination address lead **17** is provided to each of the flip-flop circuits **10** for selectively applying the signal on the destination bus **12** to a given flip-flop circuit **10**. Thus in any row of flip-flop circuits in a matrix, the only required leads are address leads **16** and **17** for the flip-flops **10** in the row, plus one common or shared source bus **14**, and one common or shared destination bus **12**.

In the normal course of operation of such a data-processing unit, a signal applied to a source address lead **16** connects one of the flip-flop circuits **10** to the source bus **14**. The signal on the source bus is then applied to a logic function unit **18** indicated only schematically in the drawing since the logic function unit **18** forms no part of this invention. This logic function unit may be any conventional arithmetic, logic or similar unit. During the normal course of operation, the signal from the logic function unit **18** is applied to the destination bus **12**. During display mode the logic function unit is not connected to the destination bus.

A destination address signal may also be present on a destination address lead **17** to one or more of the flip-flop circuits **10** so that the addressed flip-flops are set or cleared in accordance with the signal on the destination bus. The individual flip-flop circuit **10** that serves as a source may or may not also serve as a destination. The signal from the logic function unit is usually but not always applied to a different flip-flop from the one serving as a source, and the signal may even be sent to a destination bus which serves a different row of a matrix.

A typical flip-flop circuit **10** includes set and reset functions in a bus organized data processor is illustrated in the drawing with additional similar flip-flop circuits **10** indicated only schematically. Each flip-flop circuit **10** has a conventional bistable flip-flop **21** having a set terminal S for setting the flip-flop to a **1** or on state, a reset terminal R for resetting the flip-flop **21** to a **0** or off state, and an output terminal I, which in conventional operation has a true state thereon when the flip-flop is on, and a false state thereon when the flip-flop is off. The true and false states in the apparatus are normally distinguished by different voltage levels.

The output terminal I of the flip-flop **21** is connected as an input to an AND gate **22** and the source address lead is also connected as the only other input to the AND gate **22**. The output of the AND gate forms the output **13** of the flip-flop circuit **10** and is connected to the source bus **14**. Thus when the selected flip-flop circuit **10** is addressed as a source by a true signal on the source address lead **16** the state of the flip-flop **21** is applied to the source bus **14**.

When the selected flip-flop circuit **10** is intended as a destination, a true signal is applied on the destination address lead **17** which is connected as one input to an AND gate **23**. The destination bus **12** is connected as the other input to the AND gate **23** by the input lead **11**, so that when the flip-flop circuit is addressed the state of the destination bus **12** is applied to the flip-flop **21** for setting or resetting.

The output of the AND gate **23** is connected to the set terminal S of the flip-flop **21** so that a true signal on both the address lead **17** and destination bus **12** sets the flip-flop. The destination address lead **17** is also the input to an inverting amplifier **24** the output of which is in turn connected as an input through an OR gate **25** to a second inverting amplifier **26**. The output of the inverting amplifier **26** is connected to the reset terminal R of the flip-flop. The output of the AND gate **23** is also connected through OR gate **25** as an input to the second inverting amplifier **26** so that when a true signal is applied to the set terminal S, a false signal is applied to the reset terminal R.

When a true signal is applied to the destination address lead **17**, the input to the second inverting amplifier **26** from the first

inverting amplifier 24 will always be false and the response of the second inverting amplifier will be determined by the state of the destination bus 14. If the destination bus has a true signal the output of the AND gate 23 is true thereby applying a true signal to the set terminal S and a false signal to the reset terminal R of the flip-flop 21. Conversely, when the destination bus 14 has a false signal, the output of the AND gate 23 is false and a false signal is applied to the set terminal S and a true signal is applied to the reset terminal R so that the flip-flop 21 is cleared to a zero or off state.

It will also be apparent that when there is a false signal on the destination address lead 17, the AND gate 23 will be false, the output of the first inverting amplifier 24 will be true, and the output of the second amplifier 26 will be false so that no change occurs in the state of the flip-flop 21 because both input terminals receive a false signal.

In order to display and optionally manually control a selected flip-flop circuit 10, true signals are applied to both the source address and destination address leads, 16 and 17, respectively, of the selected flip-flop by means of a rotary selector switch 27 or the like. Clearly, an automatic sequencing switch 27 can be employed if desired. By activating both the source address and the destination address of the same flip-flop, the state of the flip-flop can be displayed and also maintained. The address signals from the rotary selector switch 27 are true only in a display mode of computer operation, that is, in a nonnormal operating condition.

The combined display and manual control unit 28 has as its input a connection to the source bus 14 that serves as an input to a source AND gate 29. The other input to the source AND gate 29 is a normally true signal from an inverting amplifier 31. The output of the source AND gate 29 is connected by way of an amplifier 32 to an indicator lamp 33 or the like. The lamp is lighted when the source bus 14 carries a true signal from the flip-flop circuit 10, and the lamp is not lighted when the source bus carries a false signal due to the flip-flop circuit being off.

The output of the source AND gate 29 is also connected to a destination AND gate 34 which has a display mode lead 36 as its other input. Thus the output of the destination AND gate 34 can reflect the condition of the flip-flop 21 only when a true signal is applied on the display mode lead 36. The display mode lead 36 has a true signal when it is desired to display or control the state of the selected flip-flop; and during normal operation of the data processor the display mode lead is false and a false signal is provided at the output of the destination AND gate 34. This output is applied to an amplifier 37 which is in turn connected to the destination bus 12 by an OR connection 38 with the logic function unit 18. Thus during normal operation the logic function unit 18 controls the state of the destination bus 12, and during display mode the state of the destination bus is determined by the state of the selected flip-flop 21 since the logic function unit 18 would have no output signal during display mode.

In order to manually set or reset the flip-flop 21, a normally open (NO) pushbutton 39 is provided having a true signal as its input. The NO pushbutton 39 is connected as the input to the inverting amplifier 31 the output of which serves as one of the inputs to the source AND gate 29. The output of the inverting amplifier 31 is therefore normally true as hereinabove mentioned. When the NO pushbutton 39 is depressed and provides a true output, the input to the source AND gate 29 is false and the current state of the flip-flop 21 as carried by the source bus 14 is blocked so that the flip-flop can be selectively set or cleared without interference from the present state of the flip-flop.

In order to set the flip-flop 21, the NO pushbutton 39 is also connected to one input of a control AND gate 41, the output of which is connected in an OR relation 42 with the output of the source AND gate 29 to the input to the destination AND gate 34. The other lead to the control AND gate 41 is normally true so that when the NO pushbutton 39 is depressed the output of the control AND gate 41 is true, thereby applying a true signal to the destination AND gate 34, the amplifier 37, and the destination bus 12 to set the flip-flop 21 to a true or on state as hereinabove described.

In order to provide the manual reset function, the normally true lead to the control AND gate 41 has a normally closed (NC) pushbutton 43 connected to a true signal. When the NC push button 43 is open, its output is false. When it is desired to clear the flip-flop 21, both the pushbuttons 39 and 43 are depressed so that a false signal is applied to one lead of the control AND gate 41 by the NC pushbutton 43 and a false signal is also applied to one lead of the source AND gate 29 by the inverter 31. Thus the input to the destination AND gate 34 is assuredly false thereby applying a false signal to the destination bus 12 for clearing or resetting the flip-flop 21 as hereinabove described.

It might be noted that if the NC push button 43 is depressed without closing the NO pushbutton 39 that a false signal is applied to one lead of the control AND gate 41, however, a true signal is still applied to one lead of the source AND gate 29 and the output thereof will still reflect the original state of the flip-flop 21 so that that state is maintained.

A single NC push button 43 is all that is needed for the entire matrix and is shared by the several display and manual control units corresponding to rows of flip-flops. Thus a matrix may have 24 or more rows of flip-flop circuits with a source bus and destination bus for each row and a single display and control unit for each row. Each of these units would include one NO pushbutton 39 since this determines which row is being manually controlled. The shared NC pushbutton 43 determines the function of the NO pushbutton 39, that is, whether the selected flip-flop is set when the NC pushbutton is closed or reset when the NC pushbutton is open. Depressing the shared NC pushbutton 43 has no effect unless the NO pushbutton 39 in a selected control unit is also depressed.

Although but one example of a combined display and manual control unit has been provided in the description, it will be apparent to one skilled in the art that many modifications and variations can be made in such a combined unit for a bus organized flip-flop matrix and still remain within the principles of this invention.

What is claimed is:

1. A plurality of flip-flops:
   - a common source bus selectively connectable to the outputs of the plurality of flip-flops;
   - a common destination bus selectively connectable to the inputs of the plurality of flip-flops;
   - address means for selecting one of the flip-flops for connection to the source bus and to the destination bus;
   - display means connected to the source bus for displaying the state of the selected flip-flop and connected to the destination bus for maintaining the state of the flip-flop; and
   - control means connected to the destination bus for selectively manually setting and clearing the selected flip-flop.

2. A combination as defined in claim 1 wherein the display means comprises:
   - an indicator connected to the source bus;
   - a destination AND gate having the source bus as an input;
   - means for applying a display enable signal as another input to the destination AND gate; and
   - means for connecting the output of the destination AND gate to the destination bus so that the state of the selected flip-flop applied to the source bus is applied to the selected flip-flop input for maintaining the state of the flip-flop.

3. A combination as defined in claim 2 wherein the control means comprises:
   - an OR gate connected to the destination AND gate input from the source bus;
   - a control AND gate having its output connected to the OR gate;
   - means for normally applying a first true signal to the control AND gate; and

means for manually applying a second true signal to the control AND gate, whereby a true signal is applied to the destination AND gate regardless of the state of the selected flip-flop.

4. A combination as defined in claim 3 wherein said control means further comprises:

a source AND gate interposed between the source bus and the destination AND gate;

means for applying a normally true signal to an input to the source AND gate so that the output thereof normally is the same as the state of the selected flip-flop; and

means for manually removing the normally true signal from the input to the source AND gate so that the output thereof is false for blocking the state of the selected flip-flop from affecting the destination AND gate.

5. A combination as defined in claim 4 wherein said control means further comprises:

means for manually removing the first true signal to the control AND gate, whereby the output thereof is false;

both of said means for manually removing being separately and simultaneously operable whereby, upon simultaneous operation of both means for manually removing, a false signal is applied to the input of the destination AND gate regardless of the state of the selected flip-flop.

6. A combination as defined in claim 1 wherein the control means comprises:

a source AND gate, the source bus being connected as an input to the source AND gate;

an inverting amplifier, the output of the inverting amplifier being connected as an input to the source AND gate;

a normally open pushbutton connected to the input of the inverting amplifier, and normally connected to the output of the source AND gate;

normally true lead connected to the normally open pushbutton;

a destination AND gate having an input connected to the output of the source AND gate, and an output connected to the destination bus; and

a display mode enable lead connected as an input to the destination AND gate.

7. A combination as defined in claim 6 wherein the control means further comprises a control AND gate interposed between the normally open pushbutton and the input to the destination AND gate so as to have the normally open pushbutton as an input, and the destination AND gate as the output;

a normally closed pushbutton connected to another input to the control AND gate; and

a normally true lead connected to the normally closed pushbutton.

8. In a flip-flop matrix having a source bus common to a plurality of flip-flops, a destination bus common to the plurality of flip-flops, and means for selectively addressing an individual flip-flop, the improvement comprising;

a combined flip-flop display and manual control unit connected to the flip-flops only by way of the common source bus and the common destination bus for displaying an addressed flip-flop in the matrix and selectively manually setting and clearing the addressed flip-flop.

9. A combined unit as defined in claim 8 comprising:

an indicator connected to the source bus;

a destination AND gate having the source bus as an input;

means for applying a display enable signal as another input to the destination AND gate; and

means for connecting the output of the destination AND gate to the destination bus so that the state of the selected flip-flop applied to the source bus is applied to the destination bus for maintaining the state of the selected flip-flop.

10. A combined unit as defined in claim 9 further comprising:

an OR gate connected to the destination AND gate input from the source bus;

a control AND gate having its output connected to the OR gate;

means for normally applying a first true signal to the control AND gate; and

means for manually applying a second true signal to the control AND gate whereby a true signal is applied to the destination AND gate regardless of the state of the selected flip-flop.

11. A combination as defined in claim 10 wherein the combined unit further comprises:

a source AND gate interposed between the source bus and the destination AND gate;

means for applying a normally true signal to an input to the source AND gate so that the output thereof normally is the same as the state of the selected flip-flop; and

means for manually removing the normally true signal from the input to the source AND gate so that the output thereof is false for blocking the state of the selected flip-flop from affecting the destination AND gate.

12. A combined unit as defined in claim 11 further comprising:

means for manually removing the first true signal to the control AND gate, whereby the output thereof is false;

both of said means for manually removing being separately and simultaneously operable whereby, upon simultaneous operation of both means for manually removing, a false signal is applied to the input of the destination AND gate regardless of the state of the selected flip-flop.

13. A combination as defined in claim 8 wherein the control means comprises:

a source AND gate, the source bus being connected as an input to the source AND gate;

an inverting amplifier, the output of the inverting amplifier being connected as an input to the source AND gate;

a normally open pushbutton connected to the input of the inverting amplifier, and normally connected to the output of the source AND gate;

a normally true lead connected to the normally open push button;

a destination AND gate having an input connected to the output of the source AND gate, and an output connected to the destination bus; and

a display mode enable lead connected as an input to the destination AND gate.

14. A combination as defined in claim 13 wherein the control means comprises:

a control AND gate interposed between the normally open pushbutton and the input to the destination AND gate so as to have the normally open pushbutton as an input, and the destination AND gate as the output;

a normally closed pushbutton connected to another input to the control AND gate; and

a normally true lead connected to the normally closed pushbutton.