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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : G01L 9/00	A1	(11) International Publication Number: WO 93/18382
		(43) International Publication Date: 16 September 1993 (16.09.93)

(21) International Application Number: PCT/US93/01952

(22) International Filing Date: 5 March 1993 (05.03.93)

(30) Priority data:
07/847,690 6 March 1992 (06.03.92) US

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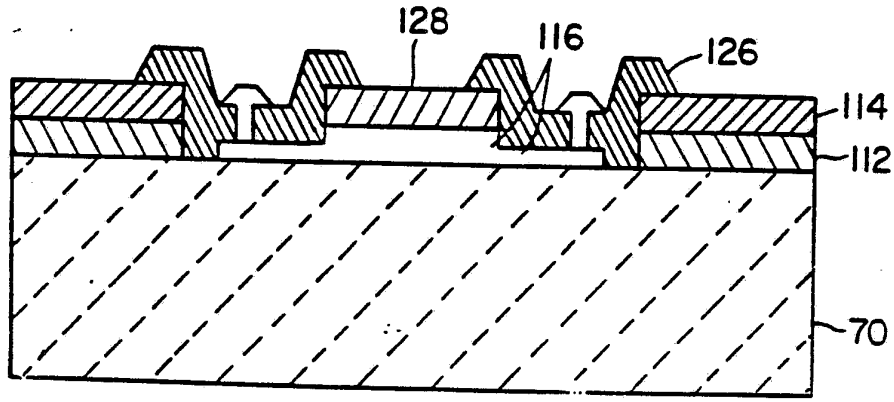
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(81) Designated States: CA, JP, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: SOI ACTUATORS AND MICROSENSORS



(57) Abstract

The present invention relates to the fabrication of diaphragm pressure sensors utilizing silicon-on-insulator technology where recrystallized silicon forms a diaphragm which may incorporate electronic devices used in monitoring pressure. The diaphragm is alternatively comprised of a silicon nitride having the necessary mechanical properties with a recrystallized silicon layer positioned thereon to provide sensor electronics.

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SOI ACTUATORS AND MICROSENSORS

Background of the Invention

The present invention relates to the field of pressure sensors, and more particularly to the field of diaphragm sensors using silicon-on-insulator (SOI) technology.

The use of pressure sensors or transducers has found numerous applications in a variety of fields in which it is desirable to monitor fluid flow, liquid level or pressure. The electronics industry has attempted to accommodate the need for low-cost and dependable sensors by utilizing integrated circuit (IC) fabrication techniques in the design and manufacture of microfabricated diaphragm transducers on IC chips. The basic types of silicon pressure transducers include (1) piezo-junction devices, (2) piezoresistive sensors, and (3) capacitive pressure transducers.

Piezoresistive sensors have been formed in polycrystalline silicon, laser recrystallized silicon and bulk single crystal silicon. The resistors have been fabricated by dopant implantation followed by annealing and metallization. The diaphragm of the sensor has been separately formed by patterning a silicon wafer with an oxide insulator, depositing polycrystalline silicon over the insulator/wafer surface and removing the oxide from between the diaphragm and the wafer.

A microfabricated capacitive pressure transducer is formed, for example, by diffusing a dopant into a region in a silicon wafer that serves as a lower electrode, and forming a compliant diaphragm of polysilicon as a second electrode that is separated from the diffused region by an oxide spacer. The oxide spacer can be removed by

etching through an opening in the backside of the wafer. See R.S. Hijab and R.S. Muller, "Micromechanical Thin-Film Cavity Structures For Low Pressure and Acoustic Transducer Applications," IEEE, CH 2127, 178, September, 1985.

Summary of the Invention

A method of forming a microfabricated pressure sensor in which a compliant membrane is formed that encloses a sacrificial insulating material. The insulating material is subsequently removed through an opening in the membrane to form a pressure sensitive diaphragm. Electrical elements are positioned in a single crystal silicon layer formed on or in the diaphragm to detect movements thereof and produce electrical signals proportional to the diaphragm displacement. The single crystal layer is formed by depositing a polycrystalline silicon layer and then zone-melt recrystallizing the film to form a high quality single crystal silicon suitable for CMOS circuitry.

The method can be used to form both silicon and silicon nitride diaphragm pressure sensors. An oxide is formed on a semiconductive wafer such as silicon using a local oxidation of silicon (LOCOS) planar process. A silicon nitride or polysilicon layer is formed over a region of the oxide. Electrical elements such as piezo-resistors are formed over the nitride or silicon layers respectively and one or more holes are etched through the layer to permit removal of the oxide spacer with a suitable etchant. Removal of the oxide insulator forms a cavity between the nitride or silicon layer such

that the layer forms a diaphragm that is highly sensitive to pressure variations to which the diaphragm is exposed. The holes or openings in the diaphragm are then sealed. The displacement of the diaphragm and the resulting electrical signals generated by piezo-resistors is directly correlated with changes in pressure. Any suitable transducer can be formed in the diaphragm structure, or alternatively, a capacitive type of transducer can be formed using electrodes formed in the diaphragm and the silicon wafer. Implanted piezo-resistors can be formed in a standard Wheatstone bridge arrangement used in microsensor systems. Other integrated circuits, driving elements or signal processing circuits can be fabricated in the recrystallized material to produce so-called "smart" microsensors.

A number of additional features can be integrated with "smart" microsensor systems such as selfcalibration, system diagnostics, and redundant systems.

The removal of the LOCOS oxide to produce a silicon diaphragm is accomplished by performing an anisotropic etch, for instance, preferably in the center of the diaphragm, to expose a small surface area of the oxide. An oxide etch is applied through the opening in the diaphragm which removes the underlying oxide. Where the diaphragm is comprised of a silicon nitride, one or more holes can be formed along the periphery of the diaphragm to expose a portion of the underlying oxide.

The above, and other features of the invention including various novel details of construction and combination of parts, will now be more particularly

described with reference to the accompanying drawings and pointed out in the claims. It will be understood that the particular method of fabricating silicon-on-insulator pressure sensors embodying the invention is shown by way of illustration only and not as a limitation of the invention. The principal features of this invention may be employed in various embodiments without departing from the scope of the invention.

Brief Description of the Drawings

Figures 1A-1E illustrate, in a series of cross-sectional views, the steps used in the fabrication of a silicon diaphragm pressure sensor of the present invention.

Figures 2A-2F illustrate the steps used in the fabrication of a nitride diaphragm pressure sensor of the present invention.

Figure 3 illustrates in a cross sectional view a sealed silicon nitride sensor with an electrode implanted in the substrate to provide a capacitive transducer.

Figure 4 illustrates in a cross sectional view a preferred embodiment of a silicon diaphragm pressure sensor having a patterned channel sealant.

Figure 5 is a graphical illustration plotting the leakage current versus the inverse temperature for both bulk and SOI MOSFETs.

Figure 6 is a cross-sectional view illustrating the use of an underlying oxide as an etch stop.

Figure 7 is a cross-sectional view illustrating the use of an oxide layer to fully isolate the sensor elements and electronics.

Figure 8 is a cross-sectional view of a sensor suspended using a polynitride structure.

Figure 9 is a cross-sectional view of a preferred embodiment in which the epitaxial layer is used as the sensor diaphragm.

Figure 10 is a cross-sectional view of a differential pressure sensor.

Figure 11 is a perspective view illustrating an epitaxial bridge structure.

Figure 12 is a perspective view illustrating a cantilever sensor structure.

Figure 13 is a perspective view illustrating an alternate method of fabricating the cantilever structure.

Figures 14A-14E illustrate a process for forming a crystallized silicon sensor device.

Figures 15A and 15B are side and top views of a diaphragm sensor.

Figure 16 is a perspective view of a cantilever accelerometer.

Figure 17 is a perspective view illustrating capacitive type accelerometer.

Figures 18A-18H illustrate another preferred method of fabricating a capacitive sensor in which the silicon layer is used as the sensor diaphragm.

Figures 19A-19C illustrate another preferred method of fabricating a clamp using a nitride layer.

Figure 20 illustrates a side view of a cantilever beam supported by a clamp.

Figure 21 illustrates a diaphragm supported by multiple clamps.

Detailed Description of the Invention

The silicon diaphragm pressure sensor of the present invention is the simplest type to fabricate in SOI technology. The ISE (isolated silicon epitaxy) process described below produces a film that is ideal for sensor applications, particularly because it can produce a diaphragm under very slight tensile stress. ISE technology is based upon existing processes known as lateral epitaxy by seeded solidification (LESS) and zone-melt recrystallization (ZMR). U.S. Patent No. 4,371,421 entitled "Lateral Epitaxial Growth by Seeded Solidification" describes these processes in greater detail. The ISE process has produced wafers of semiconductor material having low defect density, low warpage and no measurable impurities. Since the ISE material is extremely high quality, piezoresistors fabricated in this material to produce SOI microsensors have properties as good as, or exceeding those obtainable with bulk materials.

Figure 1 is a process flow diagram illustrating the fabrication of a silicon diaphragm pressure sensor. Silicon oxide grown using a high temperature LPCVD process is deposited on a silicon wafer 10 and patterned into an array of rings 12 which will ultimately represent the perimeter of the diaphragms. One such ring 12 is shown in the cross-sectional view of Figure 1A (with background sections removed for clarity). Each ring 12 need not necessarily be circular in shape, but could be square or some other shape. Note, however, that the preferred embodiment produces a circular diaphragm.

A layer 14 of oxide is then grown on the exposed silicon by a local oxidation of silicon planar process. In this process, the nitride ring 12 acts as a mask and prevents the growth of oxide on the silicon surface beneath the nitride. This process is often referred to as LOCOS, for local oxidation of silicon (Figure 1B). After LOCOS, the nitride ring 12 is stripped down to the silicon to form a support surface or ring 15 and a high purity polysilicon layer 18 is then deposited by LPCVD (liquid phase chemical vapor deposition) over the entire wafer (Figure 1C).

The polysilicon layer 18 is now capped with another silicon oxide film (not shown) and subjected to zone-melt recrystallization (ZMR). This process, which is described below in greater detail, converts the polysilicon 18 to a thin film layer of high quality single crystalline silicon. This layer 18 is suitable for the fabrication of high density CMOS circuits and, in particular, for the fabrication of piezoresistive elements 16. These devices 16 and other additional circuits are fabricated in the ISE layer 18 at this point, using standard SOI circuit fabrication technology.

A preferred embodiment of the present method utilizes zone-melt recrystallization, however, other types of crystallization procedures such as laser recrystallization, can also be used. One type of system for zone-melt recrystallization uses a scanning line heating source that is translated across the material to be recrystallized and a second heating system to raise the temperature of the entire sample close to the melting point of the material. As the line heater is activated,

it induces melting of a zone in the sample directly beneath the heater. The line heater is then translated across the surface of the sample causing the melted zone to move in unison with the heater. As the melted zone moves past a portion of the sample, the melted sample solidifies and results in lateral epitaxial growth of a single crystal structure. The diaphragm that results may be a simple layer or a multi-layered structure which includes the recrystallized film. The diaphragm is secured along its periphery, either directly to the substrate material or to intermediate layers which partially enclose the cavity in which the diaphragm moves.

After circuit processing, the wafer is coated with a second silicon nitride (or oxide) layer 20 for passivation and to protect the circuitry during subsequent processing. As shown in Figure 1D, the nitride is patterned and the silicon diaphragm 18 is anisotropically etched to form a pit or opening 22 which exposes a small portion of the underlying oxide. This step is critical as the opening 22 in the diaphragm needs to be kept as small as possible, perhaps only a fraction of a micron, so that it can easily be sealed later on. Preferably more than one opening can be used to simplify oxide removal, however, only one is illustrated here. An anisotropic silicon etch is employed to form the opening 22 in order to ease the lithographic stress. This etchant forms etch pit sidewalls 28 and 29 which slope at about 55°, gradually narrowing with depth. Therefore, the pit will be wider at the top than at the bottom. This structure results in a more stable seal in which the

sidewall geometry prevents movement of the sealing material into the sensor cavity. Note that while the opening 28 is located in the center of the diaphragm, other locations in the diaphragm can be used.

At this point, the wafer will be exposed to a concentrated HF etchant which attacks the silicon oxide 26, even through very small holes. Once the oxide is consumed, the HF exits the cavity 27 due to surface energy considerations. Only the oxide under the diaphragm is etched since it is completely isolated by the ring 15 from the surrounding oxide layer (Figure 1D).

Finally, the hole in the diaphragm is sealed with a layer 24 of material using an LPCVD process (Figure 1E). Any number of materials could be deposited including: TEOS (Tetraethyloxysilicate), a low temperature oxide, a silicon nitride, polycrystalline silicon, etc. Alternatively, thermal oxidation could be used to seal the hole. This layer 24 may be patterned to limit its extent and therefore its effect on the properties of the diaphragm. Existing silicon diaphragm sensors have tended to remove the oxide spacer either through an opening in the substrate, or laterally from the side of the diaphragm. The present device opens the moving portion of diaphragm to remove the oxide and then seals the opening. This structure operates to shift the stress experienced by the diaphragm in a manner that can enhance sensor performance depending upon the specific operating conditions. The sealing material 24 can thus function as a "stress riser" by locating the resistors 16 at locations of higher stress in the diaphragm by using specific patterns of the material 24.

For example, Figure 4 shows a sensor having a substrate 70, an oxide insulator 78, a single crystal diaphragm 80 located in the recrystallized layer 76 having two or more piezoresistive elements 82, a nitride cap 74, and a patterned sealant 72. The sealant 72 has a stiffness greater than the silicon of the diaphragm 80 so that as the diaphragm 80 is displaced under pressure, the silicon portions of the diaphragm 80 will undergo greater strain. The piezoresistive elements 82 will thus experience greater stress than would normally occur.

Figure 4 also illustrates the introduction of additional electronic components 84 and 86 into the recrystallized layer 76 adjacent the diaphragm 80. The components 84 and 86 could be used to introduce higher levels of circuit functionality into the sensor to provide, for example, self-calibration of the sensor, diagnostic or computational capabilities, compensation for non-linear characteristics or communication with other systems. Also due to the small size of each sensor, a number of sensors could be used to provide redundancy, where the failure of any one sensor could be detected and its output electronically rejected.

A silicon nitride diaphragm pressure sensor could be fabricated using a process flow similar to the one described above. As illustrated in Figures 2A-2F, the process sequence starts with a patterned silicon nitride 32 formed on a silicon wafer 30, and a LOCOS oxide 34, which in this case defines the region which will eventually be under the diaphragm (Figures 2A and 2B).

In Figure 2C, the nitride 32 has been repatterned and etched back away from the oxide area 34 to create a

greater perimeter around the diaphragm. The wafer is again oxidized but this time to a much lesser extent, perhaps as little as 2000A, to form a thin peripheral layer 36 through which the LOCOS oxide is later removed. The silicon nitride, which forms the diaphragm material, is now deposited as layer 38. This must be a high quality silicon nitride layer and is likely to be deposited using an LPCVD process. This nitride diaphragm must have the appropriate mechanical properties including a controlled thickness so that a well-defined relationship exists between applied pressure and the resulting displacement or strain of the diaphragm.

In Figure 2D, the nitride is capped with a thin oxide layer 40. This oxide layer 40 can be deposited using any number of techniques or may be thermally grown on the nitride. This layer 40 serves to protect the polysilicon from the nitride during the recrystallization step. Next, polysilicon is deposited, capped and zone-melt recrystallized to form a single crystal silicon layer 42. The capping layer must be removed (not shown) prior to fabrication of device elements. In Figure 2E, the resistors 44 are patterned and any additional electronics are fabricated in the recrystallized silicon 46 that remains around the periphery of the diaphragm.

Holes 48 are then etched down to the thin oxide layer 36 as shown in Figure 2F. These holes provide a path for the subsequent HF etch, which will be used to remove the oxide 34 from beneath the diaphragm to form cavity 50. The sensor is completed when a passivation layer is deposited and the etchout holes sealed.

If the sensor is to be a capacitive type, the resistors would be replaced with a counter electrode and a substrate contact is used to provide the capacitive transducer. Figure 3 illustrates a capacitive type transducer in which a dopant is implanted in the wafer 64 in layer 65 prior to diaphragm fabrication to form an electrode 62 in the substrate underneath the cavity 60. The holes have been sealed using a deposited silicon nitride 68 or any of the processes referenced above in connection with Figure IE. The electrodes 66 serve as counterelectrodes in the capacitive circuit.

Calibration of a sensor is essential to its proper performance. The usual approach is to connect the sensor to a calibration standard and to adjust the zero (or offset) and full-scale (or gain) values by first applying a minimum pressure level and adjusting the zero, and then applying a maximum pressure level and adjusting the span. In traditional sensors, this involves either adjusting potentiometers or trimming resistors which are components in the amplification circuit. A preferred embodiment of the present sensor uses a programmable memory to store information about the zero and span. With this type of sensor one can readjust the values after the sensor has been in use for a period of time and may have drifted out of calibration. This readjustment can be performed without removing the sensor from its location. This provides greater serviceability for the system.

A further embodiment employs a sensor having circuitry that can perform self-diagnostic functions. This capability provides information such as whether the device is either shorted or open. In this event, any

error can be compensated for in a sensor system having redundancy. The sensors can be extremely small with diameters in the tens of microns so that many sensing elements can be associated with one sensor chip. If one sensor fails, the error is reported and a new sensing element is brought on-line.

With sufficient computational power, the sensor can take environmental effects into consideration. For example, piezoresistive pressure sensors are well known to have significant temperature coefficients. Normally, the current through the sensing bridge is used to compensate for the temperature dependence of the pressure reading using an analog circuit. With the present sensors, environmental effects are compensated for during calibration. Even a very non-linear environmental effect is corrected by providing the sensor with a programmed process and tabulated data which describes the effect. This method can also be applied to the intrinsic non-linearity of the sensing element itself. In both the capacitive and piezoelectric type sensors, the output is not a linear function of the applied pressure which can be corrected using this procedure.

Communications in a noisy environment can be a problem for sensor applications. Incorporating digital communication components, particularly microprocessor based circuits, can provide the best combination of noise immunity and error detection possible.

In a preferred method of fabrication, the materials and processes found in a typical integrated circuit fabrication can be used to make microsensors. These

sensors are therefore "compatible" with the integrated circuit fabrication process.

Polysilicon has been employed as the diaphragm material in one embodiment. Polysilicon is normally used in conjunction with gates in CMOS and NMOS circuits. A significant problem to be addressed with the use of this material was the internal stress in the polysilicon. To solve this problem, careful analysis of the deposition conditions was conducted and the appropriate conditions determined for the deposition of polysilicon with a slight tensile stress. Diaphragms with a tensile stress tend to stretch themselves taut while diaphragms with compressive stress will buckle. Both piezoresistive and capacitive pressure sensors have been fabricated having diaphragms under tensile stress.

As indicated previously, the devices of the present invention can be fabricated in SOI using conventional CMOS fabrication techniques. These devices have demonstrated substantially better high temperature characteristics than equivalent bulk devices. SOI wafers have excellent characteristics for use as a high temperature material due to its good crystal quality and high purity. Measurements on large (gate width to length ratio W/L = 400/10) enhancement mode MOS transistors have indicated much lower leakage current for devices fabricated in SOI wafers versus equivalent devices fabricated in bulk silicon. Figure 5 shows a plot of the leakage current versus inverse temperature for both a bulk device and an SOI device. The significant improvements in the leakage current obtained for SOI device provide important advantages for sensors

fabricated with SOI material including high temperature operation of sensors and associated circuitry, CMOS compatible processing, simple sensor fabrication, much smaller size compared to conventional sensor technologies, redundancy of sensor elements, capability of multiscale sensor arrays, and ease of integration with circuits.

Capacitive sensors offer better temperature performance and better pressure sensitivity than piezoresistive devices. In order to take advantage of capacitive devices, it is important to place signal conditioning electronics near the devices themselves. This is because the capacitance of a microfabricated pressure sensor is very small. If the electronics are remote from the sensor, stray capacitance associated with the leads and noise induced by the environment degrade the signal from the sensor. With piezoresistive type pressure sensors, the measurement has better immunity to noise, especially for small devices, but piezoresistive devices are very temperature sensitive (in fact the temperature coefficient can exceed the piezoresistive coefficient by an order of magnitude).

The simplest and most straight forward application of SOI material is to employ the underlying oxide as an etch stop. Figure 6 shows the application of an etch stop 96 to a anisotropically etched piezoresistive pressure sensor 88. In order to fabricate this type of sensor, a typical process might start with the deposition of epitaxial silicon 90 onto a crystallized layer 92. The deposition increases the thickness of the layer to the desired value and than permits electronics and

piezoresistor 94 fabrication. In order to obtain the high temperature performance possible with SOI materials, the transistors and electrical devices that are used in the amplification circuit need to be isolated from one another. After the electronic components have been fabricated and metallization defined, the wafer is coated with a silicon nitride layer. Silicon nitride is extremely resistant to KOH etching and can act as an encapsulant for the final product. Other anisotropic etchants could be used such as EDP or Hydrazine. The back side of the wafer is now patterned and the nitride removed in the areas to be etched. Special alignment equipment is required to make sure that the front and back surfaces are registered properly. After anisotropic etching, the oxide is removed from the back of the diaphragm. This will improve the performance of the diaphragm, since silicon oxide layers are under significant stress. The wafer is completed by opening wirebond windows in the silicon nitride.

Figure 7 shows a modification of the process to provide fully isolated piezoresistors 100. In this case, a silicon wafer 70 with an epitaxial layer 102 is used as the starting material. An SOI wafer is then formed from this substrate having silicon oxide layer 106 and crystallized layer 104. The epitaxial layer, typically formed of single crystal silicon, is chosen to be the thickness of the desired diaphragm. It is also chosen such that its dopant type will be different from that of the wafer. In this way, several known etch stopping techniques can be employed such as stopping on a p+ layer or an n-layer using an electrochemical etchant. The

crystallized silicon 104 is now used to form the resistors 100 and other electronic devices required. Full isolation of the resistors and the electronics is the result.

Figure 8 shows one embodiment in which SOI wafers can be used to create high temperature pressure sensors. In order to fabricate such a device, first etch through both the epitaxial layer 114 and the lower oxide 112 in order to define the area which will become the diaphragm. Next, the epitaxial region above this area is removed and the wafer is oxidized and patterned. Next the CVD diaphragm 118 is deposited and defined. If the sensor is to be a piezoresistive type, then a second polysilicon layer must be deposited and defined over silicon oxide layer 124. Electronics 122 and metallization follows and the final step is to etch out the cavity 116 by cutting holes in the CVD layer 118 outside the perimeter of the diaphragm and to etch the underlying oxide layer. The holes are then sealed using an additional thermal oxidation process or by depositing a CVD sealing layer 120 or both. In this approach, a capacitive pressure sensor would involve fewer processing steps.

Figure 9 shows another similar approach in which the epitaxial layer 114 is used as the silicon diaphragm 128 for a capacitive pressure sensor. In this approach, a CVD deposited nitride layer 126 is used to support the 128 diaphragm from above rather than below. All other processing steps are the same as outlined above.

It should be noted that if electrical isolation of the diaphragm is required, additional insulating layers can be employed, or the CVD layers must be electrically

insulating. In addition, etched cavities can be accessed from both the back and front surfaces if the silicon wafer 70 were etched from behind as is the case for etch cavity type pressure sensors.

A further embodiment employing the concepts described above, Figure 10 shows a differential pressure sensor with both a lower and upper overpressure stop. The upper cavity 132 can be created with a deposited oxide 136 or other sacrificial layer. As in the previous example, the silicon diaphragm 130 is formed from the epitaxial layer. Access to the diaphragm is achieved from both sides of the resulting die. Thus, a lower cavity 134 can be accessed through a rear opening 138 in substrate 70.

For applications other than pressure sensors, wafers allow simple micromachining of mechanical structures. As shown in Figure 11 the underlying oxide can be used as a sacrificial layer for such structures as single crystal silicon bridges 144 formed from epitaxial layer 142 and double tuning forks, and for cantilever structures such as accelerometers.

One of the advantages of the technology described herein is the ability to use alternate underlying insulating layers or multiple underlying layers. These insulating layers can be chosen to have properties that are suitable as mechanical materials or can be chosen to become sacrificial.

A simple example of the use of alternate layers is shown in Figure 12. A silicon nitride layer 150 is used in place of the lower oxide. Silicon nitride is known to have good mechanical properties for microsensors. In

this case, the nitride 150 is used as the material from which a cantilevered accelerometer 156 is formed. A piezoresistive element, a diode, or an active device can be used as a stress detector 158 at the base of the cantilever 156 and can be fabricated in a mesa created in the epitaxial layer. High temperature electronics 160 are fabricated in this layer and in close proximity to the sensing element. To free the cantilever from the substrate, an anisotropic etchant is used. This etchant undercuts the cantilever structure at a rapid rate while stopping at the edges of the defined area. A mass 162 can be secured to cantilever 156 to define its mechanical characteristics.

Typical micromachined accelerometers are etched from Si wafers and can typically be about 0.35-0.5 cm on a side and 200-300 microns thick. For reliability this mass is supported, in one embodiment with 4 springs that are integral to the sensor. These springs have diffused resistors that sense the motion of the mass.

By using materials with higher densities than silicon, a microaccelerometer can be manufactured without the lengthy micromachining currently used. Such a material is tungsten (W) with a density of 19.4 (which is roughly 10 times that of silicon), the thickness being reduced by a factor of 10 and still having the same mass. The area would increase to .5 cm on a side. A 20 micron layer of W can be selectively deposited using chemical vapor deposition.

The frequency of the accelerometer can be expressed by the following equation:

$$f_o = \frac{1}{2\pi}\sqrt{\frac{K}{Mass}}$$

The frequency, f_o, is inversely proportional to the mass but follows the spring constant K. The stiffness of the supporting members determines K. For a typical accelerometer, the springs are 20 microns thick and 80-100 microns long. A ISE accelerometer has springs in the range of 1-2 microns thick. When this thickness can support the high stresses seen by the springs, the accelerometer has a sensitivity of:

$$Sensitivity = B\,\frac{Mass}{K}$$

Note that the spring constant K has an inverse relationship to the sensitivity. The thinner springs will have a lower K value. B is the transduction efficiency and is a function of the resistors. Such thin springs yield very high B values and very low K values and thus enhance the overall sensitivity.

Multiple springs can be employed to give the device survivability. This can increase the resonant frequency and thus decrease sensitivity.

The use of more than one lower insulating layer provides even greater advantages. Another accelerometer is shown in Figure 13. In this case, the lower insulator consists of a layer of oxide 152 upon which a layer of silicon nitride 150 has been deposited. The epitaxial layer is again patterned into mesas for the sensing elements 158 and electronics 160. Afterwards, the

nitride is patterned and the oxide etched to undercut the nitride and free the cantilever from the substrate. If undercutting of the boundary layer is a problem in a given application, one could resort to a double masking. This involves depositing a masking material. In this case, the masking material is a deposited oxide. This layer is patterned to the desired final nitride profile. A second photoresist step provides a mask whose openings are smaller than those of the final nitride profile. Both the nitride 150 and the oxide 152 are etched 166 using a plasma technique. Prior to removing the photoresist, the underlying oxide 152 is etched from beneath the cantilever. This will remove the perimeter of the cavity as well. The photoresist is now removed and the silicon nitride 150 is again etched using the upper oxide as a mask. If the mask set is properly designed, the nitride 150 can be cut back such that the undercutting from the original oxide is completely compensated.

Figures 14A-14E illustrate a process sequence for a preferred method of making a silicon diaphragm sensor. First, as seen in Figure 14A, a substrate 170 is oxidized to form layer 172 and patterned to form base support regions 174. In Figure 14B, a polycrystalline silicon layer 176 is followed by a capping layer 178. Layer 176 is then zone-melt recrystallized using a scanning energy source 180 as shown in Figure 14C to provide a single crystal silicon layer 182. In Figure 14D, the structure is patterned to reveal the diaphragm structure 184. Finally, the oxide layer 172 is etched through the side openings to suspend the diaphragm 184.

Figures 15A and 15B show more detailed side cross-sectional and top views of a structure fabricated using the process shown in Figures 14A-E. Base support regions 190 are used to support diaphragm 184. First 186 and second 188 oxide regions are used to facilitate processing. Regions 192 and 194 are undercut to suspend the diaphragm structure.

Figures 16 and 17 illustrate cantilever devices that have been fabricated using the methods outlined above to form accelerometers. Figure 16 shows a beam 204 of single crystal silicon mounted at base 202 onto substrate 200. Diffused or implanted piezoresistors 208 are formed in the beam which has a mass 206 mounted on the free end. Due to the use of a single crystal beam 204 the piezoresistors are about three times more sensitive than polysilicon structures.

Figure 17 shows a capacitive type accelerometer having a generally circular free end 212 for beam 210 with mass 214 mounted thereon. A diffused silicon electrode 218 can be formed in the substrate 200 that is connected through channel 220 with sensor circuit 216 that is formed in an epitaxial layer overlying the substrate 200.

Figures 18A-18H is another preferred sensor fabrication process in which a silicon diaphragm is supported in a capacitive pressure sensor. Referring to Figure 18A, an SOI structure or wafer is formed in accordance with any of the previously explained fabrication techniques. In a preferred embodiment, a substrate 250 is oxidized to form an oxide layer 252. A polycrystalline layer 254 is formed over the oxide layer

252. Next, the layer 254 is recrystallized using any of the aforementioned techniques to provide a single crystal or substantially single crystal film. As explained previously, the film is suitable for the fabrication of high density CMOS circuits and piezoresistive elements.

As shown in Figure 18B, the film is etched to form a silicon diaphragm 256. The oxide layer 252 is then etched through the openings 257 in the film using an HF etchant or a plasma etch as shown in Figure 18C. The oxide etching process includes undercutting the diaphragm at regions 255 in the range of about 0.2 to 10 microns, thereby suspending the diaphragm 256 on a section 260 of the oxide layer. Referring to Figure 18D, the wafer is then reoxidized to form a thin oxide layer 258 on the silicon regions. The thin oxide layer is then patterned and etched to form isolated oxide regions 262 and 263 as shown in Figure 18E.

A thin layer of silicon nitride is then deposited, preferably using an LPCVD process, as shown in Figure 18F. The silicon nitride layer 264 is then patterned which includes removing the nitride at a region 266 for exposing a portion of the oxide layer 262. Referring to Figure 18G, polysilicon is deposited over the wafer and patterned to form thick polysilicon clamps 270 extending through the openings 257 in the film and filling the channels 261. These clamps serve as a support structure for the diaphragm. In preferred embodiments the gap width (g) of each channel is less than about twice the thickness of the deposited polysilicon layer. For example, for a 2 micron blanket polysilicon deposition, the gap width is preferably about 4 microns. This

feature ensures that the polysilicon clamps 270 formed in the channels 261 during the blanket deposition have a relatively level upper surface 271.

The wafer is then exposed to a concentrated HF etchant which first attacks the silicon oxide 262 layer and then attacks the oxide sections 260 and 263. Once the oxide is consumed, the HF is removed from the cavity 274 (Figure 18H) as follows. After etching with HF, the wafer is thoroughly rinsed in deionized water. The water is subsequently replaced by alcohol. The alcohol rinsing continues to ensure as complete a displacement as is reasonable. The alcohol-wet wafer is then placed under vacuum for a time sufficient to remove by vaporization all the alcohol from beneath the diaphragm. The vapor pressure difference between the inside of the diaphragm and outside (vacuum) prevents the diaphragm from collapsing onto the substrate due to surface tension. Next, the openings about the diaphragm are sealed by forming an oxide layer 272 therein.

In this approach the silicon nitride, being known as a good electrical insulator, serves to electrically isolate the substrate 250 and the diaphragm in the sensor. As such, electrodes can be formed in or on the diaphragm and the substrate to provide a capacitive type pressure sensor. Another advantage to this approach is that a pressure sensor is fabricated in which the diaphragm is without underlying support posts. Employing the above-stated method, the pressure difference between the inside of the diaphragm and outside (vacuum) prevents the diaphragm from collapsing onto the substrate such that the diaphragm underlying supports are not necessary

inside the cavity. It is noted that a portion of the clamps may extend under the cavity (Figure 18H) in some embodiments such that the clamps provide support from above and below.

Figures 19A and 19B illustrate another preferred process for fabricating clamps. The clamps are fabricated after the isolated oxide regions 262, 263 are formed as shown in Figure 18E. As shown in Figure 19A, a single low stress nitride layer 280 is deposited. Unlike the embodiment illustrated in Figures 18F-H, a polysilicon deposition is not employed. The thickness of the nitride layer 280 is essentially equivalent to the combined thickness of the nitride 264 and the polysilicon 270 illustrated in Figures 18F-H. In this embodiment, the clamp comprises completely insulating material and provides even better capacitive insulation than the prior configuration. Figure 19B illustrates the fabricated structure after etching. Figure 19C illustrates the fabricated structure after the etch access has been filled by seal 272.

In all previously described uses of the clamp, it should be understood that the clamp serves two functions. The clamp supports the mechanical structure and also provides a well defined stop to prevent excessive undercutting of the mechanical structure as may occur without the clamp. For example, it is possible to fabricate a beam structure by simply defining an appropriate cavity and undercutting the structure. However, that process may result in a poorly defined boundary between mechanical ground and the beam. The exact position of that boundary varies depending upon

etch conditions. Those boundary variations can be avoided by using a clamp. The clamp serves as an etch barrier and defines with much greater precision the boundary of the beam structure.

It should also be noted that mechanical structures other than diaphragms are possible. These structures include bridges and cantilever beams, curved beams and bridges, beams, bridges and diaphragms with additional layers in various positions. Figure 20 illustrates a side view of a cantilever beam 300 supported by a clamp 310.

Multiple individual clamps may be used to support a single mechanical structure. A diaphragm, for example, may be supported by a number of clamps. The diaphragm may not be sealed around its edges. Figure 21 illustrates a diaphragm 305 supported by multiple clamps 310a-d.

These structures may be used to fabricate a variety of micromechanical structures that may be used individually or in association with one another for sensors, actuators, or microminiature systems. Examples include individual actuators such as electromechanical switches or valves in sensors such as flow sensors, accelerometers, and pressure sensors. In all cases, high temperature capable electronics may be fabricated in the SOI material to drive, control or condition the appropriate signals.

Drying micromechanical structures can lead to problems that prevent them from performing in the way that was intended. Specifically, structures that are to suspend freely over the substrate are often found in

contact with the substrate after drying. Several physical phenomena have been suggested as potential causes for this problem. One possible cause is the electrostatic potential that can exist between two different materials due to surface states and work function differences. Electrostatic forces can be large, especially over small distances, and these forces can bend the beam structure until it contacts the substrate. Another candidate cause is capillary action or surface tension, where the structure is drawn into contact with the substrate by surface tension as the liquid separating the structure and the substrate is removed. Typically, micromechanical structures are released after a sacrificial layer has been etched away. Following this etching process, the wafers are rinsed in water and dried. As the water dries, the microstructures can be drawn toward the substrate. The film of water remaining under the structure tends to exasperate the problem. In time, Van der Waals forces may take over.

This problem has been the impetus for considerable effort to find solutions. Several techniques for drying wafers have been proposed. One technique involves modifying the shape of the mechanical structure to help minimize the area that would come into contact with the substrate. In this approach, numerous downward protrusions of small area are placed on this structure. These protrusions may prevent the larger areas of the structure from coming into contact with the substrate, thus alleviating the problem to some extent. Another approach is to displace the water left after normal rinsing with another liquid. This other liquid is

typically one that can be placed in a system suitably configured such that the liquid will solidify. When solid, conditions are changed, for example, by applying a vacuum, such that the solid material goes directly from the solid phase into the gaseous phase. Cyclohexane is an example used in this freeze drying approach using liquid.

In a preferred embodiment of the invention, rapid evaporation is used to freely suspend a structure over the substrate using the pressure generated by evaporation to balance other forces acting on the structure. As shown in Figure 19B, an alcohol or other liquid 290 is applied for evaporation into cavity 274. Based on a situation where surface tension draws the structures into contact with the substrate, a counteracting force is being used to hold the structure away from the substrate. This force is applied by rapidly evaporating gases that increase the pressure beneath the mechanical structure. The rate of evaporation can be varied by varying the temperature during the rapid vaporization. For example, single crystalline cantilever beams and bridges can be released by rapidly increasing the temperature of the wafer wetted with alcohol to 200°C. In an alternative embodiment, the wafer can be dried in a fluidized bed of methyl alcohol. An alcohol wetted wafer is passed through the floating liquid and onto a hot platen. The wafer initially cools the bath, which quickly recovers and is again fluidized with liquid floating over the wafer surface. At equilibrium, the wafer reaches a temperature near that of the hot platen. When removed from the fluidized methanol bed, the wafer is passed

through the alcohol without re-wetting. When cooled, structures as long as 1 mm have been freely suspended over the substrate.

For a diaphragm, the liquid is confined to a much greater extent than with a beam or bridge. In surface micromachining processes, an etchant attacks the sacrificial layer through a small port. After rinsing the wafer in water, the water is displaced with methyl alcohol 290. The wet wafer is now heated more slowly on the hot platen. The vapor pressure inside the cavity forces the diaphragm away from the substrate. Care must be taken not to overpressurize the structures. The process continues until all liquid has been vaporized and the vapor has escaped from beneath the diaphragms through the etching ports.

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS

1. A pressure sensor comprising:

an insulating layer formed over a substrate, the insulating layer having a cavity formed therein;

a flexible diaphragm positioned over the cavity, the diaphragm being formed in a layer of single crystal or essentially single crystal silicon material positioned over a portion of the insulating layer; and

an insulating clamp structure extending through the silicon layer and the insulating layer along a peripheral portion of the diaphragm, the clamp structure being positioned adjacent to the cavity and attached to the diaphragm for supporting the diaphragm over the cavity, the clamp structure being formed to support the diaphragm over the cavity.

2. The pressure sensor of Claim 1 wherein the clamp structure comprises silicon nitride.

3. The pressure sensor of Claim 1 wherein the clamp structure comprises polysilicon.

4. The pressure sensor of Claim 1 wherein the insulating layer comprises silicon oxide.

5. The pressure sensor of Claim 1 wherein the support substrate comprises a semiconductor material.

6. The pressure sensor of Claim 5 wherein the semiconductor material is silicon.

7. The pressure sensor of Claim 1 further comprising channels formed in the silicon layer adjacent to a peripheral portion of the diaphragm and in the insulating layer adjacent to the cavity, wherein the clamp is positioned in a channel adjacent to the cavity.

8. The pressure sensor of Claim 1 wherein a portion of the cavity adjacent to the substrate has a cross-sectional area which is larger than a cross-sectional area of the diaphragm.

9. A pressure sensor comprising:

a semiconductor substrate;

a layer of insulating material formed on the substrate;

a layer of single crystal or essentially single crystal silicon material formed over the insulating layer;

a flexible diaphragm formed in the silicon layer and supported over a cavity formed in the insulating layer;

a channel formed through the layer of silicon material adjacent a peripheral portion of the diaphragm and into the insulating layer adjacent to the cavity; and

a clamp structure formed in the channel, the clamp structure being attached to the diaphragm for

supporting the diaphragm over the cavity and being formed of an electrical insulating material for electrically isolating the diaphragm from the substrate.

10. The pressure sensor of Claim 9 wherein the clamp structure comprises silicon nitride.

11. The pressure sensor of Claim 9 wherein the clamp structure comprises polysilicon.

12. The pressure sensor of Claim 9 wherein the layer of insulating material comprises silicon oxide.

13. The pressure sensor of Claim 9 wherein the semiconductor material is silicon.

14. The pressure sensor of Claim 9 wherein a portion of the cavity adjacent to the substrate has a cross-sectional area which is larger than a cross-sectional area of the diaphragm.

15. A method of making a pressure sensor comprising the steps of:

forming an insulating layer on a substrate;

forming a layer of single crystal silicon over the insulating layer;

forming a diaphragm positioned in or on the layer of single crystal silicon;

forming a clamp system extending through the silicon layer and the insulating layer along a

peripheral portion of the diaphragm, the clamp system being attached to the diaphragm for supporting the diaphragm over a cavity to be formed in the insulator; and

removing a portion of the insulating layer under the diaphragm to form the cavity such that the diaphragm can be displaced.

16. The method of step 15 wherein the step of forming a clamp system further comprises forming regions of silicon nitride.

17. The method of step 15 wherein the step of forming a clamp system further comprises forming regions of polysilicon.

18. An electromechanical device comprising:

a supporting substrate;

an insulating layer formed on the substrate, the insulating layer having a cavity formed therein;

a micromechanical structure positioned over the cavity, the micromechanical structure formed in a layer of single crystal or essentially single crystal silicon material positioned on the insulating layer; and

an insulating clamp extending through the silicon layer and the insulating layer at a supporting location of the micromechanical structure, the clamp being formed of an electrical

insulator for electrically isolating the micromechanical structure from the substrate.

19. The electromechanical device of Claim 18 wherein the clamp comprises silicon nitride.

20. The electromechanical device of Claim 18 wherein the micromechanical structure is a bridge.

21. The electromechanical device of Claim 18 wherein the micromechanical structure is a beam.

22. The electromechanical device of Claim 21 wherein the beam is a cantilever beam.

23. The electromechanical device of Claim 18 wherein the insulating layer comprises silicon oxide.

24. The electromechanical device of Claim 18 wherein the support substrate comprises a semiconductor material.

25. The electromechanical device of Claim 24 wherein the support substrate is silicon.

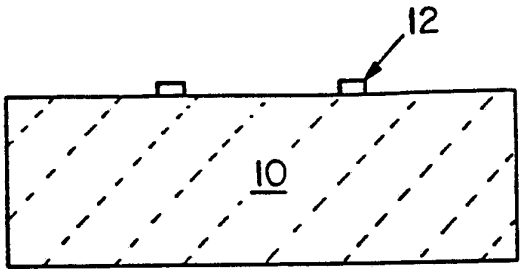


Fig. 1A

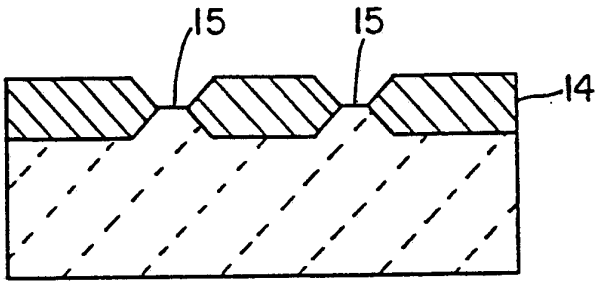


Fig. 1B

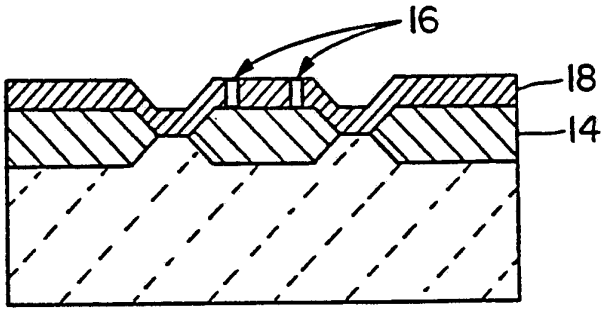


Fig. 1C

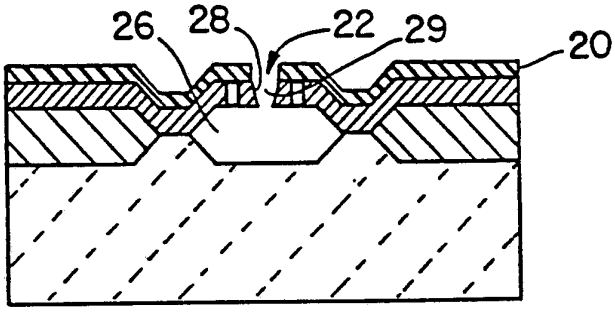


Fig. 1D

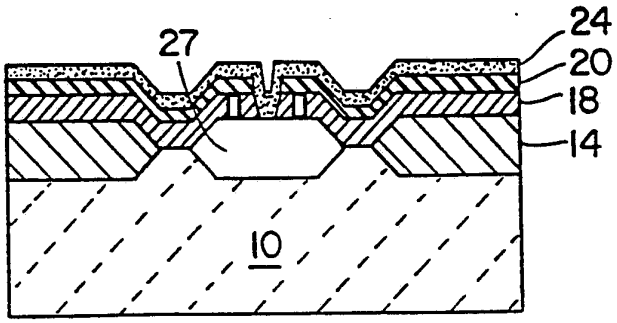


Fig. 1E

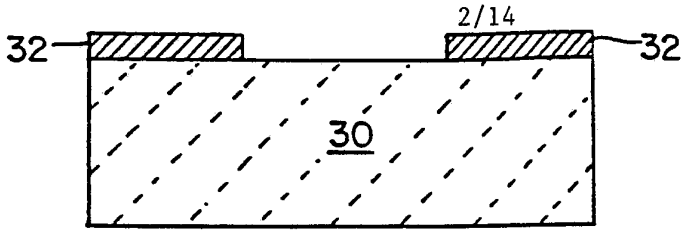


Fig. 2A

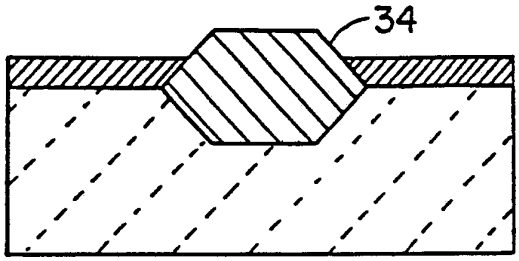


Fig. 2B

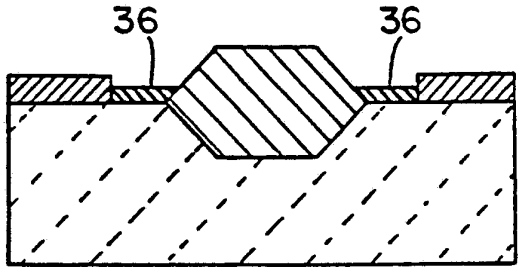


Fig. 2C

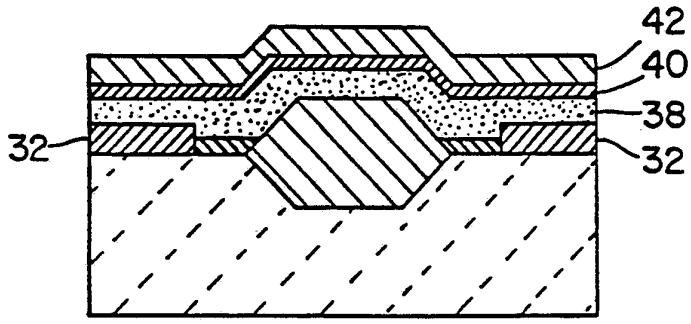


Fig. 2D

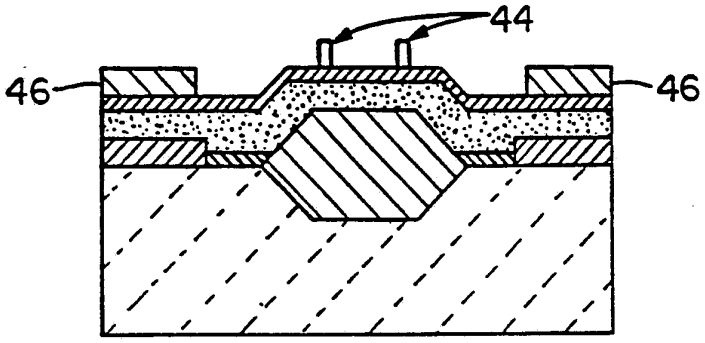


Fig. 2E

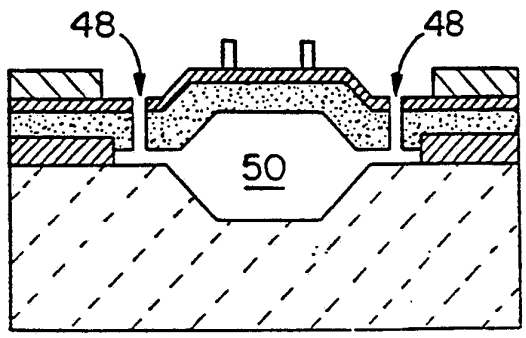


Fig. 2F

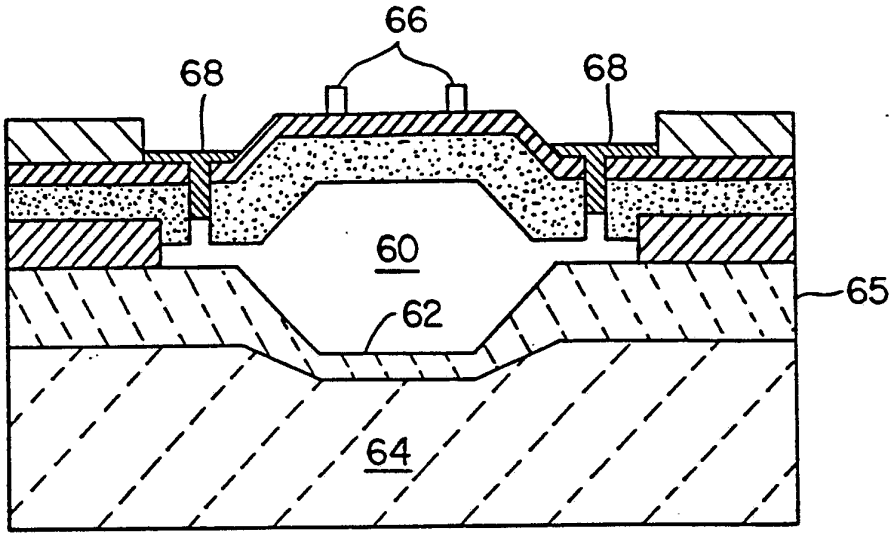


Fig. 3

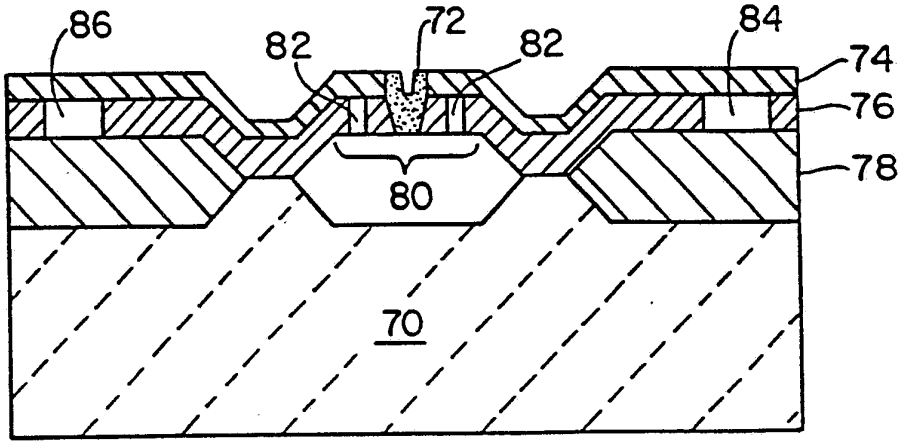


Fig. 4

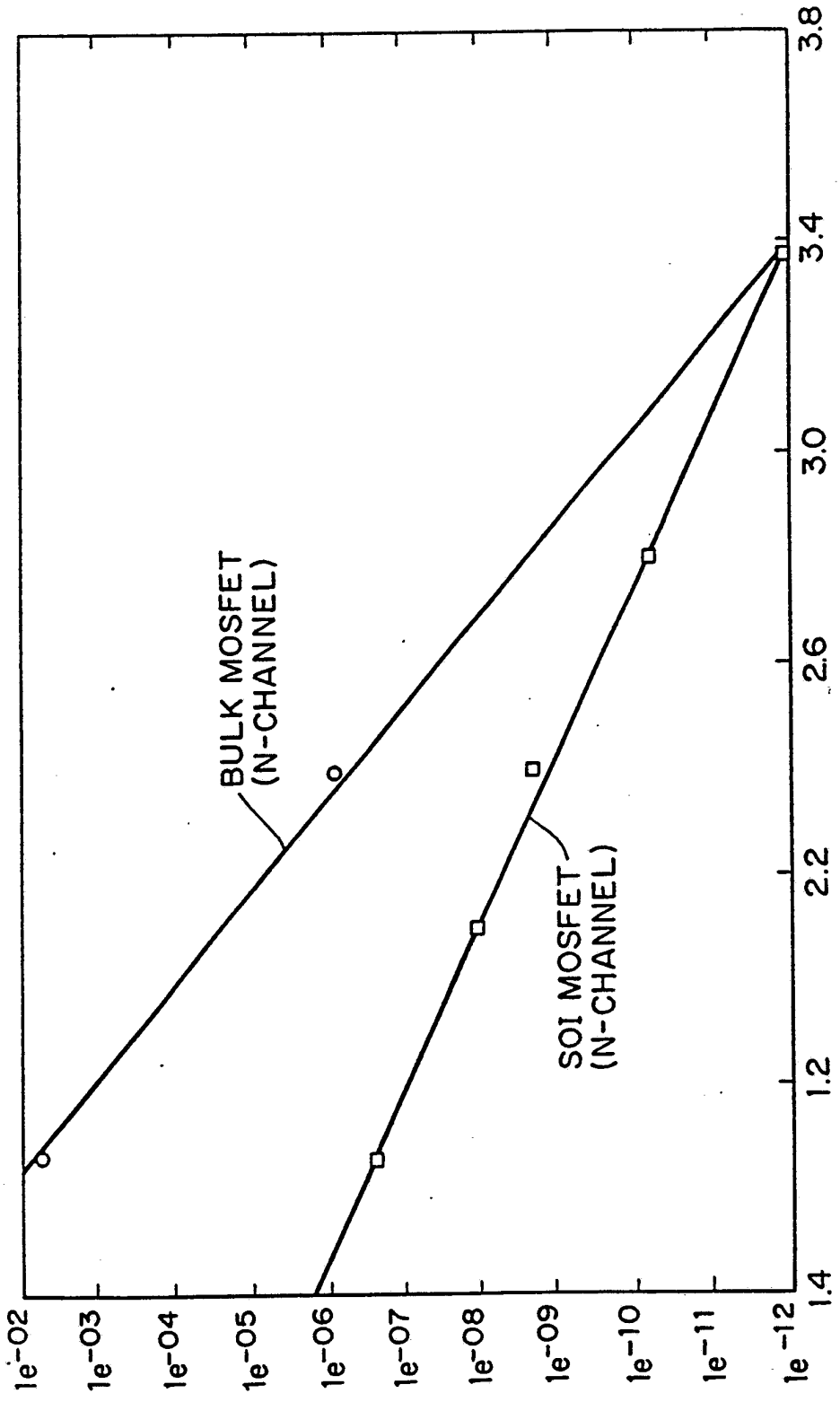

BULK MOSFET
(N-CHANNEL)
SOI MOSFET
(N-CHANNEL)
LEAKAGE CURRENT (AMPS)
1e-02
1e-03
1e-04
1e-05
1e-06
1e-07
1e-08
1e-09
1e-10
1e-11
1e-12
1000/T (1/K)
1.4
1.2
2.2
2.6
3.0
3.4
3.8

Fig. 5

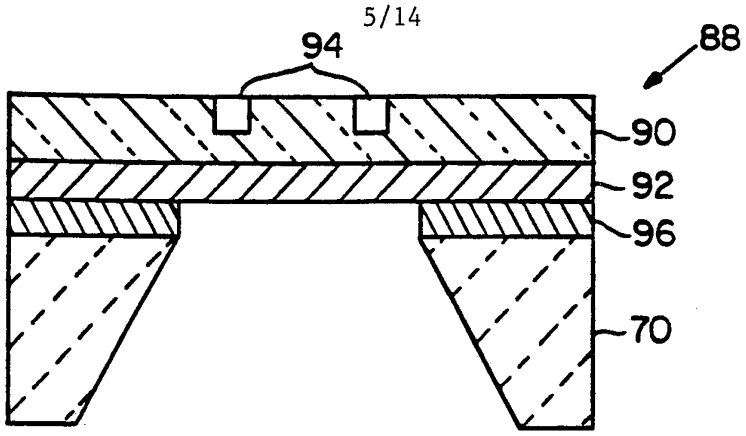


Fig. 6

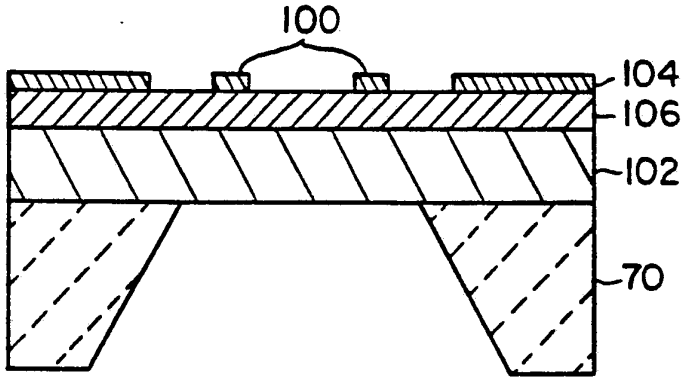


Fig. 7

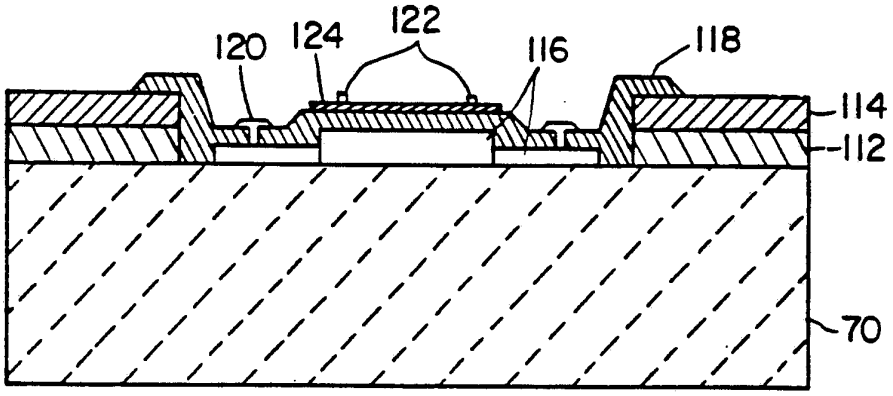


Fig. 8

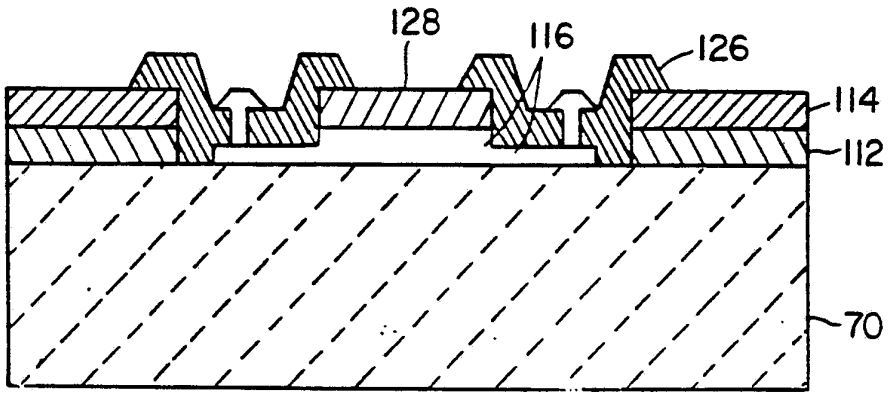


Fig. 9

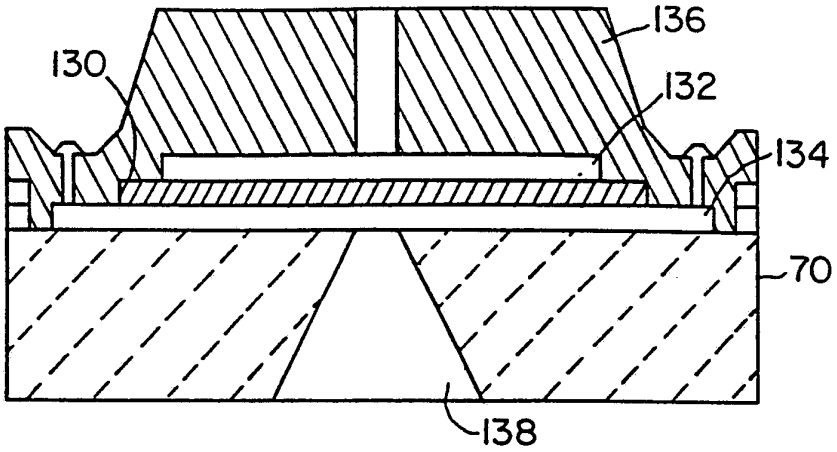


Fig. 10

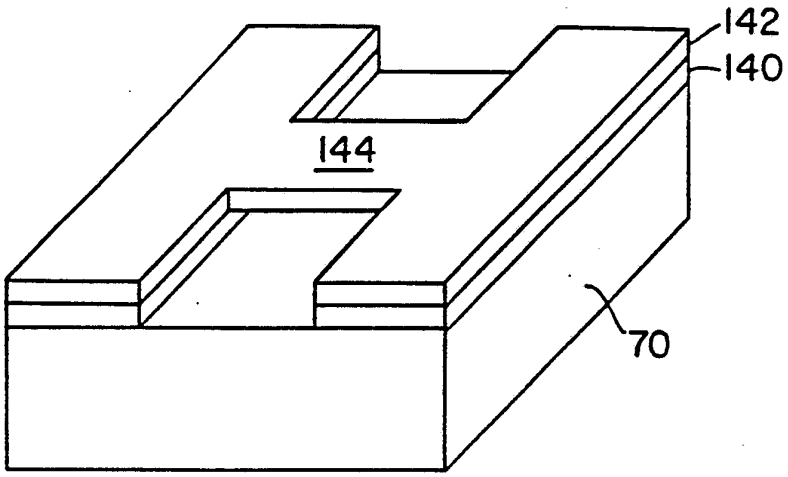


Fig. 11

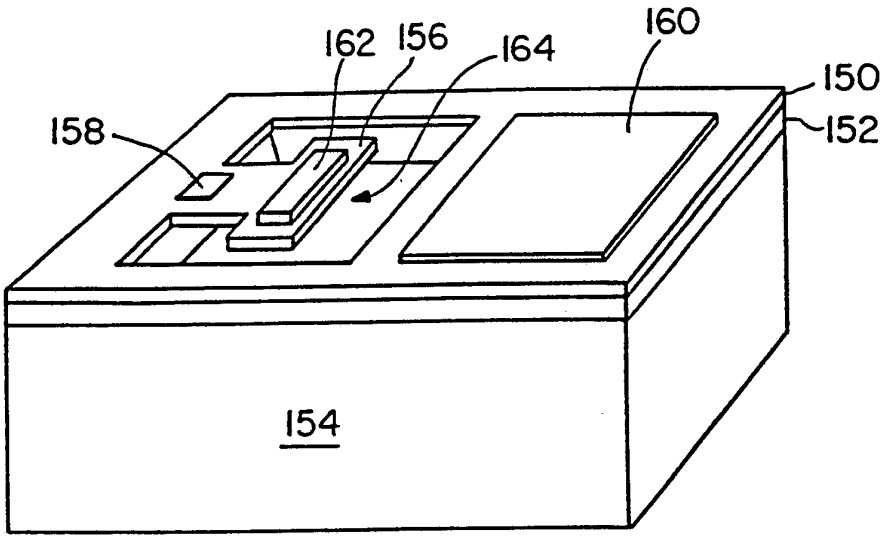


Fig. 12

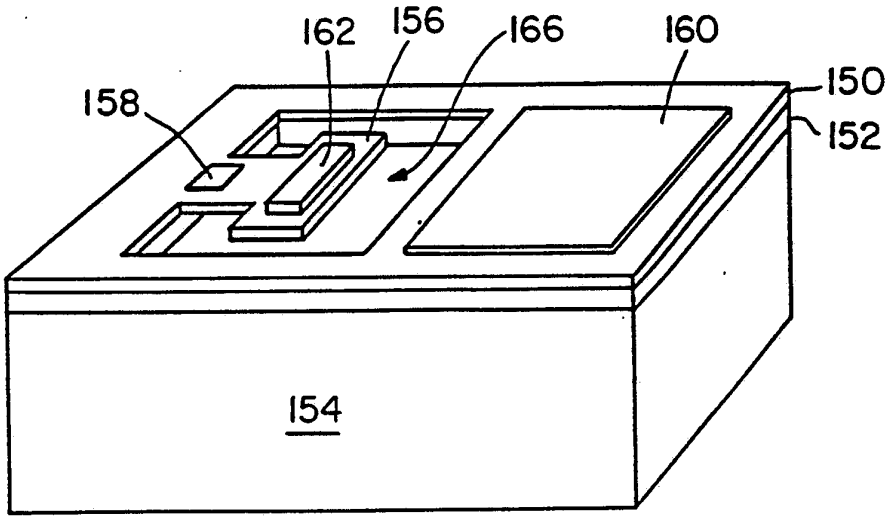


Fig. 13

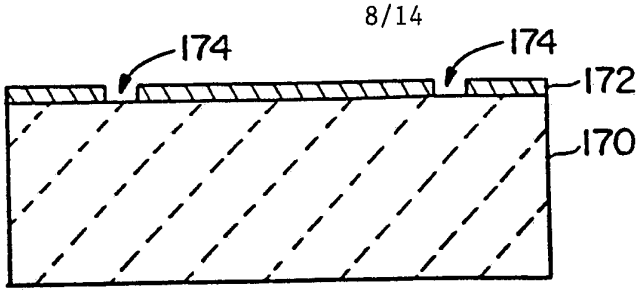


Fig. 14A

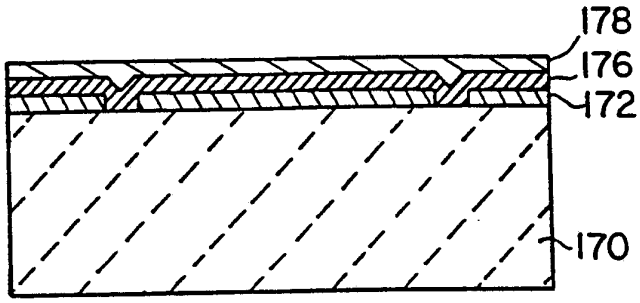


Fig. 14B

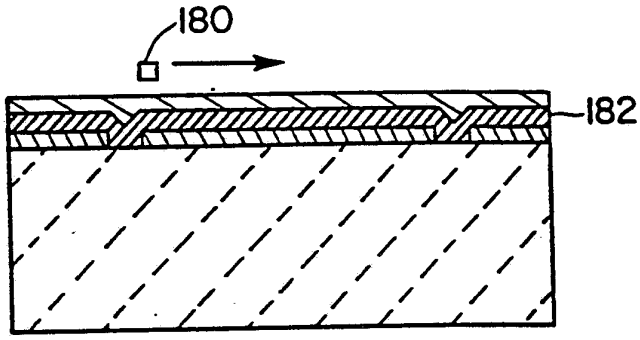


Fig. 14C

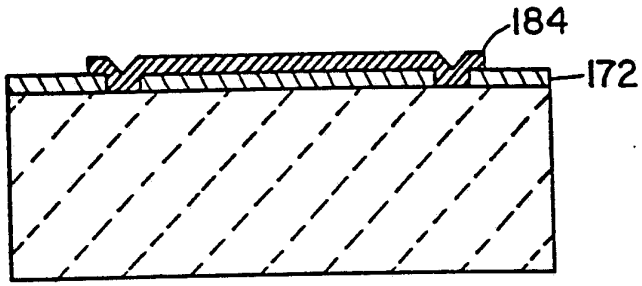


Fig. 14D

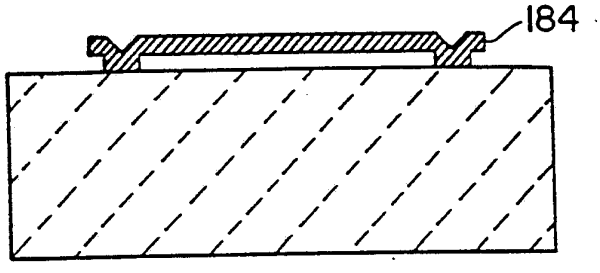


Fig. 14E

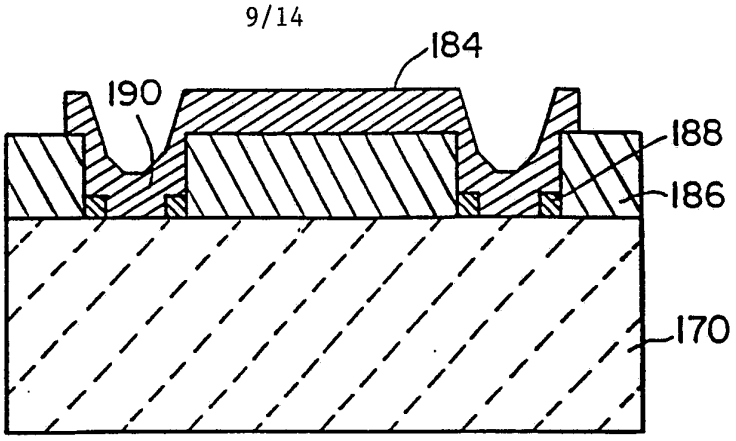


Fig. 15A

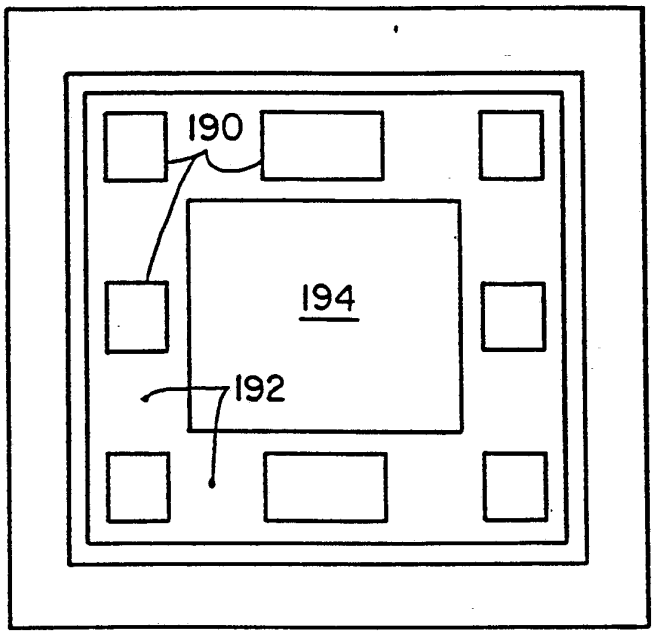


Fig. 15B

Fig. 16

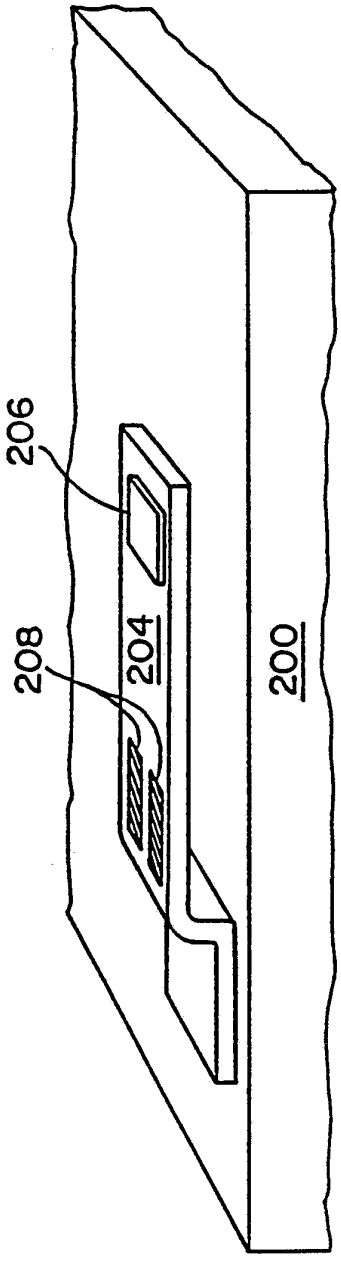
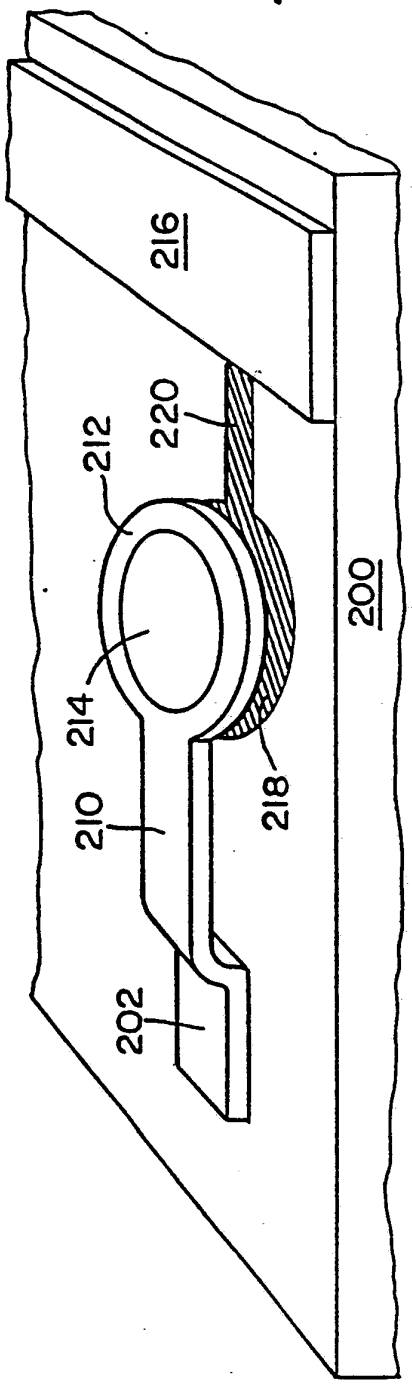


Fig. 17



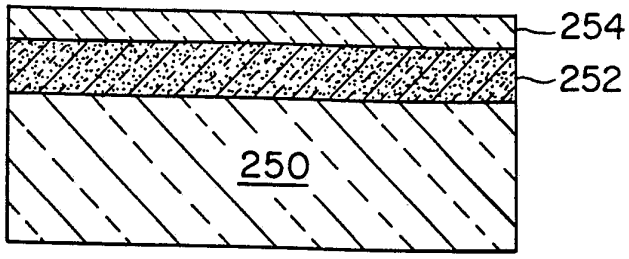


FIG. 18A

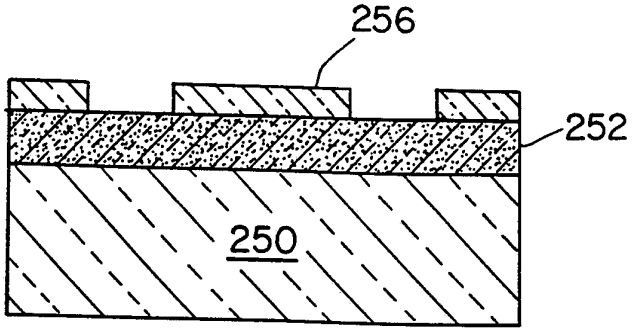


FIG. 18B

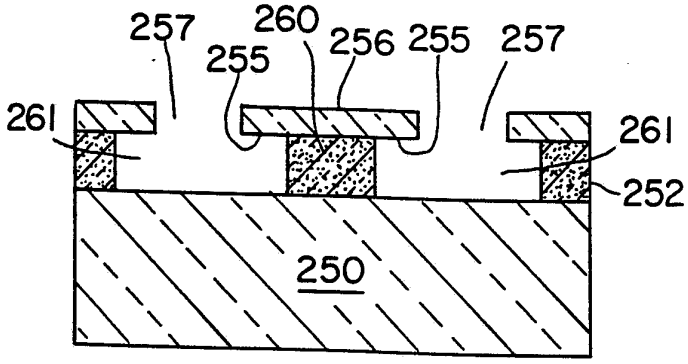


FIG. 18C

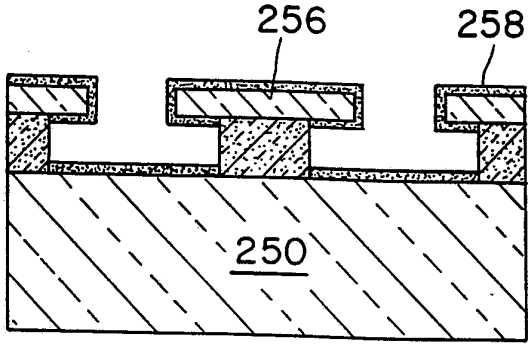


FIG. 18D

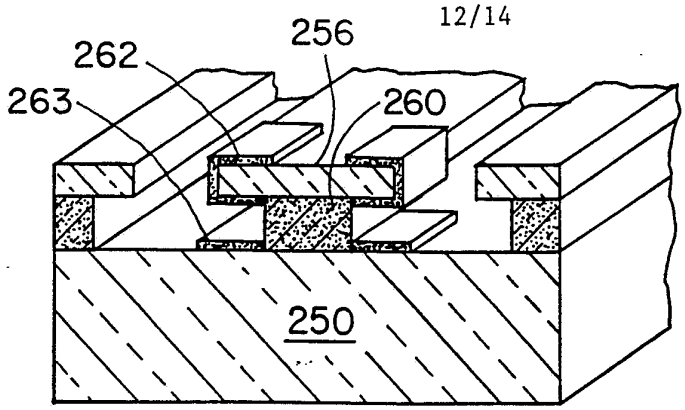


FIG. 18E

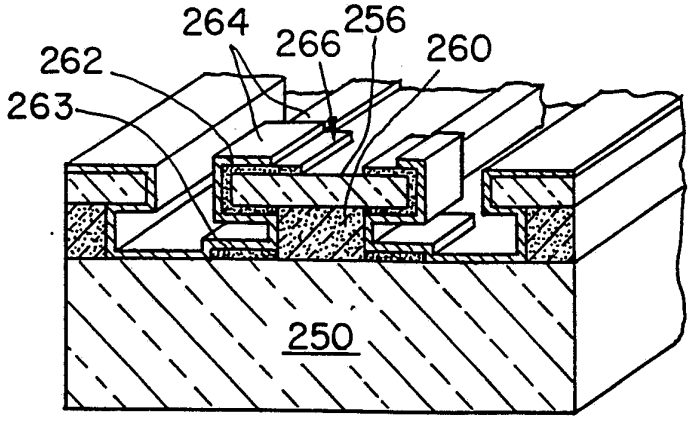


FIG. 18F

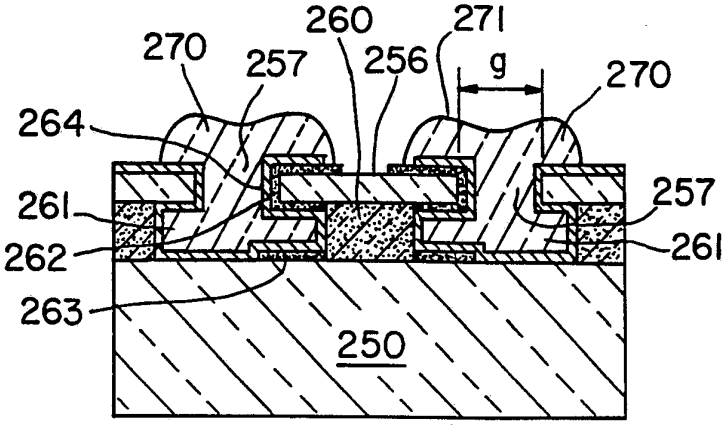


FIG. 18G

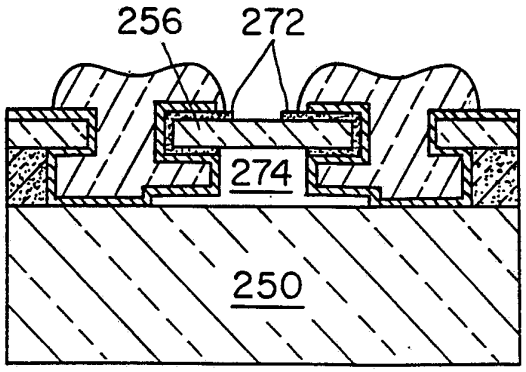


FIG. 18H

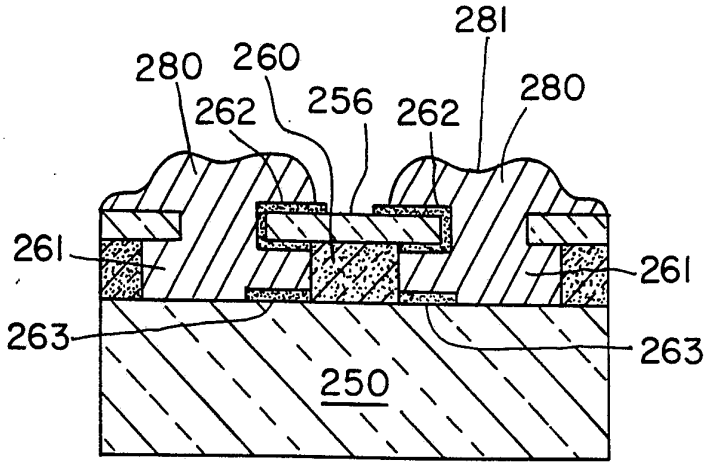


FIG. 19A

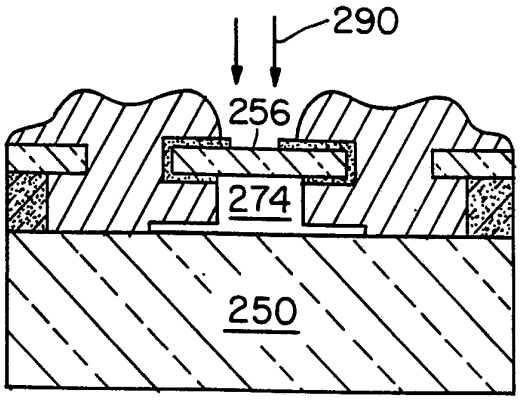


FIG. 19B

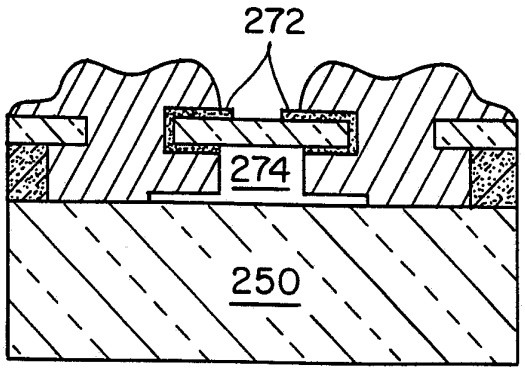


FIG. 19C

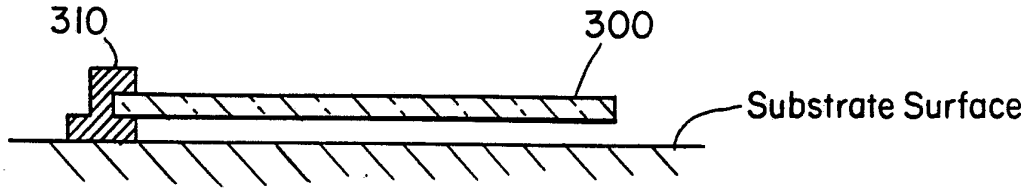

310
300
Substrate Surface

FIG. 20

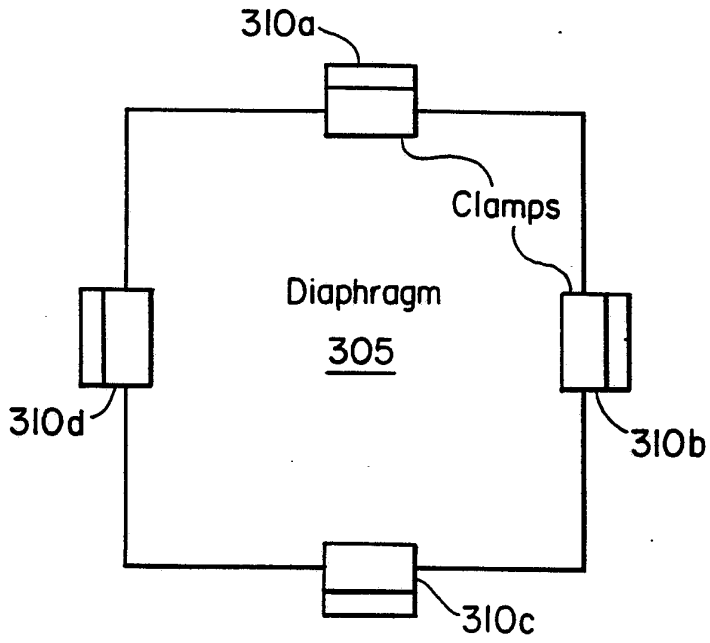

310a
Clamps
Diaphragm
305
310d
310b
310c

FIG. 21

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 93/01952

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 G01L9/00

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	G01L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
A	US,A,4 849 070 (BLY ET AL.) 18 July 1989 see column 2, line 37 - line 53; figures	1,15
A	GB,A,2 198 611 (SPECTROL RELIANCE LTD.) 15 June 1988 see the whole document	1
A	International electron devices meeting 7-10.12.1986,Los Angeles, C A S.Sugiyama et al. : " Micro-diaphragm pressure sensor" ,pp 184-187	15

° Special categories of cited documents : [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
01 JULY 1993	09. 07. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	ZAFIROPOULOS N.

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 9301952 SA 71632

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 01/07/93

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A-4849070	18-07-89	None	
GB-A-2198611	15-06-88	US-A- 4849071	18-07-89