United States Patent

Nagamatsu et al.

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[54] VIDEO DISPLAY SYSTEM INCLUDING RASTER TYPE CATHODE RAY TUBE

[72] Inventors: **Takeo Nagamatsu; Yusaku Yamada,** both of Kawasaki; **Kazumi Yamada,** Yokohama, all of Japan

[73] Assignee: **Fujitsu Limited,** Kawasaki, Japan

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[52] **U.S. Cl.** .....**340/324 A,** 178/30

[51] **Int. Cl.**.....**G06f 3/14**

[58] **Field of Search** .....340/324 A; 178/15, 30

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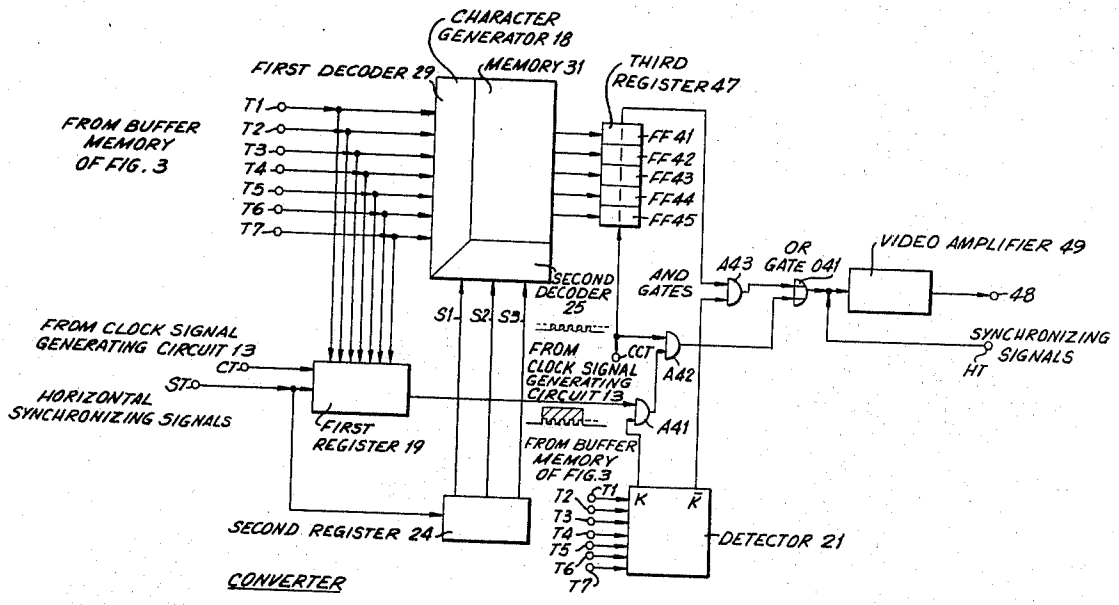
Primary Examiner—John W. Caldwell
Assistant Examiner—Marshall M. Curtis
Attorney—Curt M. Avery, Arthur E. Wilfond, Herbert L. Lerner and Daniel J. Tick

[57] **ABSTRACT**

A memory of a video display system including raster type cathode ray tube display means stores character codes, codes indicating the height of a bar graph displayed in a direction perpendicular to the raster trace of the cathode ray tube, codes indicating the start of the area of the bar graph and codes indicating the end of the bar graph in the address corresponding to the display position in the display means. The memory transfers out each code successively in the order of the display position. A character generator is connected to the memory and receives the character codes from the memory and produces character video signals corresponding to the character codes. A detector is connected to the memory and detects codes indicating the start of the area of the bar graph and codes indicating the end of the bar graph. A register connected to the memory and to a source of horizontal synchronizing signals counts the horizontal synchronizing signals for determining the number of the scanning line in the display means and for comparing the number of the scanning line determined with codes indicating the height of the bar graph. A first gate circuit is connected to the character generator and stops the output of the character generator when codes indicating the start of the area of the bar graph are detected by the detector. The first gate circuit transfers the output of the character generator to a video signal amplifier when codes indicating the end of the bar graph are detected by the detector. A second gate circuit connected to a source of clock signals transfers a clock signal for the display of the bar graph to the video signal amplifier when the number of the scanning line is greater than the number corresponding to codes indicating the height of the bar graph as determined by the register.

3 Claims, 11 Drawing Figures



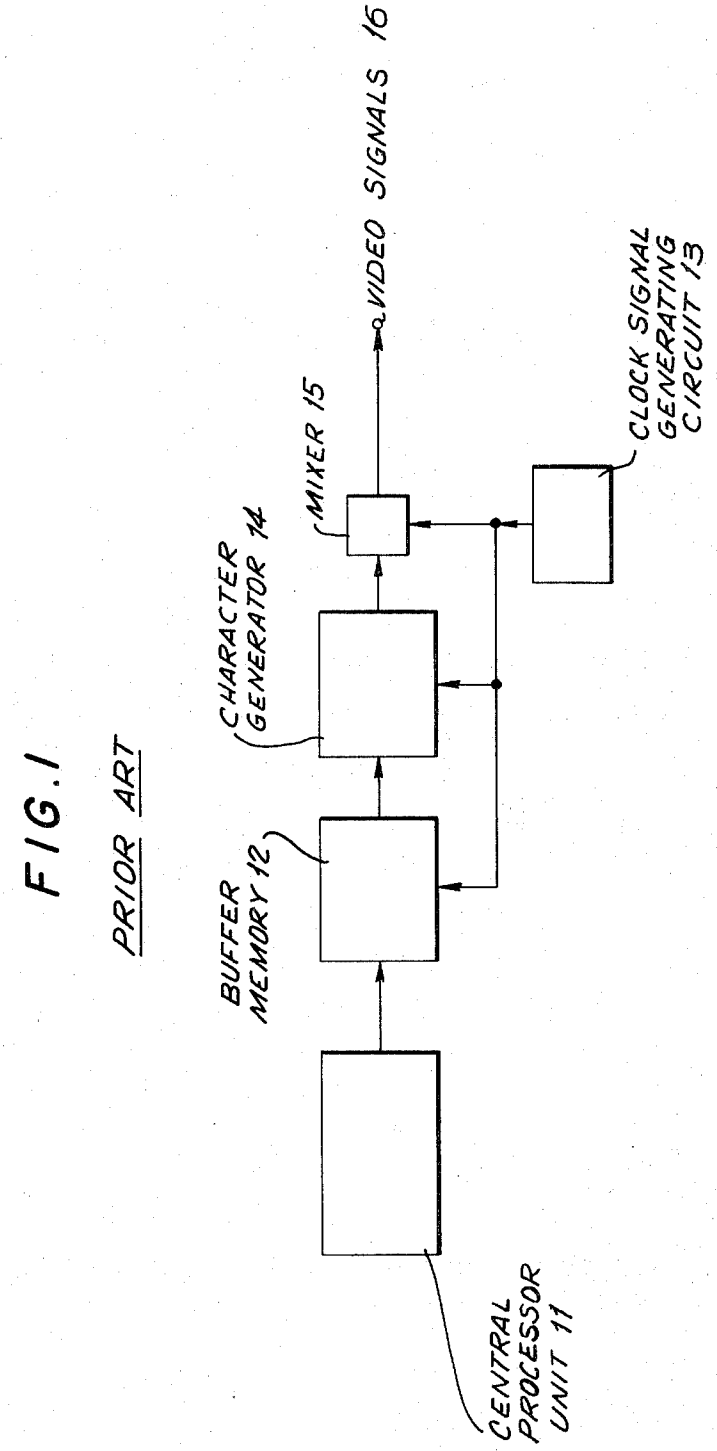


FIG. 1

PRIOR ART

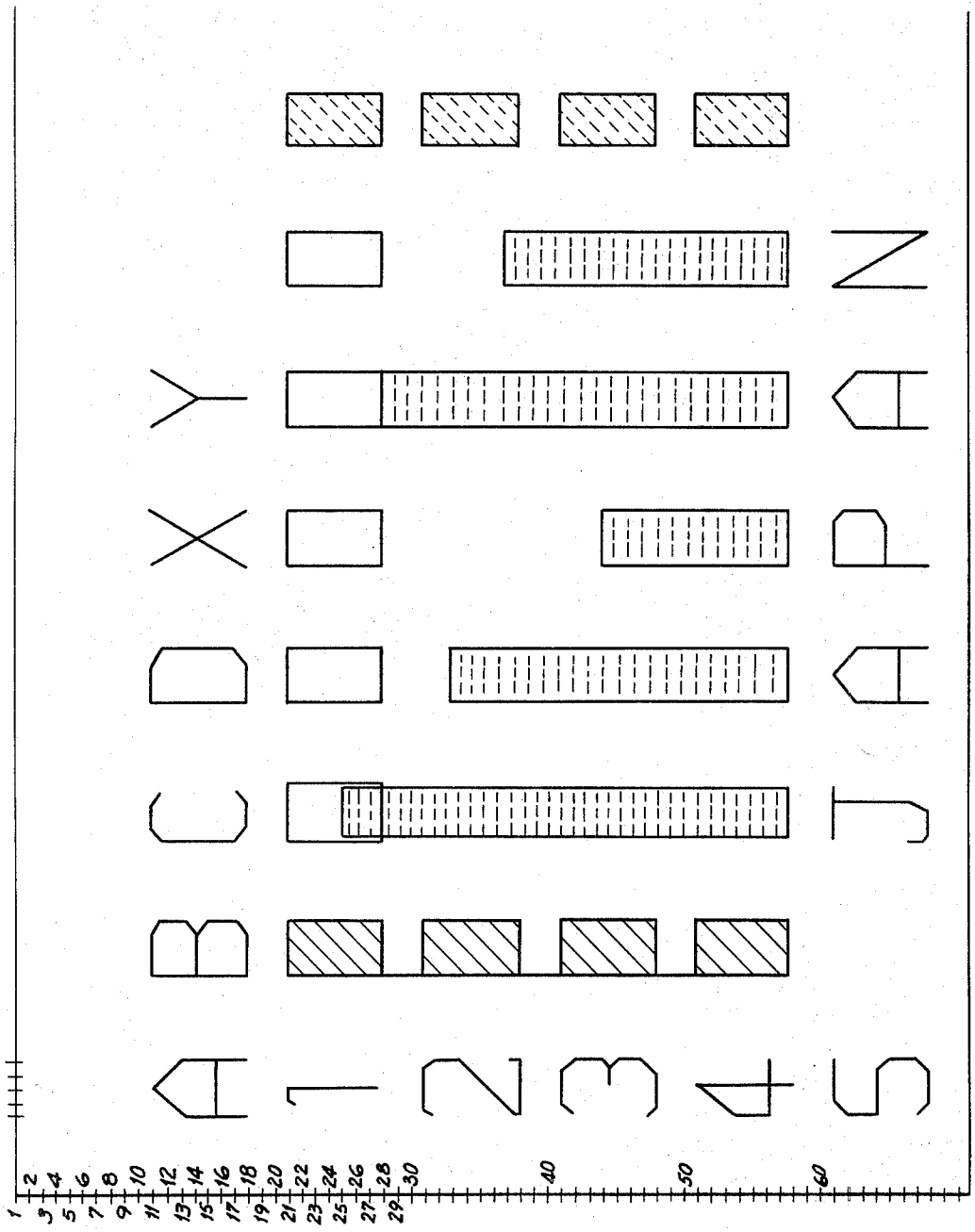

A
B
C
D
X
Y
N
P
J
1
2
3
4
5
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 40 50 60
DISPLAY PICTURE

FIG. 2

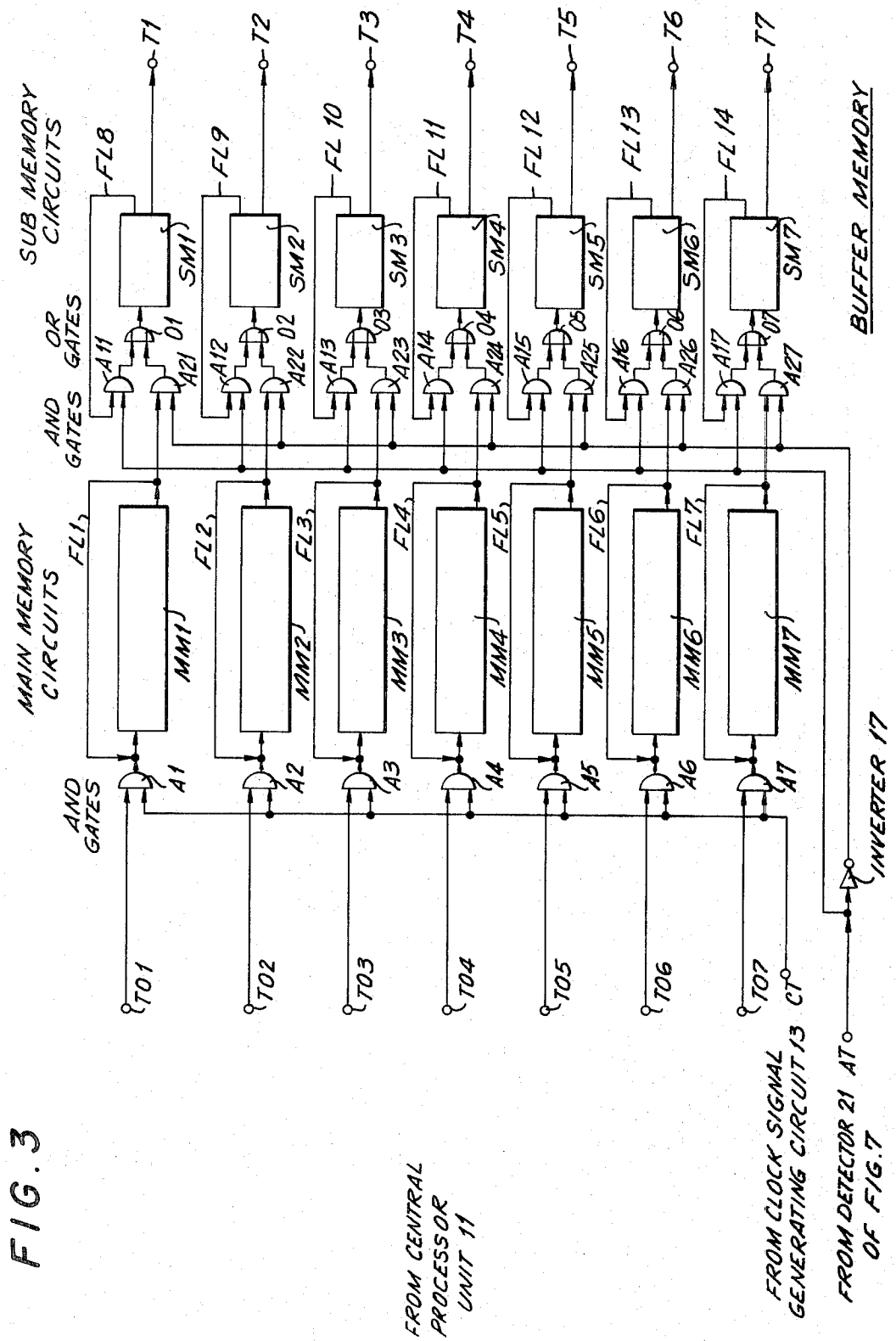

SUB MEMORY CIRCUITS
OR GATES
AND GATES
MAIN MEMORY CIRCUITS
AND GATES
BUFFER MEMORY
INVERTER 17
FROM CENTRAL PROCESSOR UNIT 11
FROM CLOCK SIGNAL GENERATING CIRCUIT 13
FROM DETECTOR 21 OF FIG. 7
T1
T2
T3
T4
T5
T6
T7
FL8
FL9
FL10
FL11
FL12
FL13
FL14
SM1
SM2
SM3
SM4
SM5
SM6
SM7
FL1
FL2
FL3
FL4
FL5
FL6
FL7
MM1
MM2
MM3
MM4
MM5
MM6
MM7
A1
A2
A3
A4
A5
A6
A7
A11
A12
A13
A14
A15
A16
A17
A21
A22
A23
A24
A25
A26
A27
01
02
03
04
05
06
07
T01
T02
T03
T04
T05
T06
T07
CT
AT

FIG. 3

FIG. 4

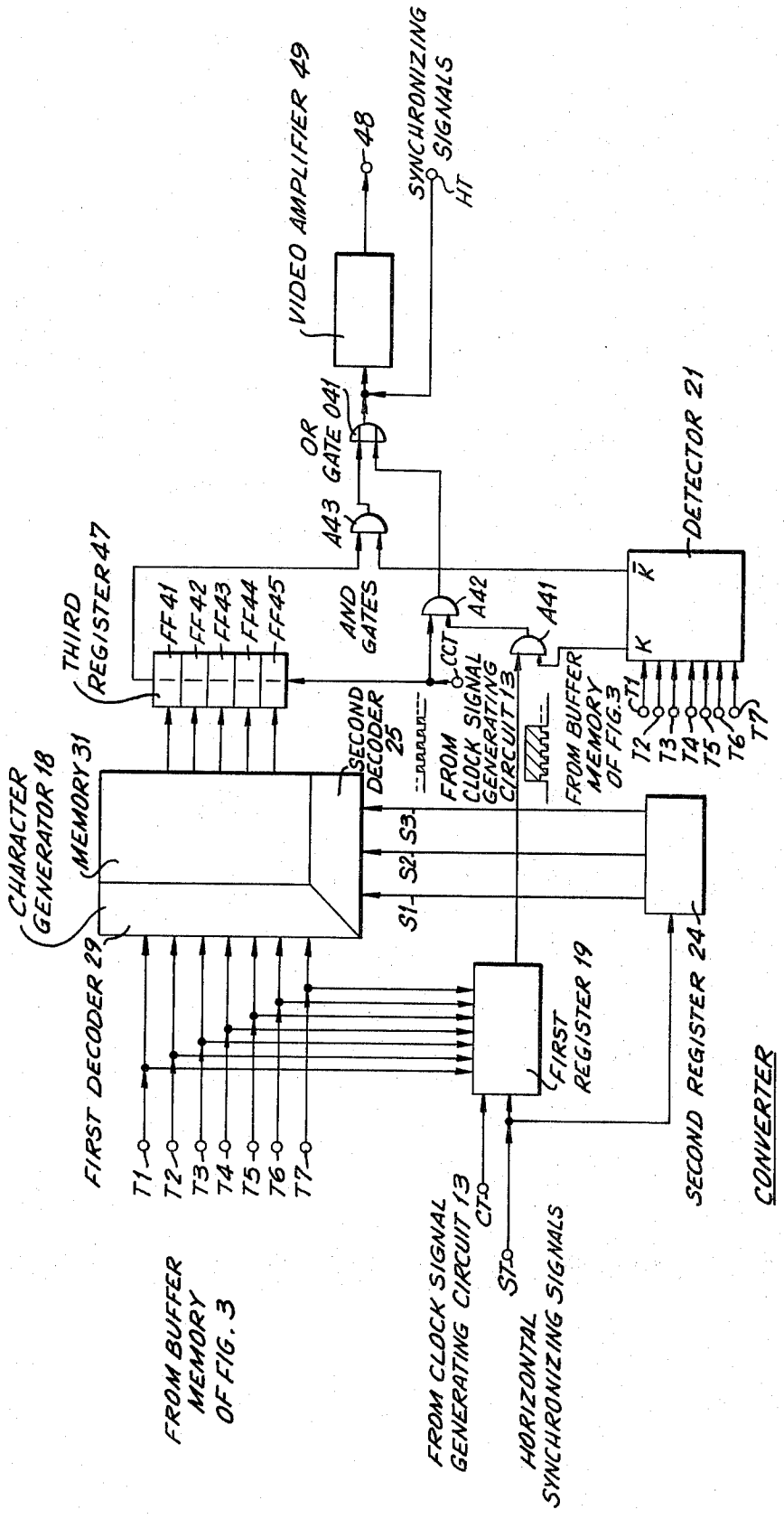

VIDEO AMPLIFIER 49
48
SYNCHRONIZING SIGNALS
HT
OR GATE 041
A43
AND GATES
THIRD REGISTER 47
FF41
FF42
FF43
FF44
FF45
A42
A41
CCT
DETECTOR 21
K
K
T1
T2
T3
T4
T5
T6
T7
FROM CLOCK SIGNAL GENERATING CIRCUIT 13
FROM BUFFER MEMORY OF FIG. 3
SECOND DECODER 25
CHARACTER GENERATOR 18
MEMORY 31
S3
S2
S1
FIRST DECODER 29
FIRST REGISTER 19
SECOND REGISTER 24
CONVERTER
T1
T2
T3
T4
T5
T6
T7
FROM BUFFER MEMORY OF FIG. 3
FROM CLOCK SIGNAL GENERATING CIRCUIT 13
CTO
STO
HORIZONTAL SYNCHRONIZING SIGNALS

FIG. 5

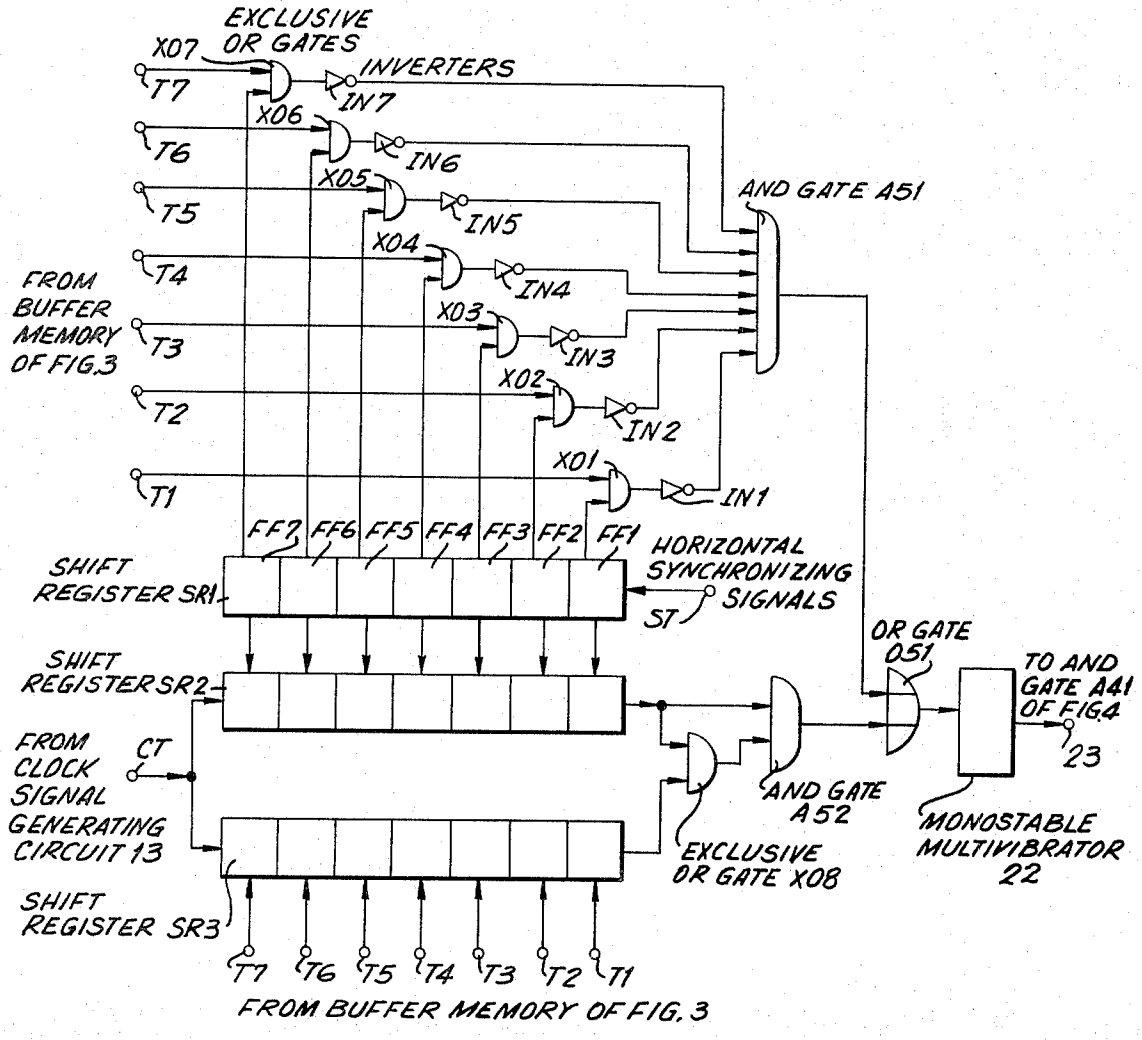

FIRST REGISTER 19
EXCLUSIVE OR GATES
INVERTERS
X07
X06
X05
X04
X03
X02
X01
IN7
IN6
IN5
IN4
IN3
IN2
IN1
T7
T6
T5
T4
T3
T2
T1
FROM BUFFER MEMORY OF FIG.3
AND GATE A51
FF7
FF6
FF5
FF4
FF3
FF2
FF1
SHIFT REGISTER SR1
HORIZONTAL SYNCHRONIZING SIGNALS
ST
SHIFT REGISTER SR2
OR GATE O51
TO AND GATE A41 OF FIG.4
23
FROM CLOCK SIGNAL GENERATING CIRCUIT 13
CT
AND GATE A52
EXCLUSIVE OR GATE X08
MONOSTABLE MULTIVIBRATOR 22
SHIFT REGISTER SR3
T7 T6 T5 T4 T3 T2 T1
FROM BUFFER MEMORY OF FIG. 3

FIG. 7

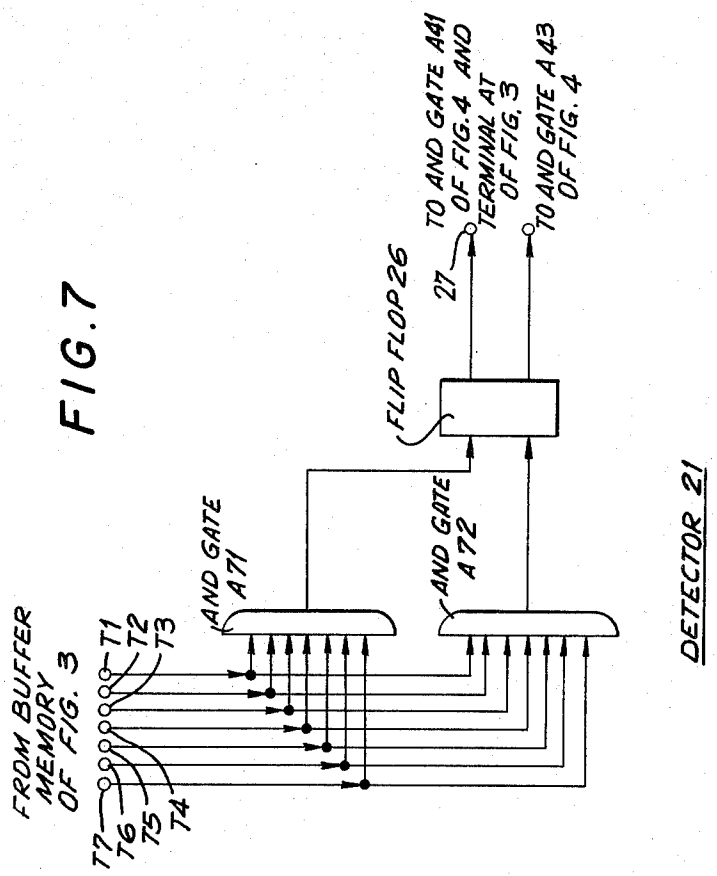

FROM BUFFER MEMORY OF FIG. 3
T7
T6
T5
T4
T1
T2
T3
AND GATE A71
AND GATE A72
FLIP FLOP 26
27
TO AND GATE A41 OF FIG. 4 AND TERMINAL AT OF FIG. 3
TO AND GATE A43 OF FIG. 4
DETECTOR 21

FIG. 6

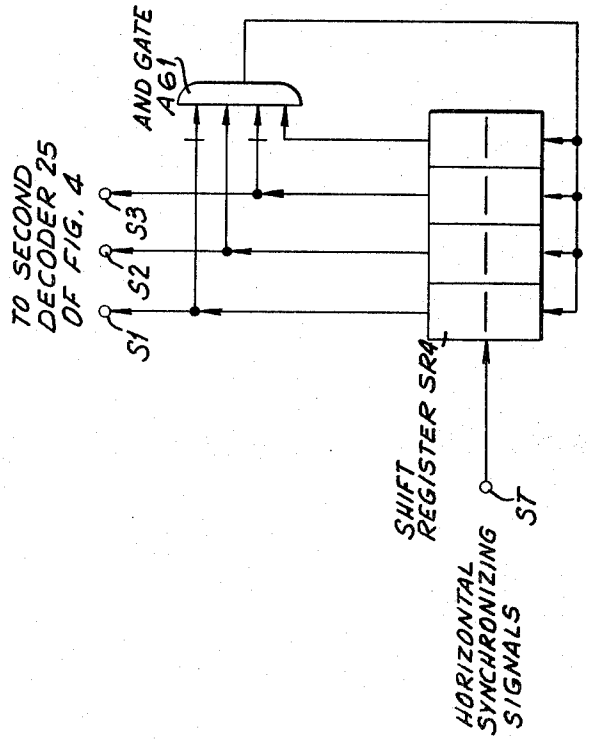

TO SECOND DECODER 25 OF FIG. 4
S1
S2
S3
AND GATE A61
SHIFT REGISTER SR4
HORIZONTAL SYNCHRONIZING SIGNALS
ST
SECOND REGISTER 24

FIG. 9

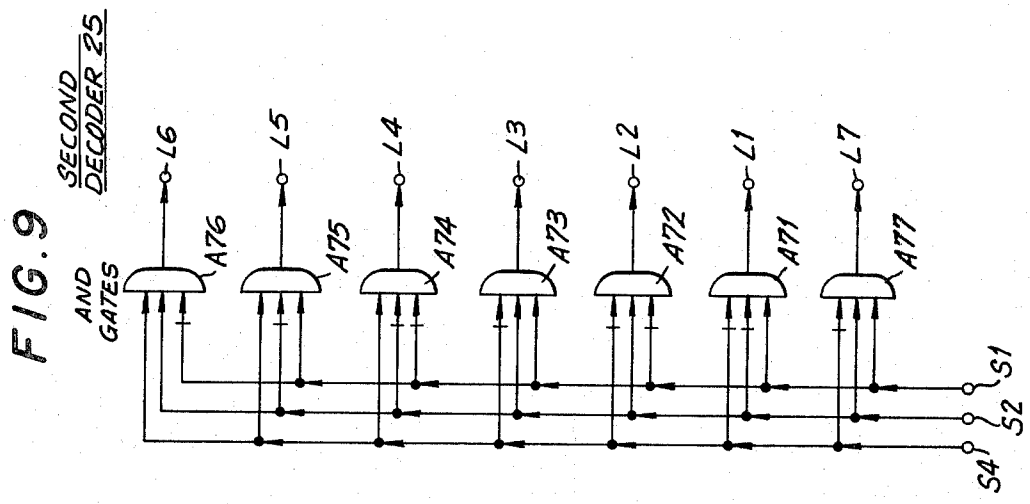

SECOND DECODER 25
AND GATES
L6
L5
L4
L3
L2
L1
L7
A76
A75
A74
A73
A72
A71
A77
S1
S2
S4

FIG. 8

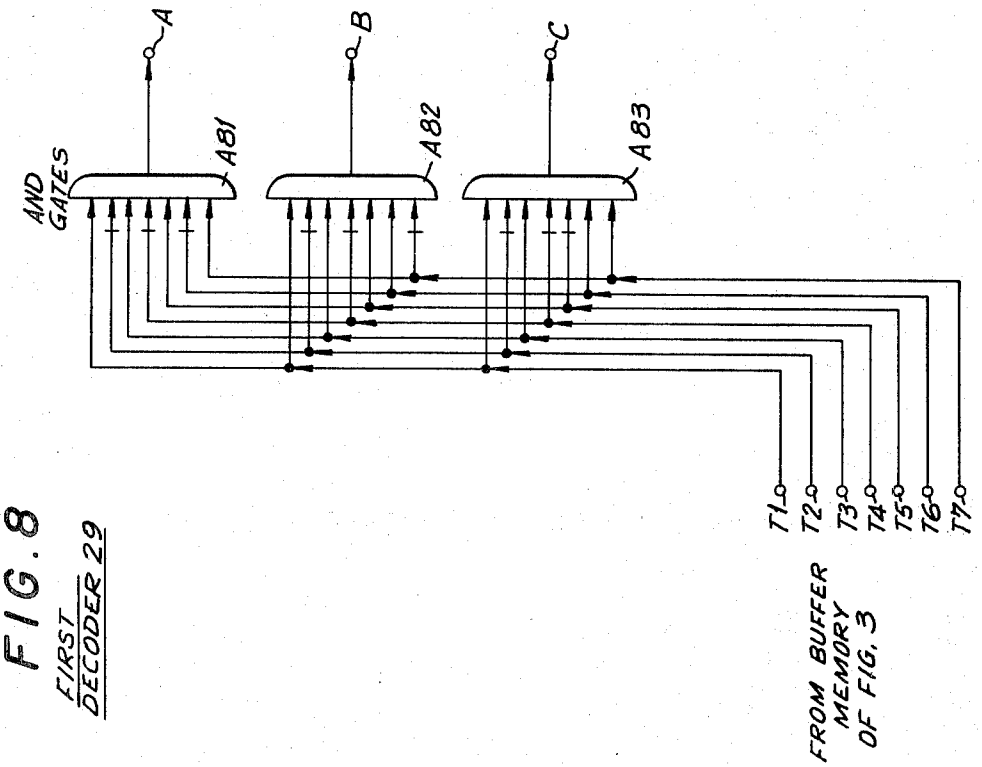

FIRST DECODER 29
AND GATES
A
B
C
A81
A82
A83
T1
T2
T3
T4
T5
T6
T7
FROM BUFFER MEMORY OF FIG. 3

FIG. 10

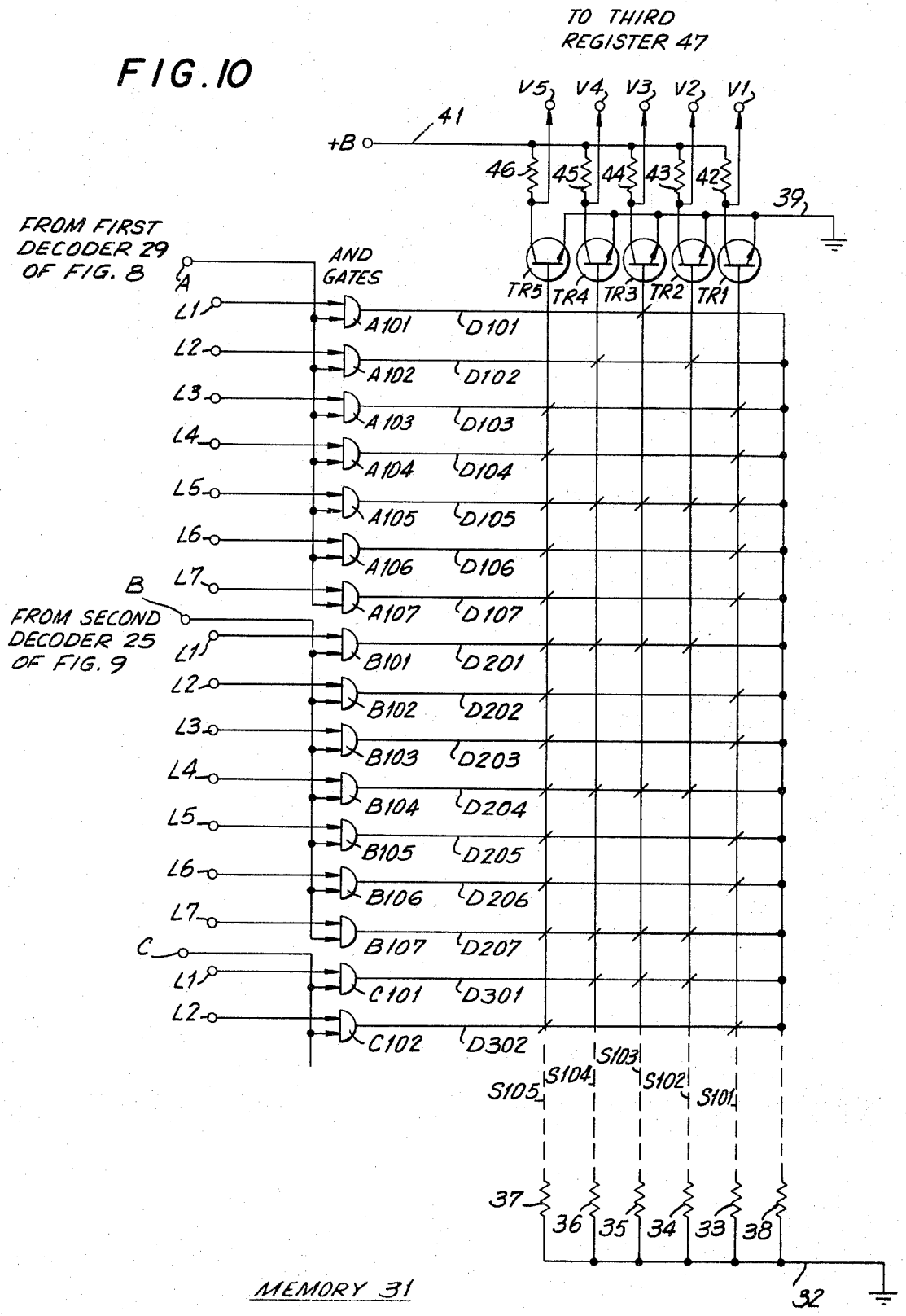
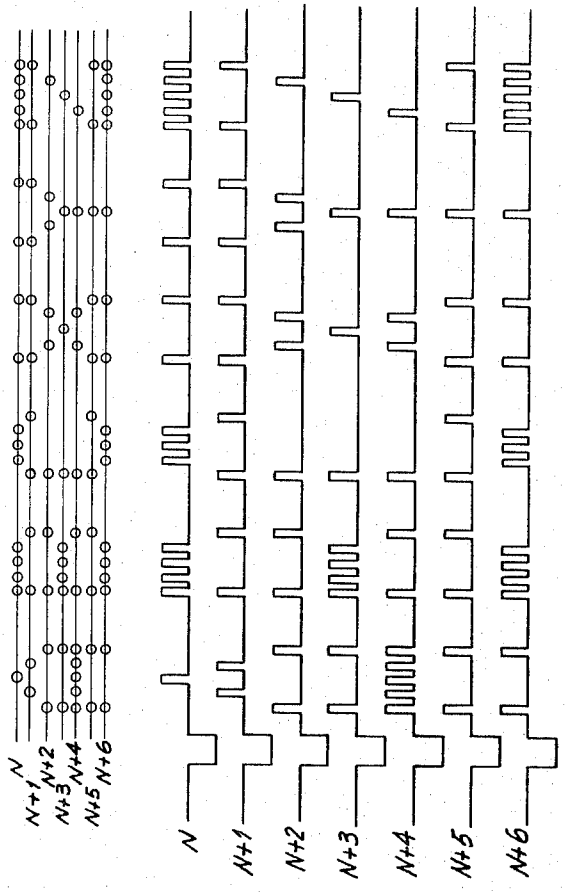

TO THIRD REGISTER 47
V5
V4
V3
V2
V1
+B
41
46
45
44
43
42
39
TR5
TR4
TR3
TR2
TR1
FROM FIRST DECODER 29 OF FIG. 8
A
AND GATES
L1
L2
L3
L4
L5
L6
L7
A101
A102
A103
A104
A105
A106
A107
D101
D102
D103
D104
D105
D106
D107
B
FROM SECOND DECODER 25 OF FIG. 9
B101
B102
B103
B104
B105
B106
B107
D201
D202
D203
D204
D205
D206
D207
C
C101
C102
D301
D302
S103
S104
S102
S105
S101
37
36
35
34
33
38
MEMORY 31
32

FIG. 11



VIDEO DISPLAY SYSTEM INCLUDING RASTER TYPE CATHODE RAY TUBE

DESCRIPTION OF THE INVENTION

The invention relates to a video display system. More particularly, the invention relates to a raster type cathode ray tube video display system.

In a conventional video display system, code signals corresponding to a character are received. A character generator generates video signals corresponding to the scanning of the character and the video signals are transmitted to the television receiver. The television picture is displayed at the receiver. It is desirable that the display system be able to display bar graphs as well as characters. However, although many conventional systems are able to display lateral bar graphs, it is difficult to provide a video display system for displaying longitudinal bar graphs, since such a system involves an increased size of the buffer memory and increased complication of the program.

The principal object of the invention is to provide a new and improved video display system.

An object of the invention is to provide a raster type cathode ray tube video display system for displaying longitudinal bar graphs as well as characters.

An object of the invention is to provide a video display system for displaying longitudinal bar graphs, which system does not require a special buffer memory, and in which the program is simple.

An object of the invention is to provide a video display system of simple structure, but efficiency, effectiveness and reliability in operation, for displaying longitudinal bar graphs as well as characters.

In accordance with the invention, in a raster type cathode ray tube video display system code informations for the display of a longitudinal bar graph are stored in a memory circuit for storing character codes. The raster signals are counted. The resultant count is compared with the code informations for the height of the longitudinal bar graph to thereby determine the position of the bright point of the longitudinal bar graph and to generate the longitudinal bar graph display signals.

In accordance with the invention, a video display system includes raster type cathode ray tube display means having memory means for storing character codes corresponding to the display position in the display means. Input means stores character codes in the address of the memory means. Character generating means has an input connected to the memory means an output for receiving designated character codes in succession from the memory means. Output means connected to the output of the character generating means reads out the output of the character generating means and displays the read out output. In accordance with the invention, the display means of the video display system comprises means included in the memory means for storing codes for starting a longitudinal bar graph, codes indicating the height of the longitudinal bar graph and codes for ending the longitudinal bar graph. Comparing means connected to the memory means compares the number of the raster signals with the codes indicating the height of the longitudinal bar graph thereby determining the position of the bright point of the longitudinal bar graph and generating the longitudinal bar graph display signals.

The codes indicating the height of the longitudinal bar graph are expressed by the number of the scanning line at which the bright point of the bar graph is started.

The video display system further comprises means for terminating the output of the character generating means and switching the output to the video signals of the longitudinal bar graph by the codes for starting said bar graph. The video display system also further comprises means for terminating the output of the character generating means and switching the output to the video signals of the longitudinal bar graph by the codes for ending the bar graph.

In accordance with the present invention, a method of displaying bar graphs in a video display system includes raster type cathode ray tube display means having memory means for storing character codes corresponding to the display position in the display means. Input means stores character codes in the address of the memory means. Character generating means has an input connected to the memory means and an output for receiving designated character codes in succession from the memory means. Output means connected to the output of the character generating means reads out the output of the character generating means and displays the read out output. In accordance with the invention, the method comprises the steps of storing in the memory means codes for starting a longitudinal bar graph, codes indicating the height of the longitudinal bar graph and codes for ending the longitudinal bar graph, and comparing the number of the raster signals with the codes indicating the height of the longitudinal bar graph thereby determining the position of the bright point of the longitudinal bar graph and generating the longitudinal bar graph display signals.

In order that the invention may be readily carried into effect, it will now be described with reference to the accompanying drawings, wherein:

FIG. **1** is a block diagram of a known type of video display system for displaying characters;

FIG. **2** is a schematic representation of the display picture of the video display system of the invention;

FIG. **3** is a block diagram of an embodiment of a buffer memory utilized in the video display system of the invention;

FIG. **4** is a block diagram of an embodiment of the converter of the video display system of the invention for converting codes into video signals in order to generate characters and longitudinal bar graphs;

FIG. **5** is a block diagram of an embodiment of the first register of the converter of FIG. **4**;

FIG. **6** is a block diagram of an embodiment of the second register of the converter of FIG. **4**;

FIG. **7** is a block diagram of an embodiment of the detector of the converter of FIG. **4**;

FIG. **8** is a block diagram of an embodiment of the first decoder of the character generator of the converter of FIG. **4**;

FIG. **9** is a block diagram of an embodiment of the second decoder of the character generator of the converter of FIG. **4**;

FIG. **10** is a circuit diagram of an embodiment of the memory of the character generator of the converter of FIG. **4**; and

FIG. **11** is a graphical presentation of various video signals converted from codes, in accordance with the invention.

In the FIGS., the same components are identified by the same reference numerals.

FIG. **1** shows a conventional video display system which is able to display only characters. In FIG. **1**, a central processor unit **11** of an electronic computer provides codes which are supplied to a buffer memory **12**. The codes from the central processor unit **11** are stored in the buffer memory **12** by clock signals from a block signal generating circuit **13**. The clock signal generating circuit **13** has outputs connected in common to each of the buffer memory **12**, a character generator **14** connected to the output of said buffer memory and a mixer **15** connected to the output of said character generator. An output terminal **16** is connected to the output of the mixer **15**.

Codes from the buffer memory **12** are supplied to the character generator **14** in accordance with the clock signals of the clock signal generating circuit **13**. The codes supplied to the character generator **14** are converted by said character generator into character signals corresponding to the codes. The character signals produced by the character generator **14** are supplied to the mixer **15**. The mixer **15** produces video signals by mixing or adding the character signals from the character generator **14** and synchronizing signals from the clock signal generating circuit **13**. The video signals are provided at the output terminal **16** and are transmitted to the cathode ray tube which displays the character.

As illustrated in FIG. 2, the video display system of the invention displays longitudinal bar graphs and characters. The longitudinal bar graph signals are generated by controlling the output of the character generator without providing a buffer memory in addition to the buffer memory 12 utilized in the video display system of FIG. 1.

In order to maintain simplicity in illustration, FIG. 2 shows several longitudinal bar graphs displayed in part of a display picture capable of displaying characters of six lines and seven columns. In the embodiment of the invention described herein, a character is constituted by seven dots in the longitudinal direction and five dots in the lateral direction. In other words, a character is displayed by seven scanning lines or scannings in the longitudinal direction and the control of bright points of five dots in the lateral direction. A space of three scannings or scanning lines is provided between two lines. Although the aforedescribed numbers are utilized in the following explanation, such numbers may be arbitrarily varied.

The video display system of the invention may display 125 types of characters and longitudinal bar graphs of 128 heights. The code informations corresponding to these characters and graphs are expressed by seven bits. 128 or 2^7 types of informations may be expressed by seven bits. Therefore, 125 types of codes utilized for characters coincide with 125 types of codes utilized for longitudinal bar graphs. In the video display system of the invention, the codes not used for characters of the 128 types of codes are utilized for the switching between the codes corresponding to characters and the codes corresponding to the heights of the longitudinal bar graphs. This is further explained with reference to FIG. 2.

Codes corresponding to characters are stored in the portions of the memory corresponding to the portions of the display picture of FIG. 2 in which characters are displayed. Bar graph starting codes for switching the character codes to the codes representing the heights of the longitudinal bar graphs are stored in the portions of the memory corresponding to the portions having solid oblique lines of the display picture. Codes representing the heights of the longitudinal bar graphs are stored in the portions of the memory corresponding to the blank rectangular portions of the display picture. Bar graph ending codes for switching codes representing the heights of the longitudinal bar graphs to character codes are stored in the portions of the memory corresponding to the portions having broken oblique lines of the display picture.

A code indicating the height of a longitudinal bar graph is expressed by the number of the scanning line at which the bright point of the graph starts by the use of the binary coded decimal notation. The highest longitudinal bar graph may thus be scanned by 128 scannings or scanning lines. If it is assumed that a code of 0001111 is received, such code indicates that the longitudinal bar graph starts at the fifteenth scanning line. This is determined by the binary code indications 1, 2, 4, 8, the sum of which is 15.

FIG. 3 illustrates a buffer memory which may be utilized in the video display system of the invention. The buffer memory of FIG. 3 comprises a plurality of main memory circuits MM1, MM2, MM3, MM4, MM5, MM6 and MM7 and a plurality of sub memory circuits SM1, SM2, SM3, SM4, SM5, SM6 and SM7. Each of the main memory circuits MM1 to MM7 comprises a shift register having a capacity for storing codes of seven bits for one picture supplied by the central processor unit 11. Each of the sub memory circuit SM1 to SM7 comprises a shift register having a capacity for storing codes of one line supplied by the corresponding main memory circuit.

A plurality of AND gates A1, A2, A3, A4, A5, A6 and A7 are provided in FIG. 3. The output of each of the AND gates A1 to A7 is connected to the input of a corresponding one of the main memory circuits MM1 to MM7. A plurality of inputs TO1, TO2, TO3, TO4, TO5, TO6 and TO7 are connected to corresponding outputs of the central processor unit 11. Each of the inputs TO1 to TO7 is connected to a first input of a corresponding one of the AND gates A1 to A7. An input terminal CT is connected to the clock signal generating circuit 13 of FIG. 1 and supplies clock signals to the buffer memory of FIG. 3. The input terminal CT is connected in common to the second input of each of the AND gates A1 to A7.

The AND gates A1 to A7 are switched to their conductive condition in succession in accordance with the clock signals provided via the input terminal CT, so that codes from the central processor unit 11 are stored in succession in accordance with said clock signals. Furthermore, codes for the display of a line are transmitted at a time from the main memory circuits MM1 to MM7 to the sub memory circuits SM1 to SM7. Simultaneously with the supply of the codes from the main memory circuits to the sub memory circuits, said codes are re-applied to said main memory circuits via feedback loops. Each of the main memory circuits MM1 to MM7 thus has a feedback loop FL1, FL2, FL3, FL4, FL5, FL6 and FL7 connected between its output and its input.

The main memory circuits MM1 to MM7 are prepared for the supplying of codes for the display of the next line to the sub memory circuits SM1 to SM7. Codes for the display of a line supplied from the main memory circuits MM1 to MM7 are stored in the sub memory circuits SM1 to SM7 and are transmitted via corresponding output terminals T1, T2, T3, T4, T5, T6 and T7, each of which is connected to a corresponding one of said sub memory circuits. At the time that the codes for the lines are transmitted via the output terminals T1 to T7, said codes are re-stored in the sub memory circuits SM1 to SM7 via feedback loops. Thus, each of the sub memory circuits SM1 to SM7 has a feedback loop FL8, FL9, FL10, FL11, FL12, FL13 and FL14 connected between its output and its input. The foregoing operation is repeated seven times, since, as seen in FIG. 2, one character may be scanned completely by seven scannings or scanning lines.

While codes for the display of a line are supplied at a time from the main memory circuits MM1 to MM7 to the sub memory circuits SM1 to SM7, as shown in FIG. 2, codes indicating the heights of the longitudinal bar graphs are stored only in the second line in which the supplied longitudinal bar graph starting code first exists. That is, the codes are stored only in the positions corresponding to the blank rectangular portion shown in FIG. 2. This may facilitate the program and such facilitating of the program is one of the features of the invention.

The codes indicating the heights of the longitudinal bar graphs are therefore not stored in the third, fourth, fifth or sixth line, Thus, in an embodiment of the invention, as hereinafter referred to, if a longitudinal bar graph starting code is detected by a detector of a converter during the transfer of codes for the display of a line from the main memory circuits MM1 to MM7 to the sub memory circuits SM1 to SM7, pulses are generated and are supplied to an input terminal AT. The pulses supplied to the input terminal AT are supplied in common to a second input of each of a second plurality of AND gates A11, A12, A13, A14, A15, A16 and A17, and switch said AND gates to their conductive condition.

The input terminal AT is also connected in common to the second input of each of a third plurality of AND gates A21, A22, A23, A24, A25, A26 and A27 via an inverter 17. Each of the feedback loops FL8 to FL14 is connected to the first input of a corresponding one of the second plurality of AND gates A11 to A17. Thus, the feedback loop FL8 is connected from the output of the sub memory circuit SM1 to the first input of the AND gate A11, and so on. The output of each of the main memory circuits MM1 to MM7 is connected to the first input of a corresponding one of the third group of AND gates A21 to A27. Thus, the output of the first main memory circuit MM1 is connected to the first input of the AND gate A21.

A plurality of OR gates 01, 02, 03, 04, 05, 06 and 07 are provided. The output of each of the OR gates 01 to 07 is connected to the input of a corresponding one of the sub memory circuits SM1 to SM7. The output of each of the second group of AND gates A11 to A17 is connected to a first input of a corresponding one of the OR gates 01 to 07. The output of each

of the AND gates A21 to A27 of the third group of AND gates is connected to the second input of each of the OR gates 01 to 07. Thus, the output of the AND gate A11 is connected to the first input of the OR gate 01 and the output of the AND gate A21 is connected to the second input of the OR gate O1, the output of said OR gate being connected to the input of the sub memory circuit SM1, and so on.

When pulses are supplied to the input terminal AT, each of the third group of AND gates A21 and A27 is switched to its non-conductive condition, since the inverter 17 changes a signal to no signal. The outputs of the main memory circuits MM1 to MM7 are therefore terminated. The sub memory circuits SM1 to SM7 thus re-store the longitudinal bar graph starting codes. It is thus unnecessary to store the codes of the heights of the portions of the memory circuits corresponding to the positions of all the longitudinal bar graphs. The program may thus be considerably simplified.

The process of converting codes supplied by the sub memory circuits SM1 to SM7 of the buffer memory of FIG. 3 into character signals for longitudinal bar graph signals is explained with reference to FIG. 4. FIG. 4 shows a converter for converting codes into character signals for longitudinal bar graph signals. The signals supplied by the sub memory circuits SM1 to SM7 of FIG. 3 are supplied via the output terminals T1 to T7 of FIG. 3 which are coincident with input terminals T1 to T7 of FIG. 4. The input terminals T1 to T7 of FIG. 4 are connected in common to corresponding inputs of a character generator 18, a first register 19 and a detector 21.

FIG. 5 illustrates the first register 19 of the con-verter of FIG. 4. The first register 19 of FIG. 5 comprises a plurality of shift registers SR1, SR2 and SR3. Each of the shift registers SR1, SR2 and SR3 comprises seven flip flops FF1, FF2, FF3, FF4, FF5, FF6 and FF7. A plurality of EXCLUSIVE OR gates XO1, XO2, XO3, XO4, XO5, XO6 and XO7 each has a first input con-nected to a corresponding one of the input terminals T1 to T7. Each of the flip flops FF1 to FF7 of the shift register SR1 has an output connected to the second input of a corresponding one of the EXCLUSIVE OR gates XO1 to XO7. The other output of each of the flip flops FF1 to FF7 of the shift register SR1 is connected to a corresponding one of the flip flops of the shift register SR2.

An AND gate A51 has seven inputs. The output of each of the EXCLUSIVE OR gates XO1 to XO7 is connected to a corresponding one of the inputs of the AND gate A51 via a corresponding one of a plurality of inverters IN1, IN2, IN3, IN4, IN5, IN6 and IN7. Clock signals from the clock signal generating circuit 13 are supplied in common to an input of each of the shift registers SR2 and SR3. Each of the input terminals T1 to T7 from the buffer memory of FIG. 3 is connected to corresponding ones of the flip flops of the shift register SR3. The output of the shift register SR2 is connected in common to a first input of an AND gate A52 and to a first input of an EXCLUSIVE OR gate XO8. The output of the shift register SR3 is connected to the second input of the EXCLUSIVE OR gate XO8. The output of the EXCLUSIVE OR gate XO8 is connected to the second input of the AND gate A52.

The output of the AND gate A51 is connected to a first input of an OR gate O51. The output of the AND gate A52 is connected to the second input of the OR gate O51. The output of the OR gate O51 is connected to the input of a monostable multivibrator 22. The output of the monostable multivibrator 22 is connected to an output terminal 23. An input terminal ST is connected to an input of the shift register SR1 and supplies horizontal synchronizing signals to said shift register.

The horizontal synchronizing signals supplied via the input terminal ST trigger the flip flops FF1 to FF7 of the shift register SR1 in succession, thereby counting the number of horizontal synchronizing signals or the number of scannings or scanning lines. The input signals at the input terminals T1 to T7 from the buffer memory of FIG. 3 comprise an information of seven bits and, as hereinbefore described, include character codes, codes indicating the heights of the longitudinal bar graphs, longitudinal bar graph starting codes and longitudinal bar graph ending codes. As hereinafter described, however, only the codes indicating the heights of the longitudinal bar graphs are considered.

It is assumed that a code 0011111 is supplied via the input terminals T1 to T7 to the EXCLUSIVE OR gates XO1 to XO7 and to the corresponding flip flops of the shift register SR3. The code indicates that a longitudinal bar graph is started at the thirtyfirst scanning line. The number 31 is derived from the sum of the binary code indications 1, 2, 4, 8, 16. The shift register SR1 counts the horizontal synchronizing signals supplied via the input terminal ST and stores the scanning number.

If it is assumed that the scanning number is 31, indicating the thirtyfirst scanning line, the outputs of the flip flops FF1 and FF2 of the shift register SR1 are 0 and the outputs of the flip flops FF3, FF4, FF5, FF6 and FF7 are 1. Consequently, the outputs of all the EXCLUSIVE OR gates XO1 to XO7 are 0. However, since each of the EXCLUSIVE OR gates XO1 to XO7 has a corresponding one of the inverters IN1 to IN7 connected in its output, a 1 signal is supplied to each of the inputs of the AND gate A51, and said AND gate transfers a 1 signal to its output. The 1 signal transferred by the AND gate A51 indicates that the height of the longitudinal bar graph is equal to the number of the scanning lines or scannings.

The outputs of the shift register SR1 are supplied to corresponding inputs of the shift register SR2. Furthermore, as hereinbefore indicated, the outputs of the sub memory circuits SM1 to SM7 of the buffer memory of FIG. 3 are supplied to the corresponding inputs of the shift register SR3. The contents of the shift registers SR2 and SR3 are supplied to the EXCLUSIVE OR gate XO8 successively under the control of the clock signals from the clock signal generating circuit 13 supplied at the input terminal CT. The output of the EXCLUSIVE OR gate XO8 and the output of the shift register SR2 are supplied to the AND gate A52. Thus, when the AND gate A52 transfers an output signal 1, it always indicates that the contents of the shift register SR2 are greater than the contents of the shift register SR3, that is, the number of scanning lines or scannings is greater than the code indicating the height of the longitudinal bar graph.

Thus, when the number of scanning lines is greater than, or equal to, the code indicating the height of the longitudinal bar graph, a 1 signal is supplied to the monostable multivibrator 22 via the OR gate O51. The monostable multivibrator 22 then generates pulses of a pulse duration equal to bright points of five dots, that is, the width of a character or a longitudinal bar graph. When the monostable multivibrator 22 is triggered by the 1 signal from the OR gate O51, a pulse of the aforedescribed pulse duration is supplied by said monostable multivibrator to an AND gate 41 of the converter of FIG. 4.

In the converter of FIG. 4, the input terminal ST, which supplies horizontal synchronizing signals, is connected in common to the inputs of the first register 19 and a second register 24. FIG. 6 shows the second register 24 of FIG. 4. The second register 24 of FIG. 6 comprises a shift register SR4. The shift register SR4 comprises four flip flops. An output of a first of the flip flops of the shift register SR4 is connected in common to an output terminal S1 and to a first input of an AND gate A61. An output of a second of the flip flops of the shift register SR4 is connected in common to an output terminal S2 and a second input of the AND gate A61. An output of a third of the flip flops of the shift register SR4 is connected in common to an output terminal S4 and a third input of the AND gate A61. An output of a fourth of the flip flops of the shift register SR4 is connected to the fourth input of the AND gate A61. The output of the AND gate A61 is connected in common to an input of each of the four flip flops of the shift register SR4.

Horizontal synchronizing signals are supplied via the input terminal ST to the shift register SR4 and are counted in said shift register in accordance with the binary coded decimal notation until the number of scanning lines 15 is reached. The information of the number of scanning lines, 1, 2 and 4, is supplied via the output terminals S1, S2 and S4 to a second

decoder 25 of the character generator 18 of FIG. 4, as shown in FIG. 4. The information of the number of scanning lines is also supplied back to the shift register SR4 from the AND gate A61 and resets said shift register. The shift register SR4 is thereby prepared to count starting from the number of scanning lines 1.

FIG. 7 shows the detector 21 of FIG. 4. The detector 21 of FIG. 7 comprises a pair of AND gates A71 and A72. Each of the AND gates A71 and A72 has seven inputs. The input terminals T1 to T7 from the buffer memory of FIG. 3 are connected to the inputs of the AND gates A71 and A72. Each of the input terminals T1 to T7 is connected in common to a corresponding input of each of the AND gates A71 and A72. Thus, the input terminal T1 is connected in common to the first input of each of the AND gates A71 and A72, and so on. The outputs of the AND gates A71 and A72 are connected to corresponding inputs of a flip flop 26. One output of the flip flop 26 is connected to an output terminal 27 which provides a signal K which is supplied to the AND gate A41 of FIG. 4. The output output of the flip flop 26 is connected to an output terminal 28 which provides an output signal $\overline{K}$ which is supplied to an AND gate A43 of FIG. 4.

The detector 21 detects the longitudinal bar graph starting codes and the longitudinal bar graph ending codes. That is; the detector 21 of FIG. 7 detects codes stored in the portions of the memory circuits corresponding to the portions having solid oblique lines in the display picture of FIG. 2 and codes stored in the portions of the memory circuits corresponding to the portions having broken oblique lines in the display picture of FIG. 2.

The starting and ending codes are arbitrary. It may be assumed, however, that the starting codes are 1111111 and the ending codes are 1111110. The starting codes are detected by the AND gate A71 from the input codes supplied by the sub memory circuits SM1 to SM7 of the buffer memory of FIG. 3 via the input terminals T1 to T7. The detected starting codes trigger the flip flop 26, so that said flip flop produces an output signal 1 at its output terminal 27. The output signal at the output terminal 28 of the flip flop 26 is thus 0. The ending codes are detected by the AND gate A72. The detected ending codes trigger the flip flop 26 to its other condition so that said flip flop produces a signal 1 at its output terminal 28. The signal at the output terminal 27 of the flip flop 26 is then 0.

The output terminal 27 of the flip flop 26 is connected to the input terminal AT of the buffer memory of FIG. 3 and is also connected to the second input of the AND gate A41 of the converter of FIG. 4. The output terminal 28 of the flip flop 26 is connected to the second input of the AND gate A43 of the converter of FIG. 4. The flip flop 26 is so controlled that its output terminal 28 provides a signal 1 at the display starting time.

The character generator 18 of the converter of FIG. 4 comprises a first decoder 29, a second decoder 25 and a memory 31. The memory 31 of the character generator 18 is utilized exclusively for read out. FIG. 8 shows the first decoder 29 of the character generator 18 of FIG. 4. In FIG. 8, code signals from the sub memory circuits SM1 to SM7 of the buffer memory of FIG. 3 are supplied via the input terminals T1 to T7, which are the same as those connected to the outputs of said sub memory circuits.

The first decoder Comprises a plurality of AND gates A81, A82, A83, . . . equal in number to the number of types of characters displayed. Thus, although only three of the AND gates A81, A82 and A83 are shown in FIG. 8, there are 125 AND gates in the embodiment of the invention described herein. Each of the input terminals T1 to T7 is connected in common to a corresponding one of the seven inputs of each of the AND gates A81, A82, ... If it is assumed that the code for indicating the character "A" is 1010101, the code for indicating the character "B" is 1010110 and the code for indicating the character "C" is 1010011, the AND gate A81 transfers an output signal 1 when the code 1010101 is supplied to the input terminals T1 to T7, the AND gate A82 transfers an output signal 1 when the code 1010110 is supplied to said input terminals and the AND gate A83 transfers an output signal 1 when the code 1010011 is supplied to said input terminals.

FIG. 9 shows the second decoder 25 of the character generator 18 of the converter of FIG. 4. The second decoder 25 comprises a plurality of AND gates A71, A72, A73, A74, A75, A76 and A77 of a number equal to the number of scanning lines constituting a character. That is, there are seven AND gates in the second decoder 25 of FIG. 9. The AND gates A71 to A77 detect the number of scanning lines constituting a character. That is, the AND gates A71 to A77 detect 1, 2, 3, 4, 5, 6 and 7.

Input terminals S1, S2 and S4 coincide with the output terminals S1, S2 and S4 of the second register 24. Each of the input terminals S1, S2 and S4 is connected in common to a corresponding input of each of the AND gates A71 to A77. It is assumed that an information is supplied indicating that the fourth scanning line is being scanned. That is, the supplied information indicates that only the signal at the input terminal S4 is 1 and the signals of the input terminals S1 and S2 are each 0. Only the output of the AND gate A74 of the second decoder 25 is then 1 and the signal 1 is transmitted via an output terminal L4 of a plurality of output terminals L1 to L7.

FIG. 10 shows part of the memory 31 of the character generator 18 of the converter of FIG. 4. The part of the memory 31 illustrated in FIG. 10 is that utilized exclusively for reading and storing the characters A, B and C. The stored characters are selected and read out by the signals from the first decoder 29 and the second decoder 25. The signals from the first decoder 29 are supplied to input terminals A, B, C, . . . of FIG. 10 which coincide with the corresponding output terminals of FIG. 8. The input terminals L1 to L7 coincide with the corresponding output terminals of the second decoder 25 of FIG. 9. It is assumed that the signals from the first decoder 29 are supplied via the input terminal A to a plurality of AND gates A101, A102, A103, A104, A105, A106 and A107 and select the character "A."

The input terminal A is connected in common to a second input of each of the AND gates A101 to A107. Each of the input terminals L1 to L7 of a first group thereof is connected to the first input of a corresponding one of the AND gates A101 to A107. The input terminal B is connected in common to the second input of each of a second plurality of AND gates B101, B102, B103, B104, B105, B106 and B107. Each of the input terminals L1 to L7 of a second group of said terminals is connected to the first input of each of the AND gates B101 to B107. The input terminal C is connected in common to the second input of each of a plurality of AND gates C101, C102, ... Each of the input terminals L1, L2, . . . of a third group of said input terminals is connected to the first input of a corresponding one of the AND gates c101, C102, ...

The signal indicating the number of the scanning line is supplied from the second decoder 25 via the input terminals L1 to L7 of the first group of said input terminals to one of the AND gates A101 to A107. It is assumed that the scanning line at such time is the fourth scanning line. The AND gate A104 is thus switched to its conductive condition by the output signals of the first and second decoders 29 and 25, respectively, and said AND gate transfers current to a driving line D104 connected to its output. Each of a plurality of driving lines D101, D102, d103, D104, D105, D106 and D107 is connected to the output of a corresponding one of the AND gates A101 to A107 of the first group of AND gates. Each of a plurality of driving lines D201, D202, D203, D204, D205, D206 and D207 is connected to the output of a corresponding one of the AND gates B101 to B107 of the second group of AND gates. Each of a plurality of driving lines D301, D302,. . . is connected to the output of a corresponding one of the AND gates C101, C102, . . . of the third group of AND gates.

In the assumed example, when current flows in the driving line D104, a current is provided in read out lines S101 and S105 of a plurality of read out lines S101, S102, S103, S104

and S105. Each of the read out lines S101 to S105 intersects each of the driving lines D101 to D107, D201 to D207, D301, D302, . . . in a core matrix arrangement.

The cores at the intersection of the driving line D104 and the read out line S105 and at the intersection of said driving line and the read out line S101 produce output signals which are transferred to transistors TR5 and TR1, respectively, of a plurality of transistors TR1 to TR5. Each of the read out lines S101 to S105 extends from a ground line 32 via a corresponding one of a plurality of resistors 33, 34, 35, 36 and 37 to the base electrode of a corresponding one of the transistors TR1 to TR5. An additional line extends from the driving line D101 to the ground line 32 via a resistor 38. The emitter electrode of each of the transistors TR1 to TR5 is connected to a ground line 39. A positive bias is applied via a terminal +B to the collector electrode of each of the transistors TR1 to TR5 via a lead 41 and a corresponding one of resistors 42, 43, 44, 45 and 46.

An output terminal V1 is connected to the collector electrode of the transistor TR1. An output terminal V2 is connected to the collector electrode of the transistor TR2. An output terminal V3 is connected to the collector electrode of the transistor TR3. An output terminal V4 is connected to the collector electrode of the transistor TR4. An output terminal V5 is connected to the collector electrode of the transistor TR5. Since the transistors TR1 and TR5 are switched to their conductive condition in the illustrated example, a code signal 10001 indicating the fourth scanning line of the character "A" is provided at the output terminals V1 to V5 and is supplied to a register 47 of the converter of FIG. 4 via said output terminals.

A character "B" may be displayed in the display picture of FIG. 2 in the following manner. In FIG. 4, it is assumed that a character may be scanned by fourteen scanning lines or scannings, so that 0001110 is counted by the first register 19 and 0000100 is counted by the second register 24. An output signal "1" is provided at the output terminal $\overline{K}$ of the detector 21 and is supplied to the second input of the AND gate A43. Consequently, the AND gates A41 and A42 in FIG. 4 are switched to their nonconductive condition.

When the code signal 1010110 is supplied to the first decoder 29 of the character generator 18 of FIG. 4 via the input terminals T1 to T7, and a code signal 100 is supplied to the second decoder 25 of said character generator from the second register 24, a signal 1 is transferred by the AND gate A82 of said first decoder (FIG. 8) and a signal 1 is transferred by the AND gate A74 of said second decoder (FIG. 9). Consequently, the AND gate B104 of the memory 31 of the character generator 18 (FIG. 10) exclusively utilized for the read out, is switched to its conductive condition via its input terminal B and its input terminal L4. Thus, in FIG. 10, pulses are supplied to the driving line D204. A signal 1 is thus provided in each of the read out lines S102, S103, S104 and S105 and a signal 0 is provided in the read out line S101, in FIG. 10. The signals are transferred through the transistors TR1 to TR5 to the third register 47 of FIG. 4.

The output signals transferred by the transistors TR1 to TR5 and the output terminals V1 to V5 of FIG. 10 are stored in succession in flip flops FF41, FF42, FF43, FF44 and FF45 of the third register 47 of FIG. 4. That is, the code signal 01111 is stored in the flip flops FF41 to FF45 of the third register 47 of FIG. 4. Then, when the contents of the memory 31 of the character generator 18 are read out to the third register 47, such contents are shifted successively by clock signals supplied from the clock signal generating circuit 13 via an input terminal CCT and are transferred via the AND gate A43 and an OR gate 041 and are mixed with synchronizing signals supplied via an input terminal HT. Video signals are thus formed and are provided at an output terminal 48 via a video amplifier 49.

The aforedescribed operation is continuous for the characters constituting a line to be displayed. Video signals, as shown in FIG. 11, are thus provided. The video signals amplified by the video amplifier 49 are transmitted to a cathode ray tube (not shown in the FIGS.) via the output terminal 48.

A longitudinal bar graph is displayed by the video display system of the invention as illustrated in the display picture of FIG. 2. A3 shown in FIG. 2, the first longitudinal bar graph, which is the longitudinal bar graph in the third column, is started at the twentyfifth scanning line. The scanning lines are indicated on the ordinate. The second bar graph is started at the thirtythird scanning line. The third bar graph is started at the fortyfourth scanning line. The fourth bar graph is started at the twentyeighth scanning line. The fifth bar graph is started at the thirtyseventh scanning line.

When the twentyfirst scanning line is scanned, that is, when the first scanning line in the second line of characters is scanned, and a video signal 1 is produced, a code signal 1111111, which is the starting code, is supplied from the sub memory circuits SM1 to SM7 of FIG. 3 to the detector 21 of FIG. 4. The starting code signal 1111111 switches the AND gate A71 of the detector 21 of FIG. 7 to its conductive condition, so that the flip flop 26 provides a signal 1 at its output terminal K or 27. The output signal provided at the output terminal 27 of the flip flop 26 of FIG. 7 is supplied to the AND gate A41 of FIG. 4. Furthermore, the number of scanning lines 0010101 is compared with the starting signal 1111111 in the first register 19 of FIGS. 4 and 5.

Since 0010101 is smaller than 1111111, however, the first register 19 produces no output signal. A code signal 0011001 is then provided which indicates the height of the first bar graph. No output is provided by the first register 19 (FIGS. 4 and 5), however. Thus, there is no video signal while the codes indicating the height of the first, second, third, fourth and fifth bar graphs are supplied. Then, when the ending code 1111110 is supplied, the flip flop 26 of the detector 21 of FIG. 7 provides an output signal 1 at its output terminal K or 28, and said output signal is supplied to the AND gate A43 of FIG. 4. The twentysecond scanning line is then scanned. The video signals produced in the scanning of the twentysecond scanning line are the same as the video signals produced in the scanning of the twentyfirst scanning line. Thus, the same video signals are produced in the scanning of the twentyfirst to twenty fourth scanning lines. The twentyfifth scanning line is then scanned. When the video signal 1 is provided, a code indicating the height of the first bar graph is supplied and a pulse, having a pulse duration which is five times the pulse duration of the clock pulses supplied to the input terminal CCT of FIG. 4, is supplied by the first register 19 of FIG. 4. At such time, therefore, the detector 21 of FIG. 4 (FIG. 7) provides an output signal 1 at its output terminal K or 21. The AND gate A41 of FIG. 4 is thus switched to its conductive condition for a period of time equal to the aforedescribed pulse duration. The AND gate A41 of FIG. 4 thus transfers an output signal 1 during the time that five clock pulses are continuously supplied to the converter of FIG. 4 via the input terminal CCT. The five clock pulses are supplied for a time to the output terminal 48 of FIG. 4 via the AND gate A42, the OR gate O41 and the video amplifier 49.

The aforedescribed operation is repeated, and when the result of the comparison between the number of scanned scanning lines and the code indicating the height of a bar graph in the first register 19 of FIGS. 4 and 5 indicates that the number of scanned scanning lines is greater than the code indication, five clock pulses are continuously supplied to the video amplifier 49 and the longitudinal bar graph is displayed.

As hereinbefore described, the video display system of the invention is able to display a longitudinal bar graph by controlling the output of the character generator 18 of the converter of FIG. 4 and by the transfer of clock pulses in accordance with the comparison between the number of scanned scanning lines and the code indicating the height of the longitudinal bar graph. In accordance with the invention, not only may longitudinal bar graphs be displayed, but the program may be simplified. Furthermore, it is not necessary to add additional buffer memories to the buffer memories util-

ized in the conventional video display system which displays only characters.

While the invention has been described by means of specific examples and in a specific embodiment, we do not wish to be limited thereto, for obvious modifications will occur to those skilled in the art without departing from the spirit and scope of the invention.

We claim:

1. A video display system including raster type cathode ray tube display means, said video display system comprising:

memory means for storing character codes, codes indicating the height of a bar graph displayed in a direction perpendicular to the raster trace of the cathode ray tube, codes indicating the start of the area of the bar graph, and codes indicating the end of the bar graph in the address corresponding to the display position in the display means, said memory means transferring out each code successively in the order of the display position;

character generating means having an input connected to the memory means and an output for receiving the character codes from the memory means and producing character video signals corresponding to the character codes;

detecting means having inputs connected to the memory means and an output for detecting codes indicating the start of the area of the bar graph and codes indicating the end of the bar graph;

a source of horizontal synchronizing signals;

register means having inputs connected to the memory means and to the source of horizontal synchronizing signals for counting the horizontal synchronizing signals, for determining the number of the scanning line in the display means and for comparing the number of the scanning line determined with codes indicating the height of the bar graph;

a video signal amplifier;

a first gate circuit connected to the output of the character generating means for stopping the output of the character generating means when codes indicating the start of the area of the bar graph are detected by the detecting means and for transferring the output of the character generating means to the video signal amplifier when codes indicating the end of the bar graph are detected by the detecting means;

a source of clock signals; and

a second gate circuit connected to the source of clock signals for transferring a clock signal for the display of the bar graph to the video signal amplifier when the number of the scanning line is greater than the number corresponding to codes indicating the height of the bar graph as determined by the register means.

2. A video display system as claimed in claim 1, wherein codes indicating the height of the bar graph are represented by the number of the scanning line displaying the highest position of the bar graph.

3. A video display system as claimed in claim 1, wherein codes indicating the height of the bar graph are common to character codes, and wherein the first gate circuit is controlled by the detecting means thereby permitting a change of the use of codes indicating the height of the bar graph and character codes.

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