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(71) Applicant: GLOBESPANVIRATA INCORPORATED [US/US]; 100 Schulz Drive, Red Bank, NJ 07701 (US).

(72) Inventor: MOORE, Mark, Justin; 17 George Street, Cambridge CB4 1AL (GB).

(74) Agents: DUNCAN, Kevin, T. et al.; Hunton & Williams, LLP, Suite 1200, 1900 K Street, N.W., Washington, DC 20006-1109 (US).

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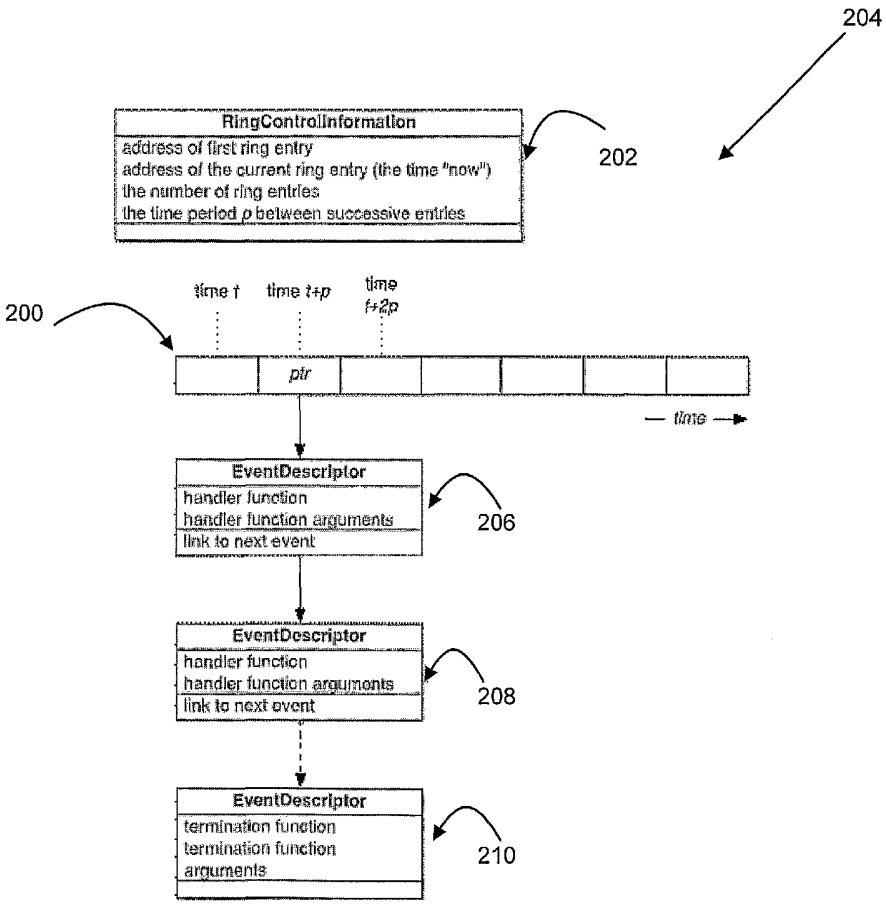
(54) Title: TIMING RING MECHANISM



(57) Abstract: A method and system for scheduling threads and timer mechanisms of events in a computer system that includes a central processing unit (CPU), a plurality of input/output (I/O) devices, such devices as storage devices, network interface devices (NIDs) and a memory which s typically used to store various applications or other instructions which, when invoked enable the CPU to perform various tasks, the timer structure provides a ring structure and an associated control block is provided. The timer mechanism of the present invention comprises a ring structure that includes an array of ring slots, with the slots relating to pointers for implementing a circular array of LIFO (Last In, First Out) queues generally where each LIFO queue maintains a listing of EventDescriptors that relate to functions which must be performed during the time slot associated with the particular pointer position.

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F9/48

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Ross, C

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	VARGHESE G ET AL: "HASHED AND HIERARCHICAL TIMING WHEELS: EFFICIENT DATA STRUCTURES FOR IMPLEMENTING A TIMER FACILITY" IEEE / ACM TRANSACTIONS ON NETWORKING, IEEE INC. NEW YORK, US, vol. 5, no. 6, December 1997 (1997-12), pages 824-834, XP000734410 ISSN: 1063-6692 abstract page 824, right-hand column, line 1 - line 16 Section II "Model" lines 1-20: page 825, left-hand column Section a. "scheme1 - Straightforward" lines 1-12: page 825, right-hand column page 826, right-hand column, line 6 - line 15 Section B. "Descrete Event Simulation", from sentence starting with "In Fig. 4..." onwards: page 827; figure 4 Section B. "Extension 2 - Exploiting Hierarchy": page 829, left-hand column - right-hand column, line 9	1-16
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Y	US 6 195 725 B1 (LUHMANN PATRICK J) 27 February 2001 (2001-02-27) abstract column 2, line 33 - line 56; figure 3 column 3, line 64 - column 4, line 6; figure 6	1-16

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