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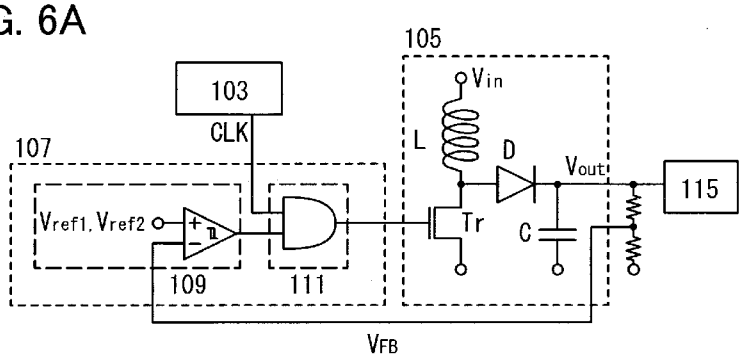
(54) **Title**: SEMICONDUCTOR DEVICE AND DISPLAY DEVICE

FIG. 6A



(57) **Abstract**: An object is to reduce power consumption of a semiconductor device including a DC-DC converter circuit. The semiconductor device includes a DC-DC converter circuit and a microprocessor. The DC-DC converter circuit includes a conversion circuit including an inductor and a transistor, and a control circuit including a comparison circuit and a logic circuit. A hysteresis comparator is used as the comparison circuit. In the control circuit, the comparison circuit compares an output signal of the conversion circuit with a first reference potential or a second reference potential, and the logic circuit performs arithmetic operation between an output signal of the comparison circuit and a clock signal of the microprocessor. In the conversion circuit, the transistor controls current flowing through the inductor in accordance with an output signal of the logic circuit, and the output signal of the conversion circuit is generated in accordance with the current flowing through the inductor.

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DESCRIPTION

SEMICONDUCTOR DEVICE AND DISPLAY DEVICE

TECHNICAL FIELD

[0001]

The technical field relates to a semiconductor device and a method for driving the semiconductor device, and a display device and a method for driving the display device.

BACKGROUND ART

[0002]

In recent years, a circuit that converts a given DC voltage into another DC voltage (also referred to as a DC-DC converter circuit or a DC to DC converter) is used in a variety of electronic devices when a stable power supply voltage is generated from a voltage with large fluctuation or when a plurality of different power supply voltages are needed, for example.

[0003]

An example of the DC-DC converter circuit is a non-isolated DC-DC converter circuit formed using a coil, a diode, and a transistor, for example (e.g., Patent Document 1). The non-isolated DC-DC converter circuit has advantages of a small circuit area and low production cost.

[Reference]

[0004]

Patent Document 1: Japanese Published Patent Application: No. S58-086868

DISCLOSURE OF INVENTION

[0005]

An object is to provide a novel circuit structure or a novel driving method for a semiconductor device including a DC-DC converter circuit. Another object is to reduce power consumption of a DC-DC converter circuit. Another object is to increase the power conversion efficiency of a DC-DC converter circuit.

[0006]

A semiconductor device includes a DC-DC converter circuit and a microprocessor. The DC-DC converter circuit is controlled using a clock signal of the microprocessor and converts an input signal (also referred to as an input voltage) into an output signal (also referred to as an output voltage).

[0007]

According to one embodiment of the present invention, a semiconductor device includes a DC-DC converter circuit and a microprocessor. The DC-DC converter circuit includes a conversion circuit including an inductor and a transistor, and a control circuit including a comparison circuit and a logic circuit. A hysteresis comparator is used as the comparison circuit. In the control circuit, the comparison circuit compares an output signal of the conversion circuit with a first reference potential or a second reference potential, and the logic circuit performs arithmetic operation of an output signal of the comparison circuit and a clock signal of the microprocessor. In the conversion circuit, the transistor controls a current flowing through the inductor in accordance with an output signal of the logic circuit, and the output signal of the conversion circuit is generated in accordance with the current flowing through the inductor.

[0008]

According to another embodiment of the present invention, a display device includes a DC-DC converter circuit, a microprocessor, and a display portion including a pixel. The DC-DC converter circuit includes a conversion circuit including an inductor and a transistor, and a control circuit including a comparison circuit and a logic circuit. A hysteresis comparator is used as the comparison circuit. In the control circuit, the comparison circuit compares an output signal of the conversion circuit with a first reference potential or a second reference potential, and the logic circuit performs arithmetic operation of an output signal of the comparison circuit and a clock signal of the microprocessor. In the conversion circuit, the transistor controls a current flowing through the inductor in accordance with an output signal of the logic circuit, and the output signal of the conversion circuit is generated in accordance with the current flowing through the inductor. In the display portion, the pixel is driven in accordance with the output signal of the conversion circuit.

[0009]

According to another embodiment of the present invention, a display device includes a DC-DC converter circuit, a microprocessor, and a display portion including a pixel. The DC-DC converter circuit includes a conversion circuit including an inductor and a transistor, and a control circuit including a comparison circuit, an amplification circuit, and a logic circuit. A hysteresis comparator is used as the comparison circuit. In the control circuit, one of a first operation and a second operation is performed. In the first operation, the comparison circuit compares an output signal of the conversion circuit with a first reference potential or a second reference potential, and the logic circuit performs arithmetic operation of an output signal of the comparison circuit and a clock signal of the microprocessor. In the second operation, the amplification circuit amplifies a difference between the output signal of the conversion circuit and a third reference potential, and the comparison circuit compares an output signal of the amplification circuit with a triangle wave. In the conversion circuit, the transistor controls a current flowing through the inductor in accordance with an output signal of the logic circuit through the first operation or an output signal of the comparison circuit through the second operation, and the output signal of the conversion circuit is generated in accordance with the current flowing through the inductor. In the display portion, one of first driving and second driving is performed. A video signal is written into the pixel at intervals of from 1 to 600 seconds in the first driving, and at intervals of 1/60 seconds or less in the second driving. In the display portion, the pixel is driven in accordance with the output signal of the conversion circuit through the first operation when the first driving is performed, and the pixel is driven in accordance with the output signal of the conversion circuit through the second operation when the second driving is performed.

[0010]

In a semiconductor device or a display device according to one embodiment of the present invention, the duty ratio in a DC-DC converter circuit can be precisely controlled, so that the reliability of the DC-DC converter circuit can be improved. Moreover, power consumption of the DC-DC converter circuit can be reduced. Further, the power conversion efficiency of the DC-DC converter circuit can be increased. In addition, production costs of the semiconductor device or the display

device can be reduced.

BRIEF DESCRIPTION OF DRAWINGS

[0011]

In the accompanying drawings:

FIGS. 1A to 1D illustrate an example of a semiconductor device;

FIG. 2 illustrates an example of a timing chart;

FIG. 3 illustrates an example of a semiconductor device;

FIGS. 4A and 4B each illustrate an example of a timing chart;

FIG. 5A illustrates an example of a semiconductor device, and FIGS. 5B and 5C each illustrate an example of a timing chart;

FIG. 6A illustrates an example of a semiconductor device, and FIG. 6B illustrates an example of a timing chart;

FIGS. 7A and 7B illustrate an example of a semiconductor device;

FIGS. 8A and 8B illustrate an example of a semiconductor device;

FIG. 9 illustrates an example of a timing chart;

FIGS. 10A and 10B illustrate an example of a display device; and

FIGS. 11A to 11D illustrate an example of a semiconductor device.

BEST MODE FOR CARRYING OUT THE INVENTION

[0012]

Embodiments will be described below with reference to the accompanying drawings. Note that the following embodiments can be implemented in many different modes, and it is apparent to those skilled in the art that modes and details can be modified in various ways without departing from the spirit and scope of the present invention. Therefore, the present invention is not construed as being limited to the description of the embodiments. In the drawings for explaining the embodiments, the same portions or portions having similar functions are denoted by the same reference numerals, and description of such portions is not repeated.

[0013]

(Embodiment 1)

In this embodiment, examples of a structure and a driving method of a

semiconductor device will be described.

[0014]

FIG. 1A is an example of a block diagram of a semiconductor device including a DC-DC converter circuit.

[0015]

The semiconductor device includes a DC-DC converter circuit 101 and a microprocessor 103. The DC-DC converter circuit 101 includes a conversion circuit 105 and a control circuit 107. The control circuit 107 includes a comparison circuit 109 and a logic circuit 111. The DC-DC converter circuit 101 generates an output signal V_{out} by conversion of an input signal V_{in}. The output signal V_{out} is input to a load 115.

[0016]

FIGS. 1B and 1C each illustrate an example of the conversion circuit 105. FIG. 1B illustrates a step-up converter ($V_{in} < V_{out}$), and FIG. 1C illustrates a step-down converter ($V_{in} > V_{out}$).

[0017]

The conversion circuit 105 at least includes a transistor Tr and an inductor L.

[0018]

The transistor Tr functions as a switch element and controls current flowing through the inductor L by being switched on (a conduction state) and off (a non-conduction state). Note that the state of the transistor Tr is determined by a pulse signal generated in the control circuit 107.

[0019]

The inductor L generates electromotive force depending on the current flowing therethrough, and generates the output signal V_{out} of the conversion circuit 105 (also called an output signal of the DC-DC converter circuit 101). The current value is determined by the level of the input signal V_{in} or the like. In such a manner, the input signal V_{in} can be converted into the output signal V_{out}. In this embodiment, the inductor L is a coil, for example.

[0020]

Next, a specific structure and operation of the conversion circuit 105 will be described, using the circuit in FIG. 1B.

[0021]

The conversion circuit 105 in FIG. 1B includes the transistor Tr, the inductor L, a diode D, and a capacitor C. A gate of the transistor Tr is electrically connected to the control circuit 107. One of a source and a drain of the transistor Tr is electrically connected to one terminal of the inductor L and an anode of the diode D. The other terminal of the inductor L is electrically connected to an input terminal to which the input signal V_{in} is input. A cathode of the diode D is electrically connected to one terminal of the capacitor C and an output terminal from which the output signal V_{out} is output. The other of the source and the drain of the transistor Tr and the other terminal of the capacitor C are electrically connected to a wiring to which a predetermined potential is input. Here, the predetermined potential is a ground potential, for example.

[0022]

Note that FIG. 1B illustrates the example in which the diode D is used for rectification and the capacitor C is used for smoothing; this embodiment is not limited to using these components.

[0023]

The conversion circuit 105 has two operations corresponding to the on state and the off state of the transistor Tr. The conversion circuit 105 steps up the input signal V_{in} by alternately repeating the two operations.

[0024]

First, when the transistor Tr is on, the inductor L generates electromotive force in accordance with current flowing therethrough. The current value is determined by the input signal V_{in}.

[0025]

Then, when the transistor Tr is off, the inductor L generates reverse electromotive force so as to maintain the current. The input signal V_{in} is added to the electromotive force generated at this time, and V_{out} becomes αV_{in}.

[0026]

Here, α is determined by the ratio of an on-state period to one switching cycle (an on-state period T_{on} + an off-state period T_{off}) of the transistor Tr, that is, by a duty ratio D (= $T_{on}/(T_{on}+T_{off})$, where $0 < D < 1$). In the case of using the step-up circuit, α

is 1/(1−D) (i.e., $\alpha > 1$), and the input signal V_{in} is stepped up.

[0027]

Then, the output signal V_{out} of the conversion circuit 105 is fed back to the control circuit 107. In the case where a feedback signal V_{FB} is higher than a desired level, the control circuit 107 decreases the duty ratio D of the pulse signal. On the other hand, in the case where the feedback signal V_{FB} is lower than a desired level, the control circuit 107 increases the duty ratio D of the pulse signal.

[0028]

Then, the transistor Tr controls the current flowing through the inductor L in accordance with the duty ratio D of the pulse signal input from the control circuit 107, and generates the output signal V_{out} by conversion of the input signal V_{in}.

[0029]

By feeding back the output signal V_{out} the control circuit 107 in such a manner, the output signal V_{out} can be closer to a desired level. DC-DC conversion can be performed in this manner.

[0030]

Similarly, in the case of using the step-down circuit in FIG. 1C, the transistor Tr is controlled in accordance with the duty ratio D ($0 < D < 1$) of the pulse signal of the control circuit 107, and V_{out} becomes αV_{in}. In the case of using the step-down circuit, α is D (i.e., $0 < \alpha < 1$), and the input signal V_{in} is stepped down.

[0031]

As the transistor Tr, a thin film transistor, a power MOSFET, or the like can be used, and a p-channel transistor or an n-channel transistor can be used as appropriate. The transistor Tr may have a top-gate structure or a bottom-gate structure. Moreover, the transistor Tr may have a channel-etch structure or a channel-stop structure. For a semiconductor material of the transistor Tr, a silicon semiconductor such as silicon or silicon germanium, an oxide semiconductor, an organic semiconductor, a compound semiconductor, or the like can be used. Alternatively, an amorphous semiconductor, a polycrystalline semiconductor, a microcrystalline semiconductor, a single crystal semiconductor, or the like can be used.

[0032]

Next, the control circuit 107 will be described. FIG. 1D illustrates an example of the control circuit 107.

[0033]

The control circuit 107 includes a comparison circuit 109 and a logic circuit 111.

[0034]

As described above, the feedback signal V_{FB} from the conversion circuit 105 is input to the comparison circuit 109. The comparison circuit 109 compares the feedback signal V_{FB} with a reference potential V_{ref}, and outputs a high-level signal (also referred to as an H signal or V_H) or a low-level signal (also referred to as an L signal or V_L) as an output signal V_{hcmp} of the comparison circuit 109.

[0035]

In this embodiment, a hysteresis comparator (HCMP) is used as the comparison circuit 109. A hysteresis comparator is a circuit that can use two reference potentials (a reference potential V_{ref1} and a reference potential V_{ref2}). The comparison circuit 109 to which the hysteresis comparator is applied can compare the feedback signal V_{FB} with the reference potential V_{ref1} or the reference potential V_{ref2}, and output a high-level signal or a low-level signal. Further, even in the case where the hysteresis comparator is used, it is possible to employ a structure where one reference potential is used instead of two reference potentials.

[0036]

The output signal V_{hcmp} of the comparison circuit 109 and a clock signal CLK of the microprocessor 103 are input to the logic circuit 111. The logic circuit 111 performs arithmetic operation of these two signals, and generates a pulse signal with a desired duty ratio D. Then, an output signal V_{GS} of the logic circuit 111 (also referred to as an output signal of the control circuit 107 or a gate signal of the transistor Tr) is output to the gate of the transistor Tr included in the conversion circuit 105. The on/off state of the transistor Tr is controlled in accordance with the duty ratio D of the pulse signal. Such control is called hysteresis control.

[0037]

In this embodiment, noise of the output signal of the control circuit 107 can be reduced by using a hysteresis comparator as the comparison circuit 109. Thus, the

duty ratio D can be precisely controlled. In other words, the output signal V_{out} of the conversion circuit 105 can be stable, and the reliability of the DC-DC converter circuit 101 can be improved.

[0038]

In this embodiment, the duty ratio D can be precisely controlled by using the clock signal CLK of the microprocessor 103. In other words, the output signal V_{out} of the conversion circuit 105 can be stable, and the reliability of the DC-DC converter circuit 101 can be improved. Moreover, the microprocessor 103 can be used also by a circuit other than the DC-DC converter circuit 101, so that production costs can be reduced.

[0039]

In particular, in the case of using the step-up circuit illustrated in FIG. 1B, the use of a hysteresis comparator and the use of the clock signal CLK are extremely effective because it is theoretically difficult to obtain a desired duty ratio D in the comparison circuit 109.

[0040]

Next, generation of a pulse signal in the control circuit 107 will be described.

[0041]

FIG. 2 is an example of a timing chart of the control circuit 107. The timing chart in FIG. 2 shows the output signal V_{hcmp} of the comparison circuit 109, the clock signal CLK of the microprocessor 103, and the output signal V_{GS} of the logic circuit 111.

[0042]

The comparison circuit 109 outputs the output signal V_{hcmp} of V_H or V_L by comparing the feedback signal V_{FB} with the reference potential V_{ref1} or the reference potential V_{ref2}.

[0043]

The logic circuit 111 performs arithmetic operation of the output signal V_{hcmp} and the clock signal CLK of the microprocessor 103. An AND circuit is used as the logic circuit 111 in this embodiment; therefore, the output signal V_{GS} is V_H when both of the two signals are V_H and is V_L in any other case.

[0044]

In such a manner, the duty ratio D of the pulse signal is determined in accordance with the output signal V_{GS}. Moreover, the on/off state of the transistor Tr is controlled in accordance with the duty ratio D, and DC-DC conversion is performed. A load 115 is driven in response to the converted output signal V_{out}.

[0045]

Note that this embodiment shows the example where an AND circuit is used as the logic circuit 111; alternatively, another logic circuit can be used without limitation to this example.

[0046]

<Structure of Hysteresis Comparator>

Next, an example of a circuit structure of a hysteresis comparator used as the comparison circuit 109 will be described with reference to FIG. 3.

[0047]

The hysteresis comparator illustrated in FIG. 3 includes a comparator 221, a comparator 222, an inverter 223, an inverter 224, a NOR gate 225, and a NOR gate 226.

[0048]

The comparator 221 has a first input terminal, a second input terminal, and an output terminal. The first input terminal is supplied with a first potential serving as a reference (also referred to as the reference potential V_{ref1} or simply V_{ref1}). The second input terminal is supplied with an input signal of the hysteresis comparator (the feedback signal V_{FB} in this embodiment).

[0049]

The comparator 222 has a first input terminal, a second input terminal, and an output terminal. The first input terminal is supplied with the input signal of the hysteresis comparator (the feedback signal V_{FB} in this embodiment). The second input terminal is supplied with a second potential serving as a reference (also referred to as the reference potential V_{ref2} or simply V_{ref2}). The reference potential V_{ref2} is smaller than the reference potential V_{ref1} (i.e., $V_{ref1} > V_{ref2}$).

[0050]

The inverter 223 has an input terminal and an output terminal. The input terminal of the inverter 223 is electrically connected to the output terminal of the comparator 221.

[0051]

The inverter 224 has an input terminal and an output terminal. The input terminal of the inverter 224 is electrically connected to the output terminal of the comparator 222.

[0052]

The NOR gate 225 has a first input terminal, a second input terminal, and an output terminal. The first input terminal of the NOR gate 225 is electrically connected to the output terminal of the inverter 223. Note that a connection point of the first input terminal of the NOR gate 225 and the output terminal of the inverter 223 is denoted by a node S.

[0053]

The NOR gate 226 has a first input terminal, a second input terminal, and an output terminal. The first input terminal of the NOR gate 226 is electrically connected to the output terminal of the NOR gate 225. The second input terminal of the NOR gate 226 is electrically connected to the output terminal of the inverter 224. The output terminal of the NOR gate 226 is electrically connected to the second input terminal of the NOR gate 225. Note that a connection point of the second input terminal of the NOR gate 226 and the output terminal of the inverter 224 is denoted by a node R. In addition, a connection point of the first input terminal of the NOR gate 226 and the output terminal of the NOR gate 225 is denoted by a node Q.

[0054]

Note that each of the logic circuits (the comparators 221 and 222, the inverters 223 and 224, and the NOR gates 225 and 226) is constituted by transistors, for example. In this embodiment, each of the logic circuits can be formed using transistors all having the same conductivity type, in which case a manufacturing process can be simplified.

[0055]

As an example, the hysteresis comparator in FIG. 3 includes two comparators. The hysteresis comparator compares an input signal of the hysteresis comparator (the feedback signal V_{FB} in this embodiment) input to each of the two comparators with the reference potential (the reference potential V_{ref1} or the reference potential V_{ref2}), and outputs a high-level signal (an H signal or V_H) or a low-level signal (an L signal or V_L).

[0056]

<Operation of Hysteresis Comparator>

Next, an example of operation of the hysteresis comparator used as the comparison circuit 109 will be described.

[0057]

For example, the operation of the hysteresis comparator can be classified according to the following cases: the case where the potential of the feedback signal V_{FB} (also simply referred to as V_{FB}) input as the input signal of the hysteresis comparator is higher than the reference potential V_{ref1} ($V_{FB} > V_{ref1}$), the case where the potential of the feedback signal V_{FB} is higher than the reference potential V_{ref2} and lower than the reference potential V_{ref1} ($V_{ref1} > V_{FB} > V_{ref2}$), and the case where the potential of the feedback signal V_{FB} is lower than the reference potential V_{ref2} ($V_{ref2} > V_{FB}$). Each of the cases will be described below.

[0058]

In the case where $V_{FB} > V_{ref1}$, the potential of the node S becomes V_H and the potential of the node R becomes V_L. At this time, the potential of the node Q becomes V_L, and the output signal of the hysteresis comparator in FIG. 3 (also referred to as the output signal V_{hcmp}) becomes V_L.

[0059]

In the case where $V_{ref1} > V_{FB} > V_{ref2}$, the potential of the node S becomes V_L and the potential of the node R becomes V_L. At this time, the potential of the node Q is kept at the state of the node Q in the previous period. For example, when the potential of the node Q is V_H in the previous period, the potential of the node Q remains at V_H and the output signal V_{hcmp} of the hysteresis comparator also remains at V_H. When the potential of the node Q is V_L in the previous period, the potential of the node Q remains at V_L and the output signal V_{hcmp} also remains at V_L.

[0060]

In the case where $V_{ref2} > V_{FB}$, the potential of the node S becomes V_L and the potential of the node R becomes V_H. At this time, the potential of the node Q becomes V_H, and the output signal V_{hcmp} of the hysteresis comparator becomes V_H.[0061]

Further, an example of the operation of the hysteresis comparator in this embodiment will be described with reference to FIGS. 4A and 4B. FIGS. 4A and 4B

are timing charts each explaining an example of the operation of the hysteresis comparator in this embodiment. FIGS. 4A and 4B each show waveforms of the feedback signal V_{FB} which is the input signal of the hysteresis comparator, the potential (V_S) of the node S, the potential (V_R) of the node R, and the output signal (V_{hcmp}) of the hysteresis comparator.

[0062]

FIG. 4A illustrates an example where the feedback signal V_{FB}, which is the input signal of the hysteresis comparator, has a triangle wave. The initial state in FIG. 4A is a state where the output signal V_{hcmp} of the hysteresis comparator is V_L and the feedback signal V_{FB} satisfies $V_{ref1} > V_{FB} > V_{ref2}$. After that, when the feedback signal V_{FB} changes from $V_{FB} > V_{ref2}$ to $V_{ref2} > V_{FB}$, the potential of the node R changes from V_L to V_H and the output signal V_{hcmp} changes from V_L to V_H. Then, when the feedback signal V_{FB} changes from $V_{ref2} > V_{FB}$ to $V_{FB} > V_{ref2}$, the potential of the node R changes from V_H to V_L. The output signal V_{hcmp} remains at V_H until the potential of the node S changes from V_L to V_H. After that, when the feedback signal V_{FB} changes from $V_{ref1} > V_{FB} > V_{ref2}$ to $V_{FB} > V_{ref1}$, the potential of the node S changes from V_L to V_H and the output signal V_{hcmp} changes from V_H to V_L. Then, when the feedback signal V_{FB} changes from $V_{FB} > V_{ref1}$ to $V_{ref1} > V_{FB}$, the potential of the node S changes from V_H to V_L. The output signal V_{hcmp} remains at V_L until the potential of the node R changes from V_L to V_H again. In such a manner, a pulse signal is generated with the hysteresis comparator.

[0063]

FIG. 4B illustrates an example where the feedback signal V_{FB}, which is the input signal of the hysteresis comparator, has a triangle wave and is adversely affected by noise (i.e., noise overlaps the triangle wave). The initial state in FIG. 4B is a state where the output signal V_{hcmp} of the hysteresis comparator is V_L and the feedback signal V_{FB} satisfies $V_{ref1} > V_{FB} > V_{ref2}$. Then, the potential of the node R changes from V_L to V_H and the output signal V_{hcmp} changes from V_L to V_H at the timing when the feedback signal V_{FB} changes from $V_{FB} > V_{ref2}$ to $V_{ref2} > V_{FB}$ for the first time.

[0064]

In FIG. 4B, because of adverse effects of noise of the input signal of the

hysteresis comparator, the relation between the reference potential V_{ref2} and the feedback signal V_{FB} is not stabilized for some time after the feedback signal V_{FB} changes from $V_{FB} > V_{ref2}$ to $V_{ref2} > V_{FB}$. The change from $V_{ref2} > V_{FB}$ to $V_{FB} > V_{ref2}$ and the change from $V_{FB} > V_{ref2}$ to $V_{ref2} > V_{FB}$ are repeated plural times, and the potential of the node R is changed accordingly. On the other hand, after becoming V_H, the output signal V_{hcmp} remains at V_H regardless of the change in the potential of the node R. The output signal V_{hcmp} remains at V_H until the potential of the node S changes from V_L to V_H. After that, the feedback signal V_{FB} changes to $V_{ref1} > V_{FB} > V_{ref2}$. The output signal V_{hcmp} remains at V_H during that time.

[0065]

Then, the potential of the node S changes from V_L to V_H and the output signal V_{hcmp} changes from V_H to V_L at the timing when the feedback signal V_{FB} changes from $V_{ref1} > V_{FB}$ to $V_{FB} > V_{ref1}$ for the first time. In FIG. 4B, because of adverse effects of noise of the input signal, the relation between the reference potential V_{ref1} and the feedback signal V_{FB} is not stabilized for some time after the feedback signal V_{FB} changes from $V_{ref1} > V_{FB}$ to $V_{FB} > V_{ref1}$. The change from $V_{FB} > V_{ref1}$ to $V_{ref1} > V_{FB}$ and the change from $V_{ref1} > V_{FB}$ to $V_{FB} > V_{ref1}$ are repeated plural times, and the potential of the node S is changed accordingly. On the other hand, after becoming V_L, the output signal V_{hcmp} remains at V_L regardless of the change in the potential of the node S. The output signal V_{hcmp} remains at V_L until the potential of the node R changes from V_L to V_H again. After that, the feedback signal V_{FB} changes to $V_{ref1} > V_{FB} > V_{ref2}$. The output signal V_{hcmp} remains at V_L during that time. In such a manner, a pulse signal is generated with the hysteresis comparator.

[0066]

By thus using the hysteresis comparator as the comparison circuit 109 in this embodiment, noise of the output signal of the comparison circuit 109 can be reduced, so that noise of the output signal of the control circuit 107 can be reduced. Thus, the duty ratio D can be precisely controlled. In other words, the output signal V_{out} of the conversion circuit 105 can be stable, and the reliability of the DC-DC converter circuit 101 can be improved.

[0067]

Note that although FIGS. 4A and 4B show that the timing of rise of the output signal V_{hcmp} is the same as that of rise of the potential (V_R) of the node R, the timing of rise of the output signal V_{hcmp} is sometimes delayed as compared to that of rise of the potential (V_R) of the node R because signal propagation delay occurs. Moreover, although FIGS. 4A and 4B show that the timing of fall of the output signal V_{hcmp} is the same as that of rise of the potential (V_S) of the node S, the timing of fall of the output signal V_{hcmp} is sometimes delayed as compared to that of rise of the potential (V_S) of the node S because signal propagation delay occurs.

[0068]

<Comparison Example>

FIGS. 5A to 5C illustrate an example of a circuit structure and operation when a comparator is used as the comparison circuit 109 instead of the hysteresis comparator shown in this embodiment. FIG. 5A illustrates a circuit structure when the comparator is used as the comparison circuit 109. The feedback signal V_{FB} and the reference potential V_{ref} are input to the comparator. The comparator compares the feedback signal V_{FB} with the reference potential V_{ref}, and outputs an output signal V_{cmp}.

[0069]

FIGS. 5B and 5C each illustrate a timing chart when the comparator is used as the comparison circuit 109. FIGS. 5B and 5C each show waveforms of the feedback signal V_{FB} which is an input signal of the comparator and the output signal (V_{cmp}) of the comparator.

[0070]

For example, the operation of the comparator can be classified according to the following cases: the case where the potential of the feedback signal V_{FB} (also simply referred to as V_{FB}) input as the input signal of the comparator is higher than the reference potential V_{ref} ($V_{FB} > V_{ref}$), and the case where the potential of the feedback signal V_{FB} is lower than the reference potential V_{ref} ($V_{ref} > V_{FB}$). In the case where $V_{FB} > V_{ref}$, the output signal V_{cmp} of the comparator becomes V_L. In the case where $V_{ref} > V_{FB}$, the output signal V_{cmp} of the comparator becomes V_H.

[0071]

FIG. 5B illustrates an example where the feedback signal V_{FB} has a triangle wave. The initial state in FIG. 5B is a state where the output signal V_{cmp} of the

comparator is V_L and the feedback signal V_{FB} satisfies $V_{FB} > V_{ref}$. After that, when the feedback signal V_{FB} changes from $V_{FB} > V_{ref}$ to $V_{ref} > V_{FB}$, the output signal V_{cmp} changes from V_L to V_H. Further, when the feedback signal V_{FB} changes from $V_{ref} > V_{FB}$ to $V_{FB} > V_{ref}$, the output signal V_{cmp} changes from V_H to V_L.

[0072]

FIG. 5C illustrates an example where the feedback signal V_{FB}, which is the input signal of the comparator, has a triangle wave and is adversely affected by noise (i.e., noise overlaps the triangle wave). The initial state in FIG. 5C is a state where the output signal V_{cmp} of the comparator is V_L and the feedback signal V_{FB} satisfies $V_{FB} > V_{ref}$. Then, when the feedback signal V_{FB} changes from $V_{FB} > V_{ref}$ to $V_{ref} > V_{FB}$, the output signal V_{cmp} changes from V_L to V_H.

[0073]

In FIG. 5C, because of adverse effects of noise of the input signal of the comparator, the relation between the reference potential V_{ref} and the feedback signal V_{FB} is not stabilized for some time after the feedback signal V_{FB} changes from $V_{FB} > V_{ref}$ to $V_{ref} > V_{FB}$. The change from $V_{ref} > V_{FB}$ to $V_{FB} > V_{ref}$ and the change from $V_{FB} > V_{ref}$ to $V_{ref} > V_{FB}$ are repeated plural times, and the potential of the output signal V_{cmp} is changed accordingly.

[0074]

In the case where the comparator is used as the comparison circuit 109 as described above, a pulse signal is generated and noise is caused at a pulse signal edge.

[0075]

By using the hysteresis comparator as the comparison circuit 109 in this embodiment, noise of the output signal of the comparison circuit 109, in particular, noise caused at a pulse signal edge as illustrated in FIG. 5C can be reduced, so that noise of the output signal of the control circuit 107 can be reduced. Thus, the duty ratio D can be precisely controlled. In other words, the output signal V_{out} of the conversion circuit 105 can be stable, and the reliability of the DC-DC converter circuit 101 can be improved.

[0076]

In addition, in this embodiment, the duty ratio D can be precisely controlled by

using the clock signal CLK of the microprocessor 103. In other words, the output signal V_{out} of the conversion circuit 105 can be stable, and the reliability of the DC-DC converter circuit 101 can be improved. Moreover, the microprocessor 103 can be used also by a circuit other than the DC-DC converter circuit 101, so that production costs can be reduced.

[0077]

In particular, in the case of using the step-up circuit illustrated in FIG. 1B, the use of the hysteresis comparator and the use of the clock signal CLK are extremely effective because it is theoretically difficult to obtain a desired duty ratio D in the comparison circuit 109.

[0078]

This embodiment can be implemented in combination with any of the other embodiments as appropriate.

[0079]

(Embodiment 2)

In this embodiment, examples of a structure and a driving method of a semiconductor device will be described.

[0080]

FIG. 6A illustrates a structure of a DC-DC converter circuit in which the circuit in FIG. 1B is used as the conversion circuit 105, the circuit in FIG. 1D is used as the control circuit 107, and an AND circuit is used as the logic circuit 111 included in the control circuit 107. That is, the circuit in FIG. 6A is a step-up DC-DC converter circuit.

[0081]

FIG. 6B is a timing chart. The timing chart in FIG. 6B shows the feedback signal V_{FB} from the conversion circuit 105, the output signal V_{hcmp} of the comparison circuit 109, the clock signal CLK of the microprocessor 103, and the output signal V_{GS} of the logic circuit 111 (also referred to as the output signal of the control circuit 107 or the gate signal of the transistor Tr).

[0082]

Here, the case where the feedback signal V_{FB} has a triangle wave is described. The comparison circuit 109 compares the feedback signal V_{FB} with the reference

potential V_{ref1} or the reference potential V_{ref2}, and outputs the output signal V_{hcmp} of V_H or V_L. The description of FIGS. 4A and 4B can be employed for the operation of generating the output signal V_{hcmp} from the feedback signal V_{FB}, the reference potential V_{ref1}, and the reference potential V_{ref2}.

[0083]

The logic circuit 111 performs arithmetic operation of the output signal V_{hcmp} of the comparison circuit 109 and the clock signal CLK of the microprocessor 103. An AND circuit is used as the logic circuit 111 in this embodiment; therefore, the output signal V_{GS} of the logic circuit 111 is V_H when both of the two signals are V_H and is V_L in any other case.

[0084]

In such a manner, the duty ratio D of the pulse signal is determined in accordance with the level of the output signal V_{GS} of the logic circuit 111. Moreover, the on/off state of the transistor Tr is controlled in accordance with the duty ratio D, and DC-DC conversion is performed. A load 115 is driven in response to the converted output signal V_{out}.

[0085]

This embodiment can be implemented in combination with any of the other embodiments as appropriate.

[0086]

(Embodiment 3)

In this embodiment, examples of a structure and a driving method of a semiconductor device will be described.

[0087]

FIG. 7A is an example of a block diagram of a semiconductor device including a DC-DC converter circuit.

[0088]

The semiconductor device in FIG. 7A has a structure where an amplification circuit 113 is additionally provided in the structure of FIG. 1A. Except for the amplification circuit 113, FIGS. 1B to 1D can be employed.

[0089]

FIG. 7B illustrates a specific circuit structure. A feature of this embodiment is

that the feedback signal V_{FB} from the conversion circuit 105 is input to one of the comparison circuit 109 and the amplification circuit 113 in the control circuit 107. Therefore, the control circuit 107 performs two operations (a first operation and a second operation). The two operations are switched and selected by a multiplexer MUX and an external signal HC-MODE for controlling the multiplexer MUX.

[0090]

In this embodiment, a hysteresis comparator is used as the comparison circuit 109. In the first operation, the comparison circuit 109 uses two reference potentials (the reference potential V_{ref1} and the reference potential V_{ref2}). In the second operation, the comparison circuit 109 uses one reference potential (a triangle wave).

[0091]

Arrows in FIG. 8A represent the case where the first operation is selected by control of the multiplexer MUX. The control with the first operation is hysteresis operation shown in Embodiment 1. That is, the feedback signal V_{FB} is input to the comparison circuit 109. The comparison circuit 109 compares the feedback signal V_{FB} with the reference potential V_{ref1} or the reference potential V_{ref2}. The logic circuit 111 performs arithmetic operation of the output signal of the comparison circuit 109 and the clock signal CLK of the microprocessor 103. The output signal of the logic circuit 111 controls the on/off state of the transistor Tr.

[0092]

Arrows in FIG. 8B represent the case where the second operation is selected by control of the multiplexer MUX. In the second operation, the feedback signal V_{FB} is input to the amplification circuit 113. The amplification circuit 113 amplifies a difference between the feedback signal V_{FB} and a reference potential V_{ref3}. The comparison circuit 109 compares an output signal V_{amp} of the amplification circuit 113 and a triangle wave. The output signal V_{GS} of the comparison circuit 109 controls the on/off state of the transistor Tr. As the amplification circuit 113, an error amplifier is used, for example. The control with the second operation is called PWM (pulse width modulation) control.

[0093]

Next, a specific example of generation of a pulse signal in the control circuit 107 will be described. Generation of a pulse signal in the first operation is as shown in

FIG. 6B.

[0094]

FIG. 9 is a timing chart in the second operation. FIG. 9 shows the feedback signal V_{FB} from the conversion circuit 105, the output signal V_{amp} of the amplification circuit 113, and the output signal V_{GS} of the comparison circuit 109 (also referred to as the output signal of the control circuit 107 or the gate signal of the transistor Tr).

[0095]

Here, the case where the feedback signal V_{FB} has a sawtooth wave is described. The amplification circuit 113 amplifies a difference between the inputted feedback signal V_{FB} and the reference potential V_{ref3}. Here, the output signal V_{amp} represents a steady-state signal and corresponds to the integral of amplified differences.

[0096]

Then, the comparison circuit 109 compares the inputted output signal V_{amp} and the triangle wave. When V_{amp} > triangle wave, the output signal V_{GS} becomes V_L. On the other hand, when triangle wave > V_{amp}, the output signal V_{GS} becomes V_H.

[0097]

In such a manner, the duty ratio D of the pulse signal is determined in accordance with the level of the output signal V_{GS}. Moreover, the on/off state of the transistor Tr is controlled in accordance with the duty ratio D, and DC-DC conversion is performed. The load 115 is driven in response to the converted output signal V_{out}.

[0098]

Note that it is important to increase the power conversion efficiency of the DC-DC converter circuit 101. The power conversion efficiency n is represented as $n = P_{out}/P_{in} < 1$, where P_{in} is an input power and P_{out} is an output power of the DC-DC converter circuit 101. The power conversion efficiency n is increased depending on the size of the load 115.

[0099]

In this embodiment, when the first operation is performed, the amplification circuit 113, a circuit for generating the triangle wave, and the like can be turned off, so that power consumption of the DC-DC converter circuit 101 can be reduced. A reduction in power consumption of the DC-DC converter circuit 101 (= $P_{in}-P_{out}$) can

increase the power conversion efficiency *n* even if the load 115 is small. In other words, the first operation is effective in the case where the load 115 is small.

[0100]

When the second operation is performed, the duty ratio D of the pulse signal of the control circuit 107 can be approximately equal to 1 ($D \approx 1$), which is larger than that in the first operation; thus, the output signal (also referred to as the output voltage) V_{out} of the DC-DC converter circuit 101 can be increased. By increasing the output signal (output voltage) V_{out} of the DC-DC converter circuit 101, the output power P_{out} is increased in the case where the load 115 is large, and the power conversion efficiency *n* can be increased. In other words, the second operation is effective in the case where the load 115 is large.

[0101]

In the semiconductor device including the DC-DC converter circuit in this embodiment, the operation is switched in accordance with the load 115 in such a manner; thus, the power conversion efficiency *n* can be increased.

[0102]

Further, the microprocessor 103 can be not only used for DC-DC conversion but have another function. For example, in a lighting device, the microprocessor 103 may be used for sensing ambient light so that the illuminance is automatically controlled. When a device is thus provided with a sensor function or a control function using the microprocessor 103, a reduction in power consumption and higher functionality can be achieved at the same time. Note that this structure can also be applied to home appliances such as air conditioners and refrigerators and other various electronic devices.

[0103]

This embodiment can be implemented in combination with any of the other embodiments as appropriate.

[0104]

(Embodiment 4)

In this embodiment, a structure and a driving method of a display device will be described.

[0105]

A display device in this embodiment includes the DC-DC converter circuit disclosed in this specification and a display panel (also referred to as a display portion) driven in accordance with the output signal V_{out} of the DC-DC converter circuit. The load 115 illustrated in FIG. 1A, FIG. 6A, FIGS. 7A and 7B, and FIGS. 8A and 8B corresponds to a display panel.

[0106]

FIG. 10A illustrates an example of a display panel. The display panel includes pixels PX, and a driver circuit GD and a driver circuit SD that drive the pixels PX. The pixels PX are arranged in matrix.

[0107]

FIG. 10B illustrates an example of the pixel PX. The pixel PX includes a switching transistor Ts, a liquid crystal element LC, and a capacitor Cs. When the transistor Ts is on, a video signal is written into the liquid crystal element LC from the driver circuit SD through a wiring S, and display based on the video signal is performed. When the transistor Ts is off, the capacitor Cs holds the video signal written into the liquid crystal element LC, so that display is maintained. The on/off state of the transistor Ts is controlled with a signal input from the driver circuit GD through a wiring G. Note that the pixel PX is not limited to having this structure.

[0108]

The display panel in this embodiment (the load 115) features two kinds of driving (first driving and second driving).

[0109]

First, in the first driving, a video signal is written into the pixel PX at intervals of 1 to 600 seconds, for example. With the first driving, writing is not performed on the pixel PX between the intervals, so that the write cycles can be reduced, leading to a reduction in power consumption. In other words, the load of the display panel is small in the first driving. Note that the first operation can be applied when pixels PX display a still image. Further, the interval may be longer than 600 seconds.

[0110]

The first operation (hysteresis operation) performed in the control circuit 107 as illustrated in FIG. 8A is effective in the case where the first driving with a small load is performed. The first operation can reduce power consumption of the DC-DC

converter circuit, so that the power conversion efficiency can be increased even when the load is small.

[0111]

Then, in the second driving, a video signal is written into the pixel PX at intervals of 1/60 seconds or less. That is, a video signal is written into the pixel PX 60 times or more per second. Specific examples of the intervals are 1/60 seconds (60 Hz), 1/120 seconds (120 Hz), and 1/240 seconds (240 Hz). Power consumption is increased because of a large number of write cycles. In other words, the load of the display panel is large in the second driving. Note that the second operation can be applied when pixels PX display a moving image.

[0112]

The second operation (PWM control) performed in the control circuit 107 as illustrated in FIG. 8B is effective in the case where the second driving with a large load is performed. Since the duty ratio D can be approximately equal to 1 ($D \approx 1$) in the second operation, the output power of the DC-DC converter circuit can be increased when the load is large, and the power conversion efficiency can be increased.

[0113]

The operation of the control circuit in the DC-DC converter circuit is switched in accordance with a method for driving the display panel as described above, so that it is possible to provide a display device in which power consumption of the DC-DC converter circuit and the display panel can be reduced and the power conversion efficiency of the DC-DC converter circuit can be increased.

[0114]

Next, a specific example of switching the operation (the first operation and the second operation) of the DC-DC converter circuit in accordance with the driving (the first driving and the second driving) of the display panel will be described with reference to FIGS. 8A and 8B and FIGS. 10A and 10B.

[0115]

In FIGS. 8A and 8B, the microprocessor 103 performs analysis, arithmetic operation, and processing of electronic data to be displayed, and generates a video signal. Here, the case where electronic data includes still image data and moving image data and the microprocessor 103 distinguishes a still image and a moving image

so that different signals (distinction signals) are output for the still image and the moving image will be described.

[0116]

In the case where electronic data to be displayed is still image data, a distinction signal indicating that the image to be displayed is a still image and a video signal corresponding to the electronic data for the still image are input to the display panel. Further, in the case where electronic data is moving image data, signals are input in a similar manner. At that time, the distinction signal is also input to the DC-DC converter circuit 101 and can be used as the external signal HC-MODE for controlling the multiplexer MUX illustrated in FIGS. 8A and 8B. In such a manner, the microprocessor 103 can be used by both the DC-DC converter circuit 101 and the display panel.

[0117]

Note that when a difference between continuous electronic data is calculated and found to be equal to or larger than a predetermined reference value, it is judged that the data is for a moving image; whereas when the difference is smaller than the reference value, it is judged that the data is for a still image. Judgment can be made with a comparator or the like.

[0118]

In the display panel, the on/off state of the transistor Ts is controlled by the driver circuit GD in accordance with a distinction signal. Moreover, the driver circuit SD performs writing on the pixel PX in accordance with a video signal. Note that a circuit for controlling the driver circuit GD and the driver circuit SD may be provided; the circuit outputs a start signal, a clock signal, and a power supply voltage to the driver circuit GD and the driver circuit SD in accordance with the distinction signal.

[0119]

The first driving is applied to a still image, and a video signal is written into the pixel PX at intervals of 1 to 600 seconds. On the other hand, the second driving is applied to a moving image, and a video signal is written into the pixel PX at intervals of 1/60 seconds or less.

[0120]

Further, in the DC-DC converter circuit 101, the multiplexer MUX is

controlled in accordance with the distinction signal, and the first operation or the second operation is selected. When the distinction signal indicating a still image is input, the first operation in FIG. 8A is performed and the output signal V_{out} is generated. When the distinction signal indicating a moving image is input, the second operation in FIG. 8B is performed and the output signal V_{out} is generated.

[0121]

As described above, the operation of the DC-DC converter circuit 101 can be switched in accordance with the amount of load of the display panel so that the DC-DC converter circuit 101 performs the first operation (hysteresis operation) when the display panel performs the first driving with a small load (displays a still image), and performs the second operation (PWM control) when the display panel performs the second driving with a large load (displays a moving image).

[0122]

This embodiment can be implemented in combination with any of the other embodiments as appropriate.

[0123]

(Embodiment 5)

In this embodiment, an example of a transistor included in a semiconductor device which is one embodiment of the disclosed invention will be described. Specifically, an example of a transistor in which a channel formation region is formed using an oxide semiconductor layer, that is, a transistor including an oxide semiconductor layer will be described.

[0124]

In the transistor described in this embodiment, a channel formation region is formed using an oxide semiconductor layer. The oxide semiconductor layer is purified to be electrically intrinsic (i-type) or substantially intrinsic. Purification means the following concepts: hydrogen which is an n-type impurity is removed from an oxide semiconductor so that the oxide semiconductor contains impurities other than the main components as little as possible, and oxygen which is one of main components of an oxide semiconductor is supplied to an oxide semiconductor layer so that defects due to oxygen vacancy in the oxide semiconductor layer are reduced.

[0125]

The number of carriers in the purified oxide semiconductor is very small, and the carrier concentration is less than 1×10^{12} /cm^3, preferably less than 1×10^{11} /cm^3. Here, a semiconductor with a carrier concentration lower than 1×10^{11} /cm^3 is called an intrinsic (i-type) semiconductor, and a semiconductor with a carrier concentration equal to or higher than 1×10^{11} /cm^3 and lower than 1×10^{12} /cm^3 is called a substantially intrinsic (substantially i-type) semiconductor.

[0126]

Since the number of carriers in the oxide semiconductor is very small, the off-state current of the transistor can be extremely low. For example, in a transistor including a purified oxide semiconductor layer, the off-state current at room temperature (per channel width of 1 μm) can be 1 aA/μm (1×10^{-18} A/μm) or lower, and further can be 100 zA/μm (1×10^{-19} A/μm) or lower.

[0127]

The off-state current can be extremely low in a transistor in which a channel formation region is formed using an oxide semiconductor layer that is purified by the removal of hydrogen contained therein and the supply of oxygen to reduce defects due to oxygen vacancy therein. Therefore, charge stored at one of a source and a drain of the transistor can be retained for a long time.

[0128]

An example of a structure and a manufacturing method of a transistor whose channel formation region is formed using an oxide semiconductor layer will be described with reference to FIGS. 11A to 11D.

[0129]

FIGS. 11A to 11D are cross-sectional views illustrating an example of a structure and a manufacturing process of a transistor whose channel formation region is formed using an oxide semiconductor layer.

[0130]

The transistor illustrated in FIG. 11D includes a conductive layer 401, an insulating layer 402, an oxide semiconductor layer 403, a conductive layer 405, and a conductive layer 406.

[0131]

The conductive layer 401 is provided over a substrate 400. The insulating layer 402 is provided over the conductive layer 401. The oxide semiconductor layer 403 is provided over the conductive layer 401 with the insulating layer 402 placed therebetween. The conductive layer 405 and the conductive layer 406 are each provided over part of the oxide semiconductor layer 403.

[0132]

Part of a top surface of the oxide semiconductor layer 403 (part of the oxide semiconductor layer 403 over which the conductive layer 405 and the conductive layer 406 are not provided) is in contact with an oxide insulating layer 407. A protective insulating layer 409 is provided over the oxide insulating layer 407.

[0133]

The transistor illustrated in FIG. 11D has a bottom-gate type structure and is also referred to as an inverted staggered transistor. Moreover, the transistor has a channel-etch structure and a single-gate structure. However, the structure of the transistor is not limited to the above. For example, the transistor may have a top-gate structure instead of a bottom-gate structure, a channel protective structure instead of a channel-etch structure, and/or a multi-gate structure instead of a single-gate structure.

[0134]

A process for manufacturing the transistor will be described below with reference to FIGS. 11A to 11D.

[0135]

First, the substrate 400 is prepared, and a first conductive film is formed over the substrate 400. There is no limitation on the substrate 400 as long as it can withstand subsequent manufacturing steps. Examples of the substrate 400 are an insulating substrate such as a glass substrate, a semiconductor substrate such as a silicon substrate, a conductive substrate such as a metal substrate, and a flexible substrate such as a plastic substrate. Moreover, an insulating layer can be provided over the substrate 400. In that case, the insulating layer serves as a base that prevents diffusion of impurities from the substrate. For example, the insulating layer serving as a base can be formed with a single-layer structure or a stacked structure including two layers or more, using an insulating layer of silicon oxide, silicon oxynitride, silicon nitride, hafnium oxide, aluminum oxide, tantalum oxide, or the like. Note that it is preferable

that the insulating layer contain hydrogen and water as little as possible.

[0136]

Examples of the first conductive film are a film of a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, and a film of an alloy material that contains any of the metal materials as a main component. Alternatively, the first conductive film can be a stack of layers of any of materials that can be applied to the first conductive film.

[0137]

Next, a first photolithography process is carried out: a first resist mask is formed over the first conductive film, the first conductive film is selectively etched using the first resist mask to form the conductive layer 401, and the first resist mask is removed. The conductive layer 401 serves as a gate electrode of the transistor.

[0138]

Then, the insulating layer 402 is formed over the conductive layer 401. The insulating layer 402 serves as a gate insulating layer of the transistor. As the insulating layer 402, a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, an aluminum oxide layer, an aluminum nitride layer, an aluminum oxynitride layer, an aluminum nitride oxide layer, or a hafnium oxide layer can be used, for example. Alternatively, the insulating layer 402 can be a stack of layers of any of the materials applicable to the insulating layer 402.

[0139]

For example, the insulating layer 402 can be formed by depositing an insulating film by high-density plasma CVD. For example, high-density plasma CVD using microwaves (e.g., a frequency of 2.45 GHz) is preferable because a dense insulating film with high breakdown voltage and high quality can be deposited. When a high-quality insulating layer is formed by depositing an insulating film by high-density plasma CVD, the interface state density between the gate insulating layer and a channel formation layer of the transistor can be reduced and interface characteristics can be favorable.

[0140]

Alternatively, the insulating layer 402 can be formed by sputtering, plasma CVD, or the like. Further, heat treatment may be performed after the formation of the

insulating layer 402. The heat treatment can improve the quality of the insulating layer 402 and the interface characteristics between the insulating layer 402 and the oxide semiconductor.

[0141]

Next, an oxide semiconductor film 530 with a thickness ranging from 2 nm to 200 nm, preferably from 5 nm to 30 nm, is formed over the insulating layer 402. For example, the oxide semiconductor film 530 can be formed by sputtering.

[0142]

Note that before the formation of the oxide semiconductor film 530, powdery substances (also referred to as particles or dust) attached on a surface of the insulating layer 402 are preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated. The reverse sputtering is a method in which voltage is applied to a substrate side with the use of an RF power supply in an argon atmosphere without applying voltage to a target side and plasma is generated in the vicinity of the substrate so that a substrate surface is modified. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used.

[0143]

The oxide semiconductor film 530 can be formed using an In-Sn-Ga-Zn-O-based oxide semiconductor, an In-Ga-Zn-O-based oxide semiconductor, an In-Sn-Zn-O-based oxide semiconductor, an In-Al-Zn-O-based oxide semiconductor, a Sn-Ga-Zn-O-based oxide semiconductor, an Al-Ga-Zn-O-based oxide semiconductor, a Sn-Al-Zn-O-based oxide semiconductor, an In-Zn-O-based oxide semiconductor, a Sn-Zn-O-based oxide semiconductor, an Al-Zn-O-based oxide semiconductor, a Zn-Mg-O-based oxide semiconductor, a Sn-Mg-O-based oxide semiconductor, an In-Mg-O-based oxide semiconductor, an In-Ga-O-based oxide semiconductor, an In-O-based oxide semiconductor, a Sn-O-based oxide semiconductor, a Zn-O-based oxide semiconductor, or the like. Here, an In-Ga-Zn-O-based oxide semiconductor is an oxide semiconductor containing at least In, Ga, and Zn, and there is no particular limitation on the composition ratio thereof. Further, the In-Ga-Zn-O-based oxide semiconductor may contain an element other than In, Ga, and Zn. The above oxide semiconductors can contain SiO_2.

[0144]

Furthermore, the oxide semiconductor film 530 can be formed using an oxide semiconductor represented by the chemical formula, $InMO_3(ZnO)_m$ ($m > 0$). Here, M denotes one or more of metal elements selected from Ga, Al, Mn, and Co. For example, M may be Ga, Ga and Al, Ga and Mn, or Ga and Co.

[0145]

For example, the oxide semiconductor film 530 can be formed by sputtering with the use of an In-Ga-Zn-O-based oxide target (FIG. 11A). The atmosphere in which the oxide semiconductor film 530 is formed can be a rare gas (typically argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere of a rare gas and oxygen.

[0146]

As a sputtering gas used for forming the oxide semiconductor film 530, a high-purity gas from which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed is preferably used, for example.

[0147]

Next, a second photolithography process is carried out: a second resist mask is formed over the oxide semiconductor film 530, the oxide semiconductor film 530 is selectively etched using the second resist mask to process the oxide semiconductor film 530 into an island-shaped oxide semiconductor layer 403, and the second resist mask is removed.

[0148]

For example, dry etching, wet etching, or both dry etching and wet etching can be employed for etching of the oxide semiconductor film 530.

[0149]

Next, the oxide semiconductor layer is subjected to first heat treatment. With the first heat treatment, dehydration or dehydrogenation of the oxide semiconductor layer can be conducted. The temperature of the first heat treatment is equal to or higher than 400 °C and lower than the strain point of the substrate (see FIG. 11B).

[0150]

A heat treatment apparatus used for the heat treatment is not limited to an electric furnace and may be an apparatus for heating an object by heat conduction or heat radiation from a heating element such as a resistance heating element. For

example, an RTA (rapid thermal annealing) apparatus such as a GRTA (gas rapid thermal annealing) apparatus or an LRTA (lamp rapid thermal annealing) apparatus can be used as the heat treatment apparatus. An LRTA apparatus is an apparatus for heating an object by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas. An example of the high-temperature gas is an inert gas that does not react with an object by heat treatment, such as nitrogen or a rare gas like argon.

[0151]

For example, as the first heat treatment, GRTA may be performed in the following manner: the substrate is transferred to an inert gas that has been heated to a high temperature of 650 °C to 700 °C, heated for several minutes, and transferred from the heated inert gas.

[0152]

In addition, after the first heat treatment is performed on the oxide semiconductor layer with an electric furnace, a high-purity oxygen gas or N_2O gas of 6N purity or higher (preferably 7N purity or higher) may be introduced into the same electric furnace while the temperature is maintained or decreased from the heat treatment temperature. In that case, it is preferable that the oxygen gas or the N_2O gas do not contain water, hydrogen, and the like. By the effect of the oxygen gas or the N_2O gas, oxygen that has been reduced through the step of eliminating impurities by the dehydration or dehydrogenation treatment is supplied; thus, the oxide semiconductor layer 403 can be purified.

[0153]

Next, a second conductive film is formed over the insulating layer 402 and the oxide semiconductor layer 403.

[0154]

As the second conductive film, a film of a metal material such as aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten or an alloy material that contains any of the metal materials as a main component can be used, for example.

[0155]

Alternatively, a layer containing a conductive metal oxide can be used as the second conductive film. Examples of the conductive metal oxide are indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an alloy of indium oxide and tin oxide (In_2O_3-SnO_2, referred to as ITO), an alloy of indium oxide and zinc oxide (In_2O_3-ZnO), and such a metal oxide material containing silicon oxide.

[0156]

The second conductive film may be formed by stacking films applicable to the second conductive film.

[0157]

Then, a third photolithography process is carried out: a third resist mask is formed over the second conductive film, the second conductive film is selectively etched with the use of the third resist mask to form the conductive layers 405 and 406, and the third resist mask is removed (see FIG. 11C). The conductive layers 405 and 406 each serve as a source electrode or a drain electrode of the transistor.

[0158]

Next, the oxide insulating layer 407 is formed over the oxide semiconductor layer 403, the conductive layer 405, and the conductive layer 406. At this time, the oxide insulating layer 407 is formed in contact with part of the top surface of the oxide semiconductor layer 403.

[0159]

The oxide insulating layer 407 can be formed to a thickness of at least 1 nm using a method by which an impurity such as water or hydrogen is not introduced into the oxide insulating layer 407, such as sputtering. If hydrogen is mixed into the oxide insulating layer 407, entry of hydrogen to the oxide semiconductor layer or extraction of oxygen in the oxide semiconductor layer by hydrogen might cause the backchannel of the oxide semiconductor layer to have lower resistance (to have an n-type conductivity), so that a parasitic channel may be formed. Therefore, in order to form the oxide insulating layer 407 containing as little hydrogen as possible, it is preferable that a method in which hydrogen is not used be employed for forming the oxide insulating layer 407.

[0160]

For example, a 200-nm-thick silicon oxide film can be formed as the oxide

insulating layer 407 by sputtering. The substrate temperature at the time of deposition is in the range of room temperature to 300 °C. Examples of the atmosphere in which the oxide insulating layer 407 is formed are a rare gas (typically argon) atmosphere, an oxygen atmosphere, and a mixed atmosphere of a rare gas and oxygen.

[0161]

As a target for forming the oxide insulating layer 407, a silicon oxide target or a silicon target can be used, for example. As a sputtering gas used for forming the oxide semiconductor layer 407, a high-purity gas from which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed is preferably used, for example.

[0162]

Before the oxide insulating layer 407 is formed, plasma treatment with the use of a gas of N_2O, N_2, Ar, or the like may be performed to remove water or the like adsorbed on an exposed surface of the oxide semiconductor layer 403. In the case where plasma treatment is performed, the oxide insulating layer 407 that is in contact with part of the top surface of the oxide semiconductor layer 403 is preferably formed without exposure to the air.

[0163]

Moreover, after the oxide insulating layer 407 is formed, second heat treatment (preferably at temperatures in the range of 200 °C to 400 °C, for example, in the range of 250 °C to 350 °C) can be performed in an inert gas atmosphere or an oxygen gas atmosphere. For example, the second heat treatment can be performed at 250 °C for one hour in a nitrogen atmosphere. In the second heat treatment, heat is applied while part of the top surface of the oxide semiconductor layer 403 is in contact with the oxide insulating layer 407.

[0164]

When a silicon oxide layer having a lot of defects is used as the oxide insulating layer 407, impurities such as hydrogen, moisture, hydroxyl groups, or hydride contained in the oxide semiconductor layer 403 are diffused into the oxide insulating layer 407 with heat treatment performed after formation of the silicon oxide layer, so that the impurities contained in the oxide semiconductor layer can be further reduced.

Note that a doping process using oxygen or halogen (e.g., fluorine or chlorine) may be performed after the second heat treatment. For the doping process, plasma doping with inductively coupled plasma is preferably employed. With the doping process, hydrogen in the oxide semiconductor layer 403 is extracted by oxygen or halogen and removed. Further, the doping process can produce a similar effect when performed before the second heat treatment, before formation of the oxide insulating layer 407, before formation of the conductive layers 405 and 406, before the first heat treatment, or before formation of the oxide semiconductor layer 403. In addition, when doping is performed with high-density plasma generated using microwaves (e.g., a frequency of 2.45 GHz), the interface state density between the oxide semiconductor layer 403 and the insulating layer 402 can be reduced and interface characteristics can be favorable.

[0165]

The protective insulating layer 409 may be further formed over the oxide insulating layer 407. As the protective insulating layer 409, an inorganic insulating layer such as a silicon nitride layer, an aluminum nitride layer, a silicon nitride oxide layer, or an aluminum nitride oxide layer can be used, for example. Alternatively, the protective insulating layer 409 can be a stack of layers of any of the materials applicable to the protective insulating layer 409. For example, the protective insulating layer 409 can be formed by RF sputtering. RF sputtering is preferably used as a film formation method of the protective insulating layer 409 because of its high productivity.

[0166]

After the protective insulating layer 409 is formed, heat treatment may be further performed at 100 °C and 200 °C for 1 hour to 30 hours in the air. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from a room temperature to a temperature of 100 °C to 200 °C and then decreased to a room temperature.

[0167]

Through the above steps, impurities such as hydrogen, moisture, hydroxyl groups, or hydride (also referred to as a hydrogen compound) can be removed from the oxide semiconductor layer, and in addition, oxygen can be supplied to the oxide

semiconductor layer. Accordingly, the oxide semiconductor layer can be purified. The transistor including the purified oxide semiconductor layer is manufactured through the above process.

[0168]

Note that the structure of the transistor is not limited to that illustrated in FIG. 11D. The transistor in FIG. 11D has a bottom-gate structure, a channel-etch structure, and a single-gate structure. Alternatively, the transistor may have a top-gate structure. Moreover, the transistor may have a channel protective structure instead of a channel-etch structure and/or a multi-gate structure instead of a single-gate structure. Even when the transistor has a different structure, layers included in the transistor can be formed using the methods for forming the layers in the transistor in FIG. 11D as appropriate.

[0169]

The transistor including the purified oxide semiconductor layer in this embodiment was subjected to a bias temperature test (BT test) at 85 °C with 2×10^6 V/cm for 12 hours. As a result, electrical characteristics of the transistor hardly changed, which suggested that the transistor has stable electrical characteristics.

[0170]

The carrier concentration of the purified oxide semiconductor layer in this embodiment can be lower than 1×10^{12} /cm^3 and still lower than 1×10^{11} /cm^3; thus, change in characteristics due to temperature variation can be suppressed.

[0171]

The transistor including the purified oxide semiconductor layer in this embodiment has electrical characteristics of much lower off-state current than a transistor including silicon or the like. For example, in the transistor including the purified oxide semiconductor layer, the off-state current at room temperature (per channel width of 1 μm) can be 1 aA/μm (1×10^{-18} A/μm) or lower, and further can be 100 zA/μm (1×10^{-19} A/μm) or lower.

[0172]

In the transistor including the purified oxide semiconductor layer in this embodiment, the off-state current does not exceed the above-described limit even when

the temperature changes. For example, the off-state current of the transistor can be 100 zA/μm or lower even when the temperature of the transistor is 150 °C.

[0173]

As has been described, the off-state current can be extremely low in the transistor in which a channel formation region is formed using the purified oxide semiconductor layer. Therefore, charge stored at one of a source and a drain of the transistor can be retained for a long time.

[0174]

For example, when the above transistor is used as the transistor Ts in the pixel PX in FIG. 10B, variation in display state of the pixel due to the off-state current of the transistor Ts can be suppressed; thus, a retention period of a unit pixel corresponding to one write operation of a video signal can be made longer. Therefore, the interval between write operations of video signals can be prolonged. For example, the interval between write operations of video signals can be 1 second or longer, preferably 60 seconds or longer, further preferably 600 seconds or longer. In addition, when a video signal is not written, a circuit that operates at the time of writing a video signal can be stopped; thus, power consumption can be further reduced as the interval between write operations of video signals is longer. In other words, the load of the display panel can be reduced.

[0175]

Furthermore, when the above transistor is used as the transistor Tr in the DC-DC converter circuit 101 in FIG. 1A and the like, the off-state current can be extremely low, so that the output signal of the DC-DC converter circuit 101 can be stable. That is, the reliability of the DC-DC converter circuit 101 can be improved.

[0176]

This embodiment can be implemented in combination with any of the other embodiments as appropriate.

EXPLANATION OF REFERENCES

[0177]

101: DC-DC converter circuit, 103: microprocessor, 105: conversion circuit, 107: control circuit, 109: comparison circuit, 111: logic circuit, 113: amplification circuit,

115: load, 221: comparator, 222: comparator, 223: inverter, 224: inverter, 225: NOR gate, 226: NOR gate, 400: substrate, 401: conductive layer, 402: insulating layer, 403: oxide semiconductor layer, 405: conductive layer, 406: conductive layer, 407: oxide insulating layer, 409: protective insulating layer, 530: oxide semiconductor film

5

This application is based on Japanese Patent Application serial No. 2010-116938 filed with Japan Patent Office on May 21, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising a DC-DC converter circuit, the DC-DC converter circuit comprising:

a wiring;

a conversion circuit comprising:

an inductor; and

a transistor comprising a drain terminal and a source terminal, one of which is connected to the inductor;

a hysteresis comparator comprising a first input terminal for a first reference potential, a second input terminal for a second reference potential, and a third input terminal electrically connected to an output terminal of the conversion circuit; and

a logic circuit comprising a first input terminal electrically connected to an output terminal of the hysteresis comparator, a second input terminal electrically connected to the wiring, and an output terminal electrically connected to a gate of the transistor.

2. A display device comprising:

a driver circuit; and

a DC-DC converter circuit electrically connected to the driver circuit and comprising:

a wiring;

a conversion circuit comprising:

an inductor; and

a transistor comprising a drain terminal and a source terminal, one of which is connected to the inductor;

a hysteresis comparator comprising a first input terminal for a first reference potential, a second input terminal for a second reference potential, and a third input terminal electrically connected to an output terminal of the conversion circuit; and

a logic circuit comprising a first input terminal electrically connected to an output terminal of the hysteresis comparator, a second input terminal

electrically connected to the wiring, and an output terminal electrically connected to a gate of the transistor.

3. A semiconductor device comprising a DC-DC converter circuit, the DC-DC converter circuit comprising:

a wiring;

a conversion circuit comprising:

an inductor; and

a transistor comprising a drain terminal and a source terminal, one of which is connected to the inductor;

an amplification circuit electrically connected to an output terminal of the conversion circuit;

a first multiplexer comprising a first input terminal electrically connected to the output terminal of the conversion circuit and a second input terminal electrically connected to an output terminal of the amplification circuit;

a hysteresis comparator comprising a first input terminal for a first reference potential, a second input terminal for a second reference potential, and a third input terminal electrically connected to an output terminal of the first multiplexer;

a logic circuit comprising a first input terminal electrically connected to an output terminal of the hysteresis comparator, a second input terminal electrically connected to the wiring; and

a second multiplexer comprising a first input terminal electrically connected to an output terminal of the logic circuit, a second input terminal electrically connected to an output terminal of the hysteresis comparator, and an output terminal electrically connected to a gate of the transistor.

4. A semiconductor device according to claim 1,

wherein the wiring is configured to transmit a clock signal.

5. A display device according to claim 2,

wherein the wiring is configured to transmit a clock signal.

6. A semiconductor device according to claim 3,
wherein the wiring is configured to transmit a clock signal.

7. A semiconductor device according to claim 1,
wherein the wiring is electrically connected to a microprocessor.

8. A display device according to claim 2,
wherein the wiring is electrically connected to a microprocessor.

9. A semiconductor device according to claim 3,
wherein the wiring is electrically connected to a microprocessor.

10. A semiconductor device according to claim 1,
wherein the logic circuit is an AND circuit.

11. A display device according to claim 2,
wherein the logic circuit is an AND circuit.

12. A semiconductor device according to claim 3,
wherein the logic circuit is an AND circuit.

13. A semiconductor device according to claim 1,
wherein the semiconductor device is a display device comprising a second transistor in a pixel, the second transistor comprising an oxide semiconductor layer.

14. A display device according to claim 2, further comprising a second transistor in a pixel, the second transistor comprising an oxide semiconductor layer.

15. A semiconductor device according to claim 3,
wherein the semiconductor device is a display device and further comprises a driver circuit electrically connected to the DC-DC converter circuit.

16. A semiconductor device according to claim 15, further comprising a second transistor in a pixel, the second transistor comprising an oxide semiconductor layer.

17. A semiconductor device according to claim 1, further comprising a load electrically connected to an output of the DC-DC converter circuit,

wherein the third input terminal of the hysteresis comparator is electrically connected to the output terminal of the conversion circuit, in accordance with a signal input into the load.

18. A display device according to claim 2,

wherein the third input terminal of the hysteresis comparator is electrically connected to the output terminal of the conversion circuit, in accordance with a signal input into the driver circuit.

19. A semiconductor device according to claim 3,

wherein a third input terminal of the first multiplexer and a third input terminal of the second multiplexer are connected to a control wiring.

20. A semiconductor device according to claim 1,

wherein a multiplexer is interposed between the output terminal of the logic circuit and the gate of the transistor.

21. A display device according to claim 2,

wherein a multiplexer is interposed between the output terminal of the logic circuit and the gate of the transistor.

22. A semiconductor device according to claim 1,

wherein a multiplexer is interposed between the third input terminal of the hysteresis comparator and the output terminal of the conversion circuit.

23. A display device according to claim 2,

wherein a multiplexer is interposed between the third input terminal of the

hysteresis comparator and the output terminal of the conversion circuit.

24. A semiconductor device according to claim 1,

wherein the hysteresis comparator is configured to compare an output of the conversion circuit with the first reference potential or the second reference potential, and the logic circuit is configured to perform an arithmetic operation between an output of the hysteresis comparator and a clock signal, and

wherein in the conversion circuit, the transistor is configured to control a current flowing through the inductor in accordance with an output of the logic circuit, and the output of the conversion circuit is generated in accordance with the current flowing through the inductor.

25. A display device according to claim 2,

wherein the hysteresis comparator is configured to compare an output of the conversion circuit with the first reference potential or the second reference potential, and the logic circuit is configured to perform an arithmetic operation between an output of the hysteresis comparator and a clock signal,

wherein in the conversion circuit, the transistor is configured to control a current flowing through the inductor in accordance with an output of the logic circuit, and the output of the conversion circuit is generated in accordance with the current flowing through the inductor, and

wherein a pixel of a display portion is configured to be driven in accordance with the output of the conversion circuit.

26. A semiconductor device according to claim 3,

wherein the semiconductor device is configured to perform one of a first operation and a second operation, in which in the first operation, the hysteresis comparator compares an output of the conversion circuit with the first reference potential or the second reference potential, and the logic circuit performs an arithmetic operation between an output of the hysteresis comparator and a clock signal, and in the second operation, the amplification circuit amplifies a difference between the output of the conversion circuit and a third reference potential and the hysteresis comparator

compares an output of the amplification circuit with a triangle wave signal; and

wherein in the conversion circuit, the transistor is configured to control a current flowing through the inductor in accordance with an output of the logic circuit through the first operation or an output of the hysteresis comparator through the second operation, and the output of the conversion circuit is generated in accordance with the current flowing through the inductor.

FIG. 1A

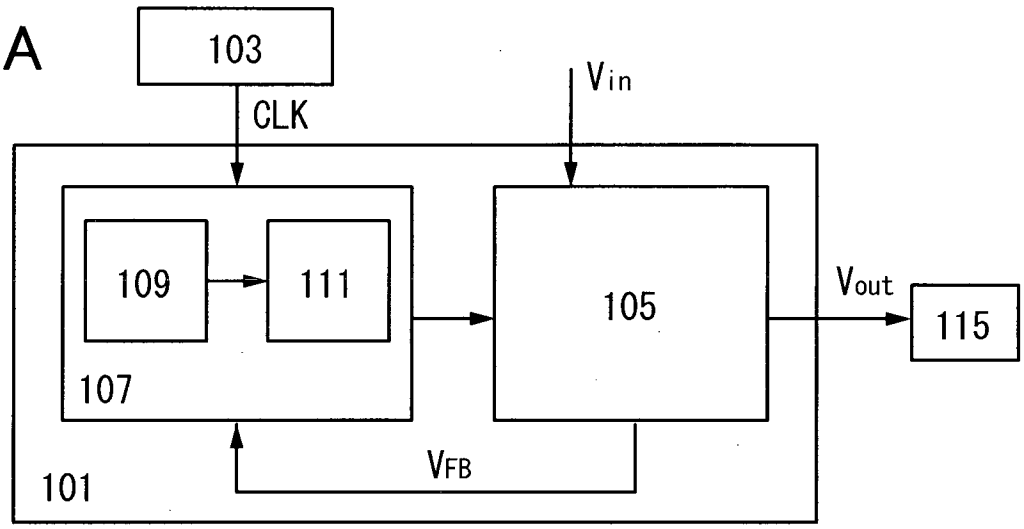


FIG. 1B

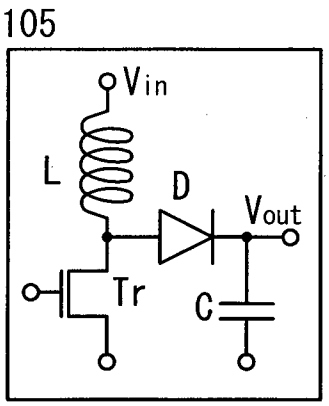


FIG. 1C

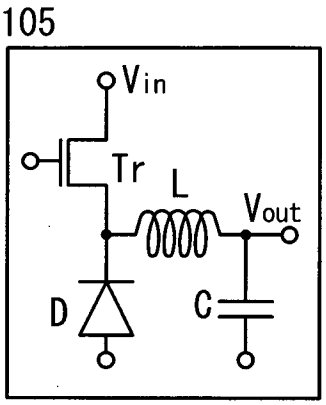


FIG. 1D

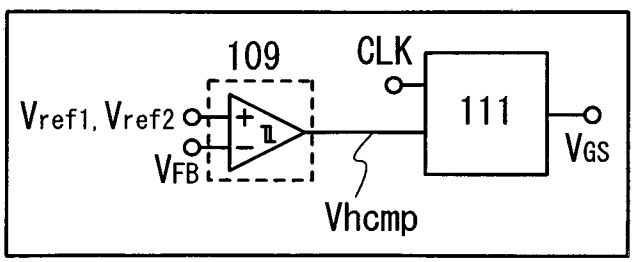


FIG. 2

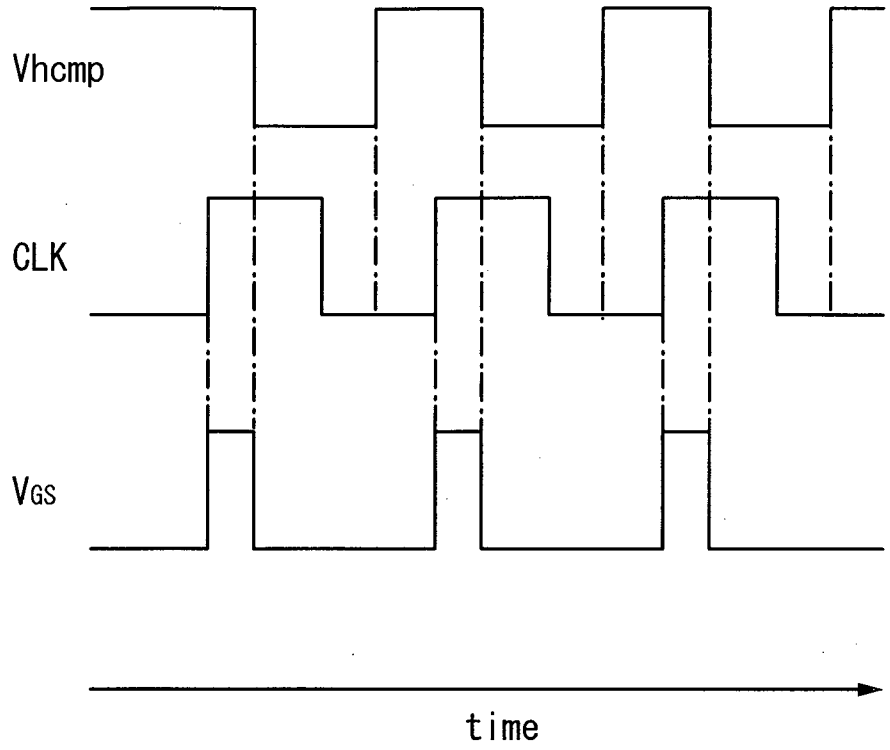


FIG. 3

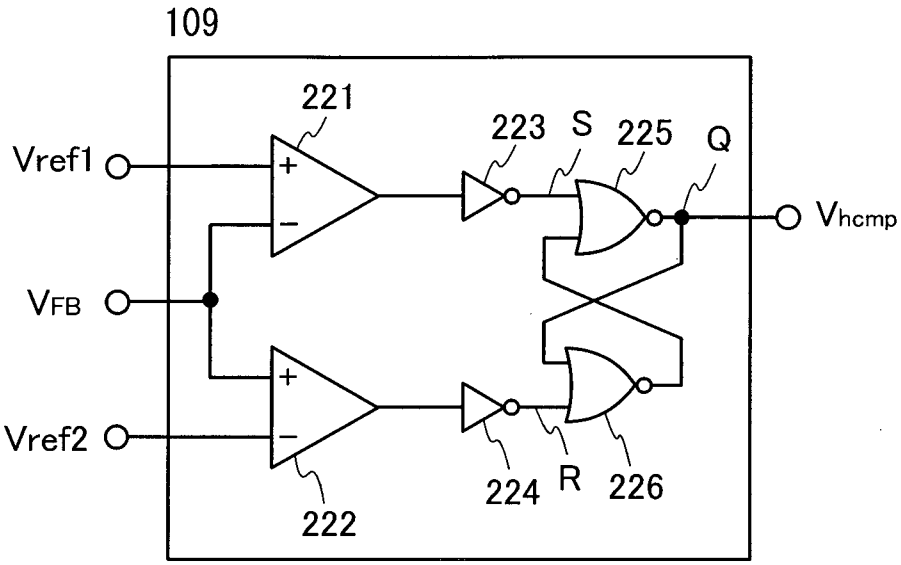


FIG. 4A

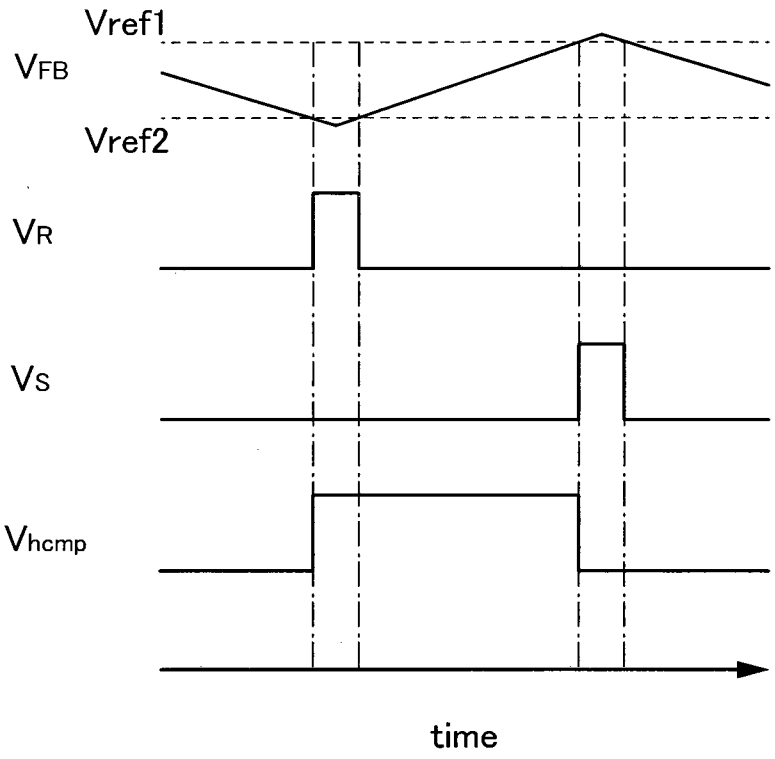

Vref1
VFB
Vref2
VR
VS
Vhcmp
time

FIG. 4B

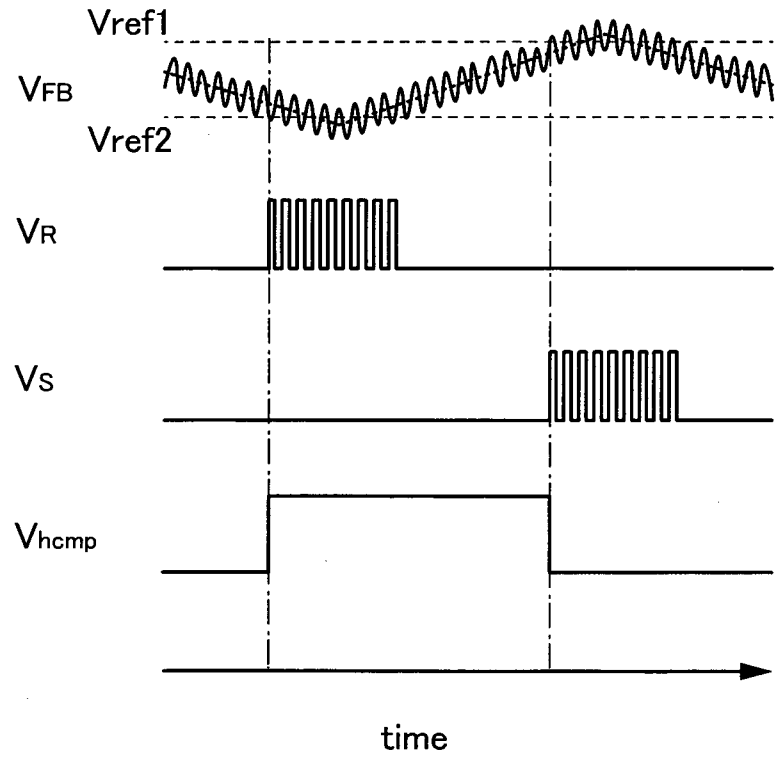

Vref1
VFB
Vref2
VR
VS
Vhcmp
time

FIG. 5A

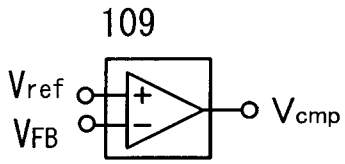


FIG. 5B

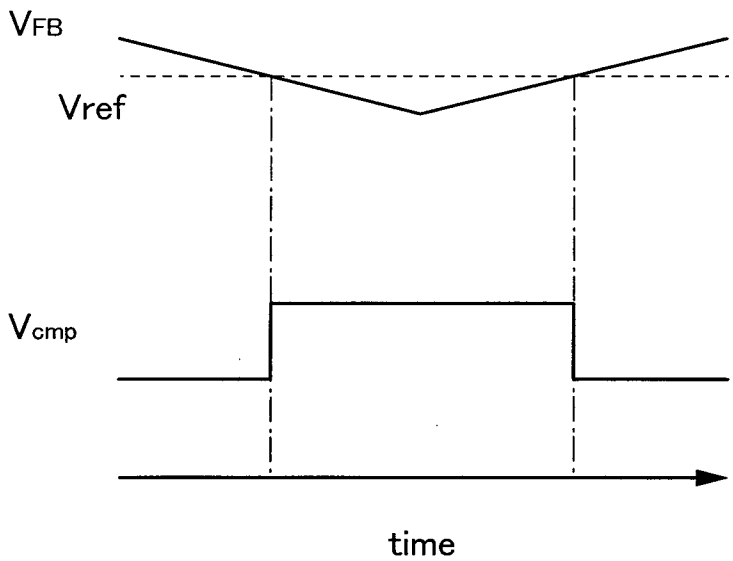


FIG. 5C

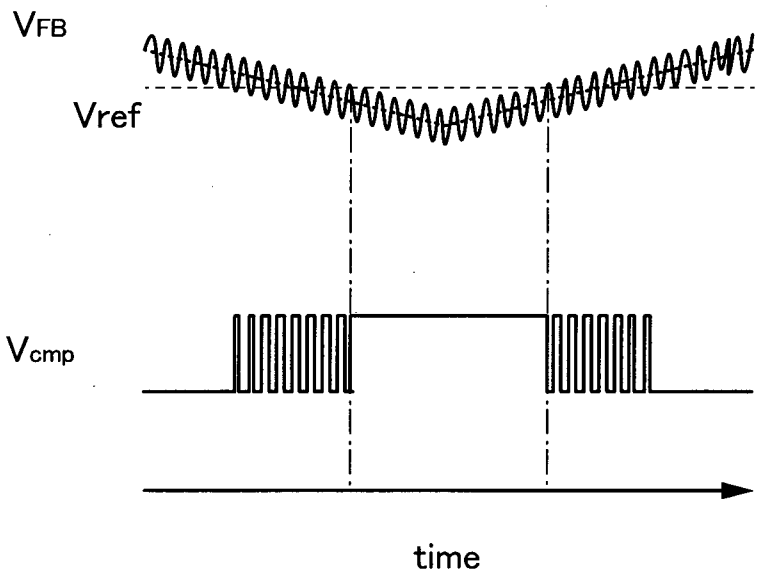


FIG. 6A

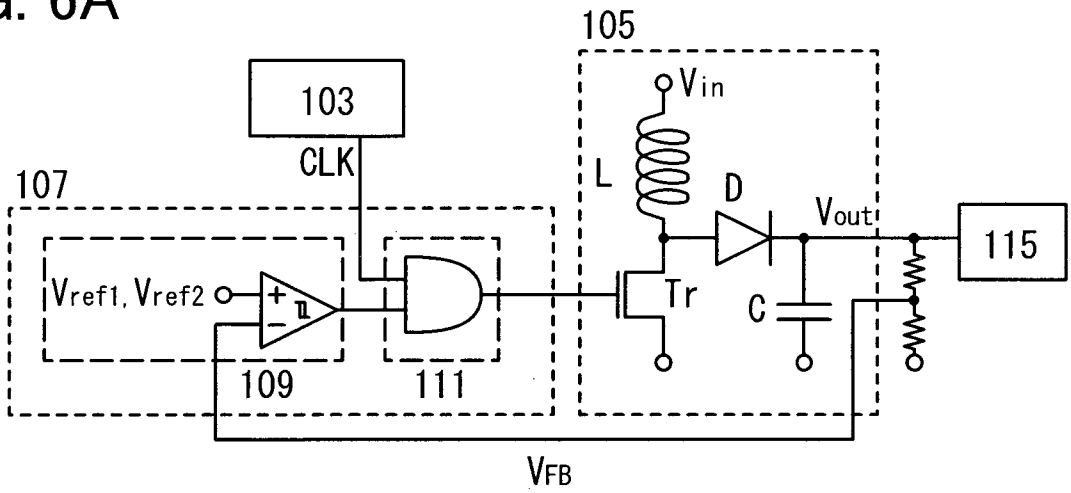

105
103
Vin
CLK
L
D
107
Vout
115
Vref1, Vref2
Tr
C
109
111
VFB

FIG. 6B

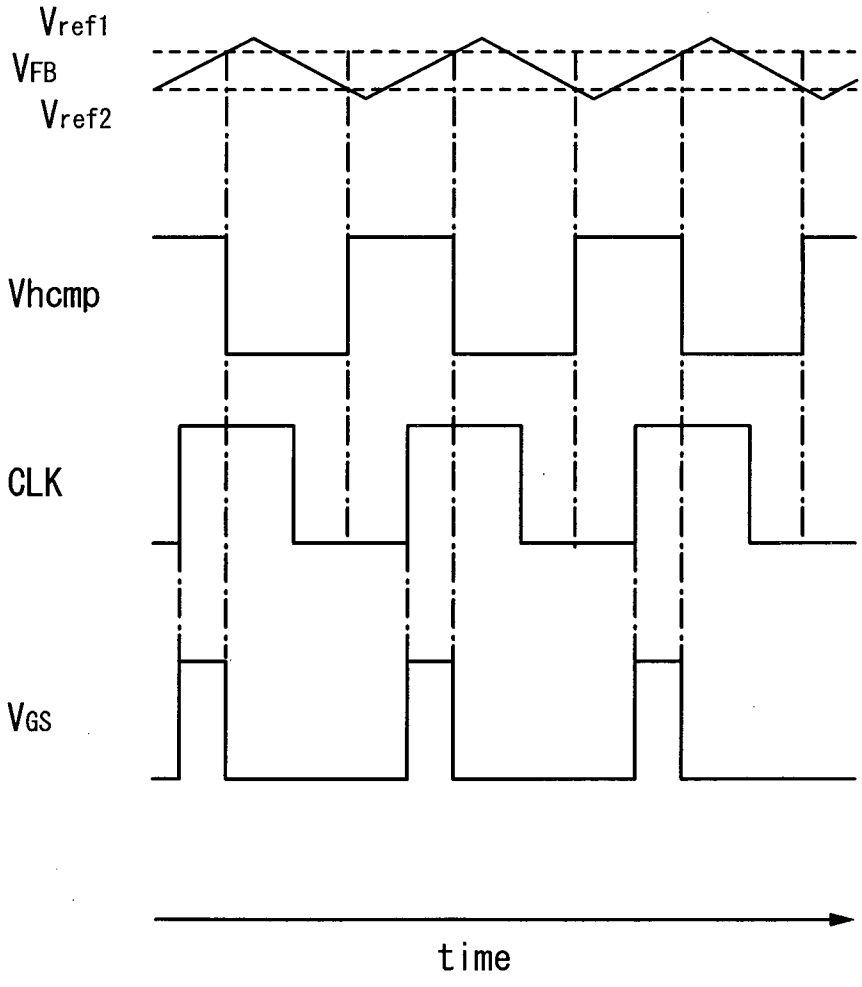

Vref1
VFB
Vref2
Vhcmp
CLK
VGS
time

FIG. 7A

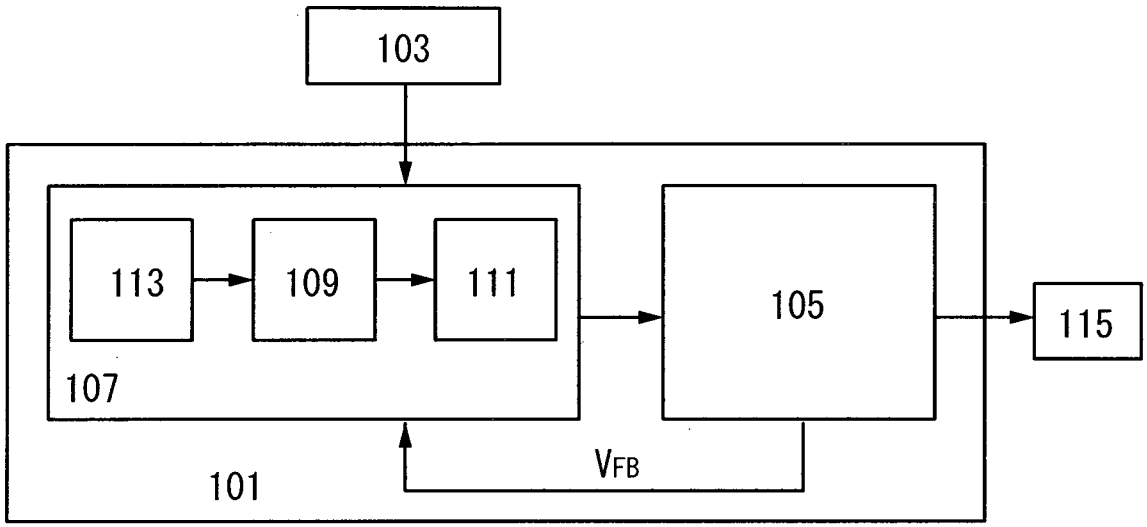

103
113
109
111
105
115
107
101
VFB

FIG. 7B

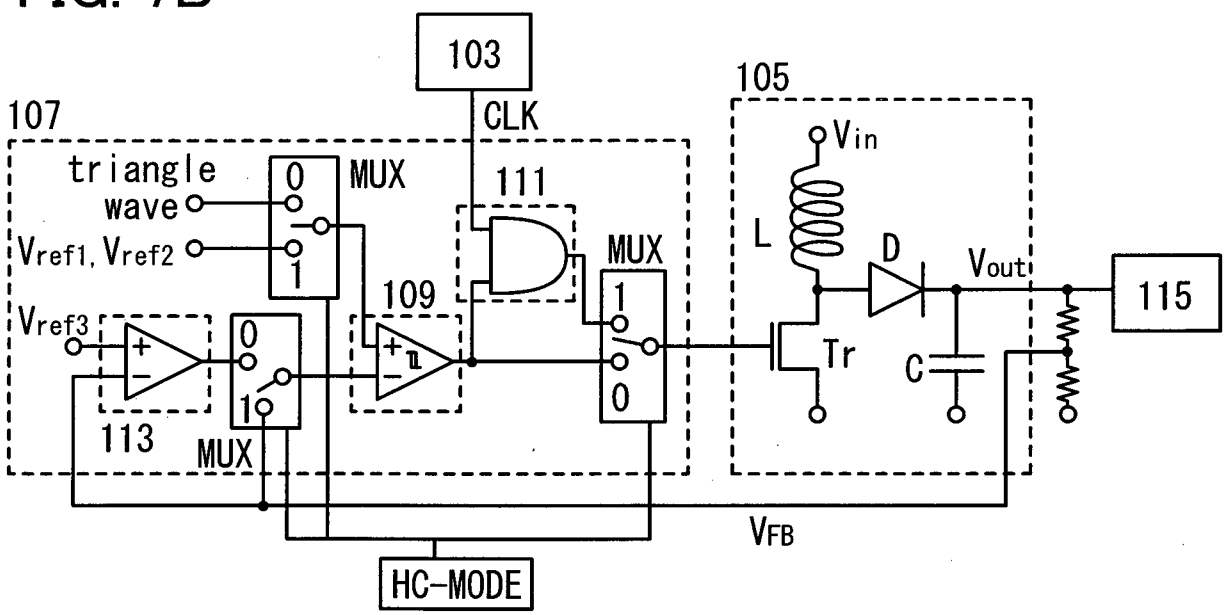

103
107
CLK
105
triangle wave
Vref1, Vref2
Vref3
0
1
MUX
111
109
MUX
Vin
L
D
Vout
115
Tr
C
113
MUX
VFB
HC-MODE

FIG. 8A

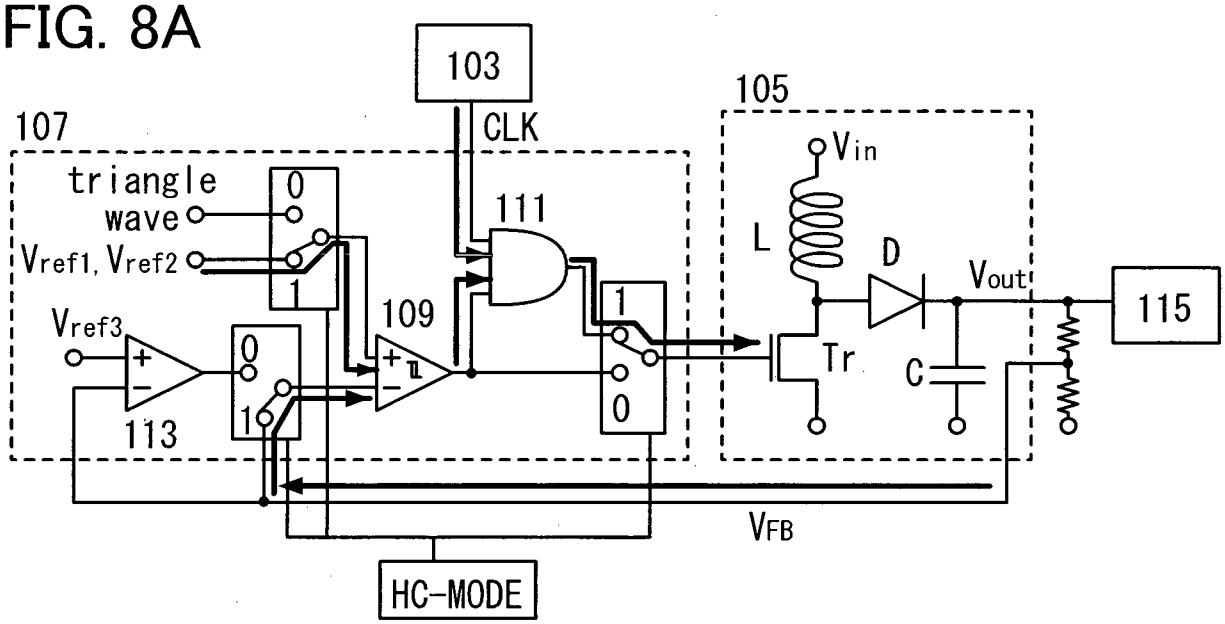

103
105
107
CLK
triangle
wave
Vref1, Vref2
Vref3
111
109
113
Vin
L
D
Vout
115
Tr
C
VFB
HC-MODE

FIG. 8B

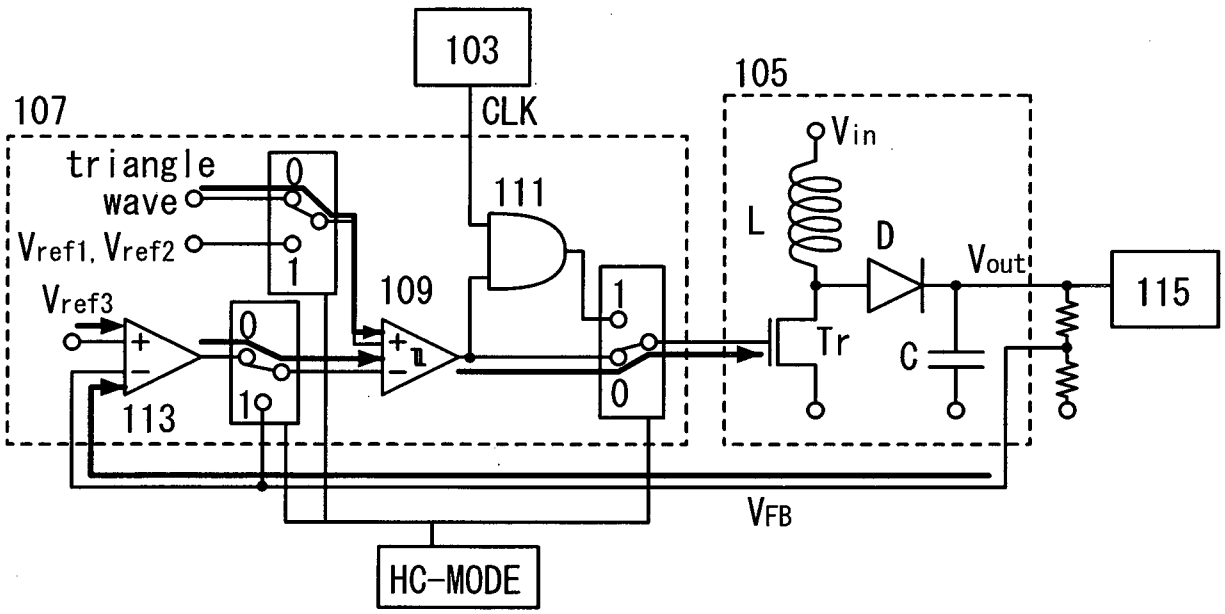

103
105
107
CLK
triangle
wave
Vref1, Vref2
Vref3
111
109
113
Vin
L
D
Vout
115
Tr
C
VFB
HC-MODE

FIG. 9

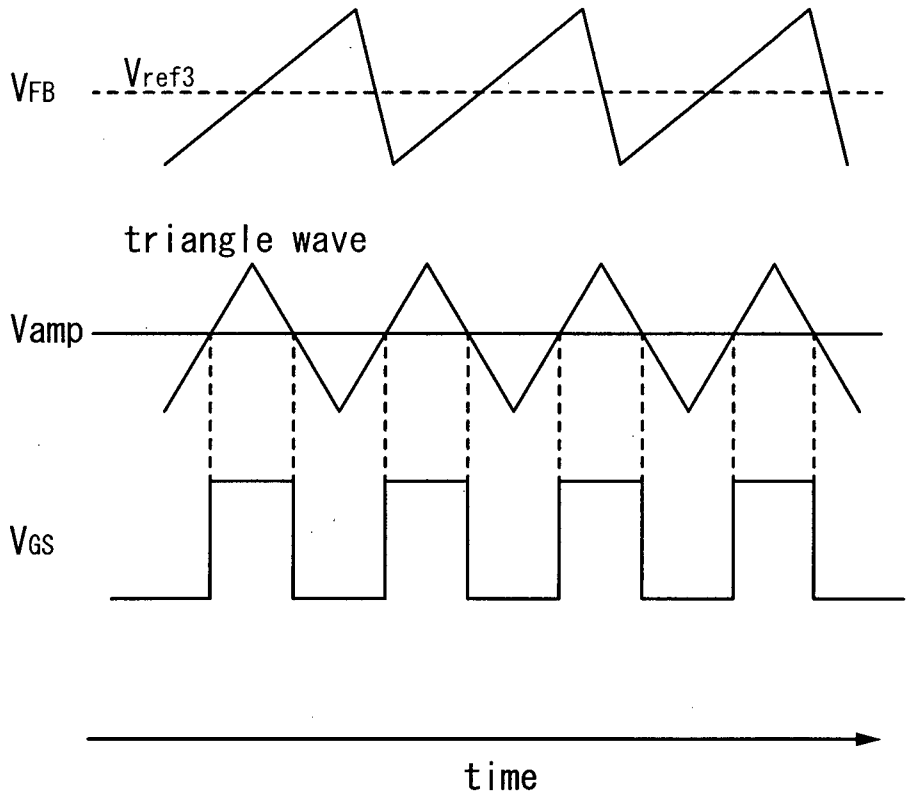


FIG. 10A

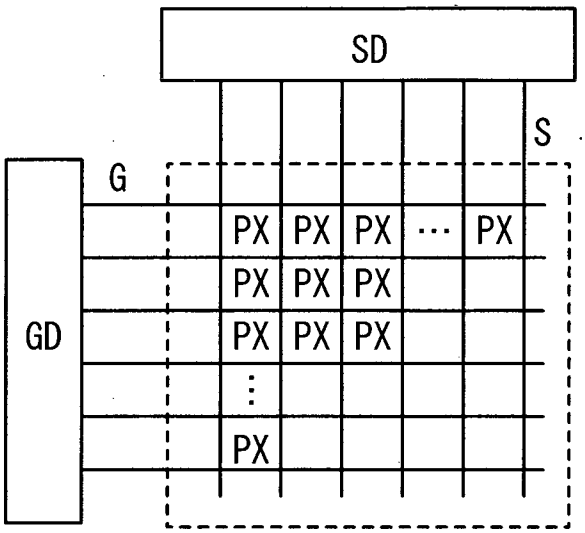


FIG. 10B

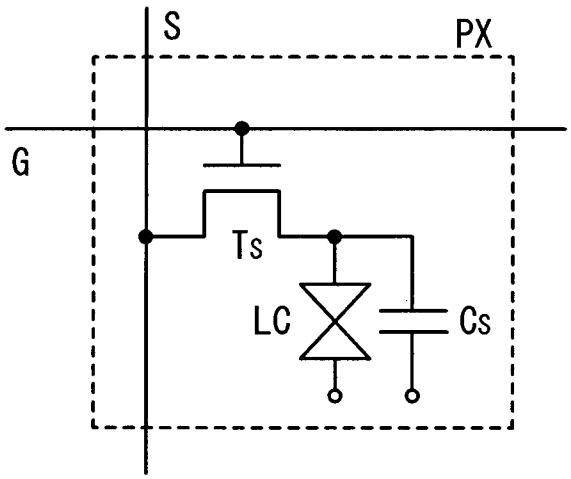


FIG. 11A

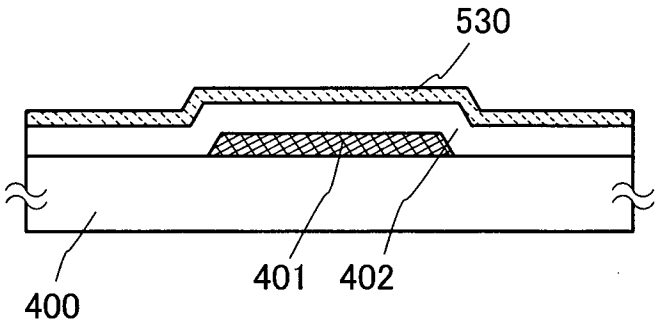


FIG. 11B

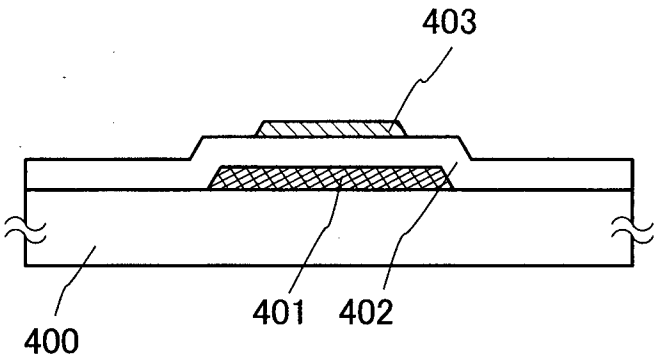


FIG. 11C

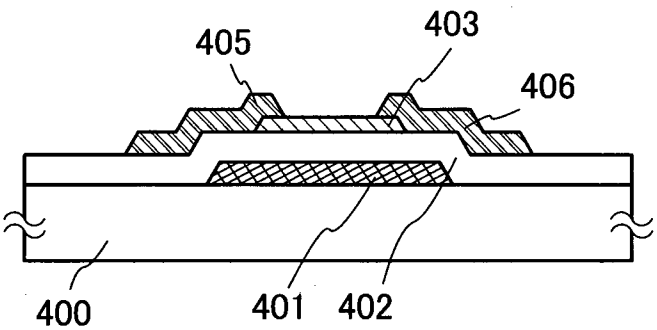
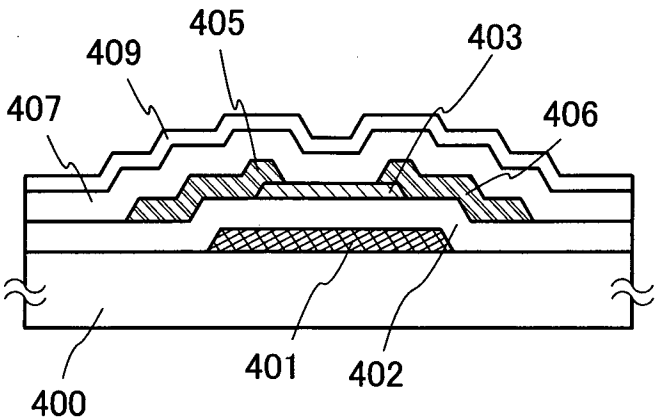


FIG. 11D



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/061593

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H02M3/155(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H02M3/155

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2004-118147 A (KYOCERA CORPORATION) 2004.04.15, 【0013】-【0016】,Fig2 (Family: None)	1-2,4-5,7-8,10-11, 13-14,17-18,24- 25
A		3,6,9,12,15,16, 19-23 ,26
Y	JP 2009-240112 A (Renesas Electronics Corporation) 2009.10.15, 【0023】-【0057】,Fig.1 (Family: None)	1-2,4-5,7-8,10-11, 13-14,17-18,24- 25
A		3,6,9,12,15,16, 19-23, 26

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
12.08.2011	23.08.2011

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/061593

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2008-191375 A (SHARP KABUSHIKI KAISHA) 2008.08.21, 【0027】-【0041】,Fig.1,Fig.2 (Family: None)	1-2,4-5,7-8,10-11, 13-14,17-18,24-25
A		3,6,9,12,15,16, 19-23, 26
Y	JP 2010-103360 A (SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.) 2010.05.06, 【0007】-【0014】 & US 2010/0102311 A1 & KR 10-2010-0045912 A & CN	1-2,4-5,7-8,10-11, 13-14,17-18,24-25
A	101728424 A	3,6,9,12,15,16, 19-23, 26