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(54) **IMAGE SENSOR CHIP, METHOD FOR MANUFACTURING THE SAME, AND IMAGE SENSOR**

BILDSENSORPLÄTTCHEN, HERSTELLUNGSVERFAHREN UND BILDSENSOR

PUCE DE DETECTEUR D'IMAGE, SON PROCEDE DE FABRICATION ET DETECTEUR D'IMAGE

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- **PATENT ABSTRACTS OF JAPAN vol. 014, no. 213 (E-0923), 7 May 1990 & JP 02 047979 A (FUJI XEROX CO LTD), 16 February 1990**

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Description

TECHNICAL FIELD

[0001] The present invention relates to an image sensor chip, and to a manufacturing method and image sensor therefor.

BACKGROUND ART

[0002] JP-A-1-208974 discloses the features of the preamble of claim 1.

[0003] Fig. 11 shows the general structure of a conventional image sensor 10 used in image-scanning devices or in the image read units of fax machines.

[0004] A plurality of image sensor chips 13 are secured within an area whose length corresponds to the read width on a substrate 12 disposed on the bottom surface of a case 11 made of a resin or the like. A transparent glass cover 14 is placed on the top surface of the case 11, and a rod lens array 15 for converging a contrast image, which is aligned with a read line L marked on the glass cover 14, as an erect image of the same size on the image sensor chip array is disposed between the read line L and the image sensor chips 13. A plurality of LEDs 16, which serve as light sources for illuminating a document D through the back surface of the glass cover 14, are mounted on a substrate 17 inside the case 11.

[0005] For example, a 1728-bit photoreceptor must be provided to obtain such an image sensor in order to read an A4 document at 8 pixels per millimeter, and 18 image sensor chips 13 should be mounted on the substrate 12 in order to provide, for example, a single image sensor chip with a 96-bit photoreceptor. Here, the length of a single image sensor chip 13 is about 12 mm.

[0006] An image sensor chip 13 is fabricated by integrating a plurality of phototransistors that correspond to the photoreceptors, analog switches connected in series with each of the phototransistors, shift registers for sequentially selecting and switching on the analog switches in accordance with clock pulses, and the like. The output side of each of the analog switches is brought out to the output terminal of the chip.

[0007] An electric current corresponding to the amount of light received during a read cycle flows through each phototransistor. When such an image sensor chip is selected, the analog switches are sequentially switched on, for example, during the fall cycles of clock pulses, with the result that microcurrent analog data corresponding to the amount of light received by each phototransistor are serially outputted to the output terminal of the chip. The output terminal of the chip is connected to a load resistor on the substrate, and the potential difference at a terminal of this load resistor is amplified by an amplification circuit mounted on the substrate.

[0008] Thus, such conventional image sensors and image sensor chips mounted thereon operate on the principle that the output microcurrent from the image sensor chips flows through the load on the substrate, and the potential at the ends of this load is amplified by an amplification circuit.

[0009] A first drawback, therefore, is that the analog data signals outputted from such image sensor chips are microsignals in the form of a high-impedance output, which, basically, facilitates noise pickup and thus impairs the read performance of the image sensor. In particular, clock pulse signals of several hundred kilohertz for use in data shifting are inputted to the substrate 12 on which the image sensor chips 13 are mounted, and these clock pulse signals are thus ultimately superposed as alternating-current components on the analog data signals (as shown in Fig. 12), adversely affecting the output characteristics.

[0010] Methods commonly undertaken in order to minimize the effect of such noise involve surrounding the analog data wiring on the substrate with grounded wiring, and placing the clock signal wiring on the back side of the substrate in a position removed as far as possible from the sensor chips.

[0011] The result is that products provided with wiring patterns on both the front and back surfaces can solely be used for the substrate 12 (as is also shown in Fig. 11). This complicates the procedures involved in fabricating such products and in mounting components on them, involves forming irregularities for the components on the back surface of the substrate 12, detracts from the aesthetic appeal of the image sensor, requires more space in the width direction for installing such an image sensor, and makes it more difficult to design compact equipment containing such image sensors.

[0012] Another drawback is that the ICs, capacitors, and resistors constituting the amplification circuit; the varistors for adjusting the gain of the amplification circuit; and a plurality of other electronic components must be mounted on the substrate separately from the image sensor chips, complicating the steps involved in the manufacture of the image sensor substrate. Specifically, the various electronic components themselves are expensive, equipment is needed for mounting these electronic components on the substrate, and the varistors must be individually adjusted while the output of the amplification circuit is measured in order to adjust the gain of the amplification circuit in accordance with the specification requirements of the customer.

DISCLOSURE OF THE INVENTION

[0013] In view of the above, it is an object of the present invention to provide an image sensor chip for use in constructing a contact-type image sensor such that the substrate on which these components are mounted can be fabricated very easily, and to provide a smaller and thinner image sensor in which the substrate does not require noise prevention and in which a substrate wired on only one side can be used.

According to a first aspect of the present invention, there

is provided an image sensor chip integrally comprising: a number of photoelectric conversion elements; analog switches connected in series to the respective photoelectric conversion elements; a switch circuit for sequentially switching on said analog switches in accordance with clock signals; an output load commonly connected in series to a respective set of each photoelectric conversion element and a corresponding analog switch; and an amplification circuit for amplifying a potential of said output load on the side of the photoelectric conversion elements; characterized in that said output load comprises a load resistor and a load capacitor connected in parallel to each other.

[0014] According to a preferred arrangement, the image sensor chip comprises a power terminal, a ground terminal, a clock signal input terminal, an analog signal output terminal, photoelectric conversion elements arranged in a row at regular intervals and connected at one end to the power terminal, analog switches connected to the respective output terminals of the photoelectric conversion elements, a switch circuit for sequentially switching on the analog switches in accordance with clock signals, and output load components jointly interposed between the ground terminal and the output terminals of the analog switches, wherein the chip is configured such that the output of the amplification circuit is outputted to the analog signal output terminal.

[0015] In the preferred embodiment, a gain-adjusting resistor of the amplification circuit is also fabricated in integral form, and the gain-adjusting resistor comprises a plurality of resistors connected in series and cuttable bypass wirings provided to all or some of the plurality of resistors.

[0016] Yet another feature of the preferred embodiment is that the amplification circuit is an operational amplifier; that the gain-adjusting resistor comprises a resistor group interposed between the inverting input and the output of the operational amplifier, and a resistor group interposed between the ground and the inverting input of the operational amplifier; and that each resistor group comprises a plurality of resistors connected in series and cuttable bypass wirings provided to all or some of these resistors.

[0017] Thus, the image sensor chip pertaining to the subject invention is fabricated by integrating output load components for photoelectric conversion elements, and an amplification circuit for amplifying a terminal potential of these output load components into a single chip in addition to the basic structure of the image sensor chip comprising a prescribed number of photoelectric conversion elements serving as photoreceptors, analog switches connected in series to the corresponding photoelectric conversion elements, a switch circuit for sequentially switching on the analog switches in accordance with clock signals, and the like. In a preferred embodiment, a resistor for adjusting the gain of the amplification circuit is also integrated into the chip.

[0018] In such an image sensor chip, the microcurrent signals outputted as image read signals from the photoelectric conversion elements are outputted (without being allowed to escape from the sensor chips) outside as analog voltage signals obtained by amplifying with an amplification circuit the potential of the output load components on the side of the photoelectric conversion elements. It is therefore possible to markedly reduce or completely prevent the conventionally observed undesirable deterioration in the image read performance due to noise induced by clock signals. As a result, there is no need to provide the substrate for mounting such image sensor chips with amplification circuits or related components, or to form special wiring patterns for noise reduction, making it possible to position the image sensor chips on one side of the substrate and to provide a power source in order to complete the image sensors.

[0019] When this is done, a substrate obtained by mounting image sensor chips and light-emitting elements (light sources) on one side in such a manner is attached to the bottom surface of a case, a glass cover is placed on the top surface of the case, and an image sensor is configured such that reflected light from a document on the glass cover illuminated by the light-emitting elements is converged on the photoelectric conversion elements of the image sensor chips, in which case the back surface of the substrate facing the reverse side of this image sensor is free from the irregularities caused by the presence of electronic components, resulting in an improved outward appearance. The thickness dimensions of the image sensor itself can thereby be further reduced, and a narrower space is sufficient for accommodating the image sensor in an instrument designed for use with such image sensors. Collectively, these factors can contribute substantially to reducing the size of an equipment assembly containing such image sensors.

[0020] When using a resistance load as the output load of the amplification circuit, the desired analog output waveform can be obtained by selecting an appropriate resistance for the load. Specifically, the analog output waveform should resemble a rectangular wave, that is, should have a horizontal or roughly horizontal top portion, to achieve accurate sensing of the output level, and the desirable output waveform can be obtained by appropriately selecting the resistance value of the resistance load.

[0021] When a load capacitor is used as the output load of the amplification circuit, correct dark level readings can be obtained because setting the capacitance of this capacitor to an appropriate level allows the electric charge accumulated in the photoelectric conversion elements in accordance with the amount of received light to flow as a burst of current through this load capacitor when the photoelectric conversion elements are selected for reading. Specifically, it is possible to reduce the amount of charge remaining in the photoelectric conversion elements during the outputting of output signals and to suppress the undesirable conditions in which, during the dark-level read cycle in which the photoelectric con-

version elements do not receive any light, an output resembling that created by the reception of weak light is generated by the charge remaining in the photoelectric conversion elements from the preceding bright-level read cycle. This means that when a document containing fine horizontal ruled lines on a white background is read, such horizontal ruled lines can be read with sufficient accuracy.

[0022] By the invention, the combined benefits of using a resistance load and a load capacitor are obtained when these resistance load and load capacitor are connected in parallel with each other as the output load components of the amplification circuit.

[0023] In an image sensor chip pertaining to a preferred embodiment, the gain-adjusting resistor for the amplification circuit integrated into the chip comprises, in particular, a plurality of resistors connected in series and cuttable bypass wirings provided to all or some of the plurality of resistors. When an operational amplifier is used as the amplification circuit, this resistor structure can be adopted for the resistors interposed between the ground and the inverting input of the amplifier and/or for the resistors interposed between the inverting input and the output terminal of the operational amplifier. For example, when four resistors of 20 kΩ, 40 kΩ, 80 kΩ, and 160 kΩ, respectively, are connected in series and respective bypass wirings are provided to these resistors to complete a resistorgroup, the resistance of the entire resistor group can be selected at a level ranging from 0 Ω to 300 kΩ in 20-kΩ increments by selecting, out of the four resistors, the bypass wiring that is to be cut. The cutting of the bypass wirings can be accomplished very easily by laser cutting at the wafer stage, as described below.

[0024] In the image sensor chip pertaining to such an embodiment, even the gain of the built-in amplification circuit is preadjusted, making it possible to dispense with the inconvenient procedures performed in the past, such as mounting varistors on the substrate, monitoring the analog output of each substrate under prescribed conditions, and adjusting the varistors to adjust the gain of the amplification circuit. This contributes greatly to simplifying the manufacture of substrates for image sensors.

[0025] According to a second aspect of the present invention, a method for manufacturing an image sensor chip pertaining to the first aspect is provided as claimed in Claim 5. This manufacturing method is characterized in that the image sensor chip provided by the first aspect is used as a constituent unit, a wafer obtained by integrating a plurality of such units is fabricated, the gain of the amplification circuit is adjusted by cutting with a laser the bypass wirings of resistors selected from a plurality of resistors constituting the gain-adjusting resistor of each chip unit at the wafer stage, and the wafer is divided into image sensor chips by dicing.

[0026] Forming a mask on the wafer allows several hundred image sensor chips having the circuit characteristics described with reference to the first aspect to be fabricated as a single lot. These characteristics sometimes vary from wafer to wafer due to minute errors in maskwork conditions. The analog output produced by each chip area under prescribed illumination conditions is checked at the wafer stage. In the meantime, the voltage conditions for analog output are established in accordance with customer requirements and the like. The gain of the amplification circuit needed to obtain the output voltage conditions is set on the basis of the analog output thus checked. Once the gain is thus set, the adjusted value of the gain-adjusting resistor is determined, a decision is made as to which of the plurality of resistors making up the resistor group is to be left in order to achieve such an adjusted value, and the bypass wirings corresponding to these resistors are cut. The bypass wirings can be cut conveniently and rapidly by, for example, scanning an excimer laser beam across the wafer while switching the beam on and off in a controlled manner. An amplification circuit or an image sensor chip having a properly adjusted amplification circuit gain can thus be fabricated.

[0027] When an image sensor is configured by mounting a plurality of such image sensor chips, the gain of the amplification circuit is adjusted for each of the image sensor chips and the output level is smoothed, making it possible to adequately prevent the read performance from being adversely affected by the output variations in the main scanning direction due to differences in the output level among the chips.

[0028] Other features and advantages of the subject invention will become more apparent from the detailed description given below with reference to drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029]

Fig. 1 is a fragmentary perspective view of an embodiment of an image sensor;

Fig. 2 is a cross-sectional view of the assembled integrated circuit depicted in Fig. 1;

Fig. 3 is an expanded plan view of an embodiment of an image sensor chip;

Fig. 4 is a fragmentary expanded plan view of a substrate for the image sensor;

Fig. 5 is an equivalent circuit diagram of a first embodiment of the image sensor chip pertaining to the subject invention;

Fig. 6 is a dynamic chart illustrating the operation of an image sensor chip having the circuit structure shown in Fig. 5;

Fig. 7 is a graph illustrating the operation of an image sensor chip having the circuit structure shown in Fig. 5;

Fig. 8 is an output waveform diagram illustrating the operation of an image sensor chip having the circuit structure shown in Fig. 5;

Fig. 9 is an equivalent circuit diagram of an arrange-

ment of an image sensor chip;

Fig. 10 is an equivalent circuit diagram of another arrangement of an image sensor chip;

Fig. 11 is a cross-sectional view of an image sensor pertaining to a conventional example; and

Fig. 12 is a dynamic chart illustrating the operation of the conventional example.

BEST MODE FOR CARRYING OUT THE INVENTION

[0030] Preferred embodiments of the present invention will now be described in detail with reference to drawings.

[0031] The overall structure of an image sensor 20 will first be described, primarily with reference to Figs. 1 and 2.

[0032] As shown in Figs. 1 and 2, the image sensor 20 is configured such that a substrate 23 carrying a plurality of LEDs 21 (illumination light sources) and a plurality of image sensor chips 22 (image read elements) is disposed on the bottom of a case 24, a transparent glass cover 25 is placed on the top surface of the case 24, and a light-guide plate 26 for efficiently illuminating the document surface D on the glass cover 25 with the light from the LEDs 21 (light sources) is disposed inside the case 24 together with a rod lens array 27 for converging reflected light from the document surface D on the image sensor chips 22 as a non-inverted image of the same size. For example, 1728 light-receiving elements must be arranged in a row at regular intervals to allow an A4 document to be read at a main scanning density of 8 pixels per millimeter. Such light-receiving elements can be realized by arranging in a row a plurality of image sensor chips 22 each having a plurality of light-receiving elements 28. When, for example, image sensor chips 22 provided with 96 light-receiving elements are used, 18 image sensor chips 22 are mounted in proximity to each other on the substrate 23 in the longitudinal direction such that all the light-receiving elements have a constant pitch.

[0033] Fig. 3 schematically shows a planar arrangement of each image sensor chip 22. The image sensor chip 22 is obtained by integrating prescribed elements or terminals with a silicon wafer by forming a mask thereon, and dividing the wafer into individual chips by dicing. The light-receiving elements 28 are arranged equidistantly at a pitch of 8 elements per millimeter along one edge of the top surface, and serial-in (SI), clock (CLK), logic power supply (VDD), ground (GND), analog-out (AO), serial-out (SO) and other terminal pads are arranged along the other edge of the top surface. These terminal pads are connected by wire bonding to the prescribed wiring patterns on the substrate 23, on which the image sensor chip 22 is mounted.

[0034] Fig. 5 depicts an equivalent circuit structure for each image sensor chip 22. A plurality of (for example, 96) photoelectric conversion elements (light-receiving elements) such as phototransistors 28 are jointly connected at their emitters to a logic power supply (VDD). Analog switches 29 are connected in series to the collectors of the corresponding phototransistors 28. These analog switches 29 are sequentially switched on by a switch circuit 30 actuated by clock signals when this image sensor chip 22 has been selected. A shift register is suitable for use as such a switch circuit. Serial-in (SI) signals and clock (CLK) signals are therefore inputted to this shift register 30.

[0035] A resistance load 31 of prescribed resistance is jointly connected in series between the ground (GND) terminals and the output terminals of the analog switches 29. A load capacitor 40 is interposed in parallel to the resistance load 31. In this embodiment, the resistance load 31 and load capacitor 40 cooperate to constitute an output load for the phototransistors 28. Specifically, the terminal sections of these resistance load 31 and load capacitor 40 on the side of the photoelectric conversion elements are connected to the noninverting input of an operational amplifier 32 (amplification circuit). A gain-adjusting resistor R comprising a resistor group Ra and a resistor group Rb is connected to the inverting input of the operational amplifier 32 such that the group Ra is interposed between the inverting input and the ground, and the group Rb is interposed between the inverting input and the output terminal of the operational amplifier 32. As is known, the gain G of the operational amplifier 32 is expressed as $G = 1 + (Rb/Ra)$.

[0036] In more specific terms, the gain-adjusting resistor R is configured in the following manner. Specifically, the resistor group Ra is configured such that four adjusting resistors Ra_1, Ra_2, Ra_3 and Ra_4 of 2 kΩ, 4 kΩ, 8 kΩ, and 16 kΩ , respectively, are connected in series to a 20-kΩ reference resistor Ra_0, and each adjusting resistor is provided with a respective bypass wiring 50 in a parallel arrangement. In addition, the resistor group Rb is configured such that four adjusting resistors Rb_1, Rb_2, Rb_3 and Rb_4 of 20 kΩ, 40 kΩ, 80 kΩ , and 160 kΩ, respectively, are connected in series to a 200-kΩ reference resistor Rb_0, and each adjusting resistor is provided with a respective bypass wiring 50 in a parallel arrangement. The bypass wirings 50 are fine aluminum wirings formed on a silicon wafer. The resistor group Ra is such that only the reference resistor Ra0 is active when all the bypass wirings 50 are connected, and the total resistance of this resistor group Ra is therefore 20 kΩ. Similarly, the total resistance of the resistor group Rb is 200 kΩ when all the bypass wirings 50 are connected. The gain G of the operational amplifier 32 in this state is therefore $G = 1 + (200/20) = 11$.

[0037] The total resistance of the resistor group Rb should be increased in order to raise the gain G. The total resistance of the resistor group Ra should be increased in order to lower the gain G. To increase the total resistance of the resistor group Ra or Rb, a decision is made as to which of the serially connected adjusting resistors Ra_1, Ra_2, Ra_3, Ra_4, Rb_1, Rb_2, Rb_3, and Rb_4 constituting these groups should be activated, and the bypass wiring 50 of the selected resistor is cut. In the embodiment il-

lustrated, the resistor group Ra comprises, for example, four adjusting resistors Ra_1, Ra_2, Ra_3, and Ra_4 of 2 kΩ , 2^2 kΩ, 2^3 kΩ, and 2^4 kΩ, making it possible to select a resistance ranging from 20 kΩ to 50 kΩ in 2-kΩ increments by selecting any of the adjusting resistors. Similarly, the resistor group Rb makes it possible to select a resistance ranging from 200 kΩ to 500 kΩ in 20-kΩ increments. Gain is adjusted using a procedure in which analog output is checked for each chip area under prescribed illumination conditions before the wafer has been divided into individual chips by dicing, the gain needed for the amplifier 32 to yield the analog output level required by the customer or the like is calculated for the analog output available at this stage, and the bypass wiring 50 of the selected adjusting resistor is cut by laser cutting in order to establish the desired total resistance of the resistor group Ra and resistor group Rb. Such laser cutting may, for example, be readily accomplished by scanning an excimer laser beam across the wafer while switching the beam on and off in a controlled manner.

[0038] Meanwhile, an analog switch 35 is interposed in parallel with an output load comprising the resistance load 31 and load capacitor 40, and this analog switch 35 is switched on and off by signals from a chip selection circuit 36. In addition, an analog switch 37 is interposed between the output terminal of the operational amplifier 32 and an analog-out (AO) terminal, and this analog switch 37 is switched on and off by signals from the chip selection circuit 36. One end of the shift register 30 is connected to a serial-out (SO) terminal and to the chip selection circuit 36, and serial-in (SI) signals and clock (CLK) signals are inputted to the chip selection circuit 36.

[0039] The chip selection circuit 36 keeps the analog switch 37 on from the moment a pulse signal is inputted to the serial-in (SI) until the moment a pulse signal is outputted from the output of the shift register 30, and keeps the analog switch 35 off during each fall period of the clock pulse.

[0040] The image sensor chip 22 thus formed is bonded to the substrate 23 in the following manner. Specifically, as shown in Fig. 4, the logic power (VDD) terminal of each image sensor chip 22 is jointly connected by wire bonding to a logic power wiring pattern 38_{VDD} on the substrate 23, the ground (GND) terminal to the a ground wiring pattern 38_{GND} on the substrate, the clock signal (CLK) terminal to a clock signal wiring pattern 38_{CLK} on the substrate, and the analog-out (AO) terminal to an analog-out wiring pattern 38_{AO} on the substrate. These terminals are also connected in cascade between the serial-out (SO) terminals and the serial-in (SI) terminals of adjacent image sensor chips via a wiring pattern 38_S on the substrate.

[0041] The substrate 23 is also provided with wiring patterns 38_{LED} for installing a plurality of LED chips 21 as illumination light sources, and these wiring patterns are used to arrange the plurality of LED chips 21 at regular intervals.

[0042] The substrate 23 may, for example, be obtained by forming the wiring patterns on a substrate material composed of an alumina ceramic. The wiring patterns can, for example, be appropriately formed by screen printing using gold paste. Each wiring pattern is concentrated in a predetermined position on the substrate 23 and is prepared for outside connection by being provided with appropriate connectors or the like.

[0043] The operation of the image sensor 20 will subsequently be described, with emphasis on the operation of the image sensor chips 22.

[0044] The contrast image of a document D on a read line L marked on the glass cover 25 is converged on 1728 light-receiving elements 28. Specifically, light whose intensity corresponds to the contrast image on the read line L strikes the 1728 light-receiving elements arranged in a row.

[0045] As indicated by the timing chart in Fig. 6, the chip selection circuit 36 switches on the analog switch 37 at the analog-out (AO) terminal when a pulse signal has been inputted to this chip from the serial-in (SI) terminal, and this state is maintained until a pulse signal is outputted (SO) from the shift register 30. Specifically, image read data are serially outputted from the analog-out (AO) terminal while the analog switch 37 is on.

[0046] Pulse signals inputted at one end of the shift register 30 are sequentially shifted by clock pulses, and this is accompanied by the sequential energizing of the analog switches 29 connected in series to the phototransistors 28. Phototransistors 28 for outputting read signals are thus sequentially selected. Meanwhile, the chip selection circuit 36 switches on the analog switch 35 during each rise cycle of the clock pulses, and switches off the analog switch 35 during the fall cycles of the clock pulses, with the result that, as indicated by the timing chart in Fig. 6, an electric charge proportional to the intensity of light received by the sequentially selected phototransistors 28 flows through the output load composed of the resistance load 31 and load capacitor 40 during the fall cycles of the clock pulses and the prescribed read cycles of the phototransistors. The corresponding microcurrent signals are sensed as the potential of the output loads 31 and 40 on the phototransistor side, this potential is converted to a voltage waveform and amplified in accordance with a prescribed gain by the operational amplifier 32, and the analog data converted to such a voltage waveform are outputted from the analog-out (AO) terminal. The pulse signals outputted by the shift register 30 are transmitted from the serial-out (SO) terminal via the pattern on the substrate to the adjacent chip, and the signals sensed by the phototransistors on the adjacent chip are read as serial data in the same manner as above.

[0047] Fig. 6 also depicts the output waveform of the image sensor chip 22 pertaining to the above-described embodiment for a variable intensity of illuminating light. It is evident from the drawing that at the dark level (when there is no illumination with light), clock pulses are not superposed as alternating-current components on the output waveform the way they are superposed in the con-

ventional examples depicted in Figs. 11 and 12. The reason for this is that because the image sensor chip 22 is such that the amplifier circuit 32 and the output loads 31 and 40 are integrated into the image sensor chip 22, a high-impedance output that tends to pick up noise is not brought out to the substrate the way it is brought out in the conventional examples. Consequently, the output waveform exactly matches the intensity of light received by each phototransistor, and, as a result, the image read performance of this image sensor chip is dramatically improved.

[0048] It should be noted that the embodiment described above involves an arrangement in which a resistance load 31 and a load capacitor 40 cooperate as loads for the phototransistors 28 (light-receiving elements). As described above, the phototransistors 28 output an electric current proportional to the amount of light received during the read cycle in the period during which the analog switch 35 is on. Because of the special properties of the capacitor operating as an output load, the charges that have been retained by the phototransistors 28 immediately flow to this capacitor at this time, making it possible to reduce the amount of charge remaining, in particular, on the bases of the phototransistors 28 when the off-cycle of the analog switch 35 has ended.

[0049] Fig. 7 depicts, in summary form, experimental results obtained when various levels are selected as output loads for the phototransistors 28 to obtain an analog output by separating a document D into "white" section and "black" sections and reading the black sections after reading the white sections. Specifically, the outputs of "white" and "black" readouts are quantitatively shown in Fig. 7, where Fig. 7a pertains to a case in which a resistance of 47 kΩ is established as the output load, Fig. 7b pertains to a case in which a resistance of 100 kΩ is established as the output load, Fig. 7c pertains to a case in which a capacitor having a capacitance of 33 pF is provided as the output load, Fig. 7d pertains to a case in which a capacitor having a capacitance of 100 pF is provided as the output load, and Fig. 7e pertains to a case in which a capacitor having a capacitance of 200 pF is provided as the output load. The corresponding power voltage is 5 V, the luminous energy of the illumination light source 0.796 μW, the read cycle 5 ms, and the gain of the operational amplifier 10. It can be seen in the drawings that a certain level of output exists even for a black readout, which, ideally, is supposed to produce zero output level. This is the result of a process in which the charge accumulated in the phototransistors during a white readout, and particularly the charge remaining in the bases, is outputted during a black readout. Specifically, the analog output of a black readout corresponds to the amount of charge remaining during the immediately preceding white readout.

[0050] It is evident in Fig. 7 that when a resistor is provided as an output load, the ratio of remaining charge to white readout output exceeds 26%, but when a capacitor is provided as the output load, the ratio can reduced to as low as about 16% by establishing an appropriate capacitance. The accuracy with which fine horizontal ruled lines are read improves with a reduction in the ratio of remaining charge, allowing the image sensor chip pertaining to this embodiment to deliver an improved performance in terms of reading horizontal ruled lines as well.

[0051] As is also shown in Fig. 8, the bright output waveform outputted from the analog-out (AO) terminal can be varied by including the resistance load 31 into the output load in such a manner and selecting appropriate resistance for this resistance load. Specifically, a comparatively large resistance load results in an output waveform that rises on the right and has a sawtooth shape (as shown in Fig. 8a), but the trailing end of the top portion of the waveform tends to decrease with a reduction in the resistance load. The bright output waveform should be as close to a rectangular wave as possible and have a horizontal or roughly horizontal top portion (as shown in Fig. 8b) to achieve optimum processing of image read data. Such a waveform can be obtained by properly selecting the resistance of the resistance load.

[0052] Thus, as described above, the subject invention is such that the output from the image sensor chip represents a voltage waveform that is free from noise and is already amplified to the desired gain level, dispensing with the need to adopt noise-suppressing actions for the substrate or to mount amplifier circuits, adjusting varistors, or other electronic components on the substrate. It is thus possible to use products obtained by forming wiring patterns on one side. Such substrates can be fabricated by performing the simple step of forming wiring patterns on alumina ceramic substrates by means of screen printing. Such fabrication can be further facilitated because the wiring patterns may be formed on only one side. In addition, the output level of each image sensor chip can be adjusted individually, making it possible to prevent read characteristics from being adversely affected by variations in the read level of each chip at different locations in the main scanning direction.

[0053] Thus, as shown in Fig. 1 or 2, the proposed image sensor chip 22 or image sensor 20, which is obtained by adopting a substrate 23 on which the image sensor chips and LED chips (light sources) are mounted on one side in the manner described above, is devoid of the irregularities created by mounting outside components on the back side, has an excellent appearance, is very easy to handle, and is made smaller in the thickness direction.

[0054] It is apparent that the scope of this invention is not limited to the embodiment described above. The analog switches connected in series to the photoelectric conversion elements may also be connected to the terminals of the photoelectric conversion elements on the power supply side. In addition, the load capacitor 40 and the resistance load 31, other than being jointly connected to the photoelectric conversion elements on the ground side (as in the embodiment), may also be jointly connect-

ed on the power supply side, and the potential difference between their terminals may be amplified by an amplifier circuit.

[0055] A resistance load 31 and a load capacitor 40 connected in parallel were used as the output load components of the phototransistors in the embodiment of the invention described above. In alternative arrangements outside the invention a load consisting solely of the resistance load 31 (as shown in Fig. 9) or load capacitor 40 (as shown in Fig. 10) are used.

INDUSTRIAL APPLICABILITY

[0056] The image sensor chip of the claimed invention is suitable for use as an element constituting the image sensor of a fax machine, image scanner, or other image reader.

Claims

1. An image sensor chip integrally comprising: a number of photoelectric conversion elements (28); analog switches (29) connected in series to the respective photoelectric conversion elements (28) ; a switch circuit (30) for sequentially switching on said analog switches in accordance with clock signals; an output load (31, 40) commonly connected in series to a respective set of each photoelectric conversion element (28) and a corresponding analog switch (29) ; and an amplification circuit (32) for amplifying a potential of said output load (31, 40) on the side of the photoelectric conversion elements (28);
characterized in that said output load comprises a load resistor (31) and a load capacitor (40) connected in parallel to each other.

2. The image sensor chip according to Claim 1, further integrally comprising a power terminal (VDD) , agroundterminal (GND) , a clock signal input terminal (CLK) , and an analog signal output terminal (AO) , said photoelectric conversion elements (28) being arranged in a row at regular intervals and connected at one end to said power terminal (VDD), said analog switches (29) being connected to respective output terminals of said photoelectric conversion elements (28) , said output load (31, 40) being jointly interposed between said ground terminal (GND) and an output terminal of each analog switch (29); an output of saidamplificationcircuit (32) being supplied to said analog signal output terminal (AO).

3. The image sensor chip according to Claim 1, wherein said amplificationcircuit (32) comprisesagain-adjustingresistor unit (Ra, Rb) formed integrally in the image sensor chip, said gain-adjusting resistor unit (Ra, Rb) including a plurality of resistors (Ra0~Ra4, Rb0~Rb4) connected in series and a cuttable bypass wiring (50) provided for at least one of said plurality of resistors (Ra0~Ra4, Rb0~Rb4).

4. The image sensor chip according to Claim 3, wherein said amplificationcircuit comprises an operational amplifier (32) ; said gain-adjusting resistor including a resistor group (Rb) interposed between an inverting input of said operational amplifier and an output of the same operational amplifier (32), and another resistor group (Ra) interposed between said ground terminal (GND) and the inverting input of said operational amplifier (32); each resistor group (Ra, Rb) including a plurality of resistors (Rao~Ra4, Rb0~Rb4) connected in series and a cuttable bypass wiring (50) provided for at least one of these resistors.

5. A method for manufacturing image sensor chips (22), each of which has the structure as defined in claim 4, said method comprising the steps of:

   preparing a wafer corresponding to a plurality of such image sensor chips (22);
   performing gain adjustment of said amplification circuit (32) by laser-cutting the bypass wiring (50) for a selected one or ones of the resistors (Rao~Ra4, Rb0~Rb4); and
   dicing said wafer for division into said plurality of individual image sensor chips (22).

6. An image sensor substrate comprising, as mounted on a surface thereof, a plurality of image sensor chips (22) together with at least one light-emitting element (21), each of the image sensor chips (22) having the structure as defined in any one of Claims 1 to 4.

7. An image sensor comprising: a case (24) having a bottom provided with an image sensor substrate (23) as defined in Claim 6, a glass cover (25) placed on top of the case (24), reflected light from a document (D) on the glass cover (25) illuminated by the light-emitting elements (21) being converged on the photoelectric conversion elements (28) of said image sensor chips (22).

Patentansprüche

1. Bildsensorchip, der integriert enthält: eine Anzahl fotoelektrischer Umwandlungselemente (28); analoge Schalter (29), die mit den entsprechenden fotoelektrischen Umwandlungselementen (28) in Reihe geschaltet sind; einen Schalterstromkreis (30) zum aufeinander folgenden Anschalten der analogen Schalter im Einklang mit Taktsignalen; eine Ausgangslast (31, 40), die zusammen mit einem entsprechenden Satz aus jedem fotoelektrischen Umwandlungselement (28) und einem entsprechenden analogen

Schalter (29) in Reihe geschaltet ist; und einen Verstärkungsstromkreis (32) zum Verstärken eines Potentials der Ausgangslast (31, 40) auf der Seite der fotoelektrischen Umwandlungselemente (28);
dadurch gekennzeichnet, dass die Ausgangslast einen Lastwiderstand (31) und einen Lastkondensator (40) umfasst, die miteinander parallel verbunden sind.

2. Bildsensorchip nach Anspruch 1, der ferner integriert umfasst: einen Energieversorgungsanschluss (VDD), einen Masseanschluss (GND), einen Eingangsanschluss (CLK) für ein Taktsignal und einen Ausgangsanschluss (AO) für ein analoges Signal, wobei die fotoelektrischen Umwandlungselemente (28) in regelmäßigen Abständen in einer Reihe angeordnet und an einem Ende mit dem Energieversorgungsanschluss (VDD) verbunden sind, wobei die analogen Schalter (29) mit entsprechenden Ausgangsanschlüssen der fotoelektrischen Umwandlungselemente (28) verbunden sind, wobei die Ausgangslast (31, 40) gemeinsam zwischen dem Masseanschluss (GND) und einem Ausgangsanschluss jedes analogen Schalters (29) zwischengeschaltet ist; wobei ein Ausgang des Verstärkungsstromkreises (32) zum Ausgangsanschluss (AO) für ein analoges Signal geliefert wird.

3. Bildsensorchip nach Anspruch 1, wobei der Verstärkungsstromkreis (32) eine verstärkungseinstellende Widerstandseinheit (Ra, Rb) aufweist, die in dem Bildsensorchip integriert ausgebildet ist, wobei die verstärkungseinstellende Widerstandseinheit (Ra, Rb) mehrere Widerstände (Ra0 - Ra4, Rb0 - Rb4), die in Reihe geschaltet sind, und eine unterbrechbare Überbrückungsleitung (50) aufweist, die für wenigstens einen der mehreren Widerstände (Ra - Ra4, Rb0 - Rb4) bereitgestellt ist.

4. Bildsensorchip nach Anspruch 3, wobei der Verstärkungsstromkreis einen Operationsverstärker (32) umfasst; wobei der verstärkungseinstellende Widerstand eine Widerstandsgruppe (Rb), die zwischen einem invertierenden Eingang des Operationsverstärkers und einem Ausgang desselben Operationsverstärkers (32) geschaltet ist, sowie eine weitere Widerstandsgruppe (Ra) aufweist, die zwischen dem Masseanschluss (GND) und dem invertierenden Eingang des Operationsverstärkers (32) geschaltet ist; wobei jede Widerstandsgruppe (Ra, Rb) mehrere Widerstände (Ra0 - Ra4, Rb0 - Rb4), die in Reihe geschaltet sind, und eine unterbrechbare Überbrückungsleitung (50) aufweist, die für wenigstens einen dieser Widerstände bereitgestellt ist.

5. Verfahren zum Herstellen von Bildsensorchips (22), von denen jeder die in Anspruch 4 definierte Struktur aufweist, wobei das Verfahren die Schritte aufweist:

Herstellen eines Wafers, der mehreren derartigen Bildsensorchips (22) entspricht;
Durchführen einer Verstärkungseinstellung des Verstärkungsstromkreises (32) durch Unterbrechen der Überbrückungsleitung (50) für einen ausgewählten oder für ausgewählte der Widerstände (Ra0 - Ra4, Rb0 - Rb4) mittels eines Lasers; und
Vereinzeln des Wafers für eine Unterteilung in die mehreren individuellen Bildsensorchips (22).

6. Bildsensorsubstrat, das als auf eine Oberfläche davon montiert umfasst:

mehrere Bildsensorchips (22) zusammen mit wenigstens einem lichtemmitierenden Element (21), wobei jeder der Bildsensorchips (22) die in einem der Ansprüche 1 bis 4 definierte Struktur aufweist.

7. Bildsensor, umfassend: ein Gehäuse (24) mit einem Boden, der mit einem Bildsensorsubstrat (23), wie es in Anspruch 6 definiert ist, versehen ist, einer Glasabdeckung (25), die auf das Gehäuse (24) aufgesetzt ist, wobei von einem Dokument (D) auf der Glasabdeckung (25), die von den lichtemmitierenden Elementen beleuchtet wird, reflektiertes Licht auf die fotoelektrischen Umwandlungselemente (28) des Bildsensorchips (22) konvergiert wird.

Revendications

1. Puce de détecteur d'image comprenant solidairement :

une pluralité d'éléments de conversion photoélectrique (28) ; des commutateurs analogiques (29) connectés en série aux éléments de conversion photoélectrique respectifs (28) ; un circuit de commutation (30) pour commuter séquentiellement en conduction les dits commutateurs analogiques conformément à des signaux d'horloge ; une charge de sortie (31, 40) connectée en commun en série à un groupe respectif de chaque élément de conversion photoélectrique (28) et d'un commutateur analogique correspondant (29) ; et un circuit d'amplification (32) pour amplifier un potentiel de la dite charge de sortie (31, 40) sur le côté des éléments de conversion photoélectrique (28) ;

caractérisé en ce que la dite charge de sortie comprend une résistance de charge (31) et un condensateur de charge (40) connectés en parallèle l'un à l'autre.

2. Puce de détecteur d'image selon la revendication 1, comprenant en outre solidairement une borne d'alimentation en énergie (VDD), une borne de terre (GND), une borne d'entrée de signal d'horloge (CLK) et une borne de sortie de signal analogique (AO), les dits éléments de conversion photoélectrique (28) étant agencés en une rangée à intervalles réguliers et connectés, à une extrémité, à la dite borne d'alimentation en énergie (VDD), les dits commutateurs analogiques (29) étant connectés à des bornes de sortie respectives des dits éléments de conversion photoélectrique (28), la dite charge de sortie (31, 40) étant interposée conjointement entre la dite borne de terre (GND) et une borne de sortie de chaque commutateur analogique (29) ; une sortie du dit circuit d'amplification (32) étant fournie à la dite borne de sortie de signal analogique (AO).

3. Puce de détecteur d'image selon la revendication 1, dans laquelle le dit circuit d'amplification (32) comprend une unité de résistances de réglage de gain (Ra, Rb) formée solidairement dans la puce de détecteur d'image, la dite unité de résistances de réglage de gain (Ra, Rb) comprenant une pluralité de résistances (Ra0-Ra4,Rb0-Rb4) connectées en série et un câblage de contournement à couper (50) prévu pour au moins une de la dite pluralité de résistances (Ra0-Ra4, Rb0-Rb4).

4. Puce de détecteur d'image selon la revendication 3, dans laquelle le dit circuit d'amplification comprend un amplificateur opérationnel (32) ; la dite résistance de réglage de gain incluant un groupe de résistances (Rb) interposé entre une entrée d'inversion du dit amplificateur opérationnel et une sortie du même amplificateur opérationnel (32), et un autre groupe de résistances (Ra) interposé entre la dite borne de terre (GND) et l'entrée d'inversion du dit amplificateur opérationnel (32) ; chaque groupe de résistances (Ra, Rb) incluant une pluralité de résistances (Ra0-Ra4, Rb0-Rb4) connectées en série, et un câblage de contournement à couper (50) prévu pour au moins une de ces résistances.

5. Procédé de fabrication de puces de détecteur d'image (22), dont chacune a la structure définie dans la revendication 4, le dit procédé comprenant les étapes de :

préparation d'une tranche correspondant à une pluralité de ces puces de détecteur d'image (22) ;
exécution d'un réglage de gain du dit circuit d'amplification (32) par coupe au laser du câblage de contournement (50) pour une ou plusieurs résistances choisies parmi les résistances (Ra0-Ra4, Rb0-Rb4) ; et
découpe de la dite tranche pour division en la dite pluralité de puces de détecteur d'image individuelles (22).

6. Substrat de détecteur d'image comprenant, montées sur une surface du dit substrat, une pluralité de puces de détecteur d'image (22) en même temps qu'au moins un élément émetteur de lumière (21), chacune des puces de détecteur d'image (22) ayant la structure définie dans une quelconque des revendications 1 à 4.

7. Détecteur d'image comprenant : un boîtier (24) ayant un fond comportant un substrat de détecteur d'image (23) comme défini dans la revendication 6, un couvercle en verre (25) placé sur le dessus du boîtier (24), la lumière réfléchie par un document (D) placé sur le couvercle en verre (25) éclairé par les éléments d'émission de lumière (21) convergeant sur les éléments de conversion photoélectrique (28) des dites puces de détecteur d'image (22).

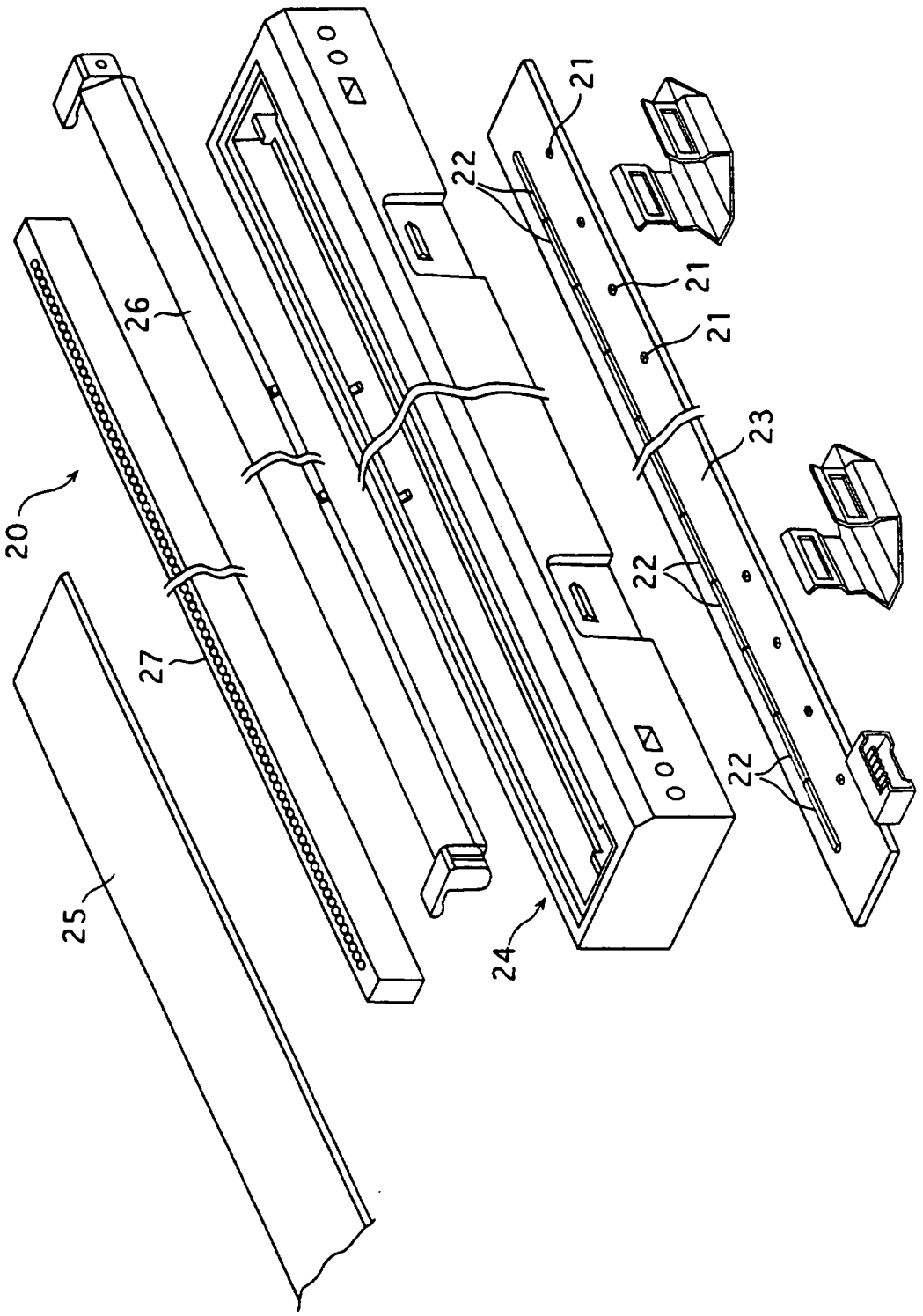


Fig.1

Fig.2

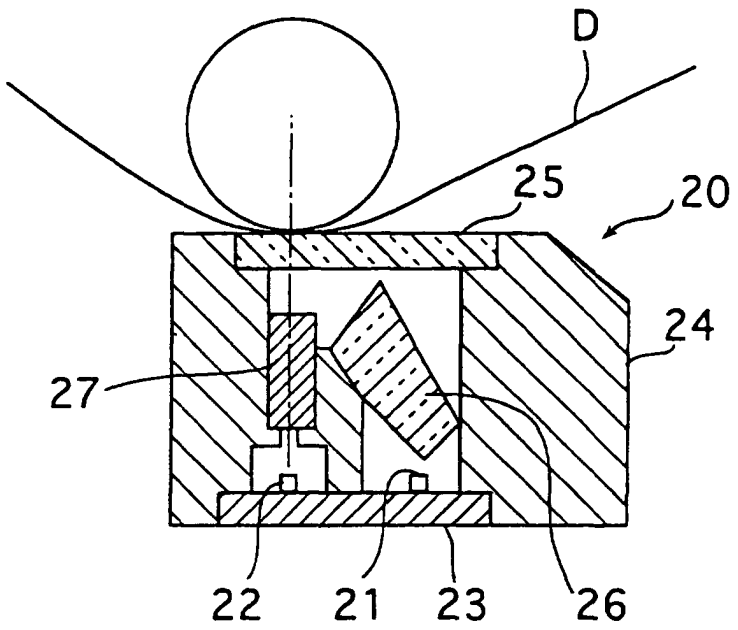


Fig.3

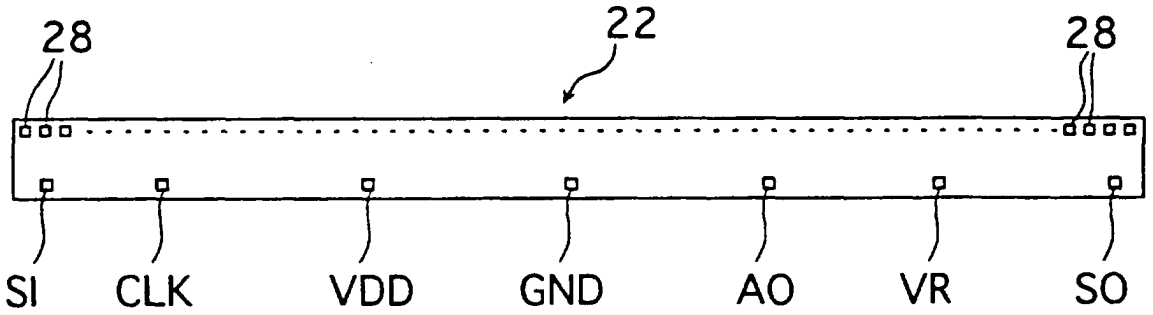


Fig.4

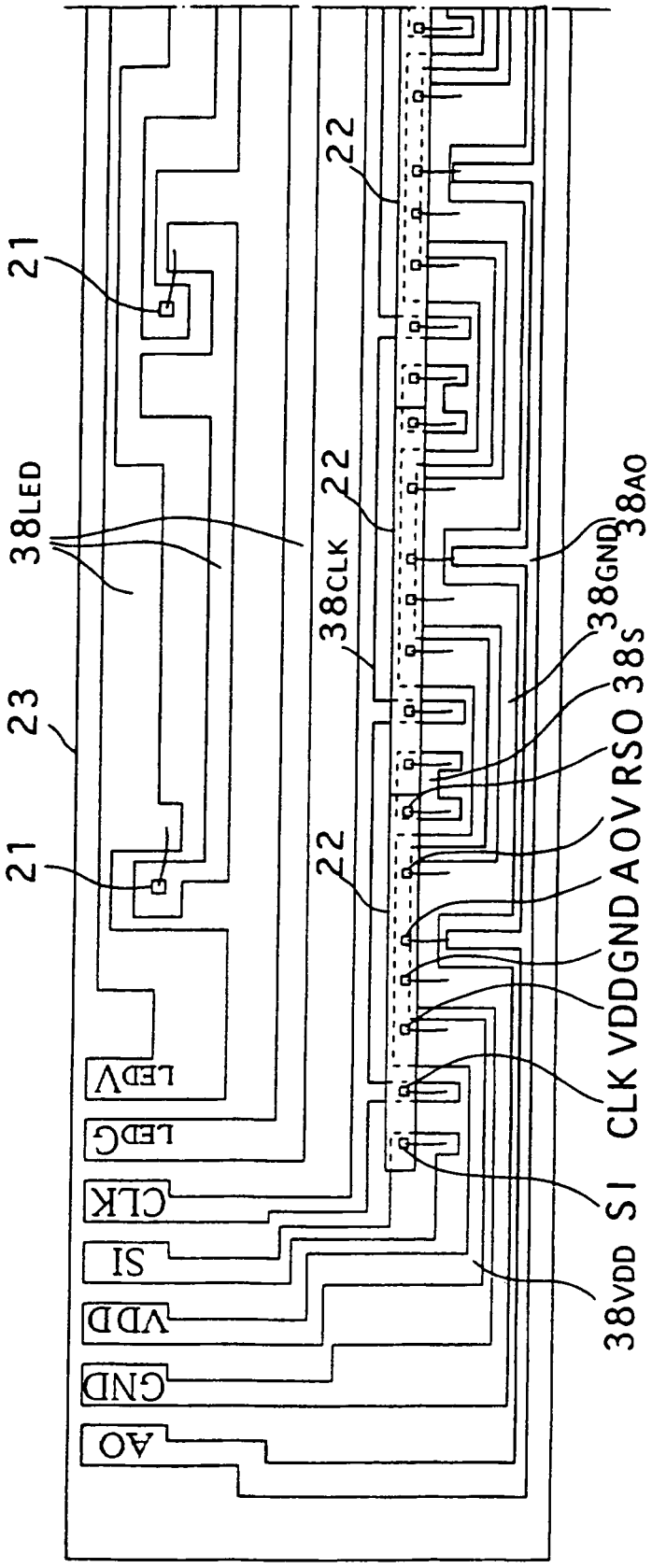

21
21
23
38LED
22
22
22
38CLK
38VDD SI CLK VDDGND AOV RSO 38S 38GND 38AO
LEDV
LEDG
CLK
SI
VDD
GND
AO

Fig.5

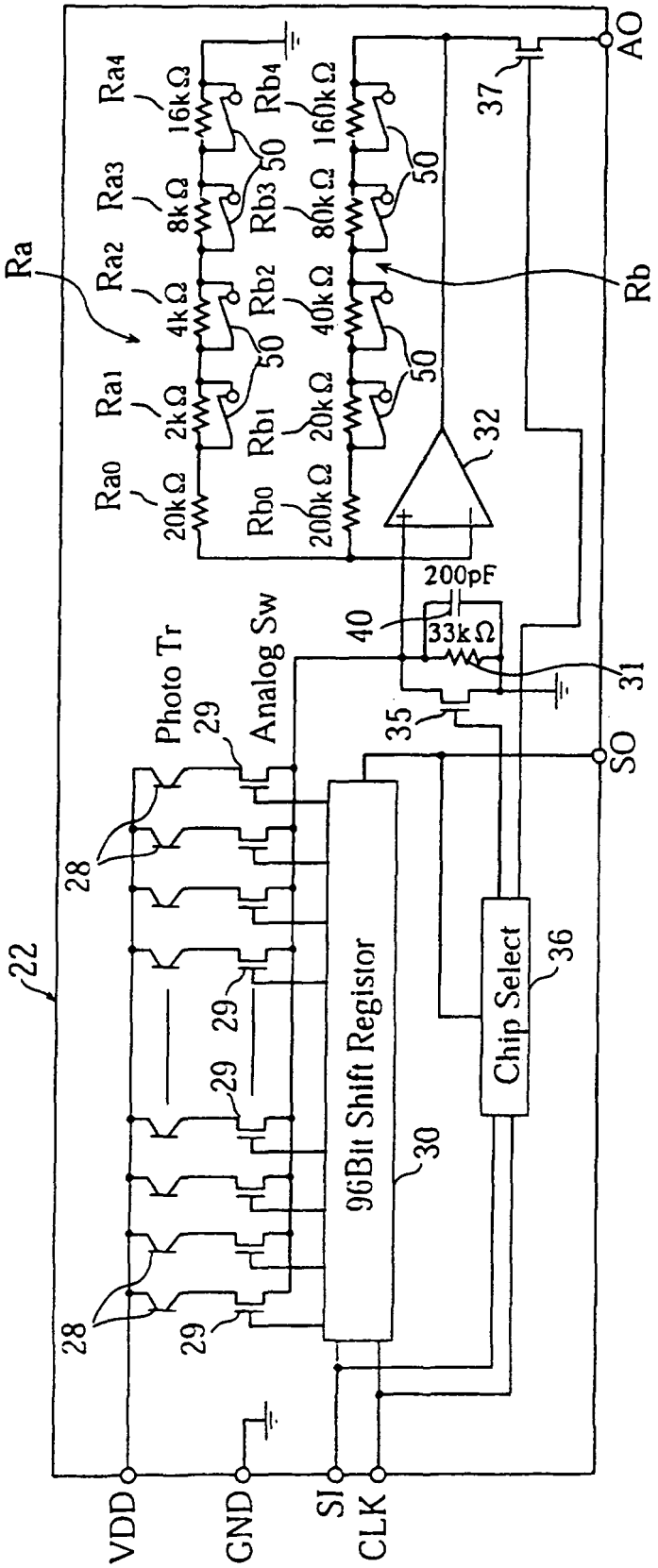

Ra
Ra4
16kΩ
Ra3
8kΩ
Ra2
4kΩ
Ra1
2kΩ
Ra0
20kΩ
Rb4
160kΩ
Rb3
80kΩ
Rb2
40kΩ
Rb1
20kΩ
Rb0
200kΩ
50
Rb
AO
37
32
200pF
33kΩ
40
31
35
SO
Photo Tr
29
Analog Sw
28
96Bit Shift Registor
30
Chip Select
36
22
VDD
GND
SI
CLK

Fig.6

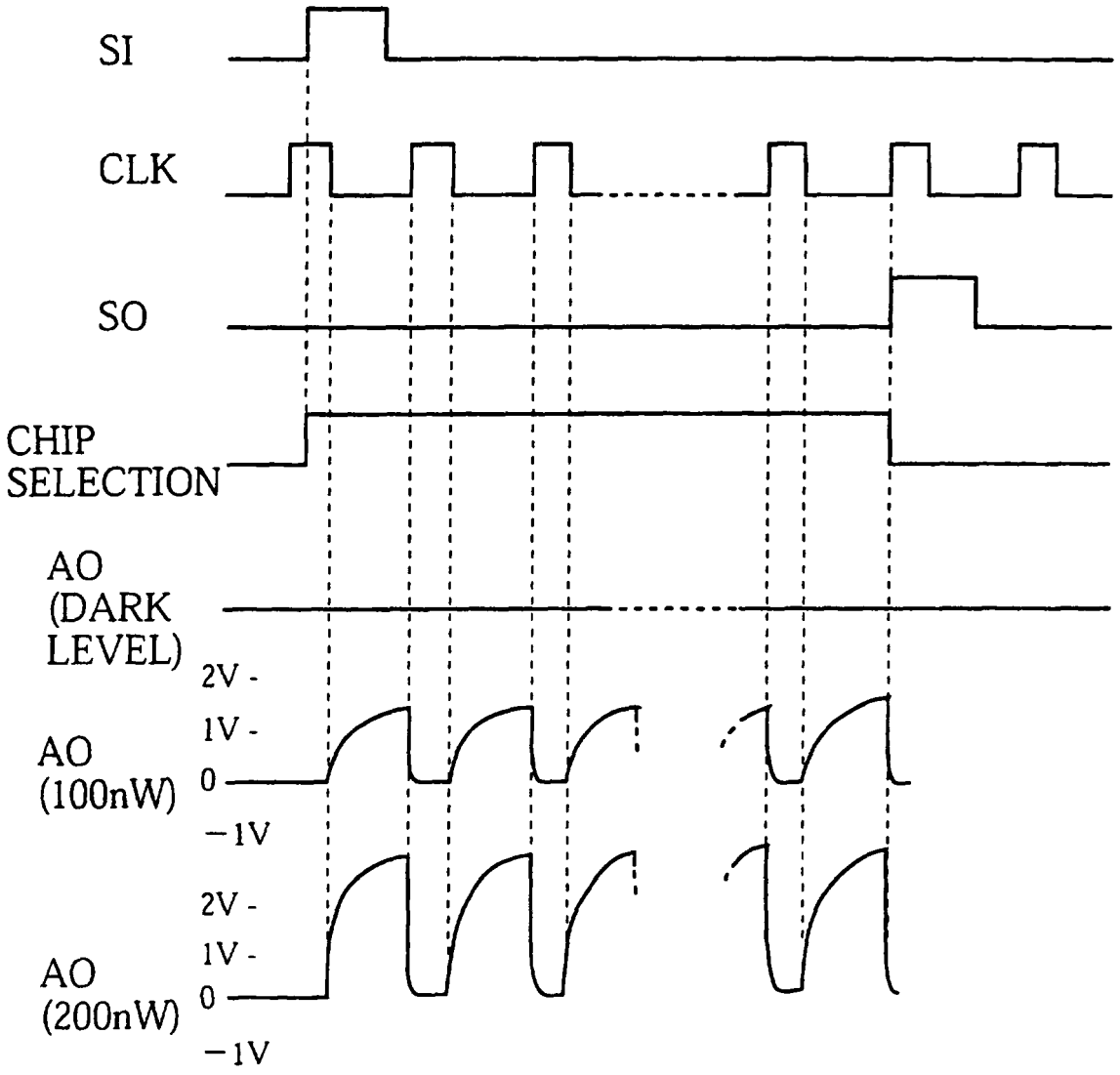

SI
CLK
SO
CHIP SELECTION
AO (DARK LEVEL)
AO (100nW)
AO (200nW)
2V
1V
0
−1V
2V
1V
0
−1V

Fig.7

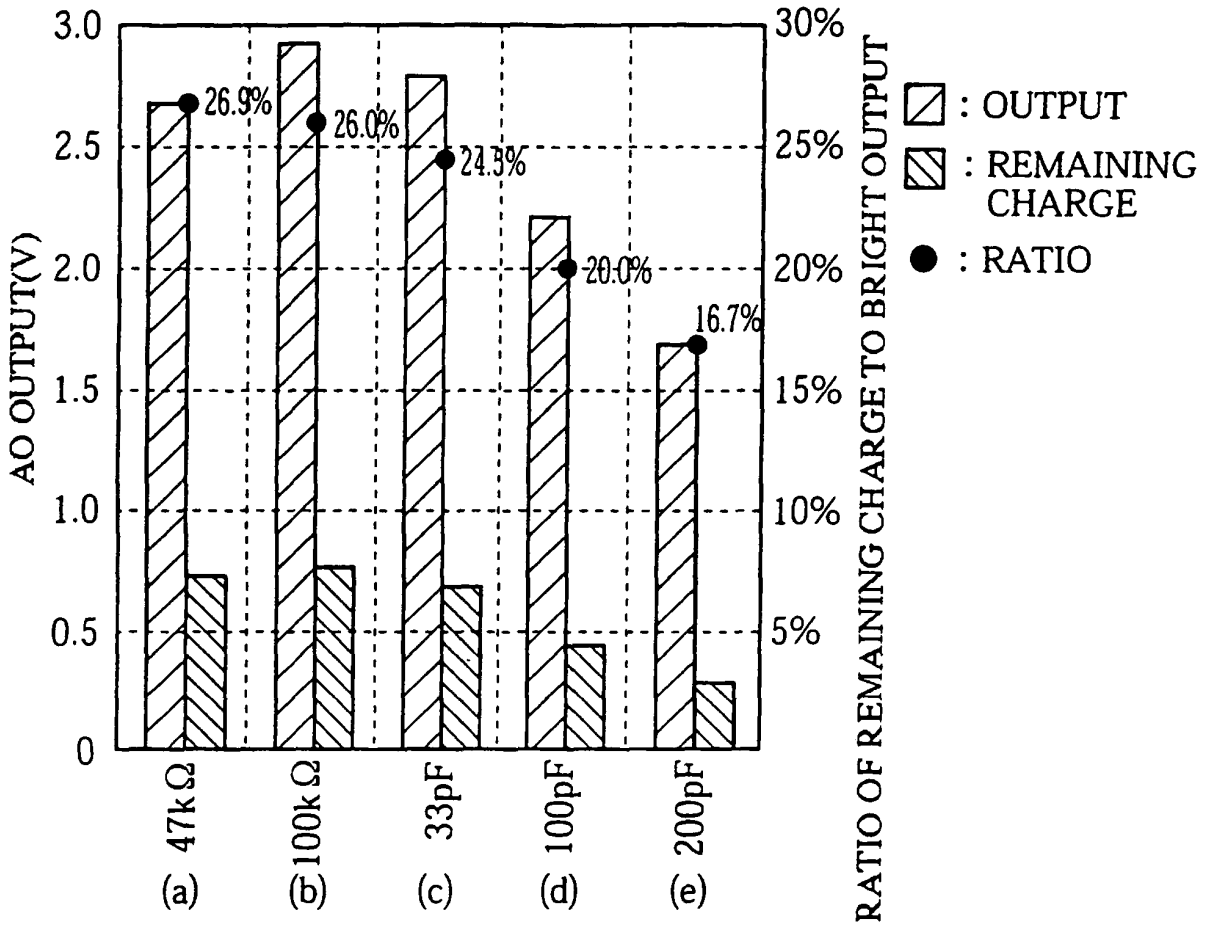

3.0
2.5
2.0
1.5
1.0
0.5
0
AO OUTPUT(V)
30%
25%
20%
15%
10%
5%
RATIO OF REMAINING CHARGE TO BRIGHT OUTPUT
26.9%
26.0%
24.3%
20.0%
16.7%
47kΩ
100kΩ
33pF
100pF
200pF
(a)
(b)
(c)
(d)
(e)
: OUTPUT
: REMAINING CHARGE
: RATIO

FIG.8

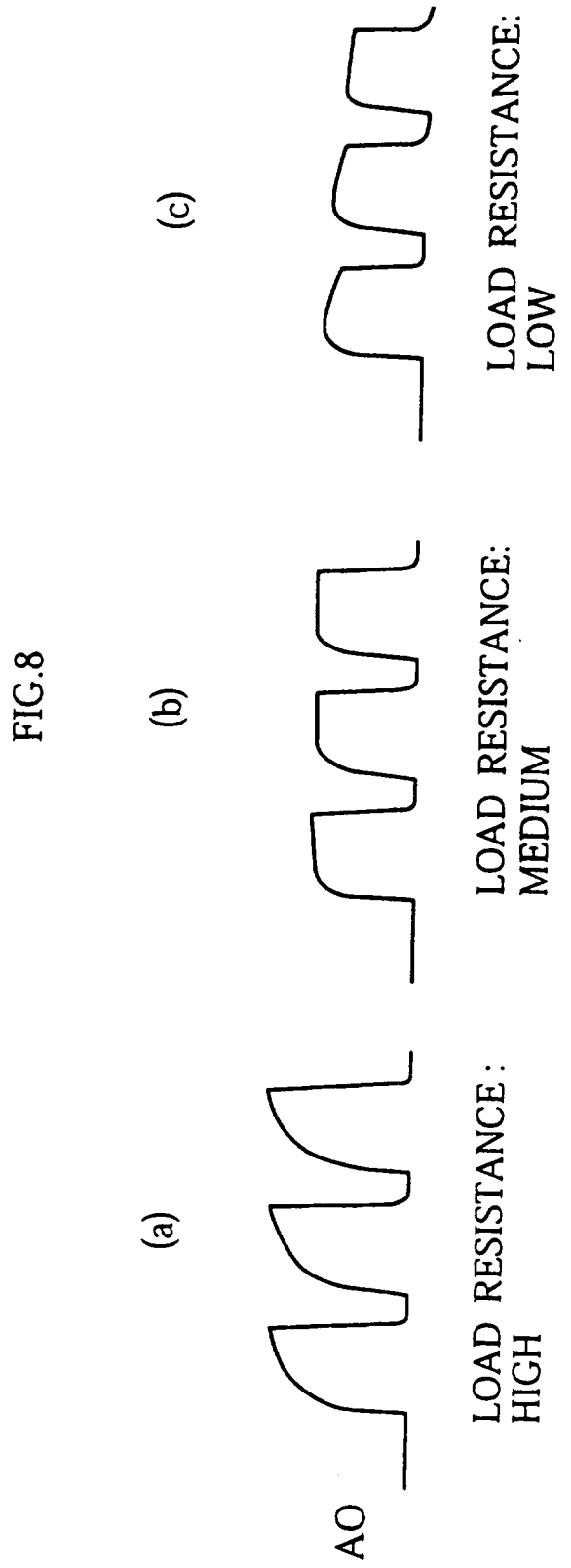

AO
(a)
LOAD RESISTANCE:
HIGH
(b)
LOAD RESISTANCE:
MEDIUM
(c)
LOAD RESISTANCE:
LOW

Fig.9

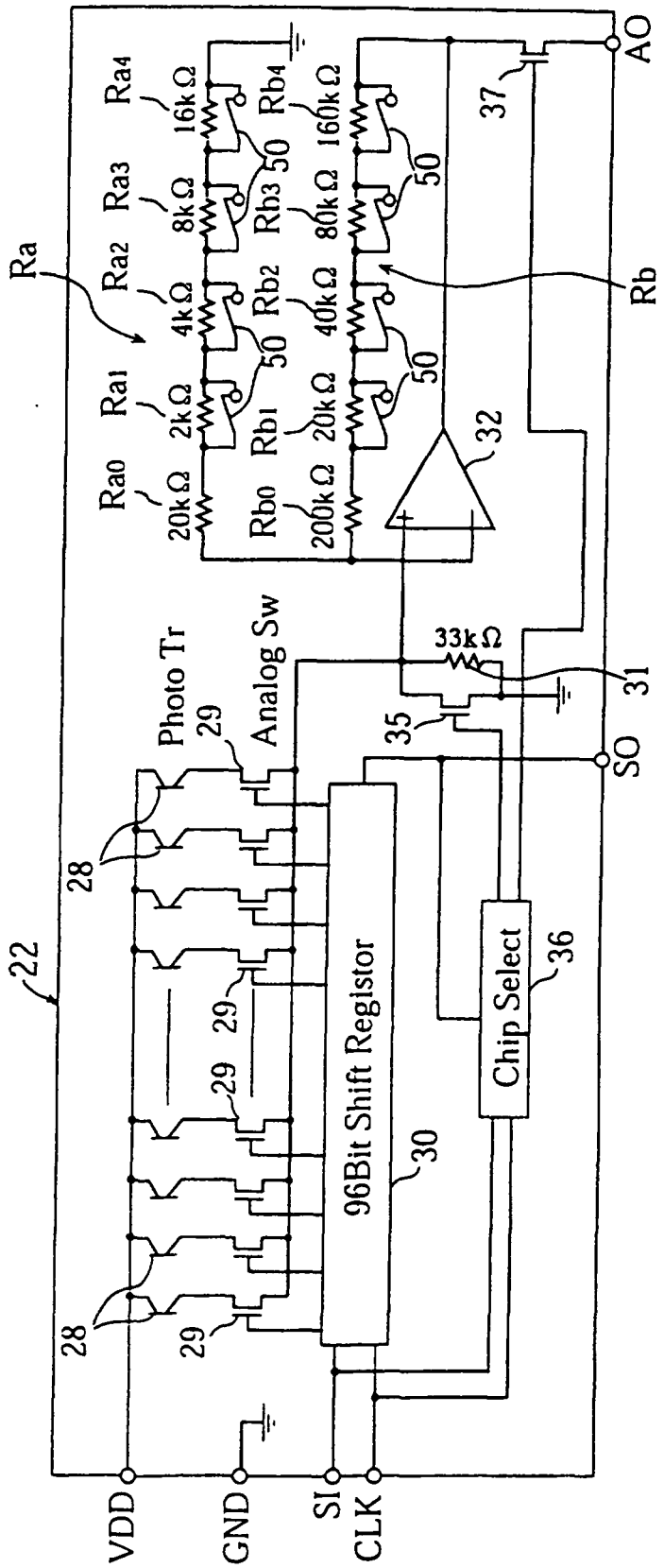

Ra
Ra0
Ra1
Ra2
Ra3
Ra4
20kΩ
2kΩ
4kΩ
8kΩ
16kΩ
Rb
Rb0
Rb1
Rb2
Rb3
Rb4
200kΩ
20kΩ
40kΩ
80kΩ
160kΩ
50
32
33kΩ
31
35
37
AO
SO
Photo Tr
Analog Sw
29
28
22
96Bit Shift Registor
30
Chip Select
36
VDD
GND
SI
CLK

Fig.10

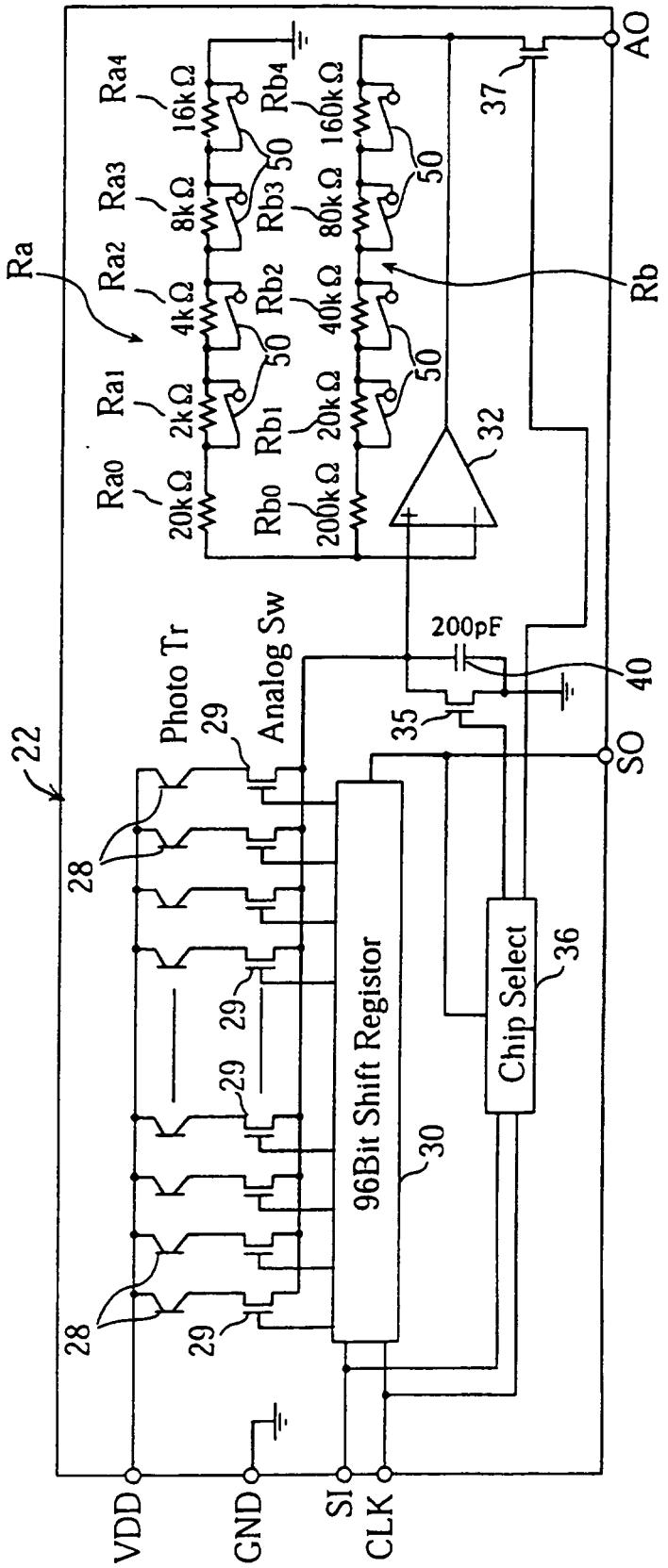

Ra
Ra0
Ra1
Ra2
Ra3
Ra4
20kΩ
2kΩ
4kΩ
8kΩ
16kΩ
Rb
Rb0
Rb1
Rb2
Rb3
Rb4
200kΩ
20kΩ
40kΩ
80kΩ
160kΩ
50
32
37
AO
200pF
40
35
SO
22
Photo Tr
29
Analog Sw
28
96Bit Shift Registor
30
Chip Select
36
VDD
GND
SI
CLK

Fig.11

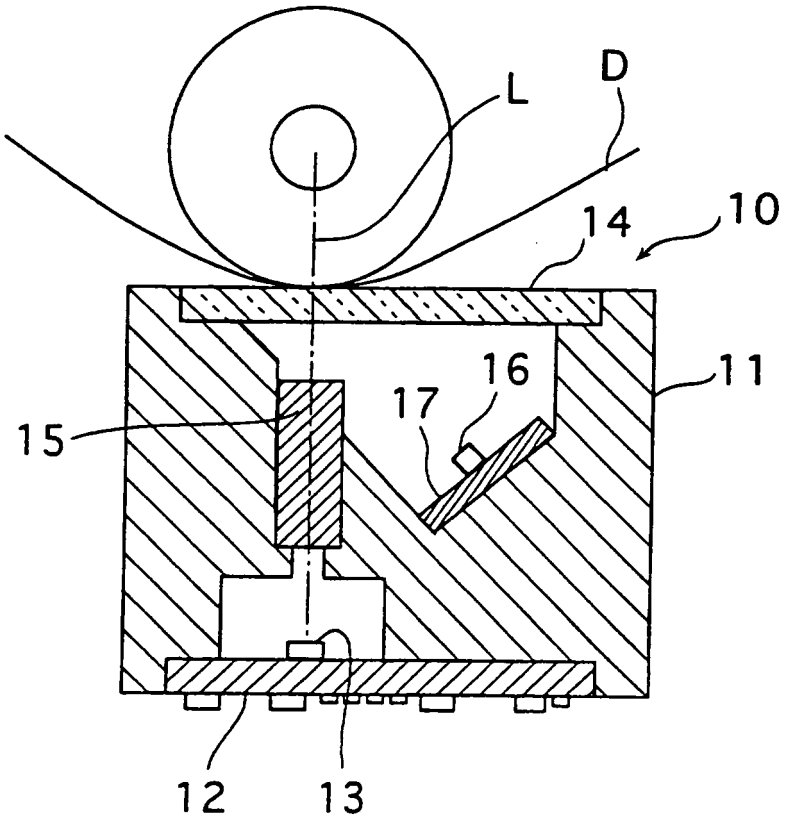
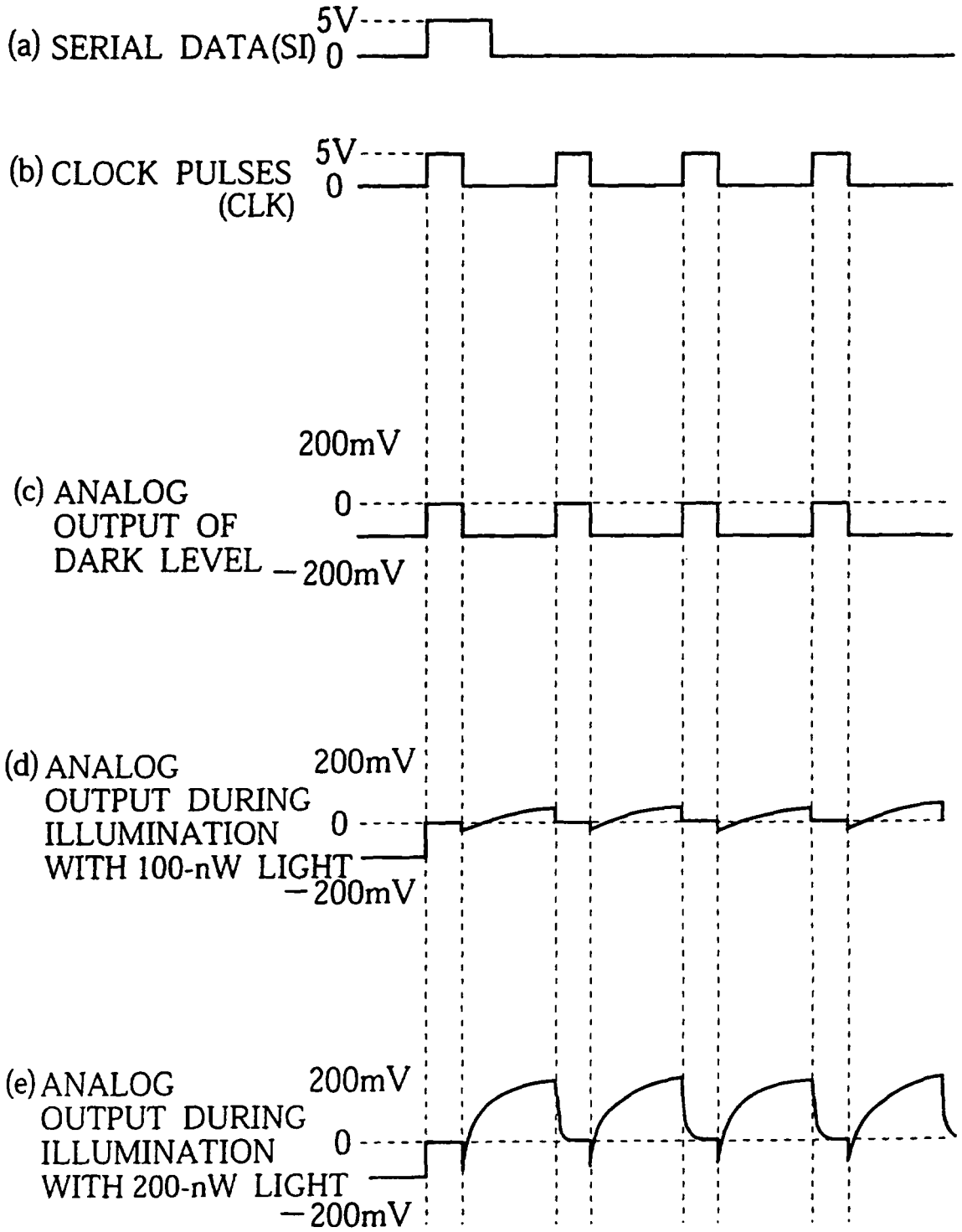


Fig.12


(a) SERIAL DATA(SI)
5V
0
(b) CLOCK PULSES (CLK)
5V
0
200mV
(c) ANALOG OUTPUT OF DARK LEVEL
0
−200mV
(d) ANALOG OUTPUT DURING ILLUMINATION WITH 100-nW LIGHT
200mV
0
−200mV
(e) ANALOG OUTPUT DURING ILLUMINATION WITH 200-nW LIGHT
200mV
0
−200mV