

March 30, 1965

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3,176,243

FULL-WAVE DIFFERENTIAL CONTROL CIRCUIT EMPLOYING
SINGLE SATURABLE CORE TRANSFORMER

Filed April 2, 1962

3 Sheets-Sheet 1

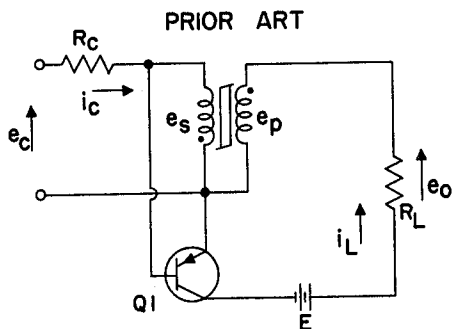


FIG. 1a

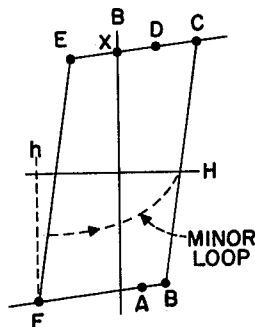


FIG. 1b

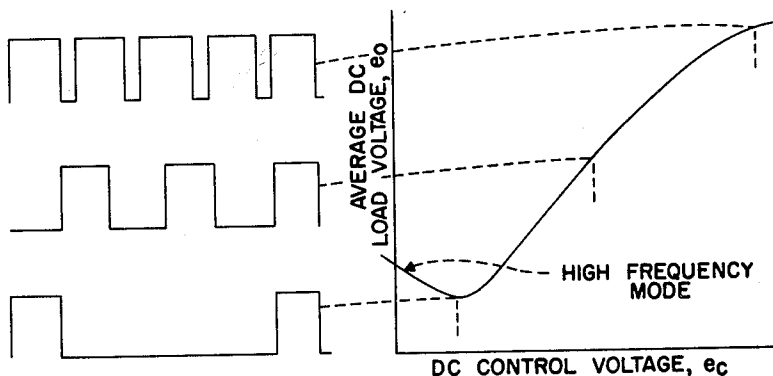


FIG. 2a

FIG. 2b

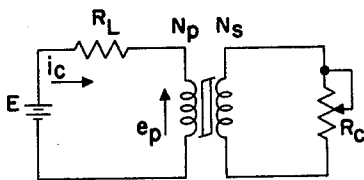


FIG. 3a

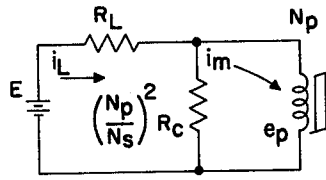


FIG. 3b

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3 Sheets-Sheet 2

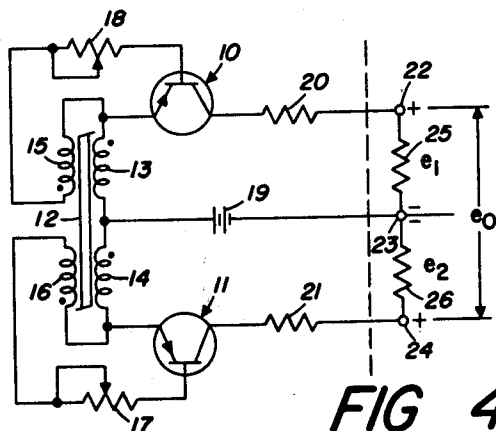


FIG 4

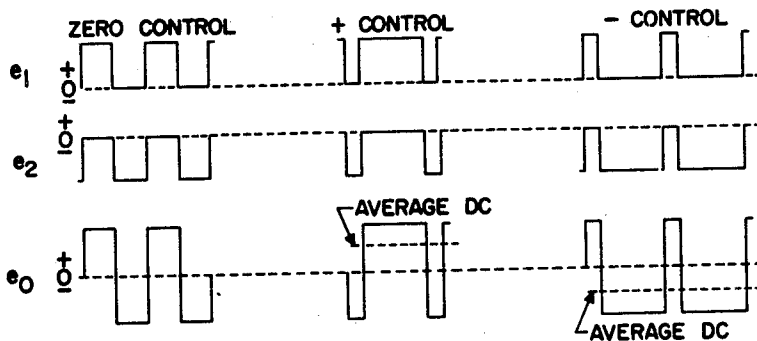


FIG 5

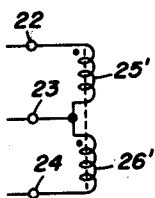


FIG 6

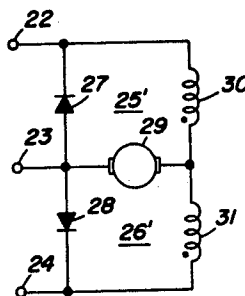


FIG 7

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3,176,243

FULL-WAVE DIFFERENTIAL CONTROL CIRCUIT EMPLOYING
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3 Sheets-Sheet 3

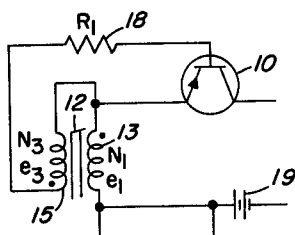


FIG 8a

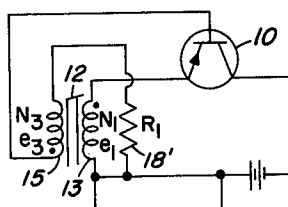


FIG. 8b

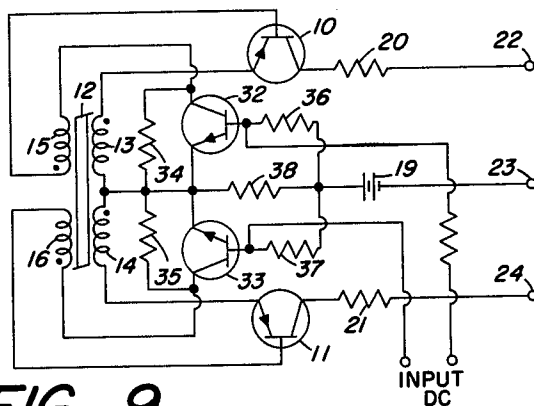


FIG 9

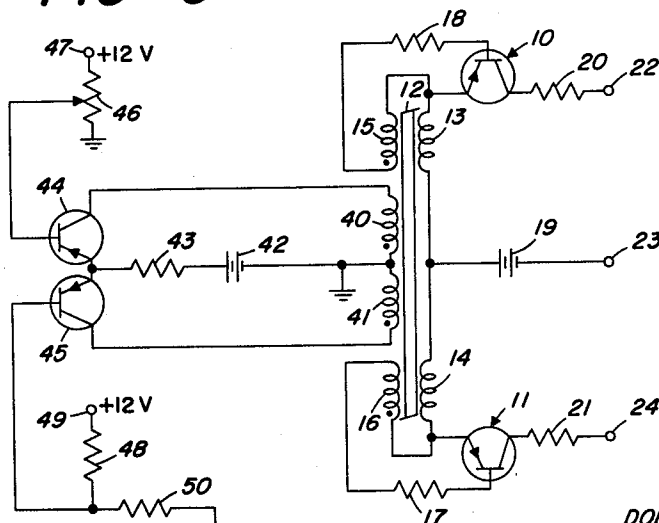


FIG 10

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1

3,176,243

FULL-WAVE DIFFERENTIAL CONTROL CIRCUIT EMPLOYING SINGLE SATURABLE CORE TRANSFORMER

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Filed Apr. 2, 1962, Ser. No. 184,357
6 Claims. (Cl. 331-113)

This invention relates generally to differential control circuitry and more particularly to a type of full wave differential control employing saturable current transformer techniques in conjunction with transistor switching.

The invention is basically embodied in the provision of a three-wire output of the double ended or two-phase type such as might be used for controlling a servo motor or other devices requiring a differential output.

Numerous circuits are employed in the art which utilize transistor switching techniques in conjunction with saturable magnetic cores and such circuits are widely employed for control of reversible motors, for example. The present invention resides in the provision of a two-phase or double-ended signal development employing a minimum of circuitry so as to reduce weight and volumetric requirements as compared with known circuitry. The general approach, as applied herein to motor control, for example, is the provision of a double-ended output which introduces an unbalance in the average flux developed in motors to produce motor rotation in either direction.

The present invention is featured in the provision of means employing a single saturable core member in conjunction with switching transistors and a direct current voltage supply source to obtain a load driving source of the double-ended or fullwave type. The minimum circuitry uniquely enables a differential pulse width modulation by novel control of both the on and off-time portions of switching duty cycles.

Additional features of the present invention are the provision of developing a double-ended or full-wave output signal which is differentially controllable by variation of the control circuit impedance as reflected into the load circuitry and in means whereby this differential control may be attained by variation of physical impedance parameters per se or by electronic variation of said reflected impedance in response to a direct current voltage control source.

These and other objects and features of the present invention will become apparent upon reading the following description in conjunction with the accompanying drawings in which:

FIGURES 1(a) and 1(b) are a schematic representation of a prior art control circuitry of a related type, and an operational diagram thereof;

FIGURES 2(a) and 2(b) are a diagrammatic illustration of the output wave forms of the circuit of FIGURE 1(a) as a function of variation in put parameters;

FIGURES 3(a) and 3(b) are an operational schematic and equivalent circuit concerning operational aspects of the circuit of FIGURE 1(a);

FIGURE 4 is a schematic representation of an embodiment of the present invention;

FIGURE 5 is a diagrammatic representation of operational waveforms of the circuitry of FIGURE 4;

FIGURES 6 and 7 are schematic embodiments of types of output circuitry controllable by the circuitry of the invention;

FIGURES 8(a) and 8(b) represent a schematic variation and modification of a portion of the circuitry of FIGURE 4;

FIGURE 9 represents a further embodiment of the present invention utilizing D.C. voltage control, and

2

FIGURE 10 represents a further embodiment of the invention employing drive current control technique.

The present invention relates to circuitry by which two-phase control may be obtained utilizing but a single saturable core in conjunction with switching transistors whereby differential control of a controlled member such as, for example, a split-phase direct current motor, may be obtained by differential control of the pulse widths of differential output drive pulses. The present invention may best be understood by a consideration of a prior art technique disclosed by R. E. Morgan and described in AIEE Communications and Electronics, Volume 77, page 558, in an article entitled, "Saturable Current Transformer and Transistor Switch." The reference article describes the use of a current transformer in series with a power transistor, a D.C. supply, and a load. This circuitry was presented for use as a single-ended control of a load and might be basically defined as a square wave oscillator with frequency controlled by a D.C. input to the current transformer. The present invention relates generally to this prior art circuitry and certain operational aspects of the circuitry of the present invention may be comprehended by a discussion of the operational aspects of the Morgan circuit as it relates to single ended control. The present invention stems from an insight suggested by a study of the operational aspects of the prior art circuit with application to two-phase control circuitry, while retaining the simplified approach of utilizing but a single saturable core.

The basic amplifier circuit disclosed by Morgan in the above referenced article is illustrated in FIGURE 1A and the approximate characteristic of the core member is shown in FIGURE 1B. With reference to FIGURE 1B, note is made of the finite slope of the core characteristic in the saturation regions which serve as a good approximation for HY Mu 80, the core material utilized in constructed embodiments of the present invention.

With reference to FIGURE 1, assume initially that flux is at F and a small amount of emitter to collector leakage current moves the flux from F to A. This causes a small voltage, e_s , to be induced positive at the dot. This voltage, e_s , causes base current to flow in Q_1 and Q_1 starts to turn on, increasing i_L to the magnetizing level at B. The net effect is a regenerative action and Q_1 turns on rapidly. A constant voltage $e_p = E - i_L R_L$ is applied to the primary causing a flux excursion from B to C. This excursion defines the "on time" and is determined by e_p , the number of primary turns, and the total change in flux. When the flux level reaches point C, e_s drops to zero, Q_1 begins to shut off and i_L decreases. During the decrease of i_L , flux moves in the direction C to D on the B-H loop, experiencing a change in slope of the flux-time characteristic. This results in an induced voltage, e_s , negative at the dot, that completely biases Q_1 to the off condition. This again is a regenerative action and Q_1 shuts off rapidly once saturation is reached. With Q_1 shut off, flux comes to rest at point x, corresponding to zero magnetizing force and the reset period is ready to begin.

In order to reset the core an external reverse magnetizing force H must be applied. This is done by applying a control voltage e_c to the secondary. With application of e_c , i_c quickly builds up to a magnetizing current corresponding to point E on the flux loop. The "off time" interval lasts during the flux excursion from E to F. The time of this interval is determined by e_c , the number of secondary turns, and the total change in flux. The off time can be controlled by varying e_c . Large values of e_c result in a short off time while small values cause a long off time. A limiting value of e_c is reached when e_c reduces to a point where $i_c = e_c / R_c$ corresponds to a

magnetizing force h . For values of e_c less than this limiting value, the flux never reaches F and begins to traverse minor loops as shown. This results in an increase of oscillator frequency. It can be seen that the circuit operates on the principle of constant on time and variable off time. A typical set of output waveforms is shown in FIGURE 2a with the corresponding control characteristic appearing in FIGURE 2b.

The original circuitry of FIGURE 1 operates on the principle of an output pulse waveform having constant on time with off time varied as a function of the input control voltage e_c . As previously discussed, the circuitry of the present invention provides, by contradistinction, a double-ended or full-wave output with provision for differential control through variation of both the on and off times in a differential manner. As means for gaining insight into the operational aspects of the present invention a mathematical analysis of the effects of impedance control as it applies to either the on or off times is herein presented. For this purpose, analysis is made in conjunction with the single-ended prior art circuitry as follows:

A simplified schematic of the circuit during the conduction period of Q_1 is shown in FIGURE 3a. The saturation resistance of Q_1 has been taken as zero and the secondary circuit consists of a control resistance, R_c . If desirable it can be considered that Q_1 saturation resistance is lumped with R_L , and that Q_1 base circuit resistance is lumped with R_c . The latter becomes important in actual designs where an external base resistor is used. The corresponding equivalent circuit is shown in FIGURE 3b. Note that core losses have been neglected. This may not be a valid assumption at the higher operating frequencies.

The voltage applied to the primary winding, e_p is defined as

$$e_p = N_p \frac{d\phi}{dt} \times 10^{-8} \quad (1)$$

where e_p is in volts and

$$\frac{d\phi}{dt}$$

is in maxwells per second and the voltage of self induction, e_p , carries a minus sign. The assumption of a linear slope (FIGURE 1b), is carried over to this derivation so that the time interval involved can be written as

$$\Delta t = N_p \frac{\Delta\phi}{e_p} \times 10^{-8} \quad (2)$$

Solving for e_p in terms of circuit parameters:

$$e_p = E - i_L R_L \quad (3)$$

from which

$$i_L = \frac{E - e_p}{R_L} \quad (4)$$

The currents may be equated as:

$$i_L = i_m + \frac{e_p}{\left(\frac{N_p}{N_s}\right)^2 R_c} \quad (5)$$

Equating (4) and (5)

$$\frac{E - e_p}{R_L} = i_m + \frac{e_p}{\left(\frac{N_p}{N_s}\right)^2 R_c} \quad (6)$$

Solving for e_p ,

$$e_p = \left(\frac{N_p}{N_s}\right)^2 R_c \times \frac{E - i_m R_L}{\left(\frac{N_p}{N_s}\right)^2 R_c + R_L} \quad (7)$$

The general expression for pulse width control results from combining Equations 2 and 7:

$$\Delta t = \frac{N_p \Delta\phi \times 10^{-8}}{\left(\frac{N_p}{N_s}\right)^2 R_c} \times \frac{\left(\frac{N_p}{N_s}\right)^2 R_c + R_L}{E - i_m R_L} \quad (8)$$

Where

t = seconds

N_p = primary turns

N_s = secondary turns

R_c, R_L = ohms

i_m = magnetizing current, amperes

$\Delta\phi$ = total flux change, maxwells

Now, i_m can be found from

$$i_m = \frac{Hc1}{0.4\pi N_p} \quad (9)$$

where Hc , oersteds and 1, centimeters are published core parameters, $\Delta\phi$ can be determined from the published values of flux density and effective cross sectional area of the core.

If

$$R_L \gg \left(\frac{N_p}{N_s}\right)^2 R_c$$

Equation 8 can be rewritten:

$$\Delta t = \frac{1}{R_c} \times \frac{N_p \Delta\phi \times 10^{-8}}{\left(\frac{N_p}{N_s}\right)^2} \times \frac{R_L}{E - i_m R_L} \quad (10)$$

In a majority of designs attempted, the above relationship held true and Equation 10 was used. Measured values of Δt agreed quite well with initial design calculations. The control that R_c exhibits over Δt is more apparent in Equation 10 than it is in Equation 8. A number of experiments were conducted using single phase or single ended amplifiers with both voltage and resistance control in conjunction with resistive and motor loads to verify the foregoing design equations.

A first embodiment of a full-wave differential control drive circuit utilizing a single core and a direct current voltage source is illustrated schematically in FIGURE 4. With reference to FIGURE 4 a single core member 12 has wound thereon a first primary winding 13, one end of which is connected to the positive terminal of a direct current voltage source 19. The other end of primary winding 13 is connected to the emitter of switching transistor 10 and to one end of a cooperating secondary winding 15, the other end of secondary winding 15 being connected through a variable resistance member 18 to the base of transistor 10. Windings 13 and 15 are wound with opposite polarization as indicated by the respective dot configurations. The collector element of transistor 10 is connected through a resistor 20 to a first output terminal 22. The negative terminal of the direct current voltage 19 is connected to a second or common output terminal 23.

The single core member 12 has additionally wound thereon a second set of windings comprising a primary winding 14, one end of which is connected to the positive terminal of direct current voltage source 19 and the other end of which is connected to the emitter of a second switching transmitter 11 and additionally to one end of a cooperating secondary winding 16. The other end of secondary winding 16 is connected through a second variable resistance member 17 to the base of transistor 11. Windings 14 and 16 are wound with opposite polarization as indicated by the respective dot configuration and each of the first and second primary windings and first and second secondary windings are seen to be like wound or like polarized. It is further to be noted that oppositely polarized ends of the secondary windings 15 and 16 are connected through the associated resistance members 18 and

17 to the switching transistors and that oppositely polarized ends of primary windings 13 and 14 are connected in common to the direct current voltage source 19 and to the emitters of the associated transistors. The collector element of transistor 11 is connected through a resistance 21 to a third output terminal 24. A three terminal resistive load is shown connected to the three wire double ended output 22, 23, 24 in the form of resistance members 25 and 26 connected respectively between output terminals 22 and 24 and the common output terminal 23.

In operation, the circuitry of FIGURE 4, assuming balanced conditions including equal settings of resistance members 17 and 18, operates essentially as a free running oscillator with equal on and off times such that the net output e_0 is zero. As indicated by Equation 10, above, the nominal frequency of oscillation is determined by the impedances reflected into the load circuit. Resistances 17 and 18 are each seen to be in series with the emitter-to-base resistance of transistors 10 and 11. Each of the symmetrical halves of the circuitry of FIGURE 4 operates in a manner defined by the above defined equations and, due to the respective polarization of the associated core windings, transistors 10 and 11 are alternately conductive with equal time intervals Δt as defined in Equation 10. Adjustment of the nominal frequency of the circuit may be obtained by varying resistances 17 and 18 in the same direction so as to impart a like effect on the Δt in Equation 10 as a function of the control resistance. With the condition of equal reflected resistances, each of the symmetrical halves of the circuit generates a square wave with the respective differential outputs e_1 and e_2 being 180° out of phase. This condition may be deemed a condition of "zero" control. Reference is made to the waveforms of FIGURE 5 which show output voltages e_1 , e_2 and the combined output voltage, e_0 , for the "zero" control condition and it is seen that for this condition (equal settings of resistances 17 and 18) the average D.C. component of e_0 is zero. As mentioned above the circuit provides means for adjusting the periodicity of the output voltage waveforms by varying the variable resistances 17 and 18 together that is, simultaneously and by the same amount either increasing or decreasing these resistances.

Control conditions, either "positive" or "negative" are defined as the development of output wave forms e_1 and e_2 wherein the on times (the conduction periods of the associated transistor) as concerns the two waveforms vary differentially. As above mentioned, this is attained through differential variation of the variable resistances 17 and 18, that is, the simultaneous increase and decrease of the respective resistances by the same amount from a nominal value. FIGURE 5 illustrates the output wave forms for conditions of "positive" and "negative" control. Under conditions of positive control, it is seen that the output, e_1 , is positive for an appreciably longer period of time corresponding to an increased on time and the off time is decreased as compared to the zero control condition. It is further seen that under positive control condition the output waveform e_2 has reduced on-time and decreased off-time by the same proportionality; the on-times being defined as the conduction periods of the associated transistors 10 and 11 during which time it is seen that the direct current voltage source 19 is essentially developed across one of output resistors 25 and 26 due to the low impedance emitter to collector path of the associated transistor. For condition of positive control, the output waveform e_0 , as illustrated in FIGURE 5 is seen to have an average direct current component which is positive.

The condition defined as negative control is attained by an opposite differential variation of resistance members 17 and 18 such that the on-time in the e_1 waveform is reduced from nominal while the on-time of output waveform e_2 is increased from nominal such that output form e_0 has a negative average direct current component. Pulse width ratios in the order of 10 to 1 may readily be obtained.

The load circuit in the embodiment of FIGURE 4 is illustrated as a resistive differential load which might correspond to using the drive circuitry as a direct current amplifier providing a differential D.C. output e_0 as a function of differential impedance variation of resistors 17 and 18. Further examples of three-terminal loads which might be operated from the circuitry of FIGURE 4 are illustrated in FIGURES 6 and 7. FIGURE 6 represents, for example, the load as being comprised of windings 25' and 26' in place of the resistive members as connected between the output terminals 22, 23 and 24. Windings 25' and 26' might be those of a hydraulic control valve or a differential relay. FIGURE 7 illustrates the load as being that of a split field series D.C. motor as it might be used in servo positioning. Each of the motor field windings 30 and 31 is connected between output terminal 22 and 24 serially with the armature 29 to the common output terminal 23 with each series connection being shunted by an appropriately polarized diode 27 or 28, the latter functioning as diverter diodes to prevent inductive voltage developed by collapse of the associated motor field from being directed into the drive circuitry. The circuitry of FIGURE 4 is very desirable as a driving source for the split field series motor as illustrated in FIGURE 7, since at its null (condition of zero control) the net D.C. current in the field windings is zero and efficiency is thereby increased. Reverse operation of the split field D.C. motor as driven by the circuitry of FIGURE 4 stems from an unbalance in the average flux developed in the field windings 30 and 31 to produce a net flux under positive control conditions which is opposite to that under negative control conditions.

The embodiment of FIGURE 4 provides a three wire differential output based on differential pulse width modulation wherein the modulation is effected by differential variation of control resistances. In many applications the desired control by means of differentially varying the resistances may not be practical and it may be desirable to effect the differential control by means of an applied signal. The circuitry of FIGURE 4 may accordingly be modified to include an electronic variation of the control resistances wherein the necessary variation of resistance as reflected into the control circuit loops may be realized by appropriate variation of an input voltage. Such a modification will be further discussed.

The attainment of control as a function of an input signal necessitates a relatively minor modification of the circuitry of FIGURE 4, a portion of which is illustrated in FIGURE 8. FIGURE 8A illustrates the portion of the circuitry of FIGURE 4 upon which the modification is made. The illustrated portion shows switching transistor 10 and its relationship with control resistance 18 and windings 13 and 15 upon the core 12. The basic modification of this portion of the circuitry is illustrated in FIGURE 8B wherein it is noted that the position of the control resistance 18 has been changed and primary winding 15 is returned through the repositioned control resistance 18' to the D.C. voltage supply 19, rather than to the "dot" end of primary winding 13 as in the basic embodiment. A comparison between the modification of FIGURE 8B and that of the basic circuitry in FIGURE 8A indicates that the operation of the circuitry is unaltered providing e_3 (the voltage induced in secondary windings 15) is much greater than e_1 (the voltage in primary windings 13). This condition may be satisfied if N_3 (the number of turns in winding 15) are chosen to be much greater than N_1 (the number of turns in winding 13). This condition might be satisfied by making the ratio N_3/N_1 equal to 25, for example.

Bearing in mind the modification illustrated in FIGURE 8B, reference is made to the operational embodiment of FIGURE 9 wherein the basic circuit of FIGURE 4 has been appropriately modified in accordance with that suggested in FIGURE 8B. In the embodiment of FIGURE 9, the control resistance 18 has been replaced,

with a resistance 34 in parallel with the collector to emitter resistance of a transistor 32. Similarly, control resistance 17 of FIGURE 4 has been replaced with a resistance 35 paralleling the collector to emitter resistance of a transistor 33. The base elements of transistors 32 and 33 are connected through resistors 36 and 37 respectively to the positive terminal of D.C. source 19 and individually to respective terminals of a source of input control voltage. The emitters of each of the transistors 32 and 33 are connected through a resistance 38 to the positive terminal of D.C. voltage source 19. Transistors 32 and 33 thus obtain a bias voltage from resistor 38 and bias current is limited by resistors 36 and 37. Control of the circuit is introduced by the application of the D.C. input control source as applied between the base elements of the transistors 32 and 33. In the absence of control input voltage a zero control situation is realized as in the previous embodiment since, assuming balanced conditions, the control impedances in each half of the circuit are equal and the output is a symmetrical square wave having a zero average D.C. as illustrated in FIGURE 5. Differential control is realized by the application of input control voltage across the bases of the transistors 32 and 33, the relative polarity of which effects a differential change in the collector to emitter resistances of transistors 32 and 33 which is reflected as a change of base resistance for switching transistors 10 and 11. Resistances 34 and 35 shunt the collector to emitter resistance of transistors 32 and 33 to limit the maximum resistance and prevent erratic operation.

A further control embodiment in accordance with the present invention is indicated in FIGURE 10 wherein resistors 18 and 17 have been replaced by fixed resistors and additional control circuitry has been added. In the embodiment of FIGURE 10 the core member 12 is provided with additional windings 40 and 41 which are like-wound with respect to the windings 15 and 16, as illustrated. The junction between windings 40 and 41 is connected to the negative terminal of a D.C. voltage source 42 and each of the windings 40 and 41 is serially connected with the collector to emitter resistance of one of transistors 44 and 45 and a common resistive member 43 to the positive terminal of the voltage source 42. The base of transistor 44 is connected to the wiper arm of a potentiometer 46 across which the D.C. supply is connected. The base of transistor 45 is connected to the junction between equal resistors 48 and 49 which are connected across the D.C. supply.

The embodiment of FIGURE 10 enables differential control by controlling the base current through transistors 44 and 45 which varies the collector to emitter resistance of these elements. This impedance is reflected into the load circuit in accordance with Equation 10 to obtain the desired control. Assuming the wiper arm of potentiometer 46 to be centered, the base currents of transistors 44 and 45 are equal and the associated windings 40 and 41 induce like control such that the aforescribed condition of zero control is realized. Adjustment of potentiometer 46 from this centered position is seen to impart a greater or lesser control of base current through transistor 44 as compared to transistor 45 and, correspondingly, the associated windings 40 and 41 introduce a differential control such that the above-described conditions of positive and negative control may be realized. The embodiment of FIGURE 10 may utilize the same D.C. control source throughout. Note that the potentiometer 46 and the resistance voltage divider 48-50 may be shunted across D.C. voltage 42 and that D.C. voltage source 42 may be additionally utilized as the D.C. voltage source 19 illustrated in FIGURES 4 and 9. The embodiment of FIGURE 9 requires a separate voltage source for the D.C. control, that is the control voltage source of FIGURE 9 must be "floating."

Concerning again the embodiment of FIGURE 10, the desired control may be effected by direct application of D.C. current to the additional core windings 40 and

41 in a differential manner. This direct application (not illustrated) causes differential control by effectively varying the " i_m " term in Equation 10.

The present invention is thus seen to provide means for developing a three-wire full-wave control circuit utilizing but a single saturable core member and a minimum of circuitry. The basic embodiment of FIGURE 4 and the further embodiments of FIGURES 9 and 10 provide means whereby control may be effected in a variety of ways to fit particular control applications. For example, considering the control circuitry as driving a servo motor, the potentiometers in FIGURES 4 and 10 might be feedback potentiometers such as control surface position potentiometers in aircraft. Further, the potentiometers might be "command" potentiometers such as the well known turn and pitch controller potentiometers utilized in autopilots. In a like manner, the input control voltage of the embodiment of FIGURE 9 could be the voltage existing at the wiper arms of such feedback or command potentiometers. In any of the described embodiments the output waveform may be filtered and used as a smooth direct current output voltage; may be used in applications where pulse width modulation is desired by independent usage of output waveforms e_1 and e_2 ; and may be used differentially (e_0) or independently (e_1 and e_2) for various gating and switching pulses.

Although the present invention has been described with respect to particular embodiments thereof, it is not to be further limited as changes might be made therein which fall within the scope of the present invention as defined in the appended claims.

I claim:

1. A differential control circuit of the type producing first and second output signals differentially referenced to a common output terminal comprising first and second control circuits each comprising a like-wound control winding on a saturable core member common to each of said control windings; a load circuit comprising a common direct current voltage source including a common terminal, first and second like-wound load windings wound on said saturable core member, said load windings being oppositely polarized with respect to said control windings, means connecting first ends of said local windings through said direct current voltage source to said common output terminal, the other ends of each of said load windings being respectively connected to the emitter elements of first and second transistors, the base elements of said first and second transistors being respectively connected to oppositely polarized ends of said first and second control windings, the other ends of said control windings being connected through first and second control resistance members to the junction between said output windings, third and fourth transistors, the emitter-collector junctions of said third and fourth transistor respectively shunting said first and second control resistance members, and means controlling the base current of each of said third and fourth transistors in a differential manner to vary the emitter-collector impedances thereof.

2. A differential control circuit of a type producing first and second output signals differentially referenced to a common output terminal comprising first and second control circuits each comprising a like-wound control winding on a saturable core member common to each of said control windings, said control windings being respectively serially connected with a control resistance means and the emitter-base junction of a transistor; a load circuit comprising a common direct current voltage source including a common terminal, first and second like-wound load windings wound on said saturable core member, said load windings being oppositely polarized with respect to said control windings, means connecting first ends of said load windings through said direct current voltage source to said common output terminal, the other ends of each of said load windings being respectively connected to the emitter element of one of said transistors,

the collector elements of said transistors being connected respectively to said first and second output terminals; a further pair of windings like-wound upon said common saturable core member and like-polarized with respect to said first and second control windings, differential current control means connected to each of said further pair of windings; said differential current control means including a direct current voltage source, first and second variable impedance means respectively serially connected with said direct current voltage source and one of said further pair of windings, and means for differentially varying said first and second variable impedance means.

3. Control circuitry as defined in claim 2 wherein said first and second variable impedance means comprises a further pair of transistors having the respective emitter elements thereof connected in common, said direct current voltage source connected between said common emitter junction and the junction between said further pair of control windings, the collector elements of each of said further transistors connected independently to one of the other ends of said further pair of control windings and means associated with the base elements of said further transistors to effect a variation in the respective biases thereon in a differential manner.

4. A full wave differential control circuit of the type producing first and second output signals differentially referred to a common output terminal comprising a saturable core member having wound thereon first and second secondary windings, said secondary windings being mutually like wound and collectively oppositely wound with respect to said primary windings, said primary windings being serially connected with the junction of first ends thereof connected serially through a direct current voltage supply source to said common output terminal, first and second transistors, the collector elements of each of said first and second transistors connected respectively to first and second output terminals, the emitters of each of said first and second transistors connected respectively to the other ends of each of said primary windings, the bases of said first and second transistors connected respectively to oppositely polarized first ends of said secondary windings, third and fourth transistors having collector elements respectively connected to the other ends of said secondary windings and emitter elements commonly connected to the junction between said primary windings, and means for biasing the emitter base junction of each of said third and fourth transistors in a differential manner to

effect a differential variation in the collector-emitter impedance thereof.

5. A full wave differential control circuit of the type producing first and second output signals differentially referred to a common output terminal comprising a saturable core member having wound thereon first and second like wound primary windings and first and second secondary windings, said secondary windings being mutually like wound and collectively oppositely wound with respect to said primary windings, said primary windings being serially connected with the junction of first ends thereof connected serially through a first resistor and a direct current voltage supply source to said common output terminal, first and second transistors, the collector elements of each of said first and second transistors connected respectively to said first and second output terminals, the emitters of each of said first and second transistors connected respectively to the other ends of each of said primary windings, the bases of said first and second transistors connected respectively to oppositely polarized first ends of said secondary windings, third and fourth transistors having collector elements thereof respectively connected to the other ends of said secondary windings, the emitter elements of said third and fourth transistors commonly connected to the junction between said primary windings, the base elements of said third and fourth transistors respectively connected through second and third resistances to said direct current voltage supply source, and a source of direct current control voltage connected between the base elements of said third and fourth transistors.

6. Control circuitry as defined in claim 5, further comprising fourth and fifth resistances respectively connected between the collector and emitter elements of said third and fourth transistors.

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