Title: BI-DIRECTIONAL BUFFER FOR INTERFACING TEST SYSTEM CHANNEL

Abstract: An emitter follower or source follower transistor is provided in the channel of a wafer test system between a DUT and a test system controller to enable a low power DUT to drive a test system channel. A bypass resistor is included between the base and emitter of the emitter follower transistor to enable bi-directional signals to be provided between the DUT channel and test system controller, as well as to enable parametric tests to be performed. The emitter follower transistor and bypass resistor can be provided on the probe card, with a pull down termination circuit included in the test system controller. The test system controller can provide compensation for the base to emitter voltage drop of the emitter follower transistor.
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codex and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.
INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/45610

A. CLASSIFICATION OF SUBJECT MATTER
IPC: G01R 31/02 (2006.01)

USPC: 324/756
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S.: 324/756

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
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<tbody>
<tr>
<td>X</td>
<td>US 5,184,029 B1 (KING) 02 February 1993 (02.02.1993), see entire document.</td>
<td>1-4, 8-11, 19</td>
</tr>
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<td>Y</td>
<td>US 6,774,653 B2 (GOLD et al) 10 August 2004 (10.08.2004), see entire document.</td>
<td>5, 6, 12-17, 20</td>
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<td>US 5,087,874 A (ROBINSON) 11 February 1992 (11.02.1992), see entire document.</td>
<td>6, 17</td>
</tr>
<tr>
<td>X</td>
<td>US 5,550,480 A (NELSON et al) 27 August 1996 (27.08.1996), see entire document.</td>
<td>12-14, 20</td>
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<td>A</td>
<td>US 6,339,338 B1 (ELDRIDGE et al.) 15 January 2002 (15.01.2002), see entire document.</td>
<td>1, 2, 7-9</td>
</tr>
</tbody>
</table>

Further documents are listed in the continuation of Box C.  See patent family annex.

Date of the actual completion of the international search
16 February 2007 (16.02.2007)

Date of mailing of the international search report
27 FEB 2007

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Form PCT/ISA/210 (second sheet) (April 2005)
Continuation of B. FIELDS SEARCHED Item 3:
EAST; US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
Search Term: wafer and burn-in with (overcurrent near protection)