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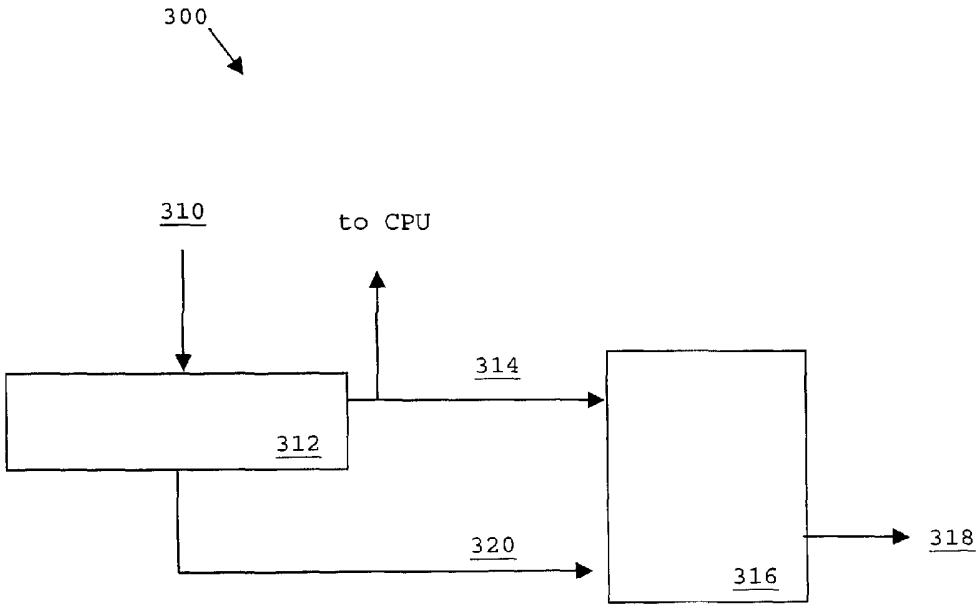
(54) Title: CLOCK ALIGN TECHNIQUE FOR EXCESSIVE STATIC PHASE OFFSET



(57) Abstract: A CPU clock signal (314) generated from a phase lock loop (PLL) circuit (312) and a feedback signal (320) of the PLL circuit (312) are used in generating a JBUS clock signal (318). The CPU clock signal (314) and the feedback signal (320) include the same amount of static phase offset introduced by the PLL circuit (312). The CPU clock signal (314) and the feedback signal (320) are input to an alignment detection circuit (316) and used in generating the JBUS clock signal (318). In one embodiment, the JBUS clock signal (318) is generated in synchronization with the CPU clock signal (314) and having the frequency of the feedback signal (320). The present invention reduces or eliminates misalignment of the leading edge of the JBUS clock signal (318) with reference to a specific leading edge of the CPU clock signal (314) due to the presence of static phase offset introduced by the PLL circuit (312).

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Declarations under Rule 4.17:

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F1/10 G06F1/12

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/199124 A1 (ADKISSON RICHARD W) 26 December 2002 (2002-12-26) paragraphs '0024! - '0038! figures 1-3	1-19
A	EP 0 735 494 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 2 October 1996 (1996-10-02) page 3, lines 3-41 figures 1,2	1,4,7, 11,14,18

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2002199124 A1	26-12-2002	NONE	
EP 0735494 A1	02-10-1996	US 5634116 A	27-05-1997
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