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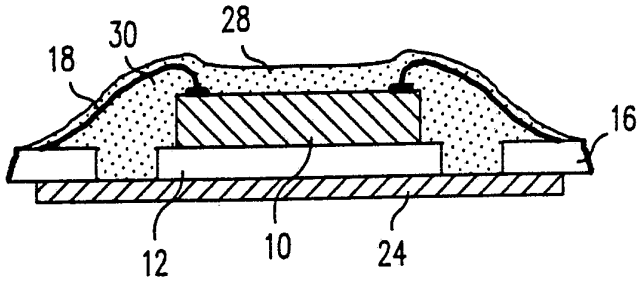
(54) Title: INTEGRATED CIRCUIT PACKAGE ASSEMBLY



(57) Abstract

An integrated circuit package assembly (22) includes a semiconductor chip (10) mounted on a die pad (12), having wire leads (18) attached to bond pads (20) on the chip and lead fingers (16) connected to the wire leads and external connections. A flexible and compressible tape (24) is attached to the bottom of the die pad and extends to the lead fingers to reduce stress and to minimize cracking of the package material that encloses the chip and the wire leads during vapor phase. An optional soft gel (28) is added to coat the chip surface including the bonds to further reduce chip surface stress.

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INTEGRATED CIRCUIT PACKAGE ASSEMBLY

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to an integrated circuit (IC) package assembly and in particular to a means for minimizing cracks that may form in the IC package during subsequent vapor phase reflow of the package to a system board.

Description of the Prior Art

During the assembly of semiconductor devices in plastic packages, the IC chips are mounted on rigid lead frames. After this "die-attach" process, the chip is bonded using gold wires. The wires connect from the bond pads on the IC chip to leads or bond fingers which are part of the lead frame. The whole die-attached and wire bonded chip configuration is encapsulated in thermoset epoxy plastic. After the encapsulation process the external leads are trimmed, formed and finished. During the manufacture of system subassemblies involving these surface mountable plastic IC packages, the packages are positioned on a printed circuit (PC) board which has solder paste spread on the active areas to enable the connection of the external formed leads to the printed circuit solder pads by solder reflow techniques.

For mass production of system subassemblies where rapid processing is desirable, vapor phase soldering using apparatus of the type shown schematically in FIG. 1 is preferably employed. With this process the PC board with the distributed solder paste and the IC packaged devices are lowered through a blanket vapor formed by condensing coils 1 into a vapor phase region 2, wherein the assembly 3 heats up to the vapor temperature. Dipping rack 4 and assembly 3 may

be in region 2 for about 15 minutes. Vapor phase soldering is achieved by use of electrical immersion heaters 5 which boils fluorinated fluid 6 to its boiling temperature of about 220°C - 225°C, whereby the solder paste reflows and makes the desired connections between the leads of the IC package and the circuit connections of the printed circuit board.

One major problem that is encountered as a result of moving the IC package assembly from an ambient environment to the vapor phase soldering environment which is at a relatively very high temperature is the formation of cracks in the epoxy plastic that encloses the IC device. These cracks may be either external or internal. The epoxy plastic is subject to the absorption of moisture through the bulk by diffusion process and along the leads or through cracks. The moisture may reside generally throughout the plastic body and in higher concentrations at surfaces with high surface energy such as at the chip and plastic interface. The equilibrium moisture level in the package is dependent on duration of storage of the package assemblies and the conditions under which storage occurs, and particularly on humidity level of the ambient.

During the vapor phase reflow soldering process, the entrapped moisture within the package is heated and vaporizes. The resulting water vapor is superheated, and provided enough moisture is present, the vapor attains the equilibrium vapor presence of steam at the soldering temperature. For example, at a temperature of about 224°C, the pressure of dry saturated steam would be about 25 bar absolute pressure or 367 pounds per square inch absolute. This level of pressure combined with regular thermomechanical stresses arising from the differences in expansion coefficient of the plastic chip and lead frame may give rise to cracking in the plastic material. When using the vapor phase technique for soldering IC package leads to the

printed circuit, cracks tend to form from the corners or edges of the supporting pad or IC die. If the cracks are thin and small, they are difficult to find.

During operation of a system incorporating a cracked component, the cracks would allow moisture to enter the package to the detriment of the integrated circuit. Furthermore the cracks can cause mechanical or physical damage so that the IC package becomes inoperable at the onset. As a result, the IC assembly production yield is decreased and field operation of assembled units with undetected cracks would be unreliable.

One solution is to bake the IC packages slowly at about 150°C for at least 16 hours to rid the package of moisture, for example. But the slow bake process does introduce a 16 hours long additional step to the board manufacture and is not economically feasible.

SUMMARY OF THE INVENTION

An object of this invention is to provide an improved IC assembly with minimal cracked IC packages after vapor phase reflow.

In accordance with this invention, a plastic package housing an IC assembly comprises an IC die having an integrated circuit chip mounted on a rigid frame. A flexible and compressible continuous tape is joined to the bottom surface of the lead frame that supports the IC die and to the leads or bond fingers extending from the IC die. The thin tape is preferably made of Kapton (trademark of DuPont) and has an adhesive backing for facile attachment to the IC die pad and the bond fingers. In one embodiment, a silicon gel is applied in addition as a coating over the wires, lead fingers and the IC die to absorb stress that may be applied to the IC package elements.

Description of the Drawings

The invention will be described in greater detail with reference to the drawings in which:

FIGURE 1 is a representation of a vapor phase soldering apparatus;

FIGURE 2 is a cut-away top view of an integrated circuit package assembly, incorporating the invention;

FIGURE 3 is side view of the integrated circuit package assembly illustrated in FIGURE 2; and

FIGURES 4A and 4B are sectional views of alternative embodiments of the integrated circuit package assembly illustrated in FIGURE 1.

Similar numerals refer to similar elements throughout the drawing.

Detailed Description of the Invention

With reference to FIGS. 2 an 3, an integrated circuit chip 10 is mounted on a die pad 12 that is an integral part of a lead frame, as is known in the prior art. Lead fingers 16 are joined to one end of wires 18, and the other ends of the wires are connected to bond pads 20 on the IC chip. The assembly of the bonded IC chip on the die pad is encapsulated in a plastic epoxy package 22. The outer portions of the leads 16B are trimmed and formed to shape for external connection to circuit traces on a board.

To minimize the problem of cracking of the package material, which may occur as a result of the vapor phase soldering process that is employed in the manufacture of some integrated circuit system subassemblies, a thin tape or film 24, preferably made of Kapton and having an adhesive backing, is attached to the bottom portions 16A of the lead fingers and to the bottom surface of the die pad. The tape is made as a continuous flexible piece that is compressible and has a thickness in the range of about .002-.005 inch, by way of example. The tape may be made of any material that

can withstand the high temperatures associated with the processing of the integrated circuit package assembly and the epoxy encapsulation process, provided that the tape has the characteristics of flexibility and compressibility.

In addition, to reduce stress on the bond wires 18, a protective coating 28, such as a soft gel, is placed over the bond wires and chip 10 prior to encapsulation, as shown in FIGS. 4A and 4B. The gel is supported by the continuous tape backing. In FIG. 4A, a full gel overcoat 30 is applied to encompass the wires 18 and the chip 10. In FIG. 4B, a partial gel overcoat 32 is applied over the surface of the chip and covers the bonds on the chip. The gel overcoat in each implementation is intended to absorb stresses that may appear as a consequence of the thermomechanical action of assembling the integrated circuit device with materials with different thermal properties.

By virtue of the flexible and compressible tape that is provided at the bottom of the die attach pad and which extends to the lead fingers, crack initiation and propagation are impeded, stresses and the transmission of forces arising from stresses in the IC package are significantly reduced. In particular, the flexible and compressible tape which is located to extend between the die attach pad and the lead fingers reduces the effect of stress concentration at "weak" points in the package assembly by blunting sharp radii, such as nicks and burrs. Also, the disclosed arrangement allows the application of full coverage of soft gel to the IC chip surface and wires without gel overflow to the backside during gel application. The application of soft gel further reduces stress at critical points in the package assembly, especially in packages incorporating relatively large dies.

CLAIMS

What is claimed is:

1. An integrated circuit package assembly comprising:

a lead frame comprising a die pad and lead fingers, said lead fingers having inner and outer portions;

an integrated circuit chip mounted to said die pad;

wires connecting said chip to the inner portions of said lead fingers;

an encapsulant enclosing the assembly of said integrated circuit chip and said die pad to form a package; and

a flexible and compressible continuous tape attached to the bottom of said die pad and to said lead fingers so that cracking of said encapsulant material is minimized.

2. An integrated circuit package as in Claim 1, including a silicon gel material for forming a stress absorbing coating on top of said IC die and said wires.

3. An integrated circuit package assembly as in Claim 2, wherein said silicon gel material encompasses the exposed surfaces of said chip, said die pad, said wires and lead fingers, said gel being supported by said continuous tape.

4. An integrated circuit package assembly as in Claim 2, wherein said silicon gel covers only the bond pads on a surface of said chip including the ends of the wire leads attached to said bond pads, and said surface of said chip.

5. An integrated circuit package assembly as in Claim 1, wherein said tape is made of Kapton having an adhesive backing for attachment to said die pad and said lead fingers.

6. An integrated circuit package assembly as in Claim 1, wherein said outer portions of the lead fingers extend from said package.

7. An integrated circuit package assembly as in Claim 1, wherein said encapsulant is made of an epoxy plastic material.

8. An integrated circuit package assembly as in Claim 1, further including a printed circuit board to which said packaged chip assembly is mounted for electrical connection.

9. An integrated circuit package assembly as in Claim 8, wherein said electrical connection is effectuated by vapor phase soldering.

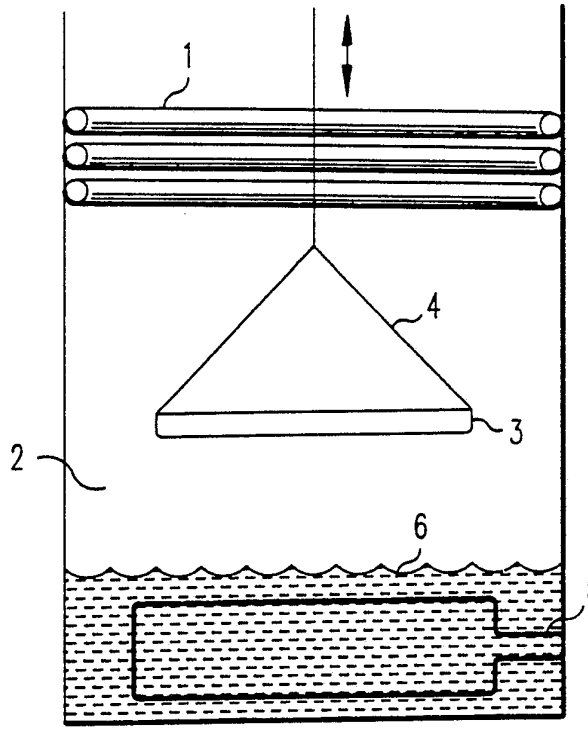

FIG. 1

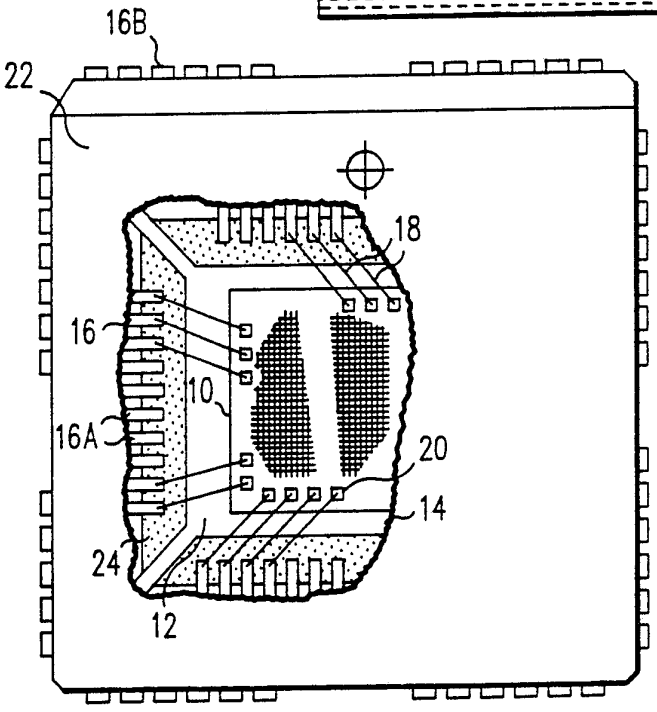

FIG. 2

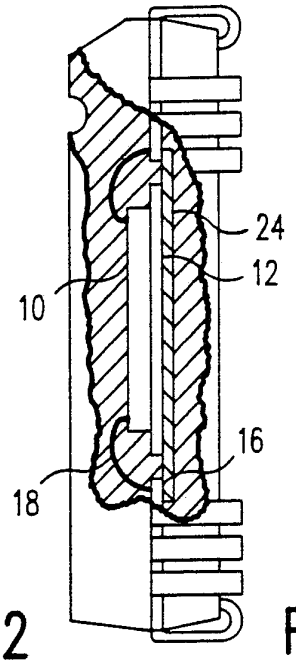

FIG. 3

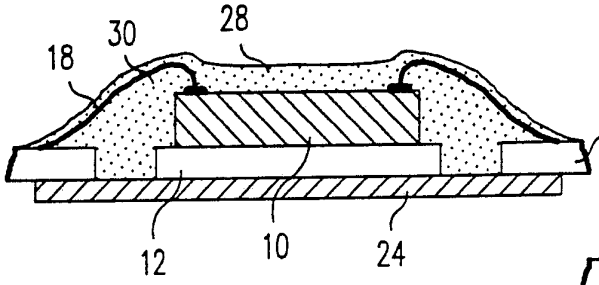

FIG. 4a

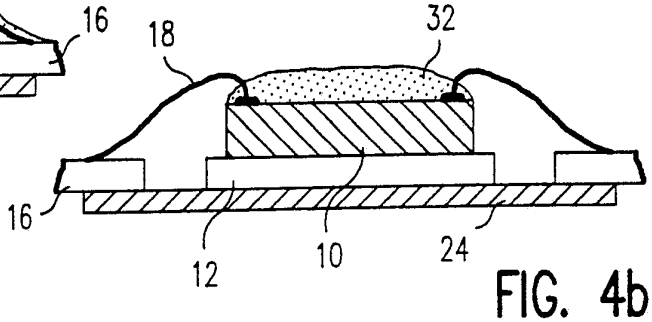

FIG. 4b

INTERNATIONAL SEARCH REPORT

International Application No PCT/US87/02363

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (4): H01 L23/30
US 357/72

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	174/52FP, 52PE; 357/72 361/398

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y,P	US, A, 4,649,415 (HERBERT) 10 March 1987 See the entire document.	1 to 9
Y	US, A, 4,558,510 (TANI) 17 December 1985 See the entire document.	1 to 9
Y	US, A, 4,480,150 (JONES) 30 October 1984 See the entire document.	1 to 9
Y	JA, A, 60-84854 (TAKEYYUMI) 14 May 1985 See the entire document.	1 to 9
Y	JA, A, 54-144872 (DENKI) 12 November 1979 See the entire document.	1 to 9
A	US, A, 3,440,027 (HUGLE) 22 April 1969 See the entire document.	1 to 9
A	US, A, 4,631,820 (HARADA) 30 December 1986 See the entire document.	1 to 9
A	US, A, 3,691,289 (ROHLOFF) 12 September 1972 See the entire document.	1 to 9

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
20 October 1987	25 NOV 1987
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	R. Kucia R. R. Kucia

Form PCT/ISA/210 (second sheet) (May 1986)

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A	US, A, 4,621,278 (MIURA) 04 November 1986 See the entire document.	1 to 9
A	GB, A, 2081,974 (HOPPE) 24 February 1982 See the entire document.	1 to 9

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers . ..., because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers....., because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.