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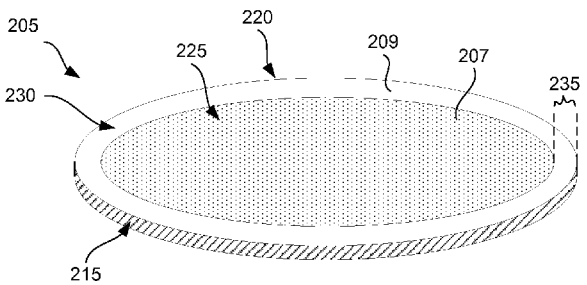


FIG. 2B

(57) Abstract: A protective cover for an electrostatic chuck may include a conductive wafer and a plasma resistant ceramic layer on at least one surface of the conductive wafer. The plasma resistant ceramic layer covers a top surface of the conductive wafer, side walls of the conductive wafer and an outer perimeter of a bottom surface of the conductive wafer. Alternatively, a protective cover for an electrostatic chuck may include a plasma resistant bulk sintered ceramic wafer and a conductive layer on a portion of a bottom surface of the plasma resistant bulk sintered ceramic wafer, wherein a perimeter of the bottom surface is not covered.

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PROTECTIVE COVER FOR ELECTROSTATIC CHUCK

TECHNICAL FIELD

[0001] Embodiments of the present invention relate to a protective cover for an electrostatic chuck that can protect an electrostatic chuck during a cleaning process.

BACKGROUND

[0002] Electrostatic chucks are used to support substrates during processing. One function of an electrostatic chuck is to regulate a temperature of the supported substrate. To facilitate such temperature regulation, a surface of the electrostatic chuck that supports the substrate includes multiple surface features including mesas and a sealing band around a perimeter of the surface. During processing, a heat conductive fluid such as helium gas is pumped into an interface between the electrostatic chuck and the supported substrate. The sealing band seals the interface between the electrostatic chuck and the suspended substrate, preventing the heat conductive fluid from escaping. Over time, processing and cleaning of the electrostatic chuck erodes the surface features such as the sealing band and mesas, increasing their roughness, reducing a height of the mesas, and introducing leakage pathways. This introduces or increases a leakage rate of the fluid.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like references indicate similar elements. It should be noted that different references to "an" or "one" embodiment in this disclosure are not necessarily to the same embodiment, and such references mean at least one.

[0004] FIG. 1 depicts a sectional view of one embodiment of a processing chamber including a protective cover on a substrate support assembly;

[0005] FIG. 2A depicts a top surface and side walls of one embodiment of a protective cover;

[0006] FIG. 2B depicts a bottom surface and side walls of one embodiment of a protective cover;

[0007] FIG. 2C depicts a cross sectional side view of one embodiment of a protective cover;

[0008] FIG. 3 depicts a cross sectional side view of another embodiment of a protective cover;

[0009] FIG. 4 depicts a cross sectional side view of yet another embodiment of a protective cover;

[0010] FIG. 5 depicts a cross sectional side view of still another embodiment of a protective cover;

[0011] FIG. 6A illustrates one embodiment of a process for manufacturing a protective cover for an electrostatic chuck;

[0012] FIG. 6B illustrates another embodiment of a process for manufacturing a protective cover for an electrostatic chuck;

[0013] FIG. 7 illustrates one embodiment of a process for cleaning a processing chamber using a protective cover for an electrostatic chuck.

DETAILED DESCRIPTION OF EMBODIMENTS

[0014] Described herein are embodiments of a protective cover for an electrostatic chuck. The protective cover is a wafer or other component that may be chucked by the electrostatic chuck during a cleaning process such as a plasma cleaning process. The protective cover may include a plasma resistant ceramic portion and a conductive portion. The conductive portion enables the protective cover to be secured (e.g., chucked) by the electrostatic chuck. The plasma resistant ceramic portion enables the protective cover to shield the electrostatic chuck from attack by corrosive chemistries of a plasma used in the plasma cleaning process. Alternatively, the protective cover may include a plasma resistant ceramic wafer that has been doped or otherwise treated to cause the plasma resistant ceramic wafer to have a resistivity of less than about 10^{13} Ohm-cm.

[0015] In one embodiment, a plasma resistant bulk sintered ceramic wafer is provided, and at least a portion of a bottom surface of the wafer is coated with a conductive layer such as silicon. In another embodiment, a conductive wafer (e.g., a silicon wafer or silicon carbide wafer) is provided, and a top surface, side walls and at least a portion of a bottom surface of the conductive wafer is coated with a plasma resistant ceramic layer.

[0016] An electrostatic chuck can be a costly chamber component for processing chambers. Embodiments of protective covers for electrostatic chucks described herein can prolong the lifespan of electrostatic chucks from about 100-200 radio frequency hours (RFHrs) for an allowed helium leak rate of 1.5 SCCM to up to about 5000 RFHrs. Accordingly, embodiments of protective covers described herein can prolong the life span of the electrostatic chucks up to about 20 times the life spans of traditional electrostatic chucks, thus providing cost savings for consumers of the electrostatic chucks.

[0017] FIG. 1 is a sectional view of one embodiment of a semiconductor processing chamber 100 having a substrate support assembly 148 disposed therein. The processing chamber 100 includes a chamber body 102 and a lid 104 that enclose an interior volume 106. The chamber body 102 may be fabricated from aluminum, stainless steel or other suitable material. The chamber body 102 generally includes sidewalls 108 and a bottom 110. An outer liner 116 may be disposed adjacent the side walls 108 to protect the chamber body 102. The outer liner 116

may be fabricated and/or coated with a plasma or halogen-containing gas resistant material. In one embodiment, the outer liner 116 is fabricated from aluminum oxide. In another embodiment, the outer liner 116 is fabricated from or coated with yttria, yttrium alloy or an oxide thereof.

[0018] An exhaust port 126 may be defined in the chamber body 102, and may couple the interior volume 106 to a pump system 128. The pump system 128 may include one or more pumps and throttle valves utilized to evacuate and regulate the pressure of the interior volume 106 of the processing chamber 100.

[0019] The lid 104 may be supported on the sidewall 108 of the chamber body 102. The lid 104 may be opened to allow access to the interior volume 106 of the processing chamber 100, and may provide a seal for the processing chamber 100 while closed. A gas panel 158 may be coupled to the processing chamber 100 to provide process and/or cleaning gases to the interior volume 106 through a gas distribution assembly 130 that is part of the lid 104. Examples of processing gases may be used to process in the processing chamber including halogen-containing gas, such as C_2F_6, SF_6, $SiCl_4$, HBr, NF_3, CF_4, CHF_3, CH_2F_3, Cl_2 and SiF_4, among others, and other gases such as O_2, or N_2O. Examples of carrier gases include N_2, He, Ar, and other gases inert to process gases (e.g., non-reactive gases). Examples of cleaning gases that may be used to clean components in the interior volume 106 include chlorine, fluorine, bromine, and other corrosive gases that are usable to produce a plasma suitable for cleaning.

[0020] The gas distribution assembly 130 may have multiple apertures 132 on the downstream surface of the gas distribution assembly 130 to direct the gas flow. Additionally, the gas distribution assembly 130 can have a center hole where gases are fed through a ceramic gas nozzle. The gas distribution assembly 130 may be fabricated and/or coated by a ceramic material, such as silicon carbide, yttria, etc. to provide resistance to halogen-containing chemistries to prevent the gas distribution assembly 130 from corrosion.

[0021] The substrate support assembly 148 is disposed in the interior volume 106 of the processing chamber 100 below the gas distribution assembly 130. The substrate support assembly 148 holds a substrate during processing, and may additionally hold a protective cover 144 during a cleaning process. An inner liner 118 may be coated on the periphery of the substrate support assembly 148. The inner liner 118 may be a halogen-containing gas resistant material such as those discussed with reference to the outer liner 116. In one embodiment, the inner liner 118 may be fabricated from the same materials of the outer liner 116.

[0022] In one embodiment, the substrate support assembly 148 includes a mounting plate 162 supporting a pedestal 152, and an electrostatic chuck 150. The electrostatic chuck 150 further includes a thermally conductive base 164 bonded to a ceramic body (referred to as an

electrostatic puck 166) via a bond 138. The electrostatic puck 166 may be fabricated by a ceramic material such as aluminum nitride (AlN) or aluminum oxide (Al_2O_3). The mounting plate 162 is coupled to the bottom 110 of the chamber body 102 and includes passages for routing utilities (e.g., fluids, power lines, sensor leads, etc.) to the thermally conductive base 164 and the electrostatic puck 166.

[0023] The thermally conductive base 164 and/or electrostatic puck 166 may include one or more optional embedded heating elements 176, embedded thermal isolators 174 and/or conduits 168, 170 to control a lateral temperature profile of the support assembly 148. The conduits 168, 170 may be fluidly coupled to a fluid source 172 that circulates a temperature regulating fluid through the conduits 168, 170. The embedded isolator 174 may be disposed between the conduits 168, 170 in one embodiment. The heater 176 is regulated by a heater power source 178. The conduits 168, 170 and heater 176 may be utilized to control the temperature of the thermally conductive base 164, thereby heating and/or cooling the electrostatic puck 166 and a substrate (e.g., a wafer) being processed. The temperature of the electrostatic puck 166 and the thermally conductive base 164 may be monitored using a plurality of temperature sensors 190, 192, which may be monitored using a controller 195.

[0024] The electrostatic puck 166 may further include multiple gas passages such as grooves, mesas and other surface features that may be formed in an upper surface of the puck 166. The gas passages may be fluidly coupled to a fluid source 172 of a thermally conductive gas, such as He via holes drilled in the puck 166. In operation, the gas may be provided at controlled pressure into the gas passages to enhance the heat transfer between the electrostatic puck 166 and a chucked substrate such as protective cover 144.

[0025] The electrostatic puck 166 includes at least one clamping electrode 180 controlled by a chucking power source 182. The electrode 180 (or other electrode disposed in the puck 166 or base 164) may further be coupled to one or more RF power sources 184, 186 through a matching circuit 188 for maintaining a plasma formed from process and/or other gases within the processing chamber 100. The sources 184, 186 are generally capable of producing RF signal having a frequency from about 50 kHz to about 3 GHz and a power of up to about 10,000 Watts.

[0026] The protective cover 144 may be a wafer or other component used to shield the electrostatic chuck 150 from a corrosive plasma during cleaning of the components in the interior volume 106. For example, the protective cover 144 may have a disc shape, a flat square shape, a flat rectangular shape, or other appropriate shape. The protective cover 144 may include a conductive portion that enables the protective cover 144 to be secured (chucked) by the electrostatic chuck 150 during the cleaning process. The protective cover 144 may additionally include a plasma resistant ceramic portion that is exposed to the corrosive plasma. The plasma

resistant ceramic portion may have a plasma erosion rate of less than approximately 10 nanometers (nm) per radio frequency hour (RFHr). As shown, the protective cover 144 may have a diameter that is slightly greater than a diameter of the electrostatic chuck 150. For example, the protective cover 144 may have a diameter that is about 1-5 mm greater than a diameter of the electrostatic chuck 150. Accordingly, the protective cover 144 may extend beyond the edge of the substrate support assembly 152. This may decrease the exposure of the substrate support assembly 152 to the corrosive plasma during the cleaning process.

[0027] FIGs. 2A-2C depict various views of one embodiment of a protective cover 205 for an electrostatic chuck. FIG. 2A depicts a top surface 210 and side walls 215 of the protective cover 205. FIG. 2B depicts a bottom surface 220 and side walls 215 of the protective cover 205. FIG. 2C depicts a cross sectional side view of the protective cover 205.

[0028] In one embodiment, the protective cover 205 has a shape that corresponds approximately to a shape of an electrostatic chuck that is to be protected. For example, a top of an electrostatic chuck may be circular, and the protective cover 205 may have a disc or wafer shape as shown. Alternatively, other shapes may be used for the protective cover 205. The protective cover 205 may include a solid bulk conductive wafer 207 at least partially coated by a plasma resistant ceramic layer 209.

[0029] The solid bulk conductive wafer 207 may be a silicon wafer, a silicon carbide wafer, a doped aluminum nitride wafer, a doped aluminum oxide wafer, or another type of conductive wafer. Doped aluminum oxide wafers and doped aluminum nitride wafers may be doped with samarium (Sm), cerium (Ce), or other rare earth metal to cause the wafers to have resistivity of less than about 10^{13} Ohm-cm. In one embodiment, the solid bulk conductive wafer 207 is a metal wafer such as an aluminum wafer. The wafer 207 may have a thickness of between about 100 microns to about 2 mm. Thicker wafers may have greater structural strength and greater rigidity. Thinner wafers may have a lower structural strength and greater flexibility.

[0030] The plasma resistant ceramic layer 209 is a deposited or grown layer. The plasma resistant ceramic layer 209 may be a ceramic such as Y_2O_3 (yttria or yttrium oxide), $Y_4Al_2O_9$ (YAM), Al_2O_3 (alumina), $Y_3Al_5O_{12}$ (YAG), YAlO3 (YAP), Quartz, Si_3N_4 (silicon nitride), AlN (aluminum nitride), AlON (aluminum oxynitride), TiO_2 (titania), ZrO_2 (zirconia), TiC (titanium carbide), ZrC (zirconium carbide), TiN (titanium nitride), TiCN (titanium carbon nitride), Y_2O_3 stabilized ZrO_2 (YSZ), and so on. The plasma resistant ceramic layer 209 may also be a ceramic composite such as $Y_3Al_5O_{12}$ distributed in Al_2O_3 matrix, Y_2O_3-ZrO_2 solid solution or a SiC-Si_3N_4 solid solution. The plasma resistant ceramic layer 209 may also be a ceramic composite that includes a yttrium oxide (also known as yttria and Y_2O_3) containing solid solution. For example, the plasma resistant ceramic layer 209 may be a ceramic composite that is composed of

a compound $Y_4Al_2O_9$ (YAM) and a solid solution Y_2-xZr_xO_3 (Y_2O_3-ZrO_2 solid solution). Note that pure yttrium oxide as well as yttrium oxide containing solid solutions may be doped with one or more of ZrO_2, Al_2O_3, SiO_2, B_2O_3, Er_2O_3, Nd_2O_3, Nb_2O_5, CeO_2, Sm_2O_3, Yb_2O_3, or other oxides.

[0031] In one embodiment, the plasma resistant ceramic layer 209 is a composite ceramic coating composed of a compound $Y_4Al_2O_9$ (YAM) and a solid solution Y_2-xZr_xO_3 (Y_2O_3-ZrO_2 solid solution). In a further embodiment, the plasma resistant ceramic layer includes 62.93 mol% Y_2O_3, 23.23 mol% ZrO_2 and 13.94 mol% Al_2O_3. In another embodiment, the plasma resistant ceramic layer can include Y_2O_3 in a range of 50-75 mol%, ZrO_2 in a range of 10-30 mol% and Al_2O_3 in a range of 10-30 mol%. In other embodiments, other distributions may also be used for the composite ceramic coating. In one embodiment, the composite ceramic is a yttrium oxide containing solid solution that may be mixed with one or more of ZrO_2, Al_2O_3, or combination thereof.

[0032] In one embodiment, the plasma resistant ceramic layer 209 is yttrium aluminum garnet (YAG) composed of 35 mol% Y_2O_3, 65 mol% Al_2O_3. In another embodiment, the plasma resistant ceramic layer 209 can be YAG composed of 30-40 mol% Y_2O_3 and 60-70 mol% Al_2O_3.

[0033] The exterior top surface 210 and side walls 215 of the protective cover 205 are composed of the plasma resistant ceramic layer 209. The bottom surface 220 of the protective cover includes an inner region 225 made up of the solid bulk conductive wafer 207 and an outer perimeter 230 made up of the plasma resistant ceramic layer 209. A width 235 of the outer perimeter 230 may be approximately 3-5 microns. Alternatively, the width 235 may be greater, such as up to 10 or 20 microns. In a further embodiment, the width 235 may be up to about 1-5 millimeters.

[0034] Some plasma resistant ceramic materials may have a hardness that is lower than a hardness of the conductive wafer. Due to the lower hardness, the plasma resistant ceramic coating could wear out and introduce particle contamination if the plasma resistant ceramic coating were to rest on the electrostatic chuck. Accordingly, in one embodiment, the inner region 225 has a diameter that matches or is greater than diameter of an electrostatic chuck that is to be protected. The width 235 may be sufficient to span up to the distance between the outer edge of the protective cover 205 and the electrostatic chuck when the protective cover is chucked. Accordingly, the uncoated inner region 225 and not the outer perimeter 230 makes contact with (e.g., rests on) the electrostatic chuck while the protective cover is chucked.

[0035] The plasma resistant ceramic layer 209 on the top surface 210 may have a thickness of about 3-20 microns (with a thickness of about 5-10 microns in one embodiment). The plasma resistant ceramic layer 209 on the side walls 215 may have a thickness that approximately

matches the thickness of the plasma resistant ceramic layer 209 on the top surface 210. The plasma resistant ceramic layer 209 on the bottom surface may have a thickness of between about 2 microns and about 20 microns.

[0036] In one embodiment, in which the conductive wafer 207 has a thickness of greater than about 200 microns, the conductive wafer 207 is a rigid structure. In one embodiment, the wafer has a thickness of about 200 microns to 2 mm. Deposition of the plasma resistant ceramic layer 209 on the top surface 210 may introduce strain, which can cause the conductive wafer 207 (and thus the protective cover 205) to bow or cup. As the bow of the protective cover 205 increases, the ability of an electrostatic chuck to secure the protective cover 205 decreases. A bow of about 300 microns or more (or 200 microns or more in some embodiments) may prevent an electrostatic chuck from chucking the protective cover 205.

[0037] The thickness of the plasma resistant ceramic layer 209 on the bottom surface 220 may be selected to counteract bowing of the conductive wafer caused by the plasma resistant ceramic layer 209 on the top surface 210. Because less of the bottom surface 220 is covered, a thickness of the plasma resistant ceramic layer 209 on the bottom surface 220 may be thicker than a thickness of the plasma resistant ceramic layer 209 on the top surface 210. For example, the plasma resistant ceramic layer 209 on the bottom surface may have a thickness of 10-20 microns to counteract stress introduced by a 3-5 micron layer on the top surface 210.

[0038] In one embodiment, in which the conductive wafer 207 has a thickness of less than about 200 microns, the conductive wafer 207 is a flexible structure. For example, the conductive wafer may have a thickness of about 50-200 microns in one embodiment. If the conductive wafer 207 is a flexible structure, it can be pulled flat by the electrostatic chuck during chucking with relative ease. Accordingly, the protective cover 205 can be chucked successfully even if it has a curvature of greater than 300 microns.

[0039] As mentioned, the curvature of the conductive wafer 207 may be of reduced importance if the conductive wafer 207 is flexible. Additionally, the bottom surface 220 of the protective cover 205 may be ground flat after deposition of the plasma resistant ceramic layer 209. In either instance, a thickness of the plasma resistant ceramic layer 209 on the bottom surface 220 may be the same as or lower than the thickness of the plasma resistant ceramic layer 209 on the top surface 210. A lower thickness on the bottom surface 220 is acceptable because the bottom surface will not be in a direct line of sight of a produced plasma. Accordingly, wear on the bottom surface 220 will be less than wear on the top surface 210. The thickness of the plasma resistant ceramic layer on the bottom surface 220 may therefore be less than 5 microns (e.g., 1-3 microns in one embodiment).

[0040] FIGs. 3-5 illustrate cross sectional side views of various embodiments for protective covers. FIG. 3 depicts a cross sectional side view of a protective cover 305 having a conductive wafer 307 completely coated on a top surface 310, side walls 315 and bottom surface 320 by a plasma resistant ceramic layer 309. Some plasma resistant ceramics such as YAG have a high hardness and will not wear out due to contact with an electrostatic chuck. If such plasma resistant ceramic materials are used, then prolonged contact of the plasma resistant ceramic layer 309 to the electrostatic chuck should not introduce particle contamination. In one embodiment, the plasma resistant ceramic layer 309 has an approximately uniform thickness of up to about 5 microns on the top surface 410, the bottom surface 420 and the side walls 415.

[0041] FIG. 4 depicts a cross sectional side view of a protective cover 405 composed of a plasma resistant bulk sintered ceramic wafer 407 with a conductive layer 409 deposited thereon. The plasma resistant bulk sintered ceramic wafer 407 may include any of the aforementioned species of ceramics. However, the previously discussed ceramics were deposited ceramics, whereas the ceramic wafer 407 is a bulk sintered ceramic. Alternatively, the plasma resistant ceramic wafer may be a sapphire or MgAlON wafer. The ceramic wafer 407 may have a thickness of about 1-3 mm. The plasma resistant ceramic wafer may have a plasma erosion rate for the plasma environments that it will be used in of less than about 10 nm/RFHr.

[0042] As shown, a top surface 410 and side walls 415 of the plasma resistant bulk sintered ceramic wafer 407 are not coated by the conductive layer 409. Additionally, an outer perimeter 430 of the bottom surface 420 of the ceramic wafer 407 is not covered by the conductive layer 409. Since the conductive layer 409 may not be plasma resistant, leaving the outer perimeter 430 of the ceramic wafer 407 uncoated may prevent corrosion of the conductive layer 409. A width 435 of the uncoated outer perimeter 430 may be about 3-5 microns in one embodiment or up about 5 mm in another embodiment. A coated inner region 425 that is covered by the conductive layer 409 may have a diameter that corresponds to an outer diameter of a top of an electrostatic chuck that the protective cover 405 will be used on. Alternatively, the coated inner region 425 may have a diameter that is larger or smaller than the diameter of the electrostatic chuck.

[0043] Note that in some embodiments, the plasma resistant ceramic wafer may be doped or otherwise treated to cause the plasma resistant ceramic wafer itself to have a resistivity of less than about 10^{13} Ohm-cm. This may enable the plasma resistant ceramic wafer to be chucked by an electrostatic chuck without coating any surface of the plasma resistant ceramic wafer using a conductive layer. For example, a YAG plasma resistant ceramic wafer may be heat treated to control a defect density in the wafer. The defect density may control a resistivity of the YAG wafer. The heat treatment may be performed during sintering of the ceramic wafer. Sintering

parameters that may be adjusted during the sintering of the YAG wafer to control defect density include a sintering temperature, a time add temperature and a gas atmosphere (e.g., a ratio of oxygen to other chamber gases).

[0044] Materials such as aluminum nitride and aluminum oxide may be plasma resistant for some plasma environments but not others. For example, aluminum nitride may be plasma resistant for oxygen or nitrogen based plasmas, but may not be plasma resistant for fluorine based plasmas. If an aluminum nitride wafer is to be used in a plasma environment with nitrogen or oxygen based plasmas, then the aluminum nitride wafer may be doped to lower a resistivity of the aluminum nitride wafer to below about 10^{13} Ohm-cm. In such an instance, the aluminum nitride wafer would operate as both a plasma resistant ceramic wafer and as a conductive wafer. Dopant materials used to reduce the resistivity of the aluminum oxide or aluminum nitride wafers include cerium, samarium, or other rare earth metals.

[0045] FIG. 5 depicts a cross sectional side view of a protective cover 505 composed of a plasma resistant bulk sintered ceramic wafer 507 with a conductive layer 509 deposited thereon. Similar to the protective cover 405, in protective cover 505 a top surface 510 and side walls 515 of the plasma resistant bulk sintered ceramic wafer 507 are not coated by the conductive layer 509. Additionally, an outer perimeter 530 of the bottom surface 520 of the ceramic wafer 507 is not covered by the conductive layer 509.

[0046] As illustrated, the ceramic wafer 507 has a non-planar bottom surface 520. Specifically, the bottom surface 520 of the ceramic wafer 507 has a raised edge or outer perimeter 530. The raised outer perimeter may have a width 535 of about 3 mm to about 10 mm (e.g., about 5 mm in one embodiment), and may have a height of about 3-30 microns. The raised outer perimeter 530 may be produced by removing material from an inner region 525 of the bottom surface 520, such as by grinding or etching. The raised outer perimeter 530 may protect the conductive layer 509 from exposure to plasma during a cleaning process.

[0047] FIG. 6A illustrates one embodiment of a process 600 for manufacturing a protective cover for an electrostatic chuck. At block 602 of process 600, a conductive wafer such as a silicon wafer or a silicon carbide wafer is provided. At block 605, a top surface and side walls of the conductive wafer are coated with a plasma resistant ceramic layer. The plasma resistant ceramic layer may be deposited by traditional atmospheric plasma spray, low pressure plasma spray (LP PS), vacuum plasma spray (VPS), physical vapor deposition (PVD), chemical vapor deposition (CVD), ion assisted deposition (IAD), immersion coating, sputtering, thermal spraying, hot isostatic pressing, cold isostatic pressing, lamination, compression molding, casting, compacting, sintering or co-sintering techniques. In one embodiment, plasma resistant

ceramic layer is plasma sprayed onto the conductive wafer. In another embodiment, the plasma resistant ceramic layer is deposited on the conductive wafer using ion assisted deposition (IAD).

[0048] At block 610, an inner region of a bottom surface of the conductive wafer is masked, leaving exposed an outer perimeter of the conductive wafer. At block 615, the bottom surface of the conductive wafer is coated with the plasma resistant ceramic. At block 620, the mask is removed. Since the inner region of the bottom surface was covered by the mask, the inner region remains uncoated.

[0049] After deposition of the plasma resistant ceramic layer on the top surface, side walls and bottom surface, introduced stresses may cause the conductive wafer to bow. Accordingly, at block 625 the inner region of the bottom surface may be ground to a specified flatness. A platen that is approximately the size of the inner region may be used to flatten the inner region without disturbing the coated outer perimeter on the bottom surface. In one embodiment, the inner region is ground to a flatness of 200 microns or better (in which a highest area of a surface of the wafer is at most 200 microns higher than a lowest area of the surface). A flatness of 200 microns may also be referred to as a bow or curvature of 200 microns. In another embodiment, the inner region may be ground to a flatness of 50 microns or flatter. For example, silicon carbide is very rigid. Accordingly, a specified flatness of 50 microns may be used for silicon carbide wafers.

[0050] FIG. 6B illustrates another embodiment of a process 650 for manufacturing a protective cover for an electrostatic chuck. At block 655 of process 650, a plasma resistant bulk sintered ceramic wafer is provided. In one embodiment, at block 660 an inner region of a bottom surface of the ceramic wafer is ground. Grinding of the inner region may cause the outer perimeter of the bottom surface to be raised. Alternatively, the operations of block 660 may be skipped.

[0051] At block 670, the outer perimeter of the bottom surface is masked, leaving the inner region exposed. In one embodiment, the exposed inner region corresponds to the region that was ground at block 660. At block 675, the bottom surface of the ceramic wafer is coated with a conductive layer. Sputtering, plasma spraying, CVD, PVD, IAD, or other deposition techniques may be used to form the conductive layer. At block 680, the mask is removed. Since the mask covered the outer perimeter of the bottom surface, the outer perimeter may be uncoated by the conductive layer.

[0052] FIG. 7 illustrates one embodiment of a process 750 for cleaning a processing chamber using a protective cover for an electrostatic chuck. Process 750 may be performed between uses of the process chamber. For example, process 750 may be performed after a process is complete to clean the processing chamber and prepare it for a next process.

[0053] At block 752 of process 750 a robotic arm retrieves a protective cover from a storage area. The storage area may be a wafer transfer area or may be a dedicated storage area in or attached to the processing chamber. The dedicated storage area may hold one or a few protective covers, and may have a shield that is lowered to retrieve and return the protective covered, and that is raised prior to processing or cleaning.

[0054] At block 755, the protective cover is positioned onto an electrostatic chuck by the robotic arm. At block 760, a bias is applied to the electrostatic chuck to secure or chuck the protective cover. The protective cover may not have a flat backside. For example, the backside (bottom surface) may have a curvature of up to about 300 microns. In such an instance, a short duration pulse is applied initially. The short duration pulse is a high voltage bias (approximately 1.5 times a standard chucking bias) that shocks the protective cover, forcing the protective cover flat. After the short duration pulse, a voltage used for the bias may be reduced to the standard chucking bias, which is typically about 1800V for a coulombic electrostatic chuck. The short duration pulse enables a protective cover with a curvature of up to about 300 microns to be chucked.

[0055] At block 765, a plasma cleaning process is performed at up to about 1300 Watt power for less than 60 seconds. A typical plasma cleaning process is performed at around 1500 Watt power to minimize corrosion of an electrostatic chuck due to the cleaning. However, use of the protective cover enables the power to be increased up to about two times the standard power. By increasing the power, an effectiveness of the cleaning process is improved. As a result, the cleaning may reduce or remove a vertical wall buildup of material on a sidewall of the electrostatic chuck. Additionally, the improved cleaning process may extend an amount of time between scheduled maintenance cleanings up to about 600 radio frequency hours (RFHrs). Moreover, a duration of the cleaning process may be reduced from a typical cleaning time of 90 seconds down to below 60 seconds, and in one embodiment down to about 30 seconds. The reduced duration may improve cycle times for process chambers. At block 770, the protective cover is returned to the storage area, and the process chamber may be used for subsequent processing of wafers.

[0056] The preceding description sets forth numerous specific details such as examples of specific systems, components, methods, and so forth, in order to provide a good understanding of several embodiments of the present invention. It will be apparent to one skilled in the art, however, that at least some embodiments of the present invention may be practiced without these specific details. In other instances, well-known components or methods are not described in detail or are presented in simple block diagram format in order to avoid unnecessarily obscuring the present invention. Thus, the specific details set forth are merely exemplary.

Particular implementations may vary from these exemplary details and still be contemplated to be within the scope of the present invention.

[0057] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, the appearances of the phrase "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. In addition, the term "or" is intended to mean an inclusive "or" rather than an exclusive "or." When the term "about" or "approximately" is used herein, this is intended to mean that the nominal value presented is precise within ±25%.

[0058] Although the operations of the methods herein are shown and described in a particular order, the order of the operations of each method may be altered so that certain operations may be performed in an inverse order or so that certain operation may be performed, at least in part, concurrently with other operations. In another embodiment, instructions or sub-operations of distinct operations may be in an intermittent and/or alternating manner.

[0059] It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reading and understanding the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

CLAIMS

What is claimed is:

1. A protective cover for an electrostatic chuck comprising:

a wafer, wherein the wafer is one of a) a conductive wafer having a resistivity of less than approximately 10^{13} Ohm-cm or b) a plasma resistant bulk sintered ceramic wafer; and

a coating on at least one surface of the wafer, wherein the coating comprises one of a) a plasma resistant ceramic layer on at least one surface of the conductive wafer or b) a conductive layer on a portion of a bottom surface of the plasma resistant bulk sintered ceramic wafer.

2. The protective cover of claim 1, wherein the protective cover comprises the conductive wafer having the resistivity of less than approximately 10^{13} Ohm-cm and the plasma resistant ceramic layer on the at least one surface of the conductive wafer.

3. The protective cover of claim 2, wherein the plasma resistant ceramic layer covers a top surface of the conductive wafer, side walls of the conductive wafer and an outer perimeter of a bottom surface of the conductive wafer.

4. The protective cover of claim 3, wherein:

the conductive wafer has a thickness of approximately 50 microns to approximately 2 millimeters;

the ceramic layer on the top surface has a thickness of approximately 5-10 microns; and;

the ceramic layer on the side walls has a thickness of approximately 5-10 microns.

5. The protective cover of claim 4, wherein:

an uncoated portion of the bottom surface of the conductive wafer has post polish curvature of less than approximately 300 microns.

6. The protective cover of claim 4, wherein:

the outer perimeter of the bottom surface covered by the plasma resistant ceramic layer extends approximately 3-5 millimeters inward from an edge of the conductive wafer; and

the ceramic layer on the perimeter of the bottom surface has a thickness of approximately 10-20 microns, wherein the ceramic layer on the perimeter of the bottom surface counteracts curvature of the conductive wafer caused by the ceramic layer on the top surface.

7. The protective cover of claim 3, wherein:

the conductive wafer is a flexible wafer having a thickness of less than approximately 200 microns;

the ceramic layer on the top surface has a thickness of approximately 5-10 microns;

the ceramic layer on the side walls has a thickness of approximately 5-10 microns; and

the ceramic layer on the perimeter of the bottom surface has a thickness of less than approximately 5 microns.

8. The protective cover of claim 2, wherein the plasma resistant ceramic layer covers a top surface of the conductive wafer, side walls of the conductive wafer and a bottom surface of the conductive wafer, the plasma resistant layer having an approximately uniform thickness of 3-10 microns.

9. The protective cover of claim 2, wherein:

the conductive wafer comprises at least one of silicon, silicon carbide, doped aluminum nitride or doped aluminum oxide; and

the plasma resistant ceramic layer comprises at least one of $Y_3Al_5O_{12}$ or a ceramic compound comprising $Y_4Al_2O_9$ and a solid-solution of Y_2O_3-ZrO_2.

10. The protective cover of claim 2, wherein the bottom surface of the conductive wafer comprises a raised edge, and wherein the plasma resistant ceramic layer covers the raised edge.

11. The protective cover of claim 2, further comprising:

the plasma resistant bulk sintered ceramic wafer; and

the conductive layer on the portion of a bottom surface of the plasma resistant bulk sintered ceramic wafer, wherein a perimeter of the bottom surface is not covered.

12. The protective cover of claim 11, wherein the bottom surface of the plasma resistant bulk sintered ceramic wafer comprises a raised edge, and wherein the raised edge is not covered by the conductive layer.

13. The protective cover of claim 11, wherein:

the conductive layer comprises at least one of silicon or silicon carbide; and

the plasma resistant bulk sintered ceramic wafer comprises at least one of $Y_3Al_5O_{12}$ or a ceramic compound comprising $Y_4Al_2O_9$ and a solid-solution of Y_2O_3-ZrO_2.

14. A method of manufacturing a protective cover for an electrostatic chuck comprising:

providing a conductive wafer;

coating a top surface and side walls of the conductive wafer with a plasma resistant ceramic;

masking an inner region of a bottom surface of the conductive wafer, wherein an outer perimeter of the conductive wafer is left exposed;

coating the bottom surface with the plasma resistant ceramic, wherein the masked inner region of the bottom surface is uncoated; and

removing the mask.

15. The method of claim 14, further comprising:

grinding the inner region of the bottom surface to a flatness of at least 300 microns.

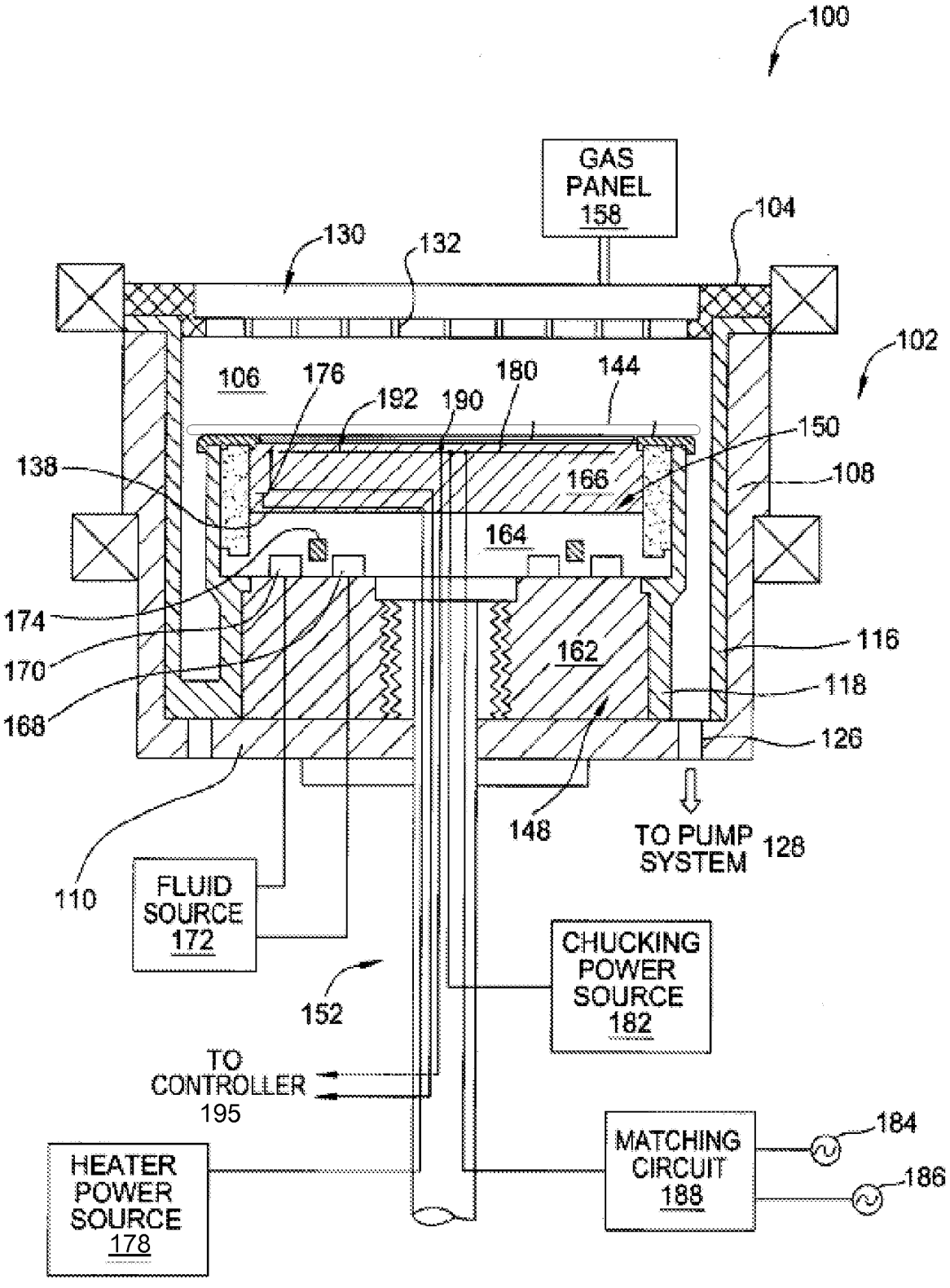

100
GAS PANEL 158
104
130
132
102
106
176
192
190
180
144
150
138
166
108
164
174
170
168
162
116
118
126
148
TO PUMP SYSTEM 128
110
FLUID SOURCE 172
CHUCKING POWER SOURCE 182
152
TO CONTROLLER 195
HEATER POWER SOURCE 178
MATCHING CIRCUIT 188
184
186

FIG. 1

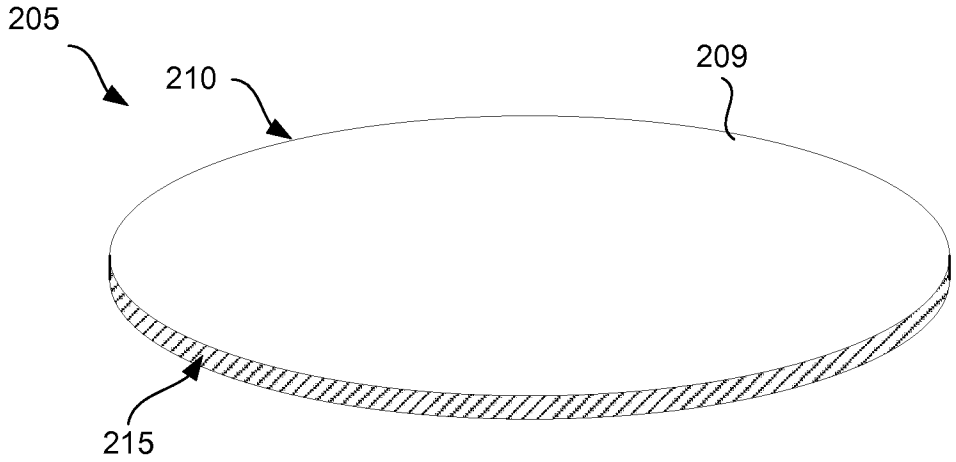


FIG. 2A

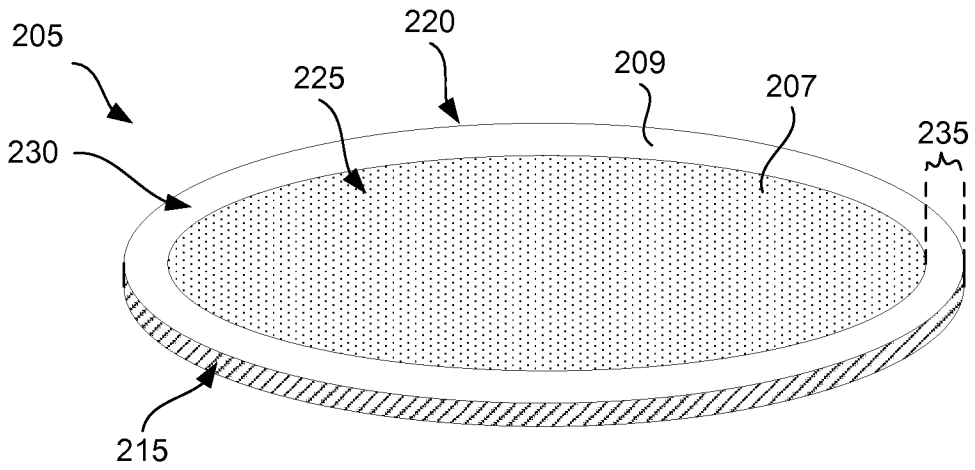


FIG. 2B

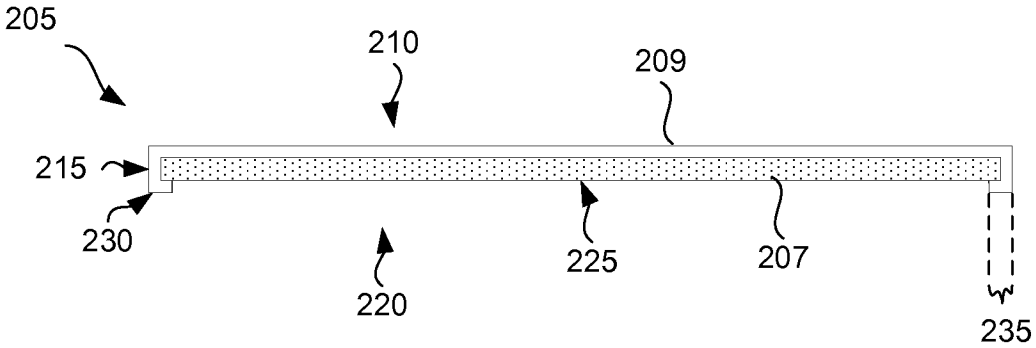


FIG. 2C

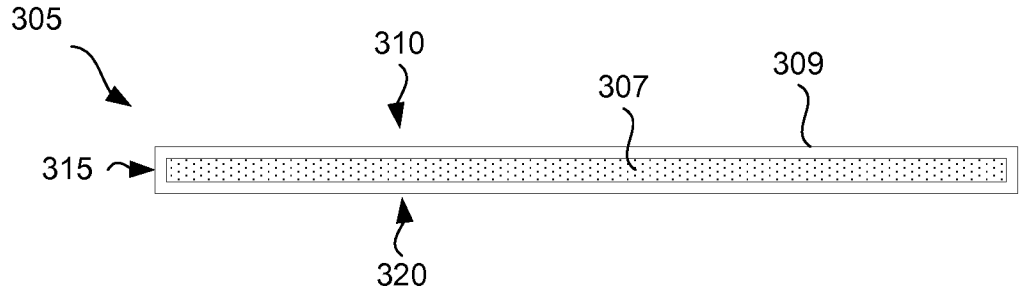


FIG. 3

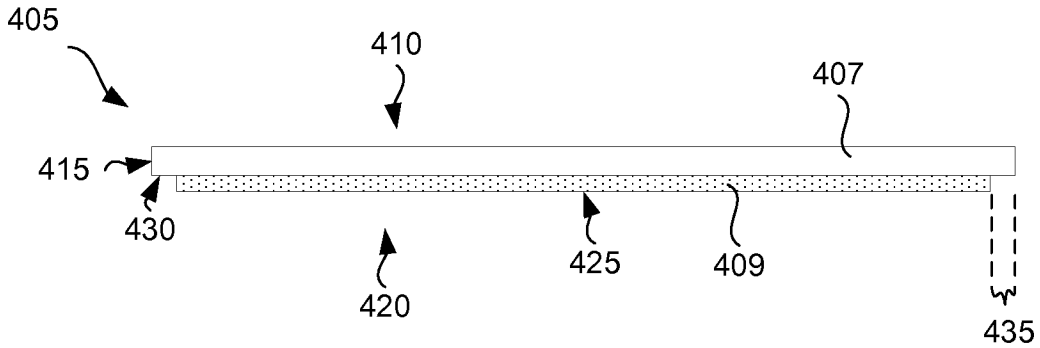


FIG. 4

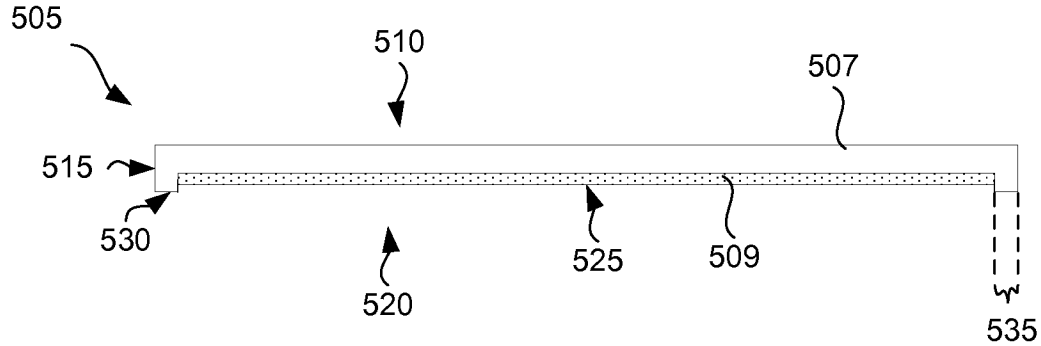


FIG. 5

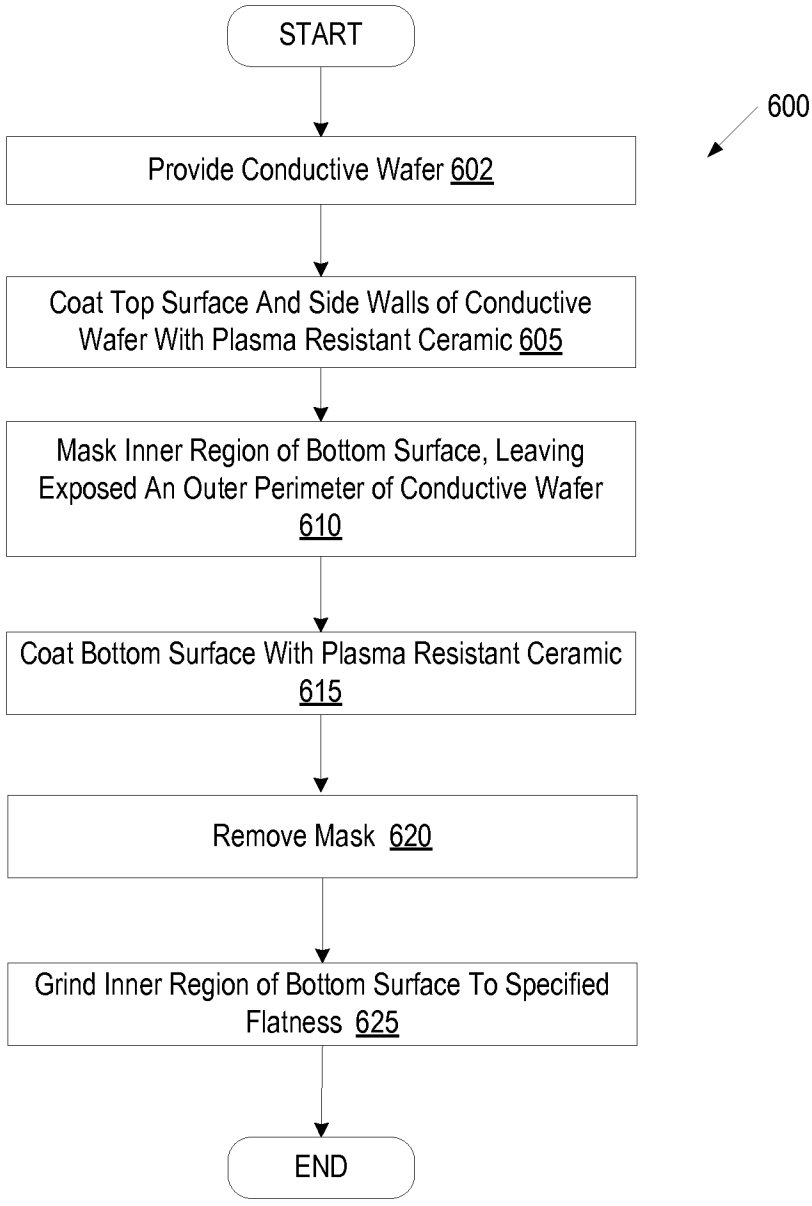

START
600
Provide Conductive Wafer 602
Coat Top Surface And Side Walls of Conductive Wafer With Plasma Resistant Ceramic 605
Mask Inner Region of Bottom Surface, Leaving Exposed An Outer Perimeter of Conductive Wafer 610
Coat Bottom Surface With Plasma Resistant Ceramic 615
Remove Mask 620
Grind Inner Region of Bottom Surface To Specified Flatness 625
END

FIG. 6A

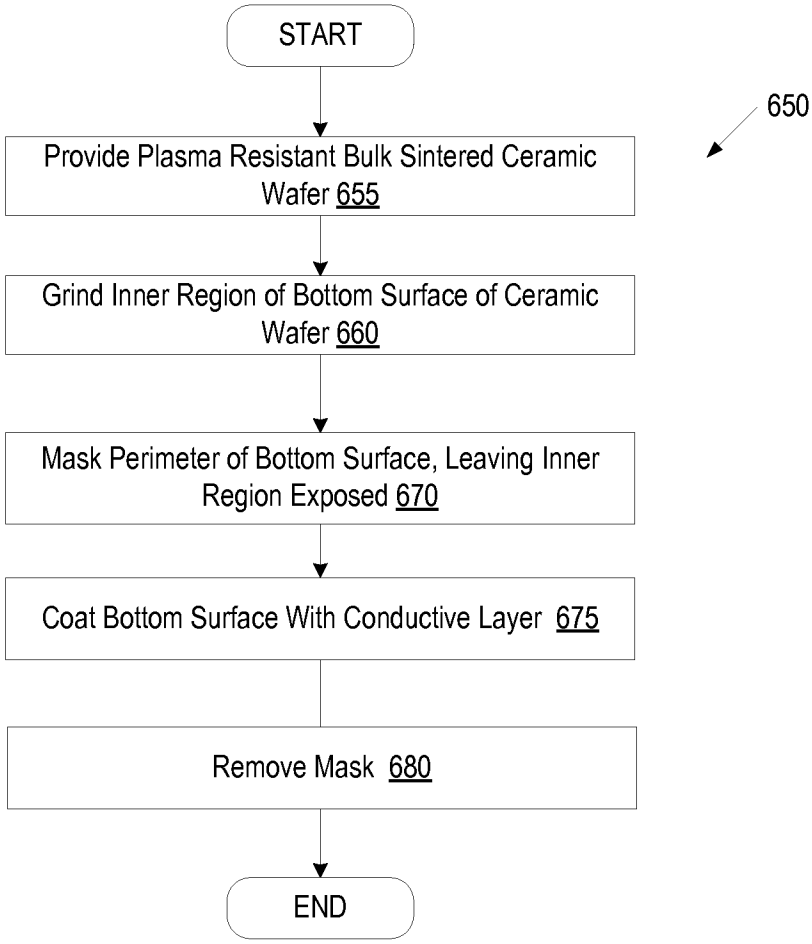

START
650
Provide Plasma Resistant Bulk Sintered Ceramic Wafer 655
Grind Inner Region of Bottom Surface of Ceramic Wafer 660
Mask Perimeter of Bottom Surface, Leaving Inner Region Exposed 670
Coat Bottom Surface With Conductive Layer 675
Remove Mask 680
END

FIG. 6B

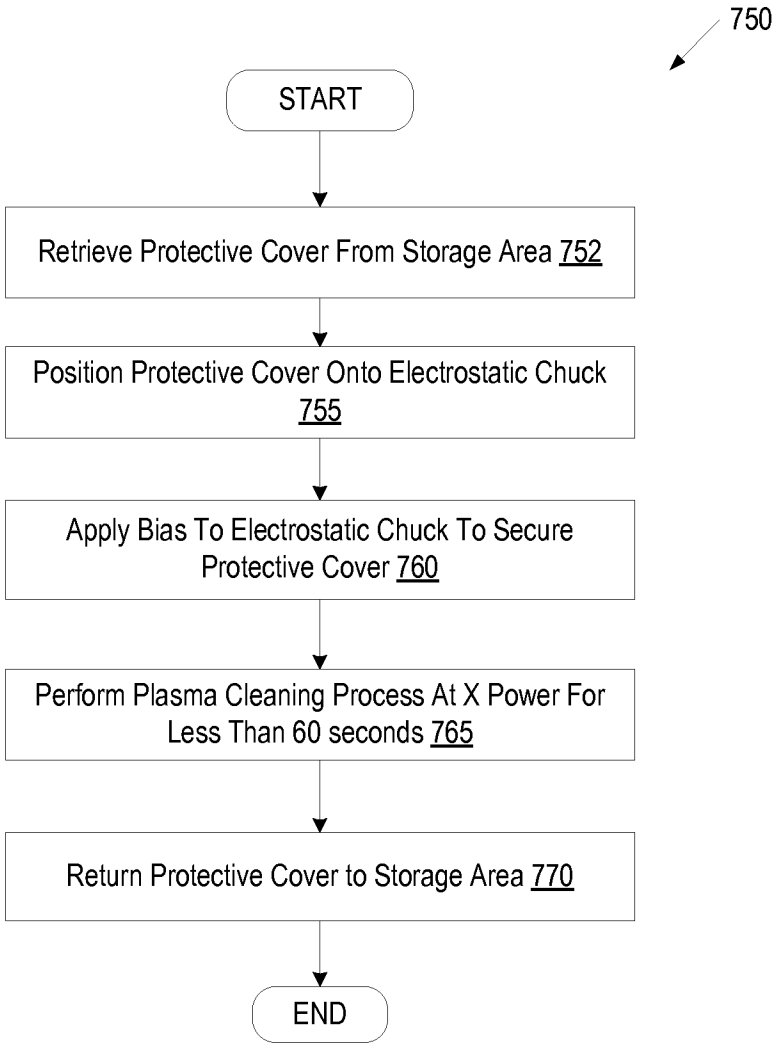

750
START
Retrieve Protective Cover From Storage Area 752
Position Protective Cover Onto Electrostatic Chuck 755
Apply Bias To Electrostatic Chuck To Secure Protective Cover 760
Perform Plasma Cleaning Process At X Power For Less Than 60 seconds 765
Return Protective Cover to Storage Area 770
END

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/035039

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/687(2006.01)i, H02N 13/00(2006.01)i, B23Q 3/15(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/687; H01L 21/68; H01L 21/3065; H02N 13/00; B05D 5/00; H01L 21/205; B32B 15/04; B32B 17/06; H01L 21/683; B23Q 3/15

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: protective cover, electrostatic chuck, conductive wafer, resistivity, plasma resistant, and coating

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010-0119843 A1 (SUN et al.) 13 May 2010 See abstract; paragraphs [0034],[0040]; and figure 4A.	1-15
A	JP 2000-306986 A (NIPPON ENGINEERING K.K. et al.) 02 November 2000 See abstract; claims 1-2, and figure 1.	1-15
A	JP 2008-016709 A (SHINKO ELECTRIC IND. CO., LTD.) 24 January 2008 See paragraphs [0012]-[0020]; and figure 1.	1-15
A	US 2012-0141661 A1 (CHO et al.) 07 June 2012 See abstract; claim 1, and figure 1.	1-15
A	JP 2001-308075 A (TOSHIBA CERAMICS CO., LTD.) 02 November 2001 See paragraph [0046]; and figure 3.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 August 2014 (25.08.2014)	**25 August 2014 (25.08.2014)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2014/035039

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0119843 A1	13/05/2010	CN 102210196 A	05/10/2011
		CN 102210196 B	25/06/2014
		JP 2012-508467 A	05/04/2012
		KR 10-1309716 B1	17/09/2013
		KR 10-2011-0091759 A	12/08/2011
		TW 201030891 A	16/08/2010
		TW I389248 B	11/03/2013
		TW I389248 I	11/03/2013
		US 8206829 B2	26/06/2012
		WO 2010-054112 A2	14/05/2010
		WO 2010-054112 A3	29/07/2010
JP 2000-306986 A	02/11/2000	None	
JP 2008-016709 A	24/01/2008	None	
US 2012-0141661 A1	07/06/2012	TW 201209957 A	01/03/2012
		US 8619406 B2	31/12/2013
		WO 2011-150311 A1	01/12/2011
JP 2001-308075 A	02/11/2001	None	