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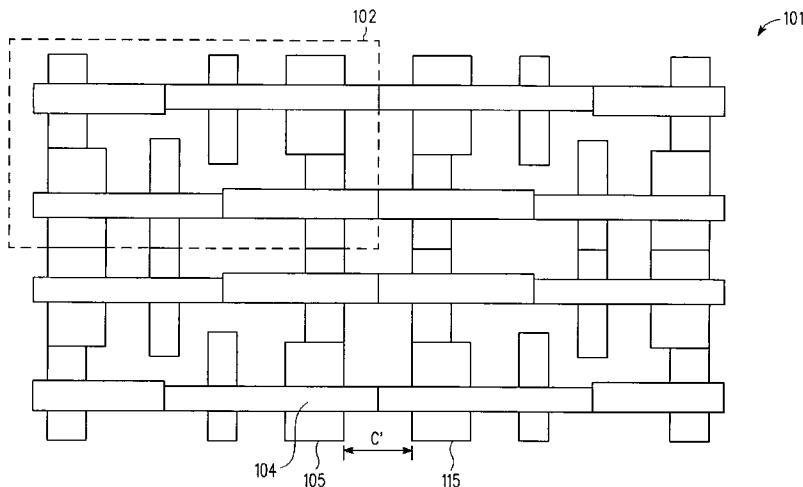


FIG. 2

(57) **Abstract:** A semiconductor device (10) is formed on a semiconductor layer (16). A gate dielectric layer (18) is formed over the semiconductor layer. A layer of gate material (20) is formed over the gate dielectric layer. The layer of gate material is patterned to form a gate structure (20). Using the gate structure as a mask, an implant (24) into the semiconductor layer is performed. To form a first patterned gate structure (20) and a trench (42) in the semiconductor layer (16) surrounding a first portion (28) and a second portion (30) of the semiconductor layer and the gate, an etch through the gate structure (20) and the semiconductor layer (16) is performed. The trench (42) is filled with insulating material (46).

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TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL

Background

Field

[0001] This disclosure relates generally to a semiconductor device, and more specifically, to trench formation in a semiconductor material.

Related Art

[0002] Minimizing the layout area required by one or semiconductor devices is important in reducing the cost of an integrated circuit.

Brief Description of the Drawings

[0003] The present invention is illustrated by way of example and is not limited by the accompanying figures, in which like references indicate similar elements. Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale.

[0004] FIG. 1 illustrates, in a top view, a circuit 1 in accordance with the prior art.

[0005] FIG. 2 illustrates, in a top view, a circuit 101 in accordance with one embodiment of the present invention.

[0006] FIG. 3 illustrates, in a top view, a circuit 101 in accordance with one embodiment of the present invention.

[0007] FIGS. 4-23 illustrate, in cross-sectional views, a semiconductor device 10 in accordance with one embodiment of the present invention. Note that the even figures from 4-22 use the same cut line (see FIG. 3), while the odd figures from 5-23 use a different cut line (see FIG. 3).

Detailed Description

[0008] The semiconductor substrate described herein can be any semiconductor material or combinations of materials, such as gallium arsenide, silicon germanium, silicon-on-insulator (SOI), silicon, monocrystalline silicon, the like, and combinations of the above.

[0009] Prior art FIG. 1 illustrates a prior art six transistor bitcell static random access memory (SRAM) circuit 1 having a 2x2 array of bitcells (e.g. bitcell 2). As illustrated in prior art FIG. 1, transistor layouts typically require the gate layer 4 to be drawn with a nonzero extension or endcap 6 extending over the edge of the transistor active region 5 in order to allow for overlay misalignment and process variation in active area critical dimensions. However, this results in an increase in the layout area required for some circuits. For example, in circuit 1 illustrated in prior art FIG. 1, the minimum of dimension C is dictated by the minimum of both dimensions A and B. Dimension A is the minimum gate overlap required to extend past active area (i.e. the length of the endcap). Dimension B is the minimum separation that can be patterned between the ends of two endcaps (e.g. between endcap 6 and endcap 7). In the illustrated embodiment, the minimum of dimension B is determined by the available processing technology. The dimension C is the distance between the active area of two separate semiconductor devices. In FIG. 1 (prior art), the minimum of dimension C is determined by the minimum of both dimensions A and B. It would be possible to reduce the dimension C (i.e. the distance between the active area of two separate semiconductor devices) if C was not determined by dimensions A and B.

[0010] FIG. 2 illustrates a six transistor bitcell static random access memory (SRAM) circuit 101 having a 2x2 array of bitcells (e.g. bitcell 102). By forming the semiconductor devices (e.g. transistors) before forming the isolation trenches, it is possible to eliminate the endcaps (6 and 7 of FIG. 1). In other words, the dimension A of FIG. 1 (prior art) may be reduced to zero in the circuit 101 of FIG. 2. The dimension C is now the same as B. And the minimum dimension of C is determined by the available processing technology.

[0011] FIG. 3 illustrates the SRAM circuit 101 of FIG. 2 after trenches (e.g. 108) have been formed. As a result of forming the trenches (e.g. 108), the gate (e.g. 104) may be made coterminous with the active area (e.g. 105). Coterminous as used herein is defined in such a manner that the gate (e.g. 104) and the active area (e.g. 105) end at the same vertical plane, or at approximately the same vertical plane, when the trench 108 having width C' is formed between the active areas 105 and 115. Note that the area required for each six transistor bitcell 102 (see FIGS. 2 and 3) has been reduced from the area required for bitcell 2 (see FIG. 1). Reducing the area of each bitcell in an SRAM can produce a very significant reduction in semiconductor die size, thus significantly reducing the cost of an integrated circuit. Although

the circuit 101 illustrated in FIGS. 2-3 was an SRAM circuit, the present invention is applicable to any type of circuit.

[0012] Note that the even figures from FIG. 4-24 are cross-sectional views taken along the cut line illustrated in FIG. 3 which illustrates a plane that is perpendicular to the direction of transistor current flow. Note that the off figures from FIG. 5-25 are cross-sectional views taken along the cut line illustrated in FIG. 3 which illustrates a plane that is parallel to the direction of transistor current flow.

[0013] FIGS. 4 and 5 illustrate, in two different cross-sectional views (see FIG. 3 for cut lines), a semiconductor device 10 in accordance with one embodiment of the present invention. In the illustrated embodiment, device 10 includes an SOI (semiconductor on insulator) wafer comprising substrate 12, with an insulating layer 14 overlying substrate 12, and a semiconductor layer 16 overlying insulating layer 14. Gate dielectric layer 18 is comprised of a dielectric material and is formed overlying semiconductor layer 16. Gate dielectric layer 18 may be grown, deposited, or formed using any other appropriate technique. Gate layer 20 is comprised of a conducting material and is formed overlying gate dielectric layer 18. Gate layer 20 may be deposited or formed using any other appropriate technique.

[0014] FIGS. 6 and 7 illustrate, in two different cross-sectional views (see FIG. 3 for cut lines), a semiconductor device 10 in accordance with one embodiment of the present invention. In the illustrated embodiment, gate layer 20 has been patterned. In one embodiment, a photoresist mask and subsequent etch are used to produce the patterning. In alternate embodiments, the patterning may be produced using any appropriate technique.

[0015] FIGS. 8 and 9 illustrate, in two different cross-sectional views (see FIG. 3 for cut lines), a semiconductor device 10 in accordance with one embodiment of the present invention. In the illustrated embodiment, one or more implant steps (e.g. implant 24) are used to form the source/drain extensions. Note that various known masking techniques may be used to select the areas for implantation. Note also that different implants may be used for different device types (e.g. various p-channel transistors and various n-channel transistors).

[0016] FIGS. 10 and 11 illustrate, in two different cross-sectional views (see FIG. 3 for cut lines), a semiconductor device 10 in accordance with one embodiment of the present invention. Sidewall spacers 25 are formed on the sidewalls of gate 20. In the illustrated embodiment, one or more implant steps (e.g. implant 26) are used to form the source/drain

junctions (see source/drain regions 28, 30). Note that various known masking techniques may be used to select the areas for implantation. Note also that different implants may be used for different device types (e.g. various p-channel transistors and various n-channel transistors).

[0017] FIGS. 12 and 13 illustrate, in two different cross-sectional views (see FIG. 3 for cut lines), a semiconductor device 10 in accordance with one embodiment of the present invention. A silicide layer 32, 34, 36 is formed overlying the gate layer 20 and the source/drain regions 28, 30.

[0018] After the processing illustrated in FIGS. 12 and 13, a variety of choices may be made in processing. In one embodiment, referring to FIG. 24, a nitride layer 41 may be deposited overlying silicide layer 32, 34, 36. In alternate embodiments, the nitride layer 41 may be deposited in multiple steps so that the nitride 41 may be compressive overlying selected areas and may be tensile overlying different areas. In yet other alternate embodiments, an oxide layer (similar to layer 38 in FIG. 15) and a nitride layer (similar to layer 40 in FIG. 15) may be deposited. Next, one or more photolithography and etch steps may be performed to etch trenches in region 47. It is well known to etch through a nitride/oxide/silicon stack for trench isolation. The polysilicon may etch the same as or very similarly to silicon. The silicide layer may be easily etched with slight modifications in chemistry. As one example, in the case of nickel silicide, the addition of CO to the conventional halogen-based trench etch chemistry will allow for the silicide to be properly etched. Other silicides may use similar etch chemistry modifications. Alternate embodiments may use other etches and chemistries that are most applicable to the specific structures and materials in the trench region. Note that alternate embodiments may use any combination of one or more of the following: chemical etch, physical sputter etch, timed etch, endpoint etch, etc.

[0019] Still referring to FIG. 24, in one embodiment, trench spacers 45 may be formed using known processing techniques. Alternate embodiments may not use trench spacers 45. Field oxide 47 is then deposited in trench region 47. Field oxide 47 may then be planarized using conventional techniques (e.g. chemical mechanical polishing or CMP). Alternate embodiments may planarize in a different manner. In some embodiments, an additional oxide layer (not shown) may be deposited overlying the entire top surface after planarization. In one embodiment, the purpose of this additional oxide layer (not shown) is to provide a

dielectric in which a damascene layer may be formed. The etch to form this damascene layer (not shown) may be selective to nitride layer 40 overlying gate 20. A short oxide etch may be used to complete the opening to gate 20, 36.

[0020] Referring to FIG. 25, one or more photolithography and etch steps may be performed to etch nitride layer 41 in order to make electrical contact to gate 20, 36. Such etches are well known in the art. An interconnect layer 49 comprising one or more conductive materials is then deposited overlying and in electrical contact with gate 20, 36. Note that any excess material 49 which rises above the surface plane of nitride layer 41 may be removed using any appropriate technique (e.g. CMP, plasma etchback). Alternate embodiments may planarize in a different manner.

[0021] Referring again to FIG. 12 and 13, after the processing illustrated in FIGS. 12 and 13, a variety of choices may be made in processing. In an alternate embodiment, referring to FIGS. 14 and 15, an oxide layer 38 is formed overlying the silicide layer 32, 34, 36. A nitride layer 40 is deposited overlying the oxide layer 38.

[0022] FIGS. 16 and 17 illustrate, in two different cross-sectional views (see FIG. 3 for cut lines), a semiconductor device 10 in accordance with one embodiment of the present invention. One or more photolithography and etch steps may be performed to etch trenches (e.g. 42). It is well known to etch through a nitride/oxide/silicon stack for trench isolation. The polysilicon may etch the same as or very similarly to silicon. The silicide layer may be easily etched with slight modifications in chemistry. As one example, in the case of nickel silicide, the addition of CO to the conventional halogen-based trench etch chemistry will allow for the silicide to be properly etched. Other silicides may use similar etch chemistry modifications. Alternate embodiments may use other etches and chemistries that are most applicable to the specific structures and materials in the trench region. Note that alternate embodiments may use any combination of one or more of the following: chemical etch, physical sputter etch, timed etch, endpoint etch, etc.

[0023] Still referring to FIGS. 16 and 17, in one embodiment trench spacers (not shown) may be formed using known processing techniques. Alternate embodiments may not use trench spacers.

[0024] FIGS. 18 and 19 illustrate, in two different cross-sectional views (see FIG. 3 for cut lines), a semiconductor device 10 in accordance with one embodiment of the present

invention. Field oxide 46 is deposited in trench 42. Field oxide 46 may then be planarized using conventional techniques (e.g. chemical mechanical polishing or CMP). Alternate embodiments may planarize in a different manner. In one embodiment, the planarization is terminated in the nitride layer 40. In alternate embodiments, the planarization may be terminated in any appropriate location.

[0025] FIGS. 20 and 21 illustrate, in two different cross-sectional views (see FIG. 3 for cut lines), a semiconductor device 10 in accordance with one embodiment of the present invention. Exposed regions of nitride layer 40 are removed using any appropriate etch known in the art (e.g. a dry etch). In addition, oxide layer 38 is removed using any appropriate etch known in the art (e.g. a wet or dry etch). Note that in the illustrated embodiment, the oxide etch may also remove a thin top layer of the thick field oxide 46. Note also that removal of the nitride layer 40 and oxide layer 38 allows electrical contact to be made to gate 20, 36.

[0026] FIGS. 22 and 23 illustrate, in two different cross-sectional views (see FIG. 3 for cut lines), a semiconductor device 10 in accordance with one embodiment of the present invention. An interconnect layer 48 comprising one or more conductive materials is then deposited overlying and in electrical contact with gate 20, 36. Conventional photolithography and etch steps may be performed to pattern the interconnect layer 48. Note that interconnect layer 48 may be used to electrically couple the gates of one or more semiconductor devices (e.g. transistors). After interconnect layer 48 is formed, standard processing may be used to complete the semiconductor device 10. For example, one or more interlevel dielectric layers and/or one or more conductive interconnect layers may be formed.

[0027] Although the invention has been described with respect to specific conductivity types or polarity of potentials, skilled artisans appreciated that conductivity types and polarities of potentials may be reversed.

[0028] Moreover, the terms “front,” “back,” “top,” “bottom,” “over,” “under” and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions. It is understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation in other orientations than those illustrated or otherwise described herein.

[0029] Although the invention is described herein with reference to specific embodiments, various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. For example, although trenches are formed for the purpose of providing trench isolation in the embodiments illustrated herein, alternate embodiments may form one or more trenches for any desired purpose. In addition, trenches may be used in forming any type of semiconductor device, and these semiconductor devices may be used to form any type of circuit. The SRAM circuit 101 illustrated herein is just one possible circuit that may use the present invention. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention. Any benefits, advantages, or solutions to problems that are described herein with regard to specific embodiments are not intended to be construed as a critical, required, or essential feature or element of any or all the claims.

[0030] The term "coupled," as used herein, is not intended to be limited to a direct coupling or a mechanical coupling.

[0031] Furthermore, the terms "a" or "an," as used herein, are defined as one or more than one. Also, the use of introductory phrases such as "at least one" and "one or more" in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles.

[0032] Unless stated otherwise, terms such as "first" and "second" are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements.

Additional Text

1. A method for forming a semiconductor device on a semiconductor layer, comprising:

forming a gate dielectric layer over the semiconductor layer;
forming a layer of gate material over the gate dielectric layer;
patterning the layer of gate material to form a gate structure;
implanting into the semiconductor layer using the gate structure as a mask;
etching through the gate structure to form a first patterned gate structure and through
the semiconductor layer to form a trench in the semiconductor layer
surrounding a first portion and a second portion of the semiconductor layer
and the patterned gate structure; and
filling the trench with insulating material.

2. The method of item 1 further comprising:

forming a sidewall spacer on a sidewall of the gate structure; and
implanting into the first portion and the second portion using the gate structure and
the sidewall spacer as a mask.

3. The method of item 1 further comprising electrically connecting a conductive line to
the first patterned gate structure.

4. The method of item 1 wherein the step of electrically connecting comprises:

depositing an insulating layer over the substrate;
forming a trench in the insulating layer over at least a portion of the gate; and
filling the trench in the insulating layer with conductive material.

5. The method of item 1 wherein the step of electrical connecting comprises:

depositing a metal layer over the first patterned gate structure; and
patterning the metal layer to leave a portion of the metal layer over the first
patterned gate structure.

6. The method of item 1 further comprising:

after the step of filling the trench, forming in the semiconductor layer a
stressor layer over the first portion, the first patterned gate structure,
and the second portion, wherein the stressor layer has a height over the
first and second portions that is greater than a height of the first
patterned gate structure.

7. The method of item 6 wherein the step of forming the stressor is further characterized by the stressor comprising nitride.
8. The method of item 1, wherein the step of etching is further characterized by the first patterned gate structure having ends coterminous with the trench in the semiconductor layer, the first portion is on a first side of the first patterned gate structure and the second portion is on a second side of the first patterned gate structure.
9. The method of item 1, wherein:
the step of etching through the gate structure is further characterized by forming a second patterned gate structure wherein the first and second patterned gate structure are separated by a width of the trench.
10. The method of item 1 wherein the step of filling the trench comprises:
forming trench sidewall spacers on sidewalls of the trench; and
depositing an insulating material in the trench after the step of forming the trench sidewall spacers.
11. A method for forming a semiconductor device on a semiconductor layer, comprising:
forming a gate structure over the semiconductor layer;
performing an implant using the gate structure as a mask;
defining an active region in the semiconductor layer, after the step of implanting, by etching through the gate structure and the semiconductor layer to form a trench in the semiconductor layer, wherein the etching results in a patterned gate structure in the active region; and
depositing isolation material in the trench.
12. The method of item 11, wherein the step of defining is further characterized by the patterned gate structure has two ends in which each end is coterminous with a boundary of the active region defined by the trench.

13. The method of item 12 wherein the step of forming the gate structure is further characterized by comprising one of a group consisting of polysilicon and metal, further comprising:

forming a high k dielectric as a gate dielectric on the semiconductor layer prior to forming the gate structure.

14. The method of item 12 further comprising:

after the step of filling the trench, forming a stressor over the active region adjacent to the patterned gate structure and over the patterned adjacent; and electrically connecting a conductive line to the patterned gate structure.

15. The method of item 14, wherein the step of forming the stressor is further characterized by the stressor having a height over active region adjacent to the patterned gate structure that is above a height of the patterned gate structure.

16. A semiconductor device, comprising:

a semiconductor layer;
a trench through the semiconductor layer defining a boundary of an active region;
a first conductive structure in the active region having a first end and a second end, wherein the first and second ends are coterminous with the boundary of the active region and the first conductive structure functions as a gate, wherein the first conductive structure is sufficiently thick to be able to function as an implant mask for source/drain implants; and

an insulating material in the trench.

17. The semiconductor device of item 16, further comprising a stressor over the active region adjacent to the patterned gate structure and over the patterned adjacent.

18. The semiconductor device of item 16, further comprising a second conductive structure characterized by:

having a portion over the first conductive structure;
being in electrical contact with the first conductive structure;
being of a material different from that of the first conductive structure; and
extending outside the active region.

19. The semiconductor device of item 16 wherein the first conductive structure comprises a layer of polysilicon and a silicide layer over the layer of polysilicon.

20. The semiconductor device of item 16, wherein the first conductive structure comprises metal wherein a high k dielectric separates the first conductive structure from the semiconductor layer.

CLAIMS

1. A method for forming a semiconductor device on a semiconductor layer, comprising:
forming a gate dielectric layer over the semiconductor layer;
forming a layer of gate material over the gate dielectric layer;
patterning the layer of gate material to form a gate structure;
implanting into the semiconductor layer using the gate structure as a mask;
etching through the gate structure to form a first patterned gate structure and through
the semiconductor layer to form a trench in the semiconductor layer
surrounding a first portion and a second portion of the semiconductor layer
and the patterned gate structure; and
filling the trench with insulating material.
2. The method of claim 1 further comprising:
forming a sidewall spacer on a sidewall of the gate structure; and
implanting into the first portion and the second portion using the gate structure and
the sidewall spacer as a mask.
3. The method of claim 1 further comprising electrically connecting a conductive line to
the first patterned gate structure.
4. The method of claim 1 wherein the step of electrically connecting comprises:
depositing an insulating layer over the substrate;
forming a trench in the insulating layer over at least a portion of the gate; and
filling the trench in the insulating layer with conductive material.
5. The method of claim 1 wherein the step of electrical connecting comprises:
depositing a metal layer over the first patterned gate structure; and
patterning the metal layer to leave a portion of the metal layer over the first
patterned gate structure.

6. The method of claim 1 further comprising:
 - after the step of filling the trench, forming in the semiconductor layer a stressor layer over the first portion, the first patterned gate structure, and the second portion, wherein the stressor layer has a height over the first and second portions that is greater than a height of the first patterned gate structure.
7. The method of claim 6 wherein the step of forming the stressor is further characterized by the stressor comprising nitride.
8. The method of claim 1, wherein the step of etching is further characterized by the first patterned gate structure having ends coterminous with the trench in the semiconductor layer, the first portion is on a first side of the first patterned gate structure and the second portion is on a second side of the first patterned gate structure.
9. The method of claim 1, wherein:
the step of etching through the gate structure is further characterized by forming a second patterned gate structure wherein the first and second patterned gate structure are separated by a width of the trench.
10. The method of claim 1 wherein the step of filling the trench comprises:
forming trench sidewall spacers on sidewalls of the trench; and
depositing an insulating material in the trench after the step of forming the trench sidewall spacers.
11. A method for forming a semiconductor device on a semiconductor layer, comprising:
forming a gate structure over the semiconductor layer;
performing an implant using the gate structure as a mask;
defining an active region in the semiconductor layer, after the step of implanting, by etching through the gate structure and the semiconductor layer to form a trench in the semiconductor layer, wherein the etching results in a patterned gate structure in the active region; and
depositing isolation material in the trench.

12. The method of claim 11, wherein the step of defining is further characterized by the patterned gate structure has two ends in which each end is coterminous with a boundary of the active region defined by the trench.

13. The method of claim 12 wherein the step of forming the gate structure is further characterized by comprising one of a group consisting of polysilicon and metal, further comprising:

forming a high k dielectric as a gate dielectric on the semiconductor layer prior to forming the gate structure.

14. The method of claim 12 further comprising:

after the step of filling the trench, forming a stressor over the active region adjacent to the patterned gate structure and over the patterned adjacent; and electrically connecting a conductive line to the patterned gate structure.

15. The method of claim 14, wherein the step of forming the stressor is further characterized by the stressor having a height over active region adjacent to the patterned gate structure that is above a height of the patterned gate structure.

16. A semiconductor device, comprising:

a semiconductor layer;
a trench through the semiconductor layer defining a boundary of an active region;
a first conductive structure in the active region having a first end and a second end, wherein the first and second ends are coterminous with the boundary of the active region and the first conductive structure functions as a gate, wherein the first conductive structure is sufficiently thick to be able to function as an implant mask for source/drain implants; and
an insulating material in the trench.

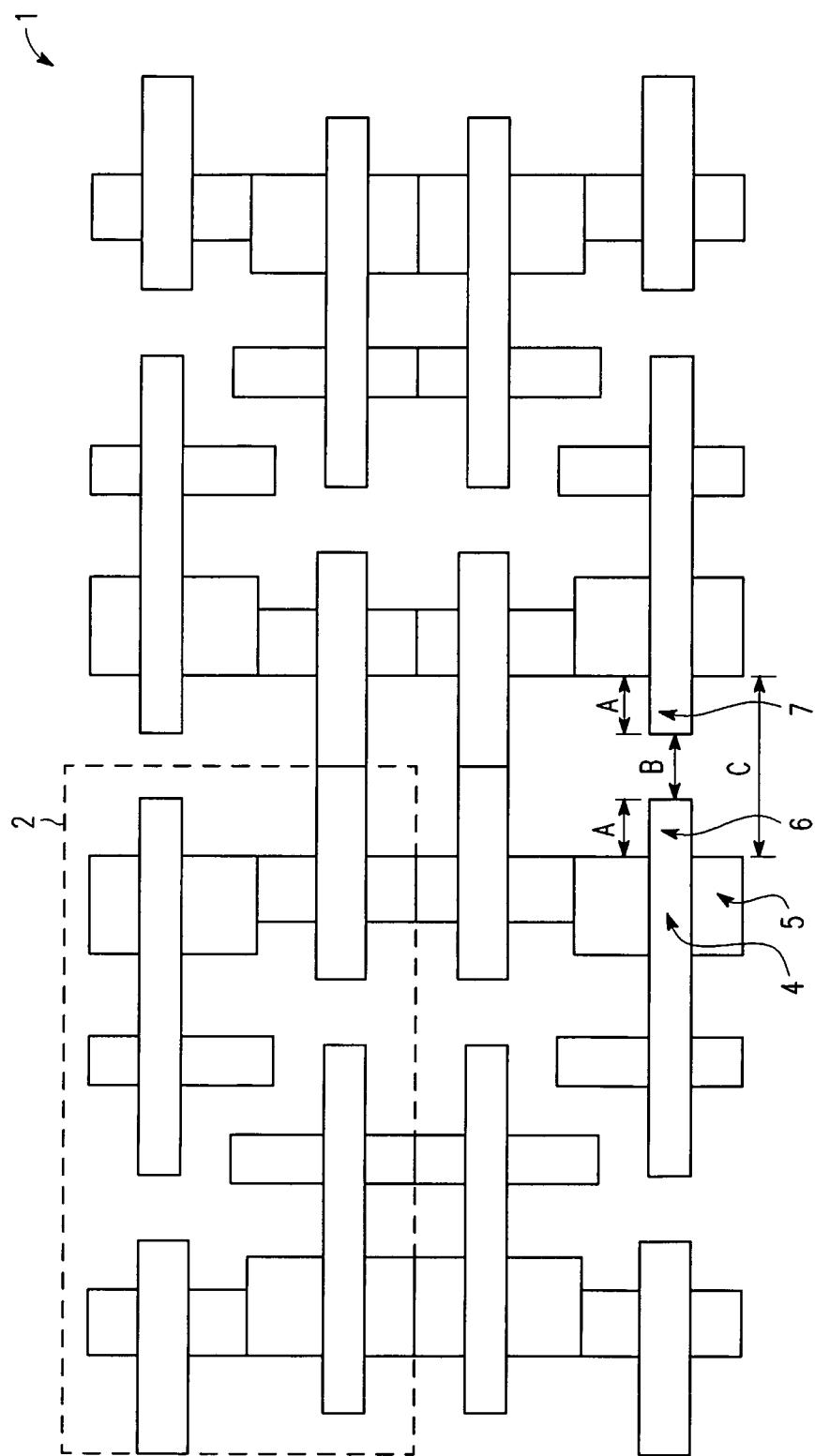
17. The semiconductor device of claim 16, further comprising a stressor over the active region adjacent to the patterned gate structure and over the patterned adjacent.

18. The semiconductor device of claim 16, further comprising a second conductive structure characterized by:

having a portion over the first conductive structure;
being in electrical contact with the first conductive structure;
being of a material different from that of the first conductive structure; and
extending outside the active region.

19. The semiconductor device of claim 16 wherein the first conductive structure comprises a layer of polysilicon and a silicide layer over the layer of polysilicon.
20. The semiconductor device of claim 16, wherein the first conductive structure comprises metal wherein a high k dielectric separates the first conductive structure from the semiconductor layer.

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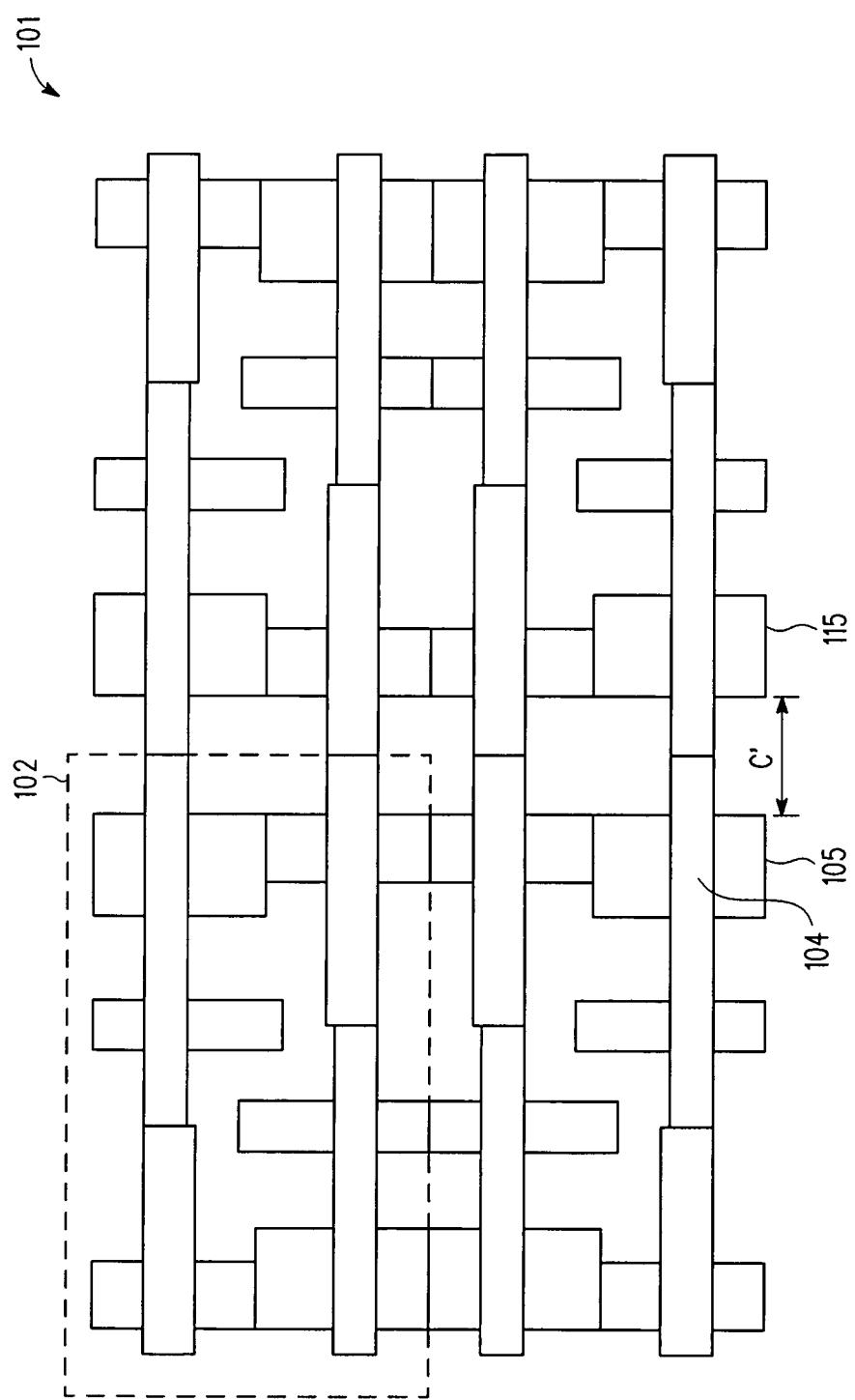


FIG. 2

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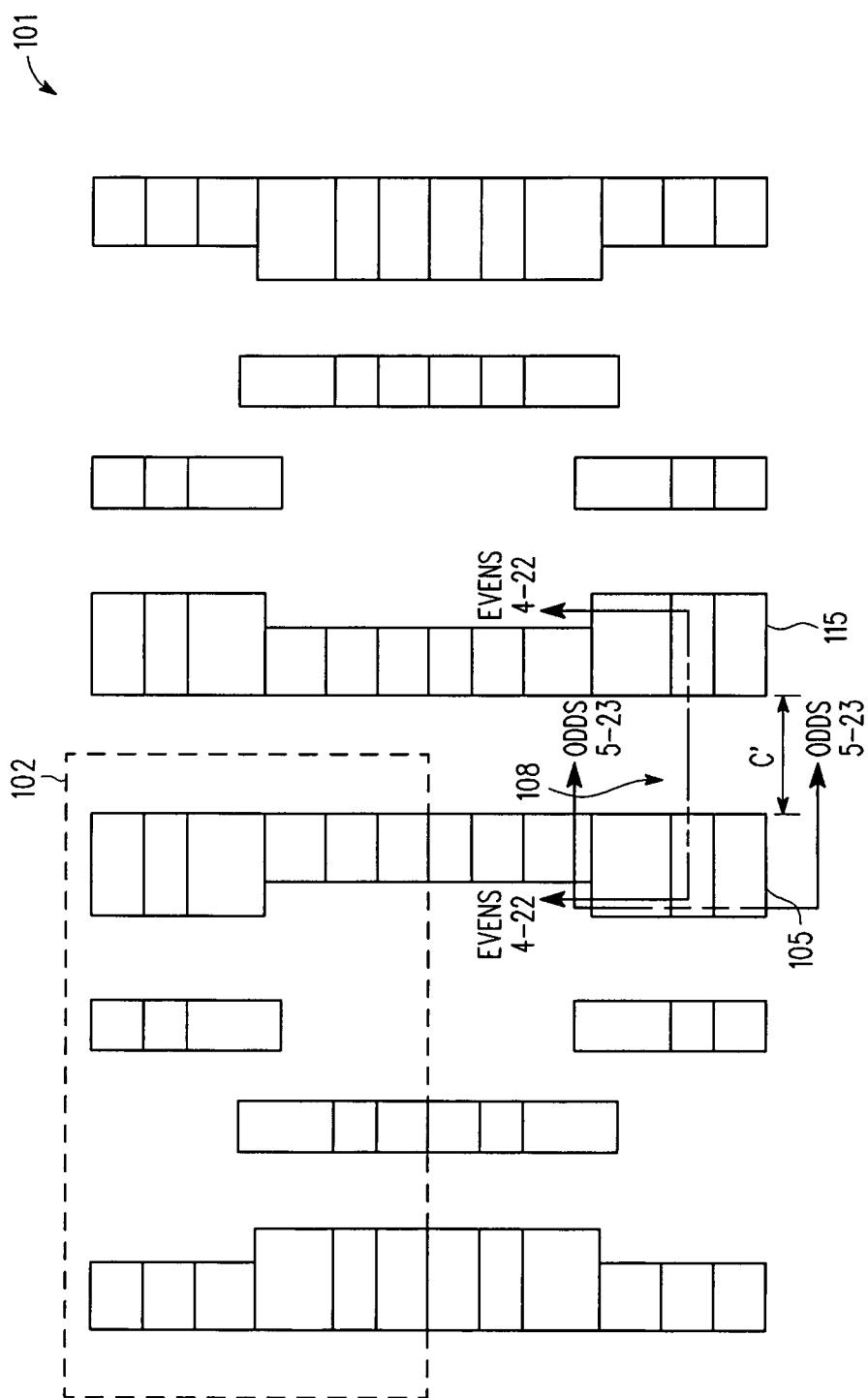


FIG. 3

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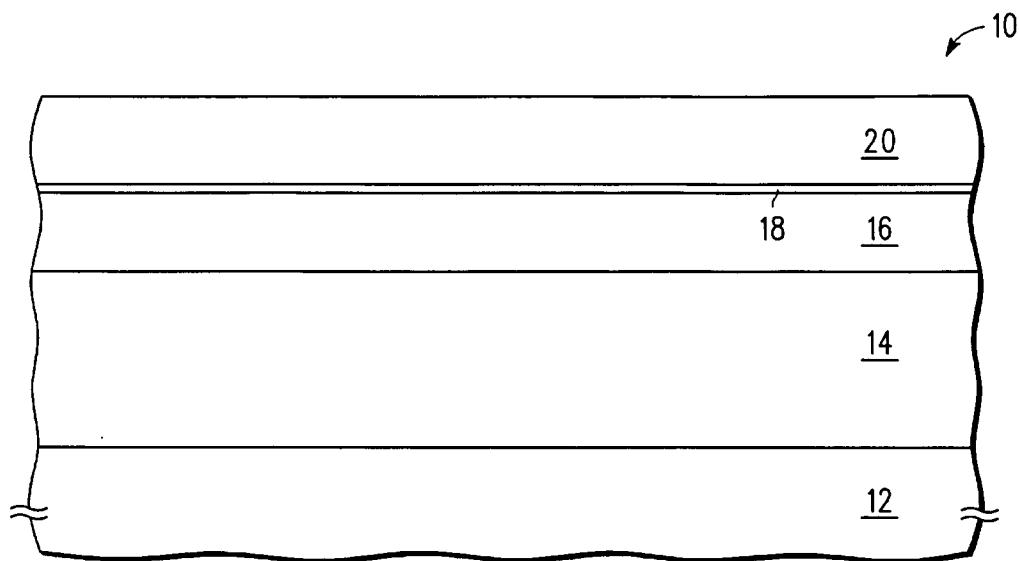


FIG. 4

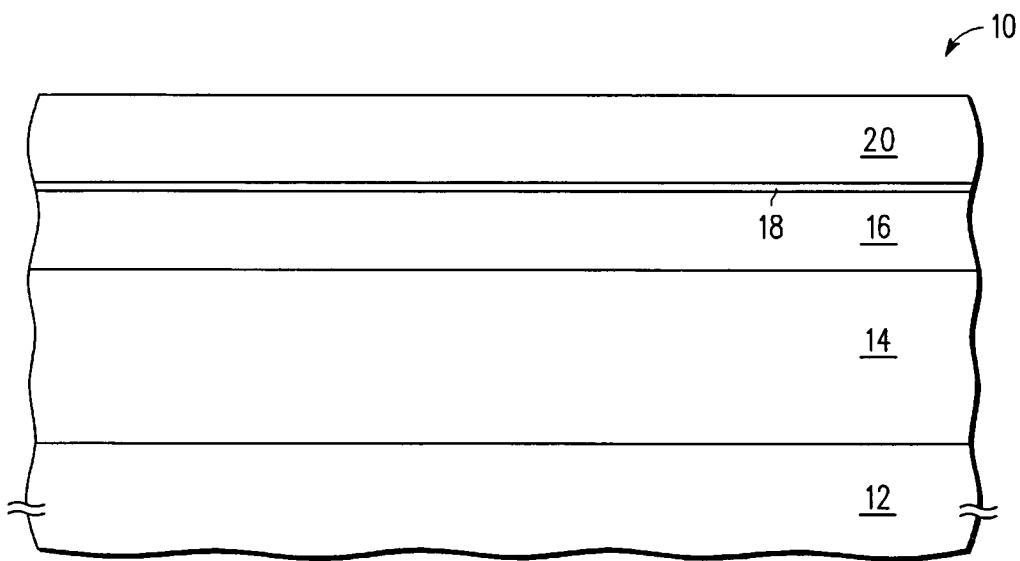


FIG. 5

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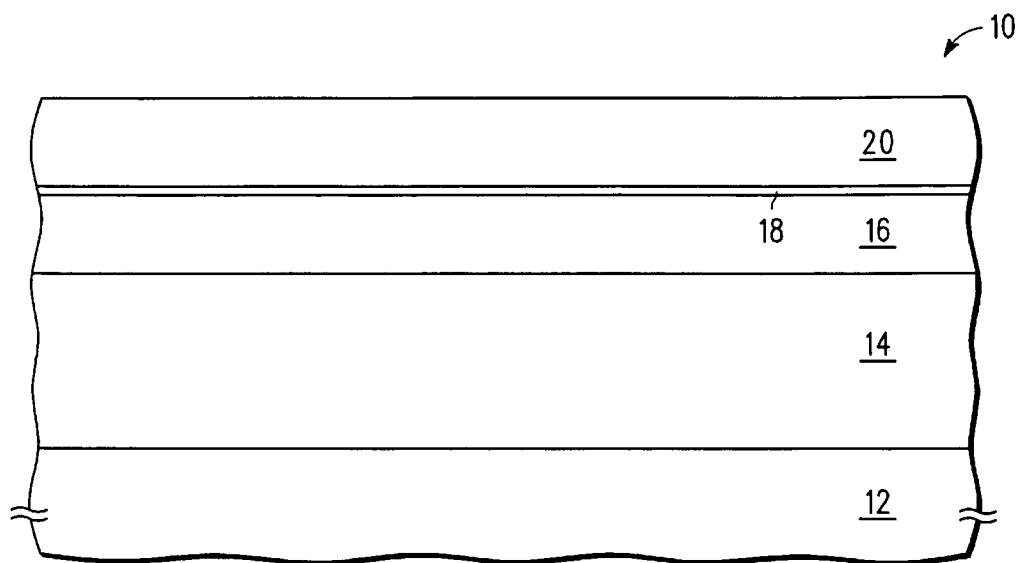


FIG. 6

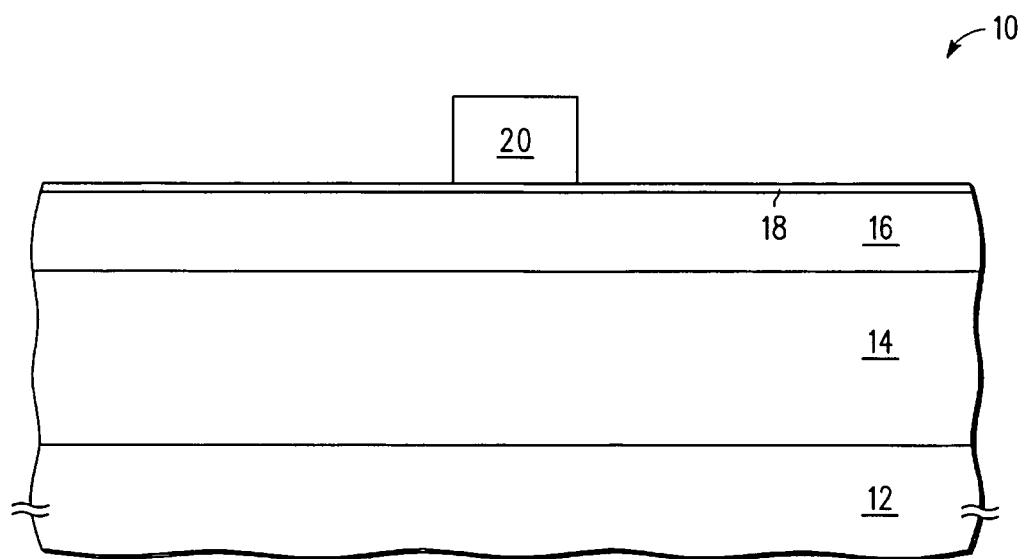


FIG. 7

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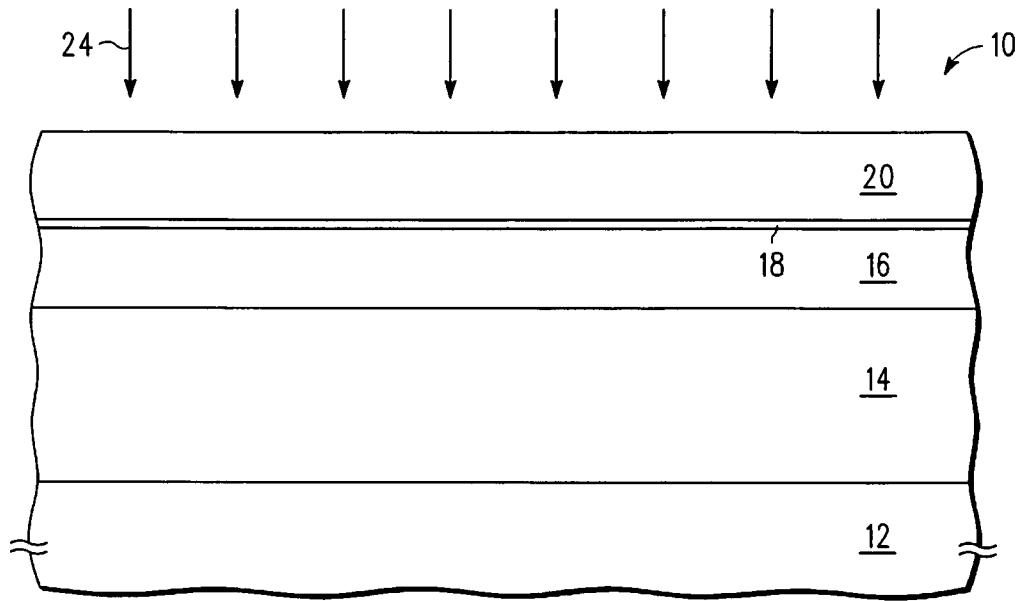


FIG. 8

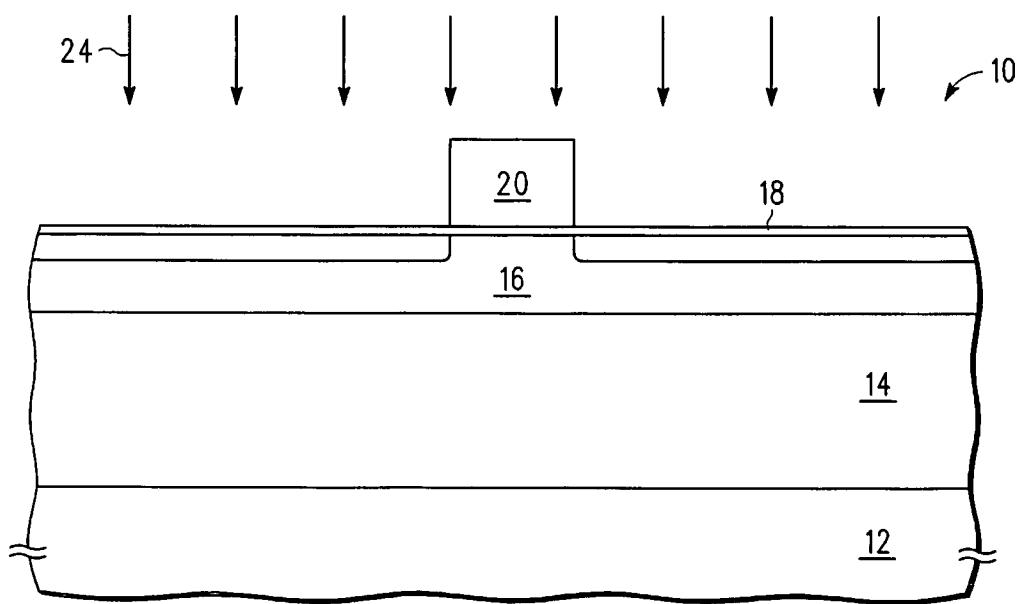


FIG. 9

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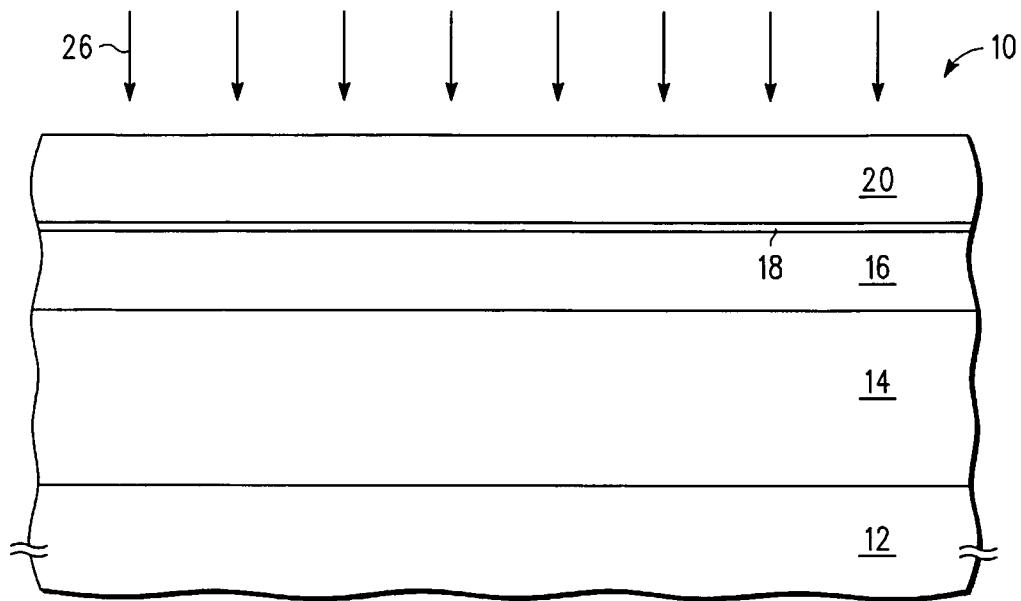


FIG. 10

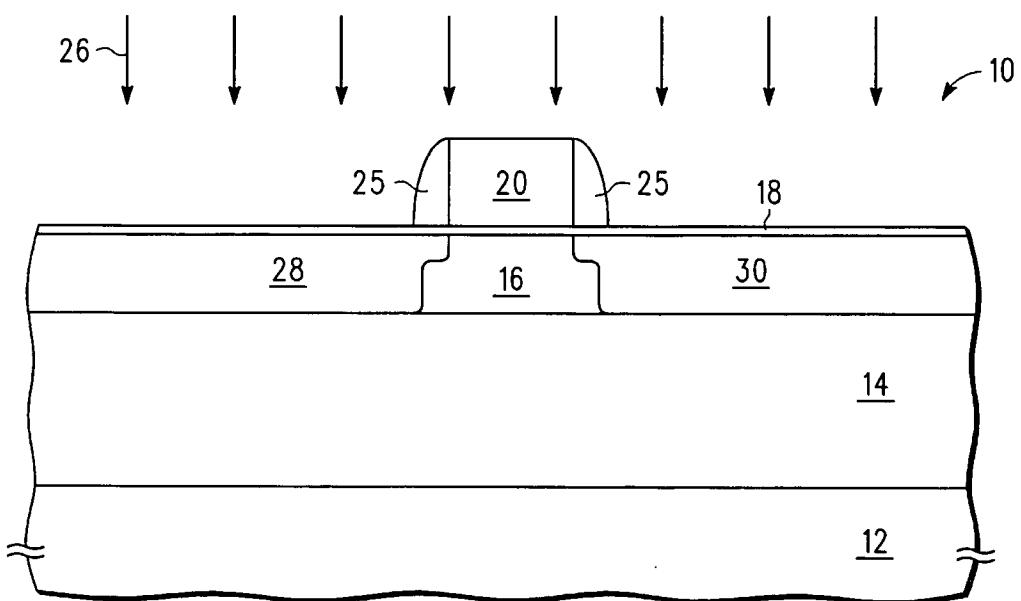


FIG. 11

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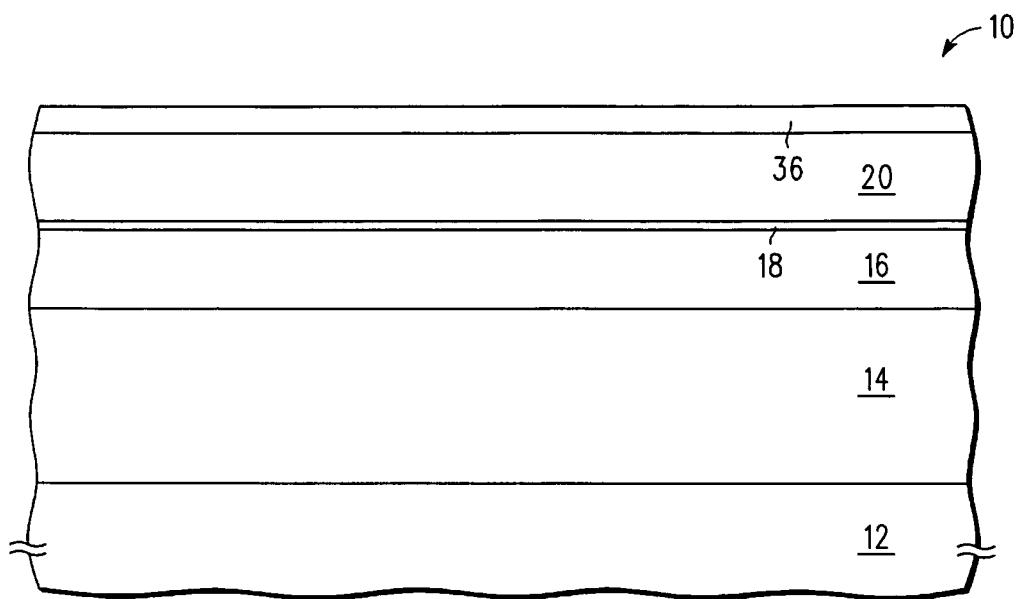


FIG. 12

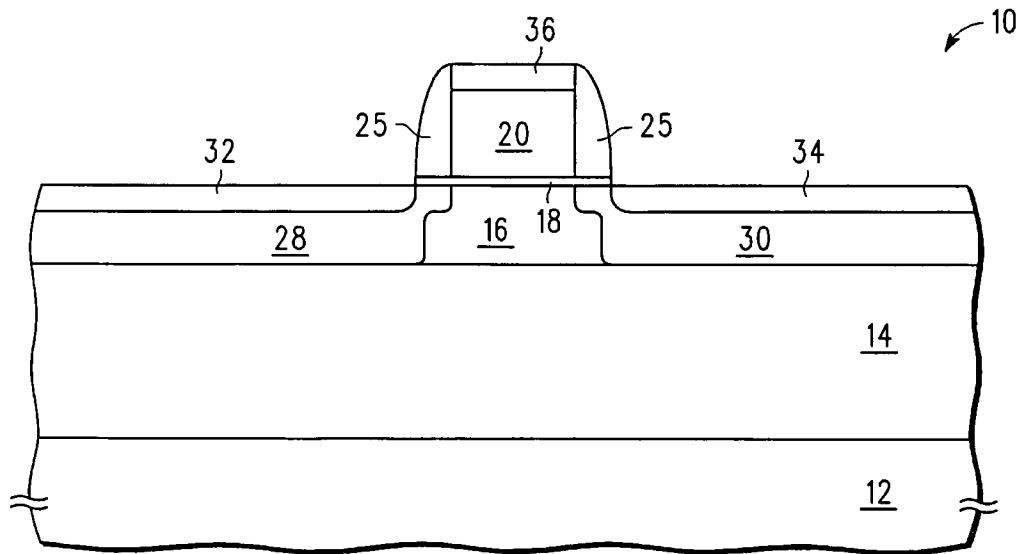


FIG. 13

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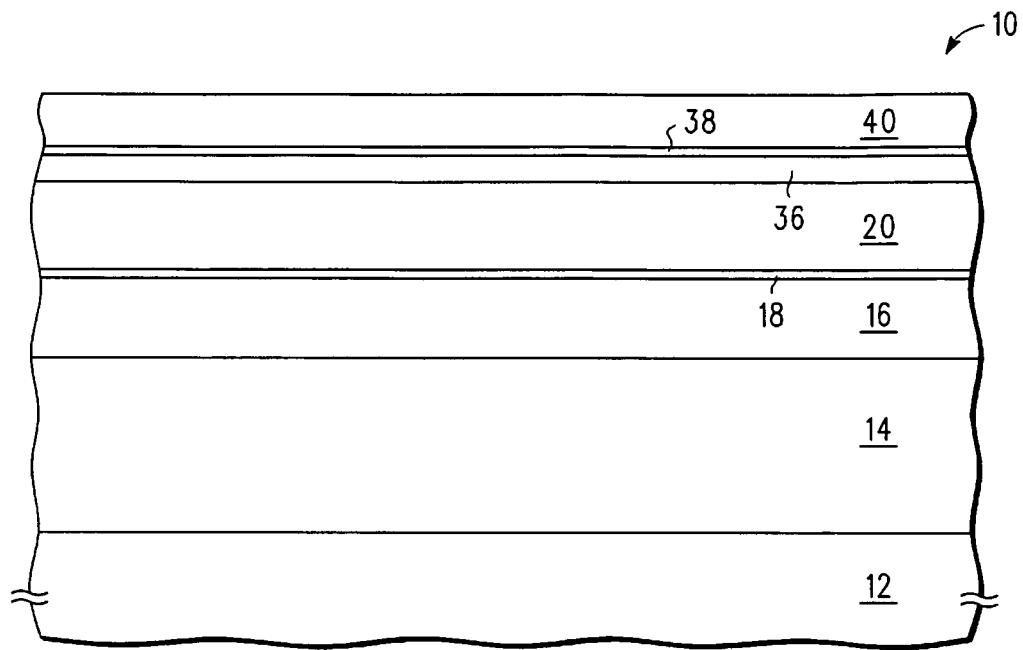


FIG. 14

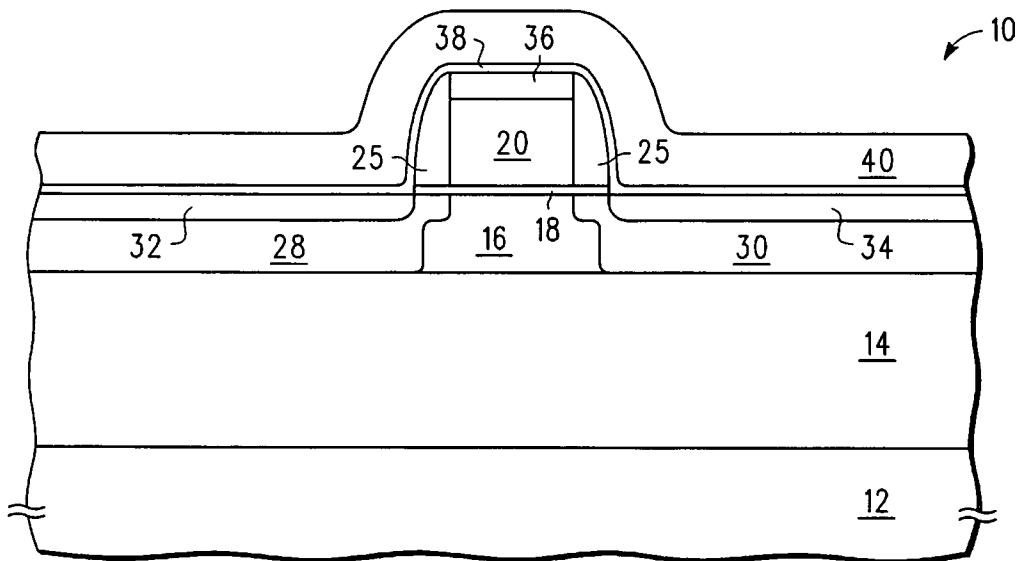
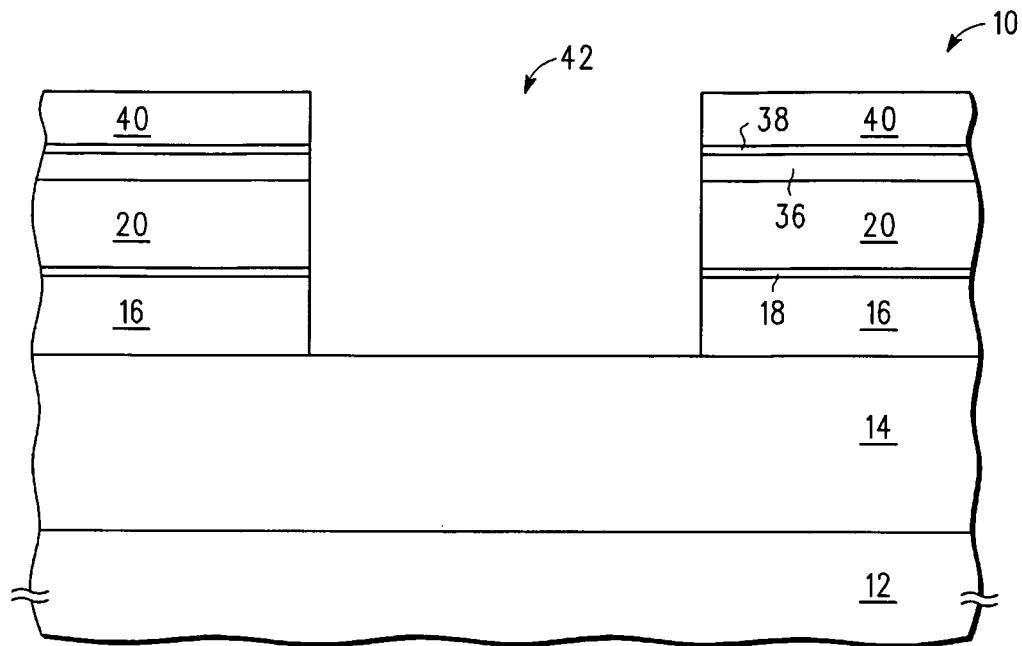
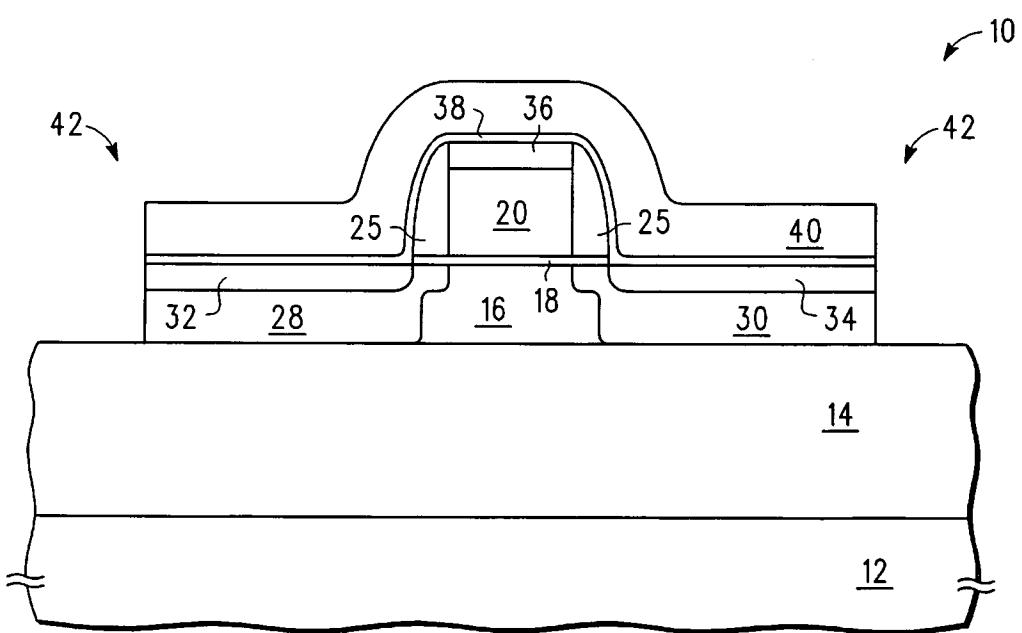
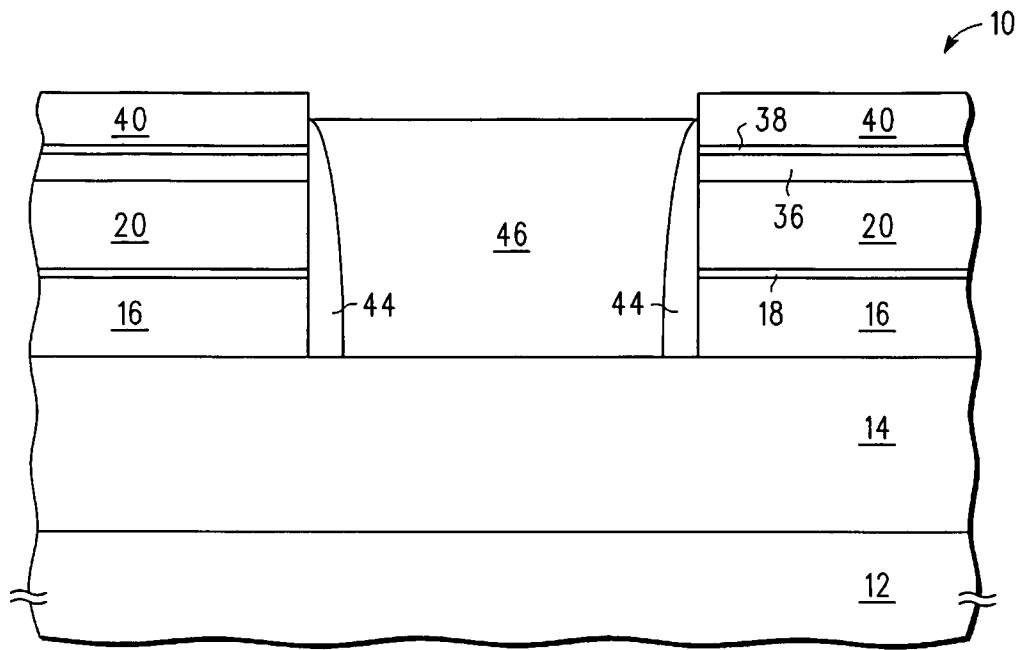
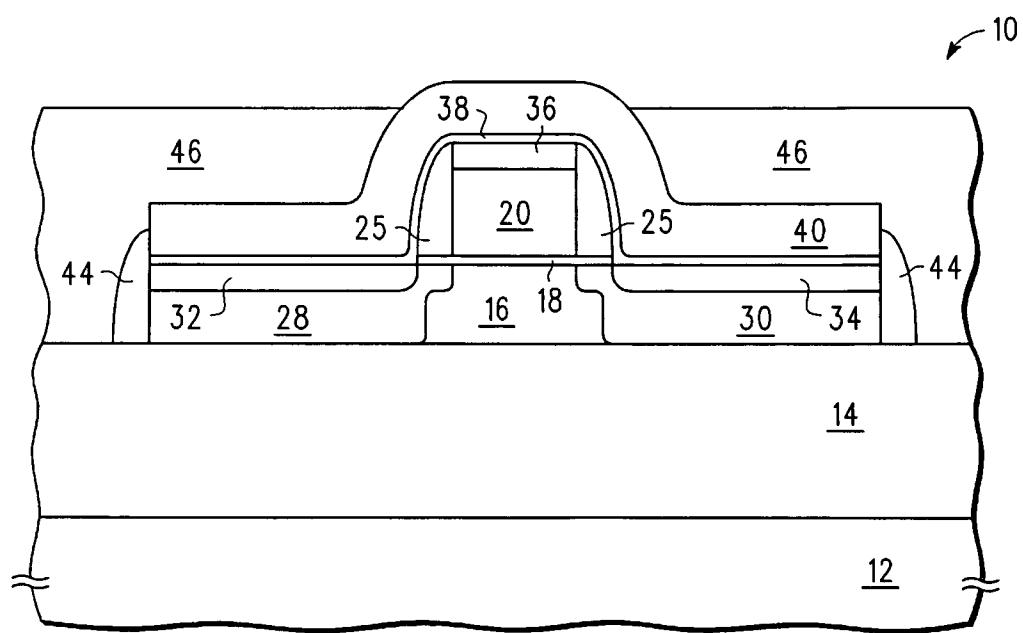


FIG. 15

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**FIG. 16****FIG. 17**

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***FIG. 18******FIG. 19***

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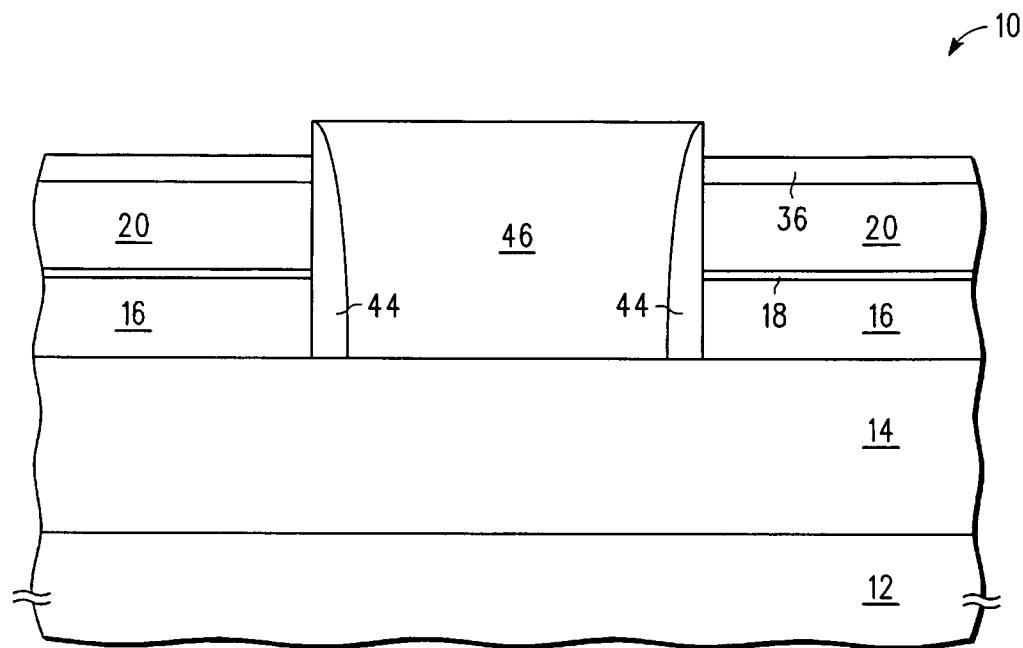


FIG. 20

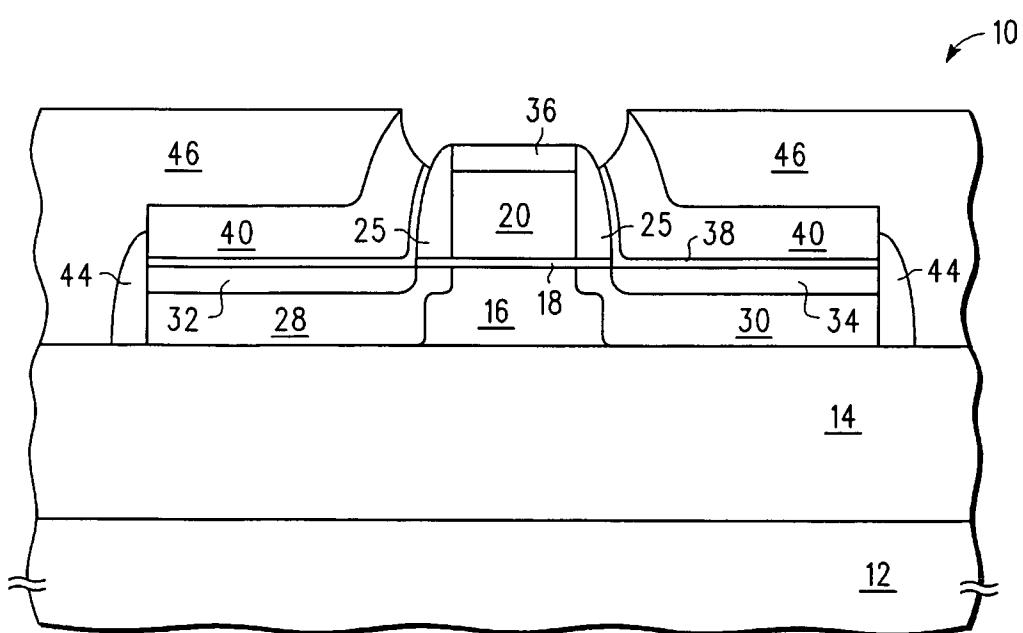
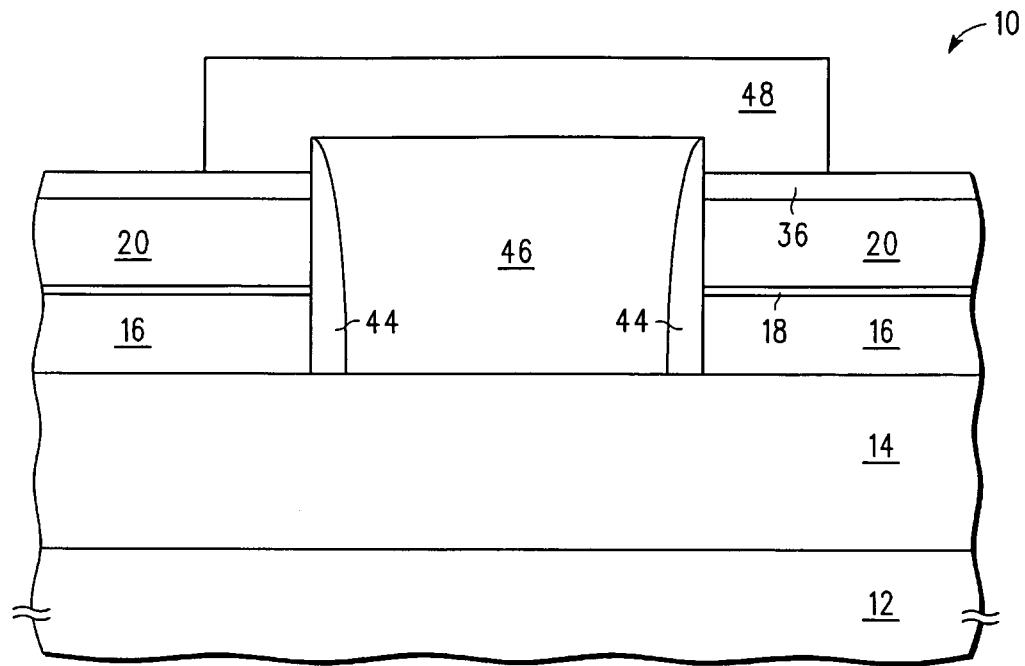
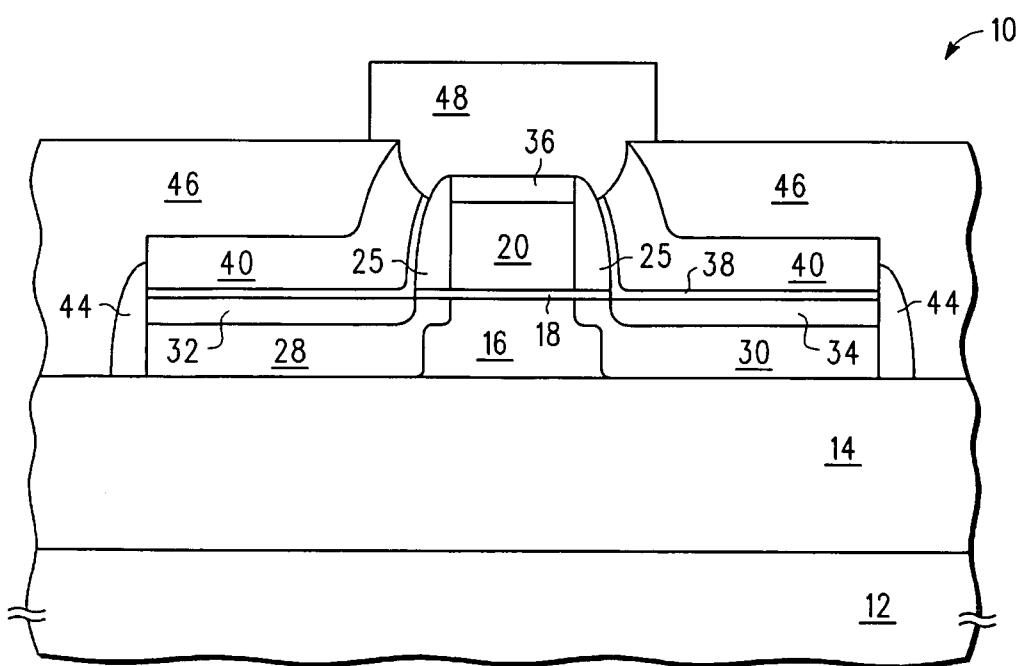
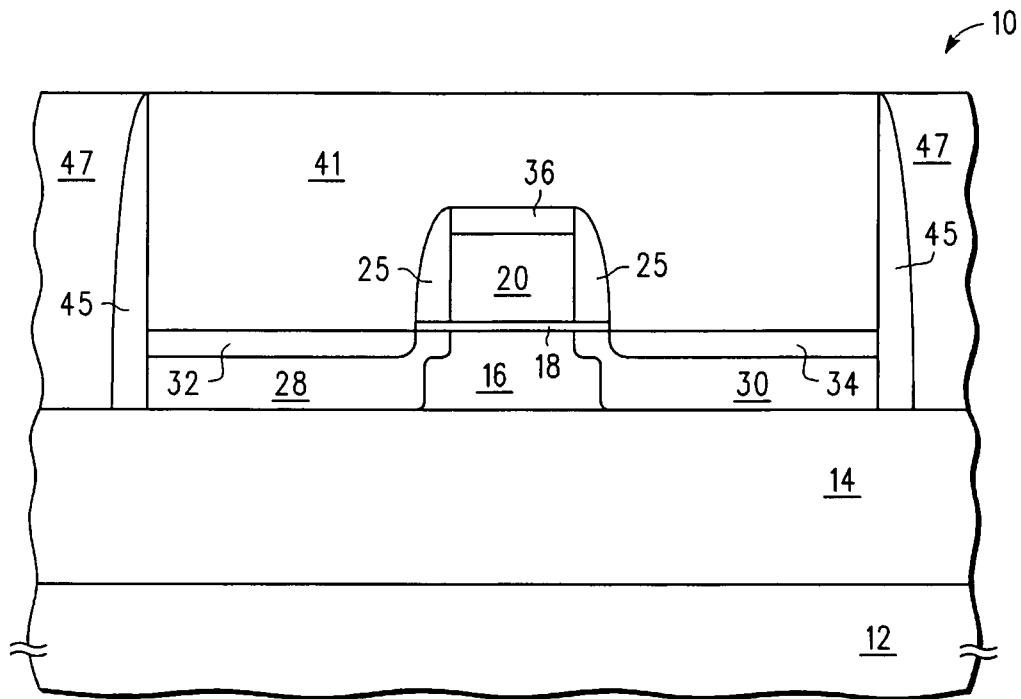
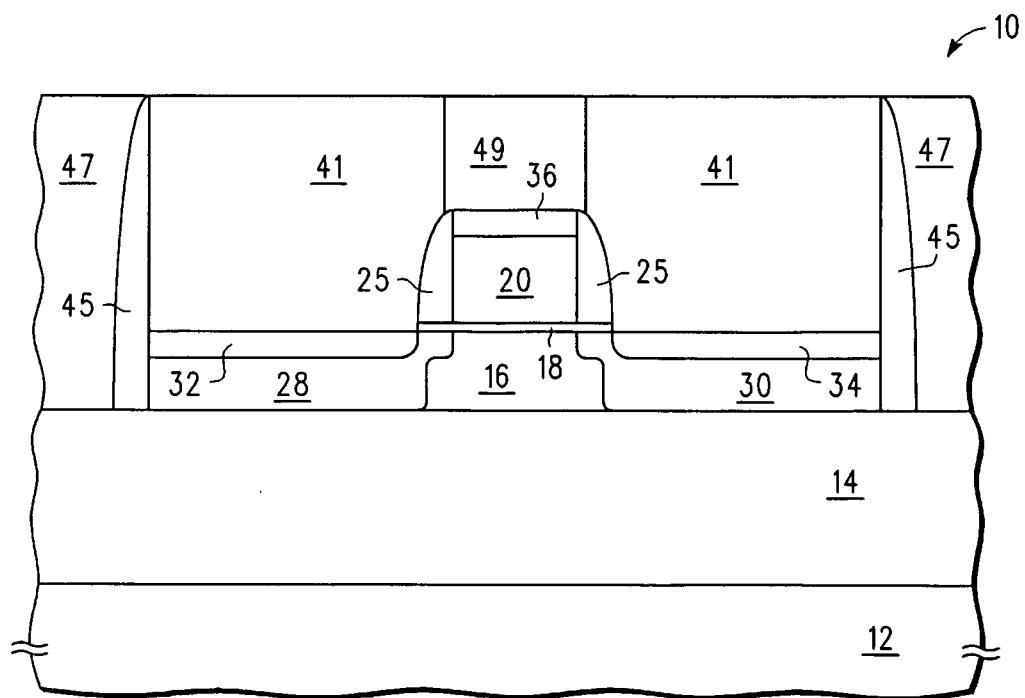


FIG. 21

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*FIG. 22**FIG. 23*

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*FIG. 24**FIG. 25*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/053133**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/76(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 : H01L 21/76

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Utility Models and applications for Utility Models since 1975
Japanese Utility Models and applications for Utility Models since 1975Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKIPASS(KIPO internal) "isolation", "trench", "STI", "gate", "dielectric", "implant"**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KR 10-2004-0059427 A (HYNIX SEMICONDUCTOR CO., LTD.) 05 July 2004. See the abstract, figures 1a-1e, claims 1-8	1-20
Y	KR 10-0196018 B1 (INTERNATIONAL BUSINESS MACHINES CO., LTD.) 18 Feberary 1999. See the abstract, figures 1-10, claims 1-28	1-20
Y	US 5,918,131 A (S.-Y. Hsu and H.-S. Huang) 29 June 1999. See the abstract, figures 2A-2E, claims 1-16.	10
Y	US 6,858,514 B2 (S.T. Hsu and Y. Ono) 22 February 2005. See the abstract, figures 1-11, claims 1-8.	13,20

 Further documents are listed in the continuation of Box C. See patent family annex.

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Date of the actual completion of the international search
02 JULY 2008 (02.07.2008)

Date of mailing of the international search report

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So, Jae Hyun

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PCT/US2008/053133

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2006-0108333 A (SAMSUNG ELECTRONICS CO., LTD.) 17 October 2006. See the abstract, claims 1-15, figures 3a-8b.	1-20
A	KR 10-2003-0055997 A (SAMSUNG ELECTRONICS CO., LTD.) 04 July 2003. See the abstract, claims 1-20, figures 3a-4.	1-20
A	KR 10-2002-0042312 A (SAMSUNG ELECTRONICS CO., LTD.) 05 June 2002. See the abstract, claims 1-6, figures 2a-2e.	1-20
A	KR 10-2000-0074841 A (SAMSUNG ELECTRONICS CO., LTD.) 15 December 2000. See the abstract, claims 1-3, figures 2a-2d.	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2008/053133

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-2004-059427 A	05.07.2004	NONE	
KR 10-0196018 B1	18.02.1999	JP 08-241925 A JP 3017064 B2 US 5545581 A	17.09.1996 06.03.2000 13.08.1996
US 5918131 A	29.06.1999	NONE	
US 6858514 B2	22.02.2005	CN 1591832 A EP 1498945 A2 EP 1498945 A3 JP 2005-039280 A KR 10-2005-0009246 A TW 248171 B US 2004-0140504 A1 US 2005-088898 A1	09.03.2005 19.01.2005 26.09.2007 10.02.2005 24.01.2005 21.01.2006 22.07.2004 28.04.2005
KR 10-2006-0108333 A	17.10.2006	US 7361591 B2 US 2006-226448 A1	22.04.2008 12.10.2006
KR 10-2003-0055997 A	04.07.2003	NONE	
KR 10-2002-0042312 A	05.06.2002	NONE	
KR 10-2000-0074841 A	15.12.2000	NONE	