

(19)  
(12)

(KR)  
(B1)

(51) 。 Int. Cl. 7  
H03K 5/13

(45)  
(11)  
(24)

2001 12 12  
10 - 0315610  
2001 11 12

(21) 10 - 1999 - 0060142  
(22) 1999 12 22

(65)  
(43)

2000 - 0052545  
2000 08 25

(30) 9828510.9 1998 12 22 (GB)

(73) 가 가  
가 가  
가 22 22

(72) 28 22  
44 124

(74)

:

(54) ,

가 ,

가 .

4

(static) , , , , ,

1

2 1

3

4

5 4 가

6 4 5

7

8 7 가

9

10 9 가

11

12

13

14 4, 7, 9 11 13

15 14

16 15

17 2

18 17

19 18

20 15 18

21 15 18

22 2

23 22

24 18 23

25 18 23

26

27 18 23

28 - 18

29 2

30 29

31 29

32

33

34

35 34  
(end) (terminal stage)

36 32

37 가 36

38

39a 39b

40

<

1, 2 :

3 :

4 :

6 :

(DSP)

(VLSI)  
가

D-  
가

(0)

(1)

1

4,542,301

4,612,659

4,785,297

(master)'

(slave)'

AND

NAND

1 D-  
2)

CMOS

1 (

(1)

(2)

CK

CK -

2

Nn Np

'NANDed'

2 2

1

(1)

D,

2 (2)

1

(1)

M,

2

(2)

Q

가

Nn Np가

가

4,746,915

가

가

3

1 가

1 가

'ORing'

가

5,128,974

$i$  가  $1$  ,  $N$  ,  $(i-1)$  ,  $(i+a)$  ,  $(i+2)$  ,  $(i+1)$  ,  $(i+1)$  ,  $(i+a)$  ,  $1$  ,  $1$  ,  $(i+a)$  ,  $2$  ,  $N$  ,  $N$  ,  $(N-1)$  ,  $N$  ,  $N-1$  ,  $i$  ,  $(i-a)$  ,  $(i+1)$  ,  $1$  ,  $1$  ,  $2$  ,  $2$  ,  $N$  ,  $3$  ,  $(i+a)$  ,  $가$  ,  $가$  ,  $가$  ,  $가$

가 1 1  
 2 가 , 1 2  
 1 2 , 1 2  
 1 2

1 1  
 1 2 1  
 2 1 2 가 1 , 2 1  
 2 1 2

2 1 2 1 3 4  
 2 2 2 1 2 5 6  
 , 3 5 2 가 , 4 6  
 2 1 2 가 3 5 1  
 2 가

1 1 1 7 2 1  
 1 7 8 , 7 8  
 1

CMOS

2 , 1 가

3 , 2 가

(static)

( , )

가

가 가

( )

2

(i) ( ) ;

(ii) ( ) ;

(iii) ;

(iv)

가 가  
( ' ' )  
가

4 ( )

Pp: : CK (positive - going pulse) ;

Pn: : CK 가 ;  
 Np: 가 : CK ;  
 Nn: 가 : CK 가 ;

4 /Q 가 Pn (n+1) R (n+1) (1) (3) R, S, S, Q, (n-1) Fi

(3) Q /Q CK, /CK 가 (4) G /G (4) (4) (4) O (1) Pp (n+1) (n-1) O F0

4 Pn (n+1) CK (2) (2)가 (n-1) Pp (1) (4) CK(n) /CK (1) Pp (2) P

(3) Q /Q CK /CK 2 (4) 가 (3) 1 2 O

5 (1) (2) N (1,2) 1 Pn SP (1,2) F1 Fo CK /CK N Fi gnd

6 /Q가 Pn Pp (1,2) 3 (3) Q가

tn Q 가 SP 1 /Q (1) Pn (3) Pp가 CK (4) 1

tn+1 (3) CK 가 1 (1) Pp 가 2 (2) Pn Q /Q /CK (4)

$tn+2$  , /CK 가 2  $Pn$  (2)  $Pn$  가 3  
 (1) , Q 가 .  $Pn$  1 (1) 가 (3) R  
 (1) (Pp) 가 . 1 (1) 가 1

7 (1 2) 4 .  
 $n-1$  (1, 2)  $(n+1)$  (F) (F)  
 (3) Q  $(n-1)$  (F1) (Fo)  
 (R)  $(n+2)$  . (3)

(4) , 7 (1 2)  
 5 8  
 6 (B) , 3 6 (Q)  
 1 (Q) (3) (Q) 가 .

(Q) 9 (1 2) 5' (O)  
 (1 2) (5) (4) (Fo)  
 4 (4) (O) .  
 (Q 1Q) 가 10

11 (4) 7 (1 2)  
 (3) (Q 1Q) - (T1, T2) (1)  
 (2) 2 (T1 T2) CK 1CK (T3)  
 (3) (1) (Pp) (2)  $Pn$  ,

(3) , (T1, T2) (T3)  
 (3) (T1, T2)

4, 7, 9 11 (1 2) (CK 1CK)  
 (Pp Pn) , (Nn Np) 8  
 가 . 12 (1 2)

12 가 (1) (6)가 (Np) (3) (S) (Nn) (T3)  
 (vdd) 12 가 (2) (6)가 (Nn) (3) (S)  
 (Np) 가 (3) (Q) (T3)

13 4 (1 2) (1)  
 (Pp) (2) (Nn) (1)  
 (6)가 (Nn) (3) (S) 11 (1)  
 2) (6)가 (T1, T2) (CK) 12  
 (CK)

(3) RS 14  
 F. Hill G. Peterson 'Digital Logic and Microprocessors', John Wiley and Sons, 1984  
 NOR 2 (N  
 OR1 NOR2) NOR1 가 S NOR2 가  
 R NOR1 /Q  
 NOR2 Q NOR1 2 NOR2 2 Q  
 /Q

[ 1 ]

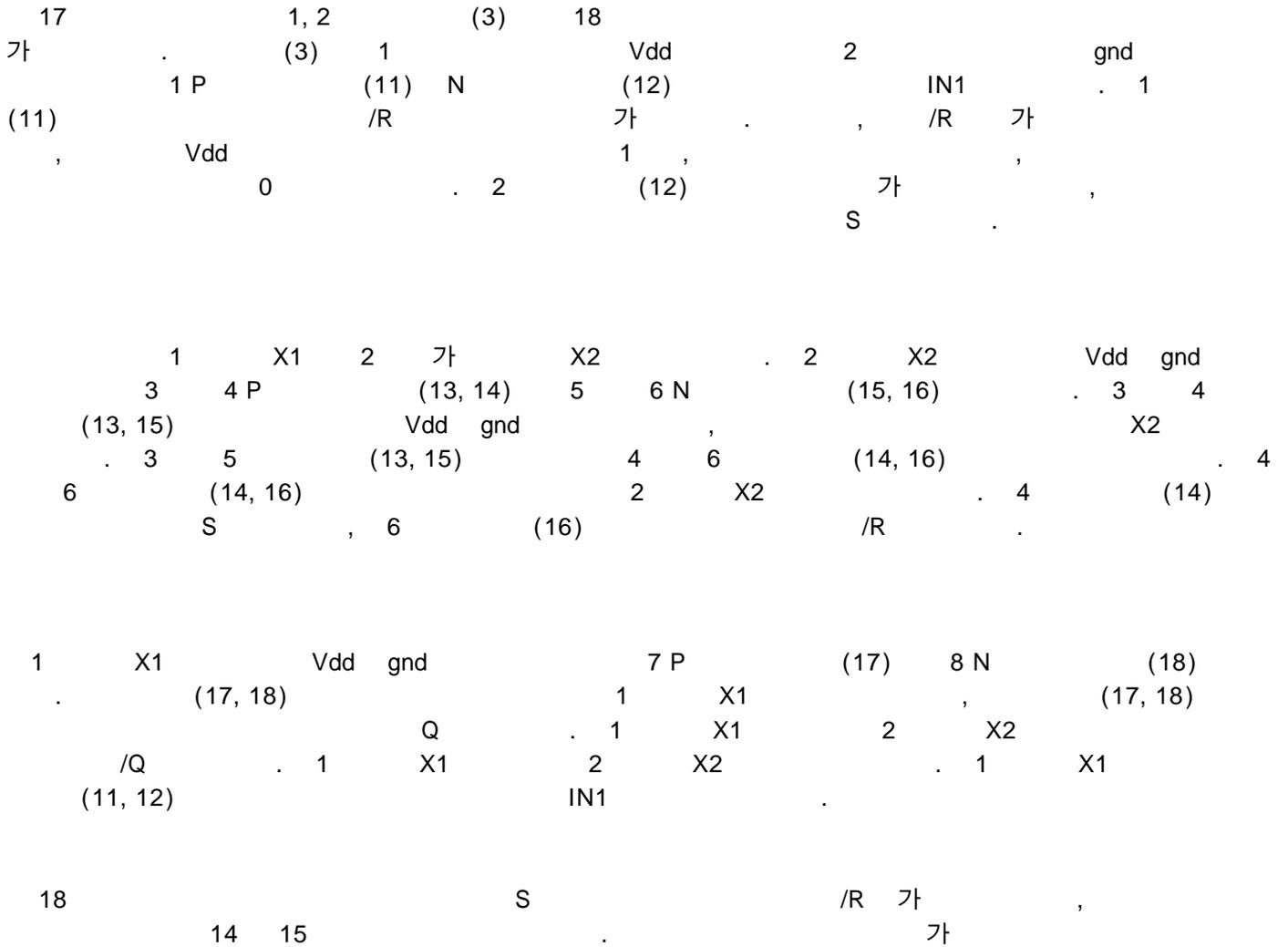
S	R	$Q_t$	$/Q_t$
0	0	$Q_{t-1}$	$/Q_{t-1}$
0	1	0	1
1	0	1	0
1	1		

( 0 1 ,  $Q_t$  / $Q_t$  ,  $Q_{t-1}$  / $Q_{t-1}$  ).  
 S R 0 Q /Q  
 R 가 S가 Q 가 가

14 RS 15 8 CMOS  
 NOR1 P I2 G2 , N M2 I1 NOR2 P  
 I4 G4 , N M4 I3

16 R S Q /Q 4  
 15 Q /Q 가

17 1, 2가 11 (3) /R 가 (3)  
 /Q 가



[ 2 ]

S	IR	Q <sub>t</sub>	IQ <sub>t</sub>
0	1	Q <sub>t-1</sub>	IQ <sub>t-1</sub>
0	0	0	1
1	1	1	0
1	0		

가 (0) 가 (1) , (1  
 12)가 (14 16) (X2) 가  
 가 Q /Q가

가 Q가 0 /Q 1 , /  
 R 1 (1) S 가 /  
 2 (12) 4 (14) 2 (X2)  
 1 Vdd 2 (X2) 1 (X1)  
 (12) (pulled) Q 1 (15) , 가

(12)가 (X1) 0 (13)

Q가 1 /1Q가 0 가 , 1 (11)  
 ( 0) ( 0) . , 1 (11)  
 (16) (X1) 1 O (15)  
 Q 2 (X2)  
 가 ( 1) , (X1 X2)

(11 , 12) Vdd 가 IN1 가  
 가

19 18 . . T1 , 18  
 Q /Q가 . ,

20 21 15 18

20 /Q T1 18 'new RS' 15 'NOR RS'  
 T3 Q 'new'  
 Q가 ( T2 )  
 20%

21 /Q T1 15 Q 18  
 /Q가 T2 18 Q , 15  
 T3

22 12 (6)가 (3) IS  
 (1 2) 18 (2)  
 , 1 R (1) 가 (X1) 23 IS 2 (2)  
 , Q (X2) Q  
 18 /Q 23 , 23

[ 3 ]

IS	R	$Q_t$	$/Q_t$
1	0	$Q_{t-1}$	$/Q_{t-1}$
1	1	0	1
0	0	1	0
0	1		

2 (13 14) (15 16) 1 vdd (13)  
 , 24 (16) 2 gnd (14) (15) ,  
 가 (13 14) D1 (15 16) 25  
 D2 .

18 23 25 1 1 vdd  
 0 2 gnd , 2  
 6 , S , ( ) vdd Vs ,  
 가 , 18 IR , Vr (12)  
 , 18 ,  
 (14) - , (14)가 .  
 , (12) (13 14) , (12)  
 가 (13 14) , 가 .

27 18 P F1 1 X1 (13)  
 F1 2 gnd .

27 , F1 0 F1  
 , , (13) 가 (13 14) -  
 , , (13)가 , (13 14) Vs .

가  
 N X1 (15) , N  
 1 Vdd .

24, 25 27 18 23 .

28 - (11`)가 18  
 (11`) (11`) P , (11) (11)  
 (11`) , (11`) (12) ,

(11') Vdd S , (11') (11) (11')가  
 28 , 가 18  
 . 28 .

[ 4 ]

S	IR	Q <sub>t</sub>	IQ <sub>t</sub>
0	1	Q <sub>t-1</sub>	IQ <sub>t-1</sub>
0	0	0	1
1	1	1	0
1	0	1	0

18 , , 가 , ,  
 , (11') , S가 IR , S가 1  
 . 가 , 가 28 , 가 , 가  
 , 1 가 , ,  
 , 가 가 , ,  
 , ,

29 1 2 , 2- 1 2 . 29  
 4 1 2 , (4)가 .

30 , (4) 9  
 10 N (19 20) , ' VLSI ' (A. Bellaouar M. Elm  
 asry, Kluwer Academic Publishers, 1995, )  
 11 13 P (21 23) (19 20)  
 , (21 22) (20 19)  
 (21 22) (23) , (23) Vdd  
 . (23) 1G .

14 16 N (24 26) . (24 25)  
 CK ICK , G . (24 25)  
 (21 22) . (26) - O g  
 nd , 1G .  
 (4)가 , G IG가 , ( 가  
 24 25) (21 22) . (23) , 가  
 CK . (26) , O가

G IG가 (23) 가 , (24 25)가 (26)  
 O가

31 (4) 17 19  
 P (27 29) , 12 N (30) (27 29)  
 Vdd (27) IG (28) (28)  
 (28) ICK (29) (30)

(29 30) 21 P (31) 22 N (32)  
 (31 32) vdd gnd O

23 N (33) (28 29) CK  
 G 24 25 N (34 35) IG  
 gnd (30 29)

가 G IG (33)  
 (29 30) (27 28) (34 35)  
 (27) O가 CK

가 G IG (29)가 (31)  
 32) (34 35) (33)  
 CK

29 30 CK ICK  
 (24, 25, 30 33)

32 11 (1) 32  
 32

Q (7 8) (1) (7)  
 (T1, T2) F0 (8)  
 Pp 32  
 (7)  
 Q  
 (T1, T2)

32 (7 8)  
 Q (8)

33 32 (1) , (F0)  
 가 33 32 (7)  
 (T1 T2) (F)  
 , 32 2

34 (1) , (Pn) , (Pn)  
 S) (7) (8) (Pn)  
 3) (R)

35 (100) (2) 35  
 (100) (100) (3) (SP)  
 (7 8) (2) (3)  
 (2) (100) (3)  
 1)( ) (100) ( )

(static) (100) (100) , 1  
 34 100 가 1  
 (7 8)

36 32 (7) (B1 - B4) 25 2 ,  
 (8) (B5 - B8) S\_0 (L, 1L)

B1, B2 B7 B3, B4, B5 B6  
 B3, B4, B5 B6 B1, B2, B7 B8  
 B5, B6, B7 B8 (QR, QL)  
 B1, B2, B3 B4 (1Q) 2  
 (RESET) (R1)가 (Vdd) (11, 12)  
 (D, FRL, F, FLR, FL FR)

36 (1) (CK) (Pp) , (T)  
 (1CK) (1CK) (Pn) (2) (T)  
 1, T2) 36

37 N L SPL IL SPR  
 (3) RESET

36 , 가 , P , T2 , N  
 T1 가 gnd vdd (swing)  
 T1 (11 12)  
 , P 가 B5 B7 (T2)가  
 B1 B1, B2 B3, B4 가 가 P  
 B3가, 가 가

38 34 , 28 IS 가  
 28 (50 51) R R S  
 (7) 34 B1, B2, B5 B6  
 (8) B3, B4, B7 B8

38 (13 16)가 D1 D2  
 28 (11') , (12) 가 R IS  
 (12') IS - (set - override) - R

39A 39B (11 18) , 31 (27 3 25)  
 5) B1 B8 D1 D6 (B1 B8) 36 S\_O  
 R1 9 5 S\_O S\_O2 36  
 가

39a 39b CK 가 P P  
 , CK 가 , CK ICK  
 (swap) 가  
 CMOS ( )  
 LSI (large scale integration) - -

40 , N x M  
 (40) (42) (41)  
 (43) (42) 4 39b  
 (44)  
 45) (46) (45) 4 39b (

(42)

(45)

가 ,  
 가 ,  
 가 ,  
 ( ' ' ' ' )  
 가 ,

(57)

1.

N

i 가,

(i - 1)

( , a 1 , 1 < i (N - a) )  
 - ;

(set signal)

(reset signal)

, (i+a)

2.

1 ,

3.

1 , i (i+2)

4.

1 , i (i+1)

5.

1 , i (i+1)

6.

5 ,

7.

1 , (1+a)<sup>2</sup>  
 - ; 1

8.

1 , (N - 1)  
 - ; N N (N - 1)

9.

1 , i , (i - a) (i+1)  
 1

10.

7 , 1 , 2  
 2 , 1

11.

8 , N ,  
 (N - 1) 2

12.

1 ,

13.

1 ,

14.

1 ,

15.

1 , , .

16.

15 , - 가

17.

1 , 2 .

18.

14 , .

19.

18 , .

20.

19 , .

21.

19 , .

22.

1 , .

23.

15 , .

24.

23 , ,

25.

1 , .

26.

1 , .

27.

1 , 가 가 2 ; 1 2 1  
;  
1 2 가 1 2 1 2 ,  
2 2 .

28.

27 , 1 , 2 .

29.

28 , 1 1 , 1 , 2 , 1  
1 , 1 ; 1 2 , 2 , 1  
2 .

30.

29 , 1 2 .

31.

29 , 1 2 , 1 2 가  
1 2 .

32.

28 , 2 , 1 , 2 1  
3 4 ; 2 , 2 1  
2 5 6 ,  
3 5 1 2 2 , 4 6  
1 2 .

33.

32 , 3 5 가  
2 .

34.

33 , 가 1 2 .

35.

27 7 , 1 1 , 2 1 , 1 7 ;  
8 ,

7 8 1 .

36.

1 , CMOS .

37.

1 .

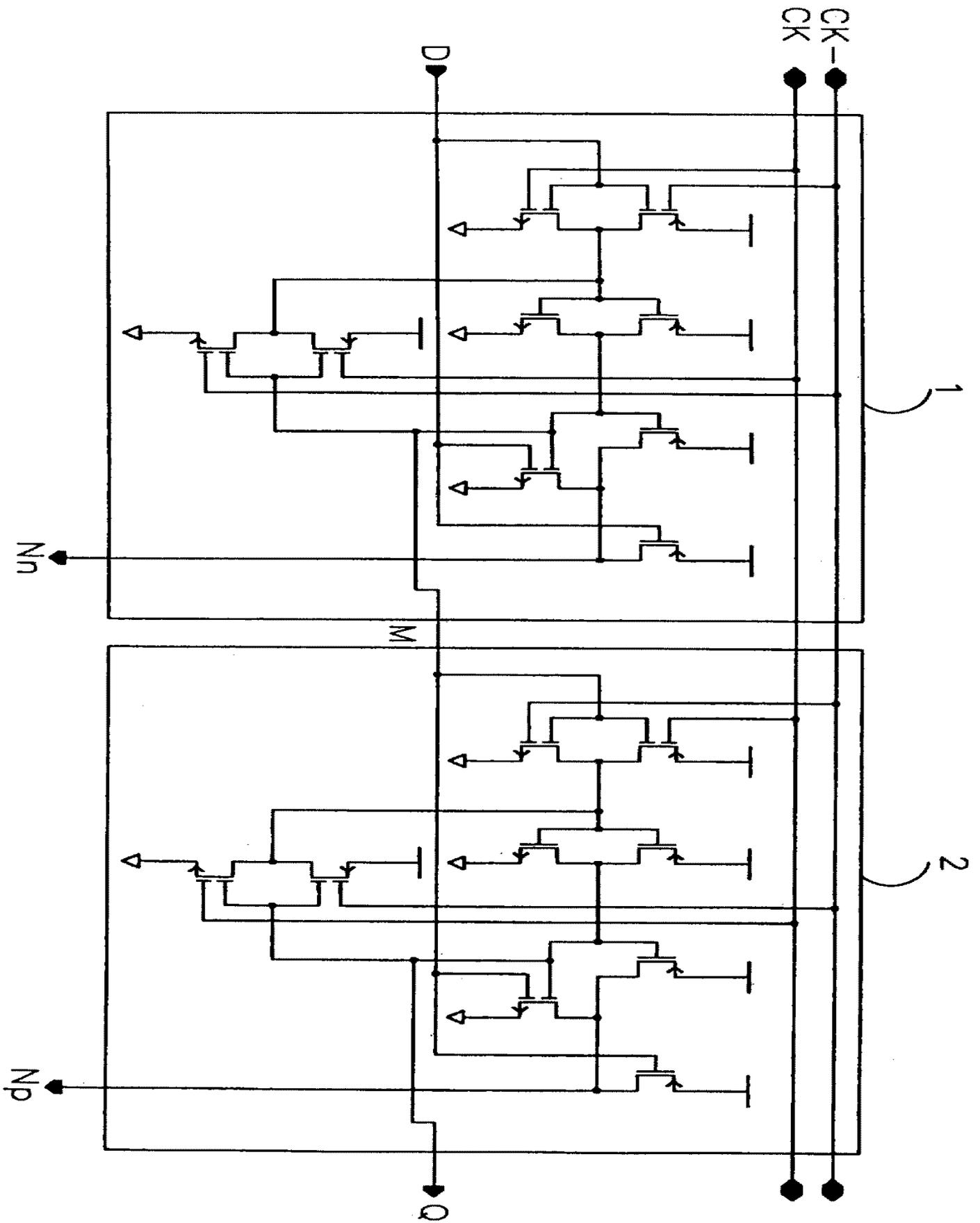
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37 , .

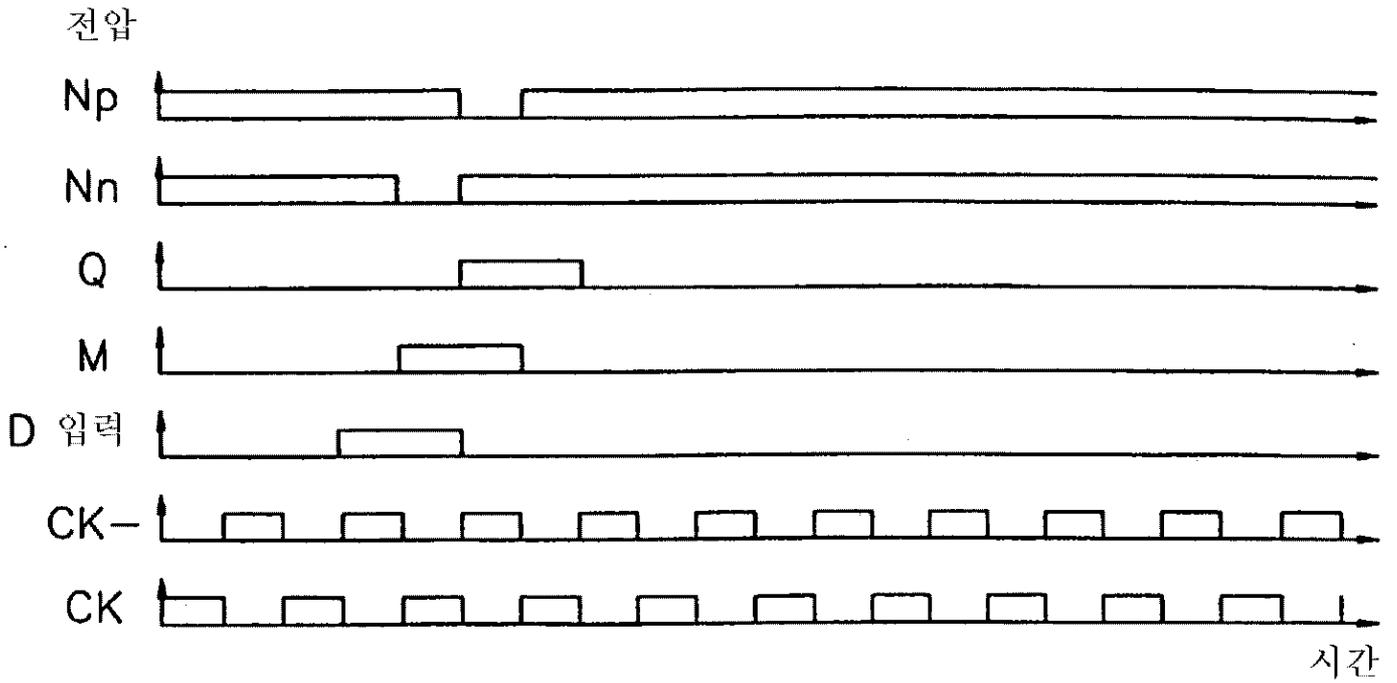
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37 .

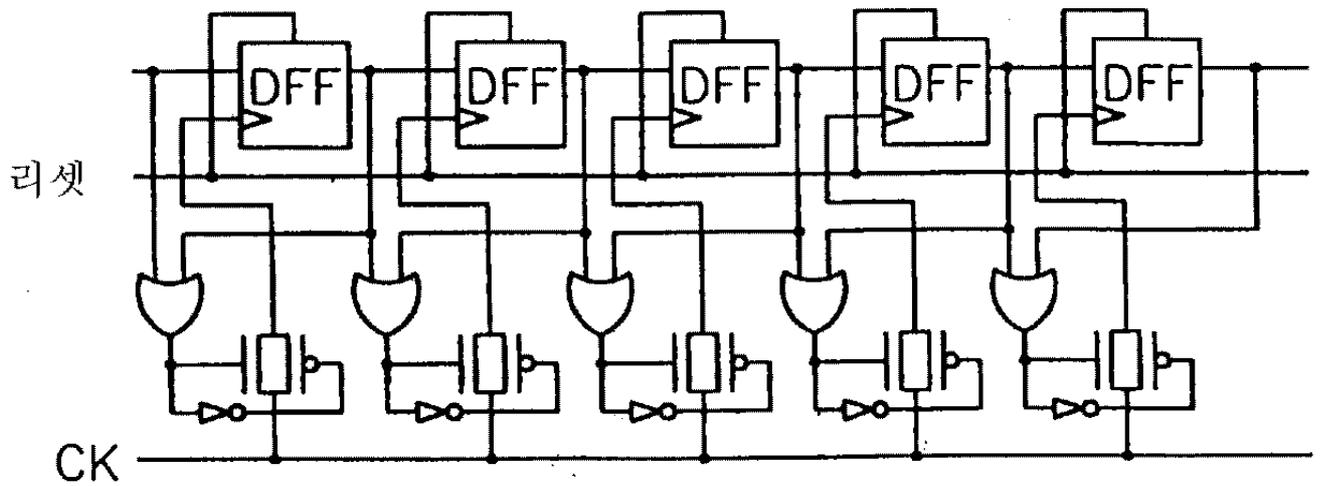
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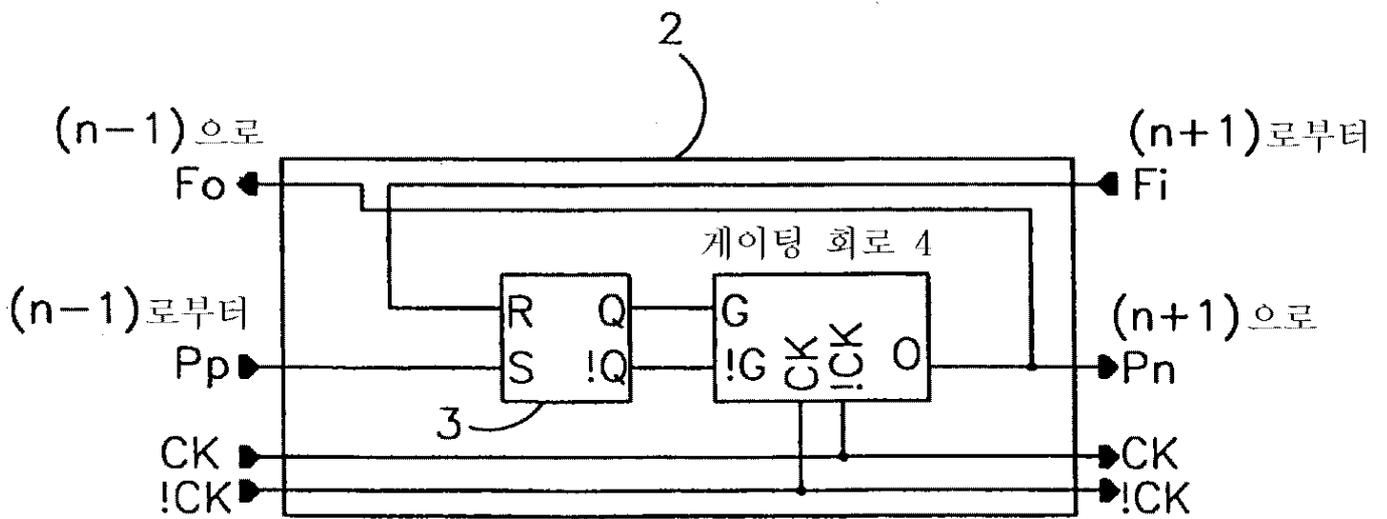
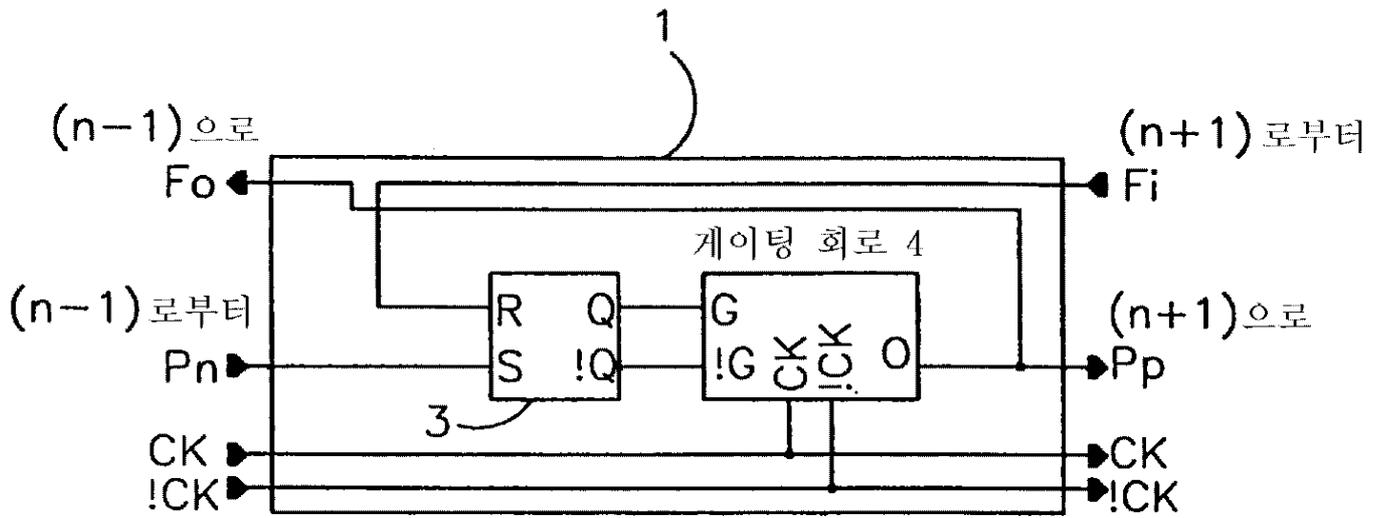
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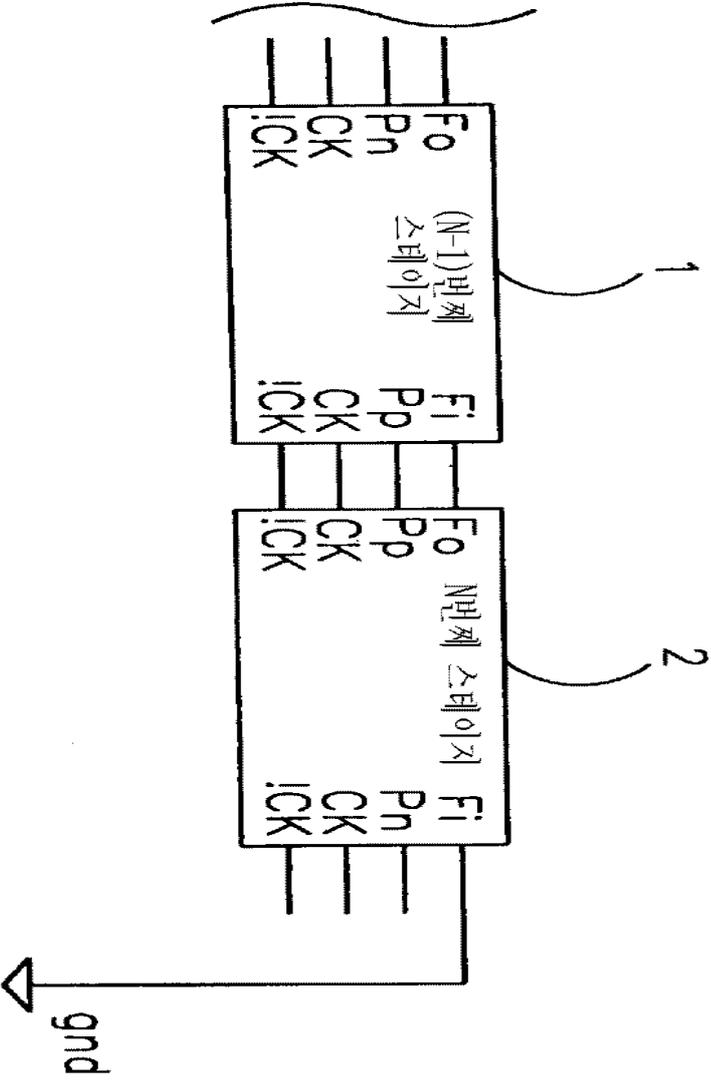
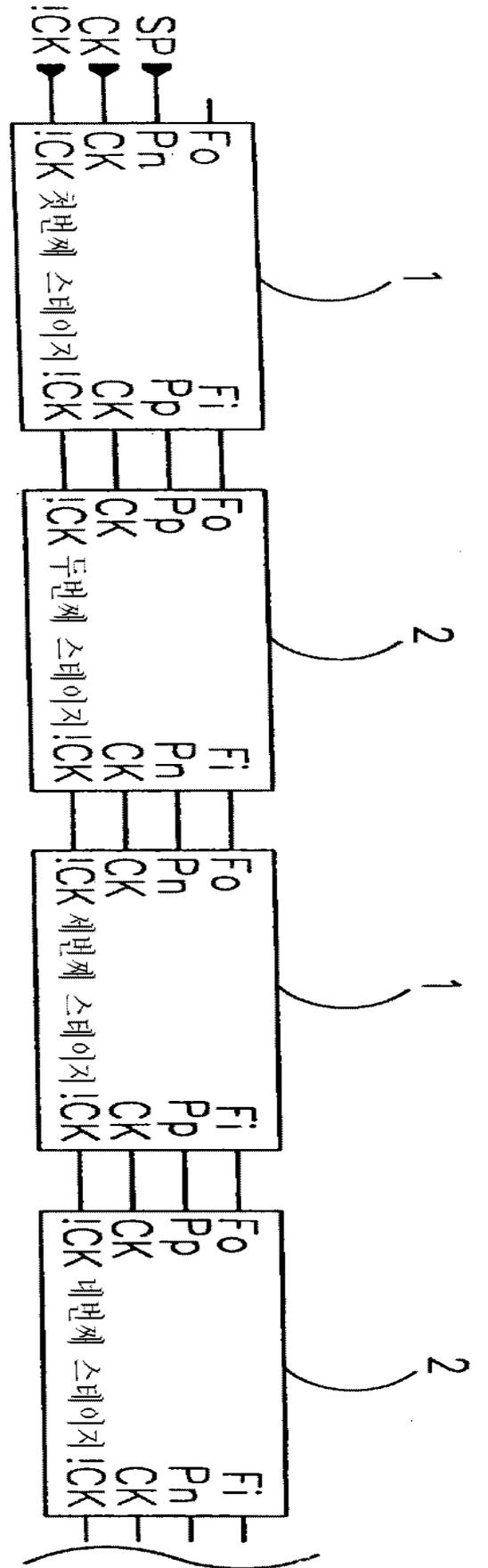
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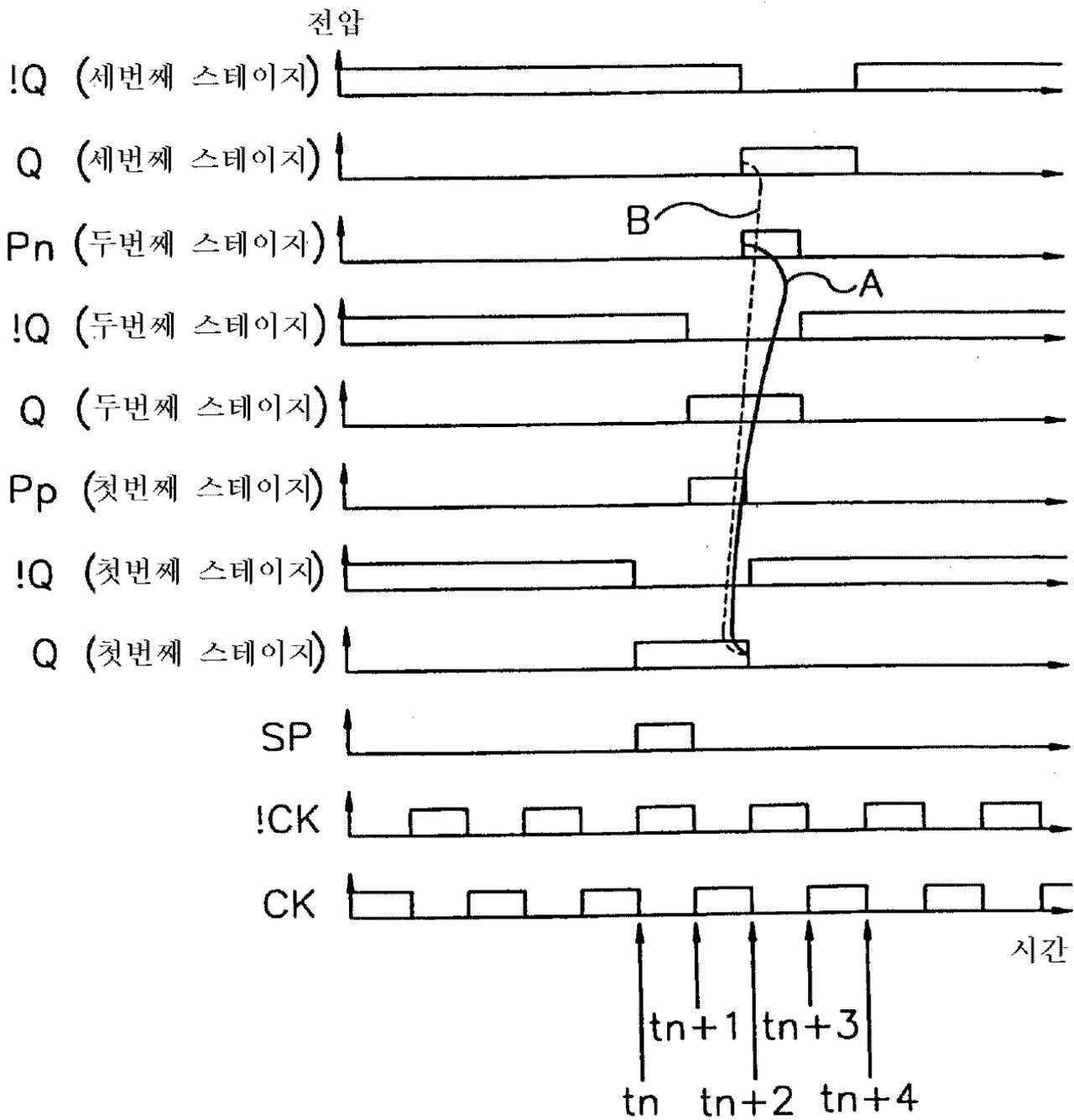


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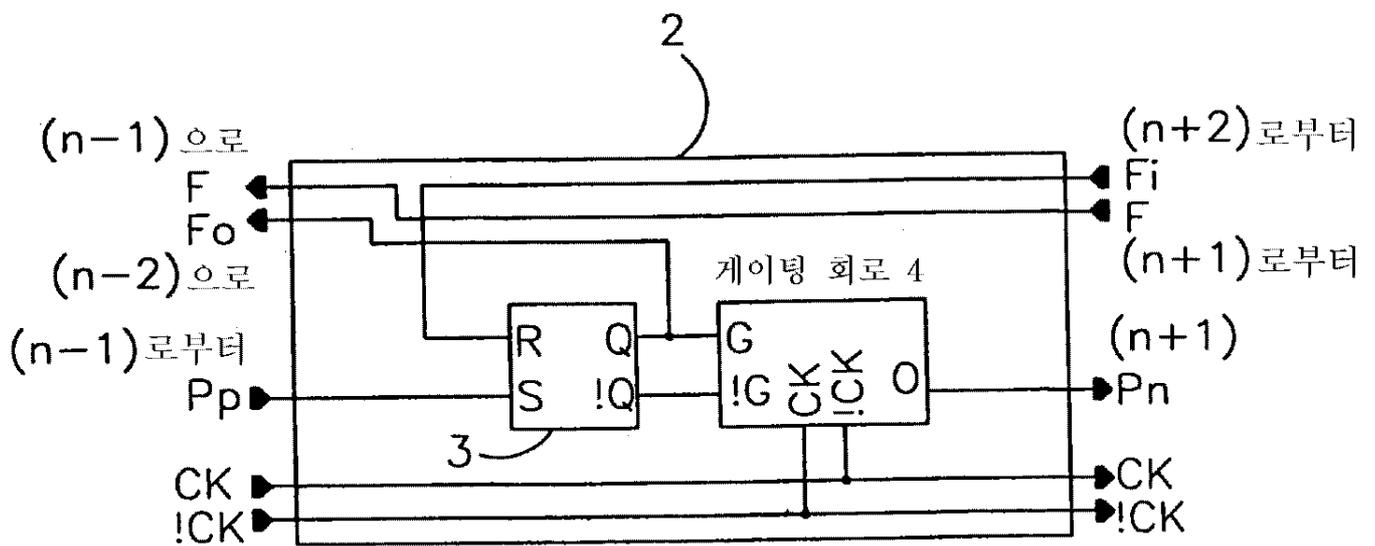
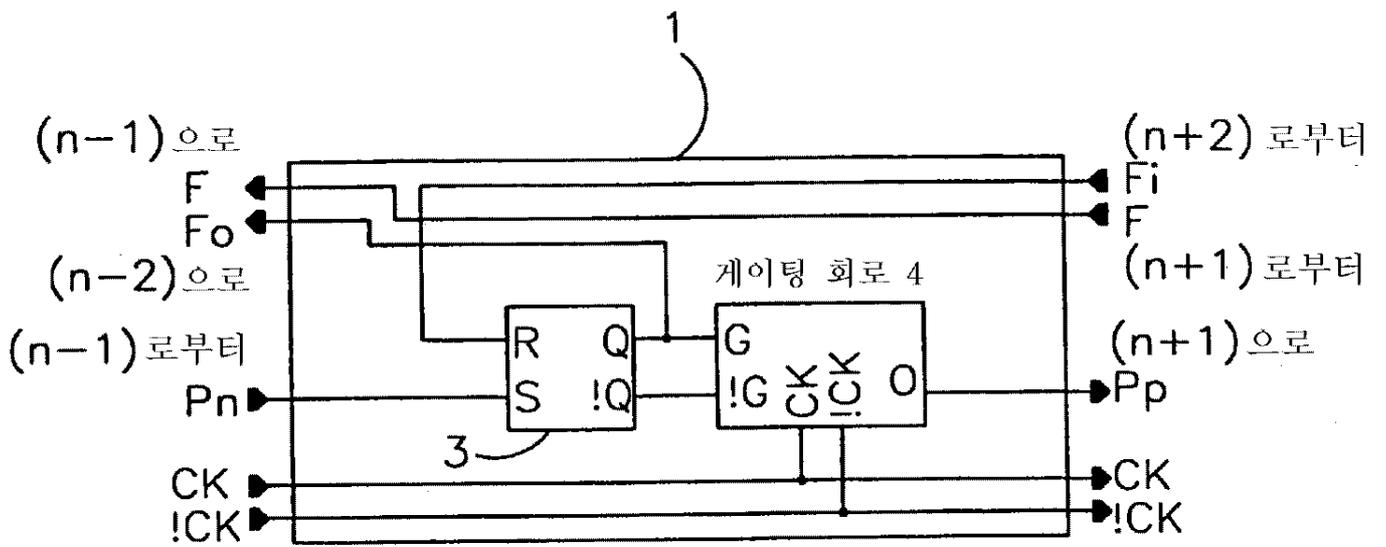


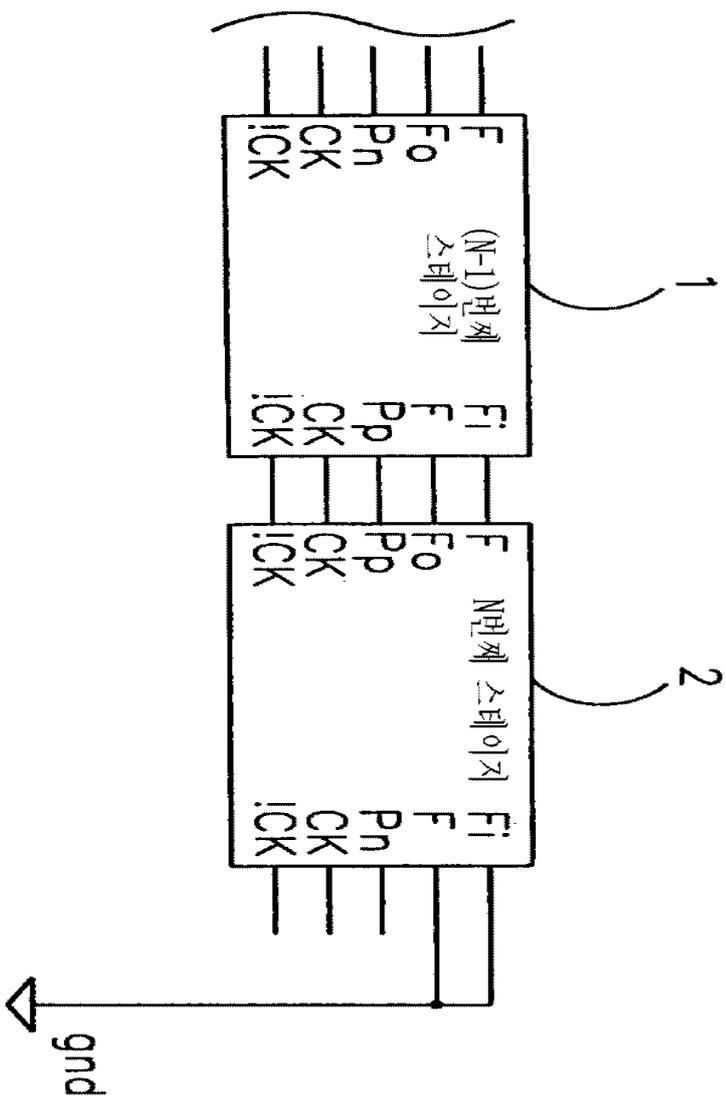
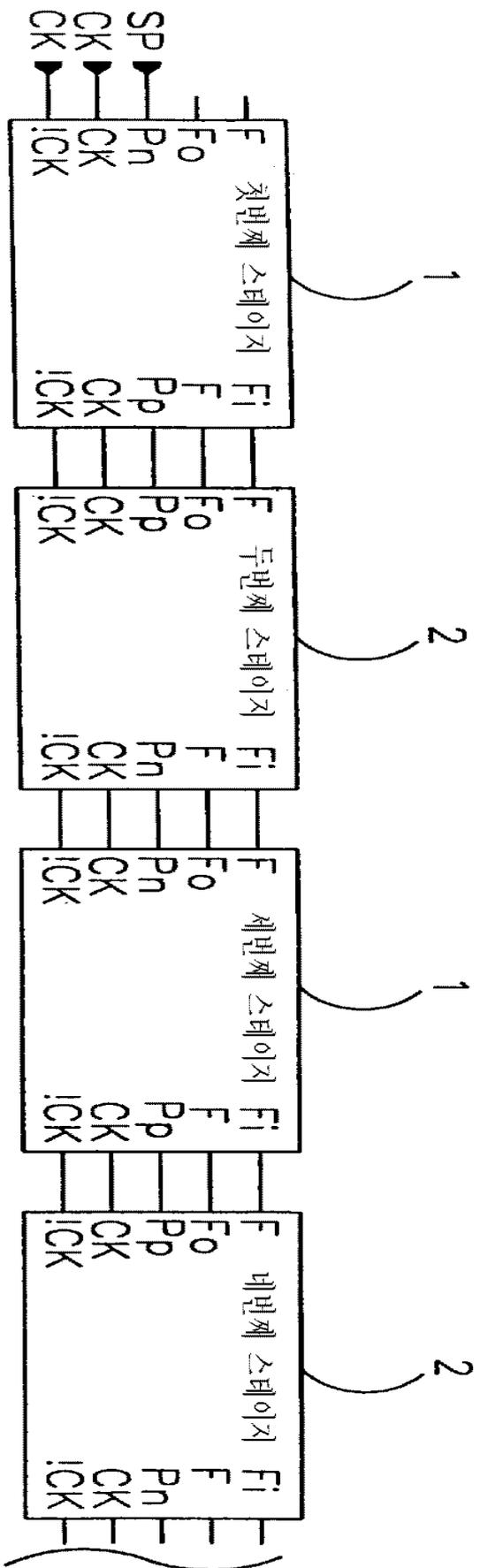
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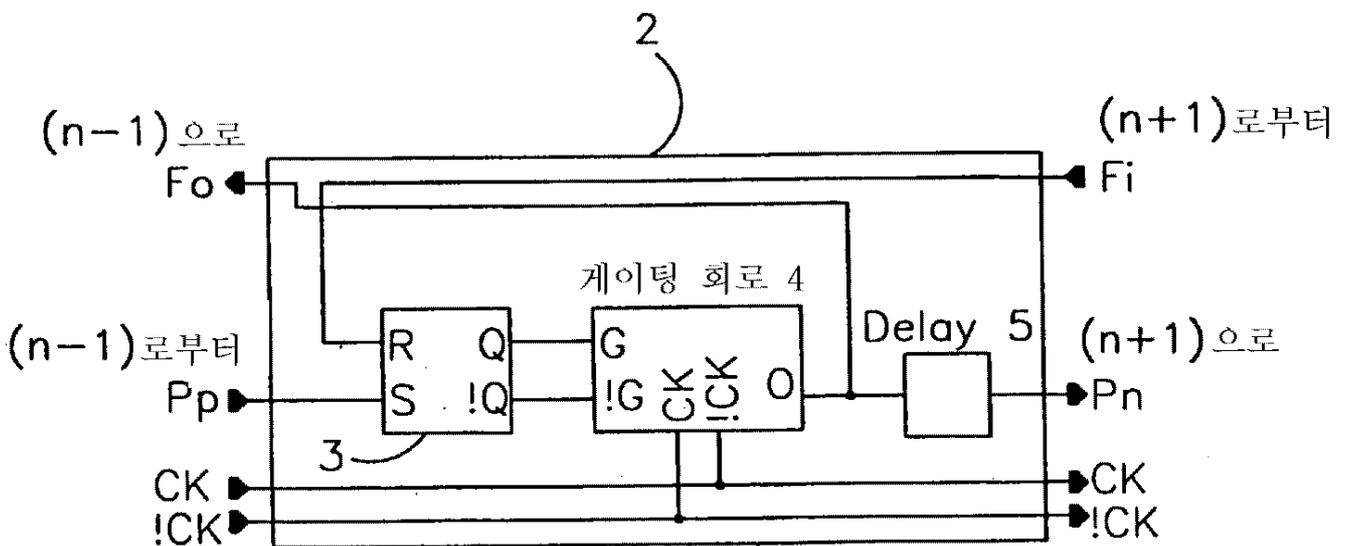
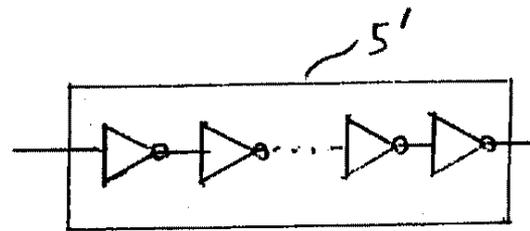
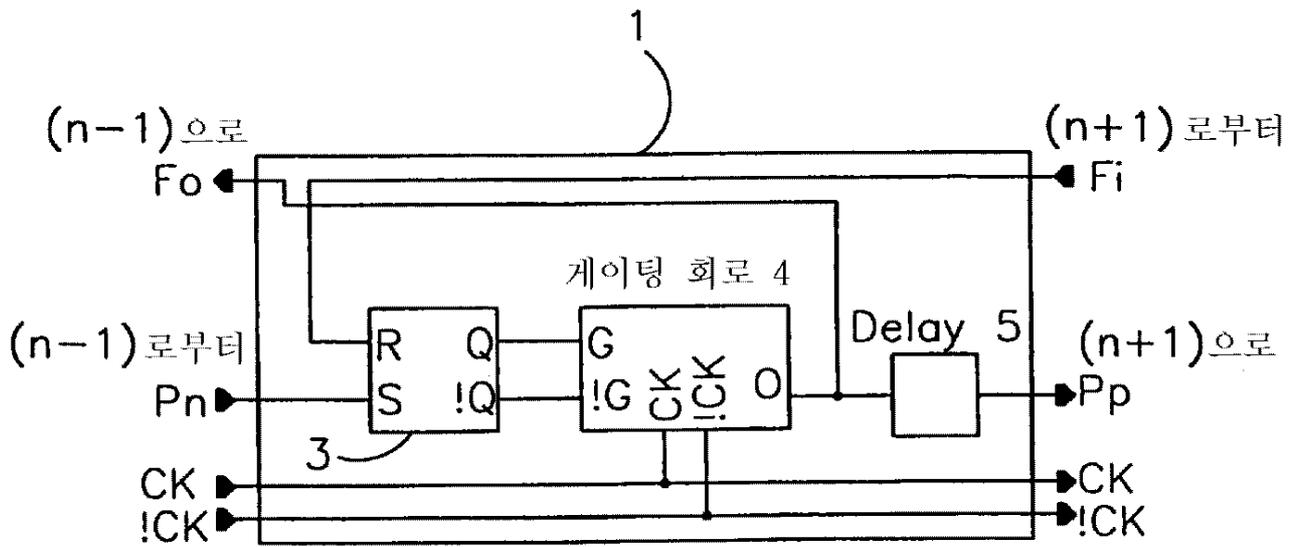




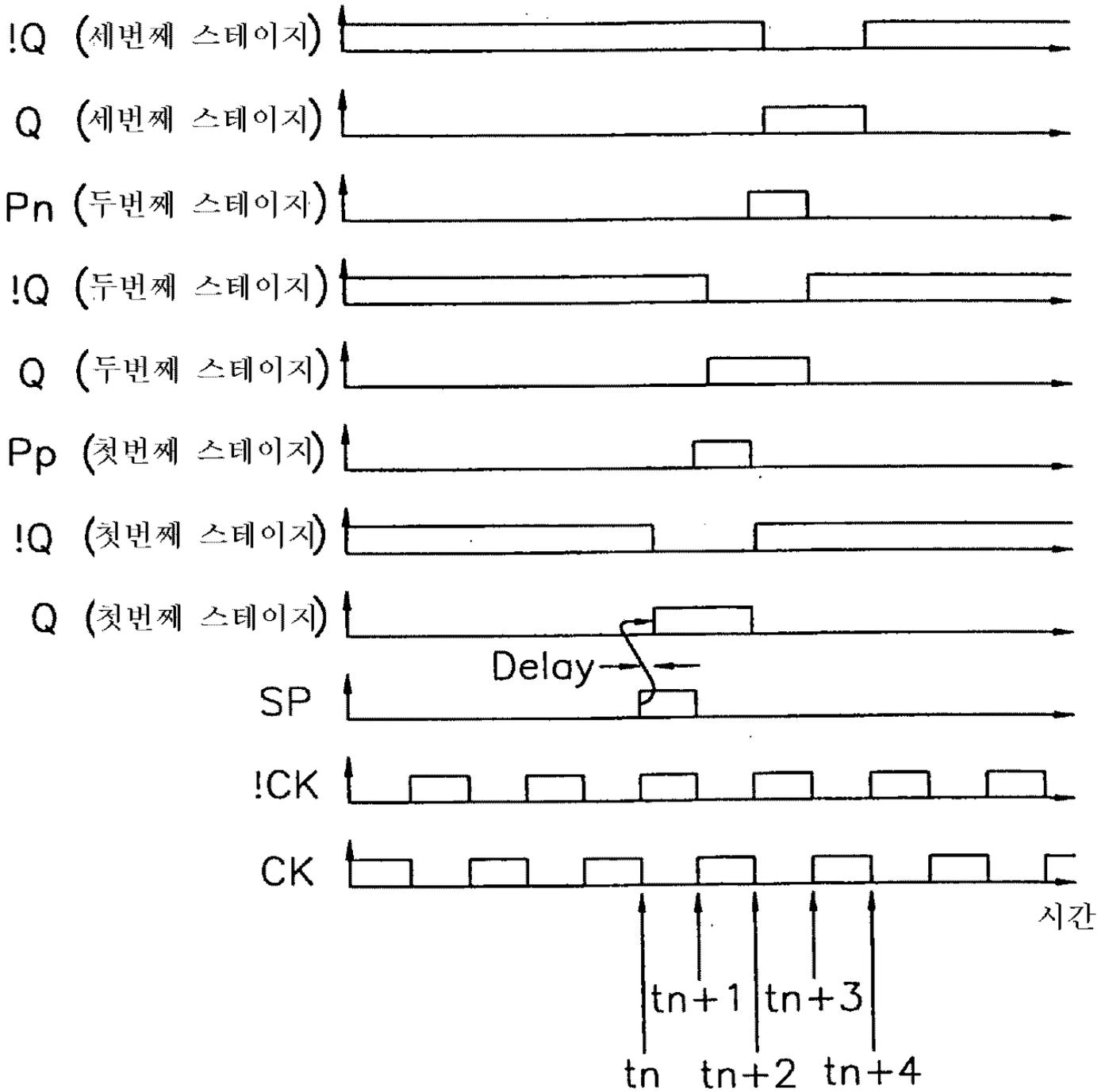
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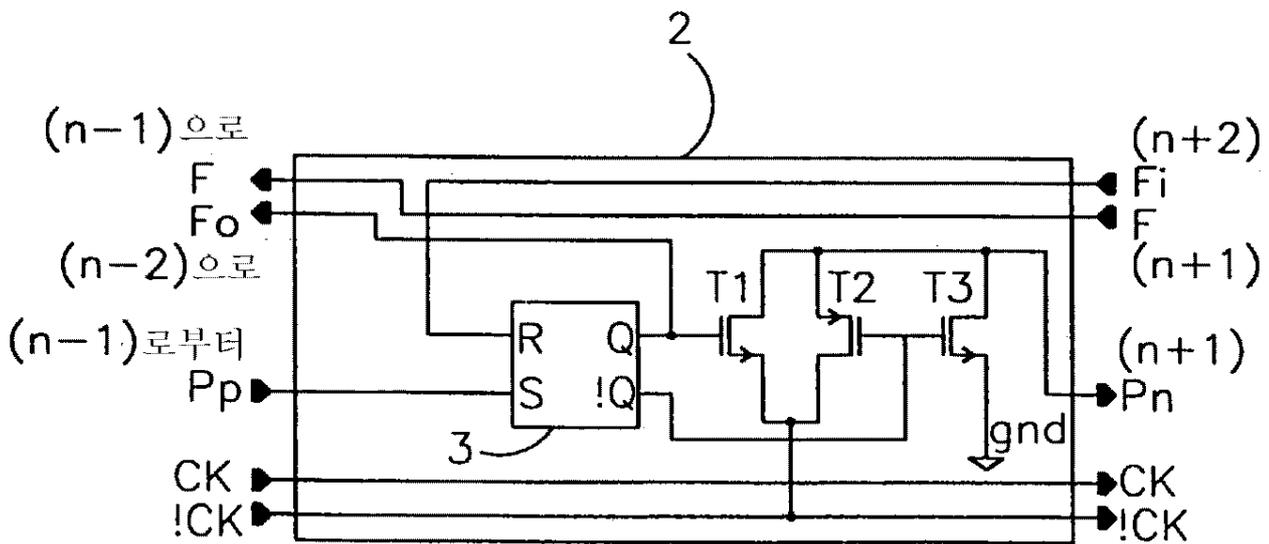
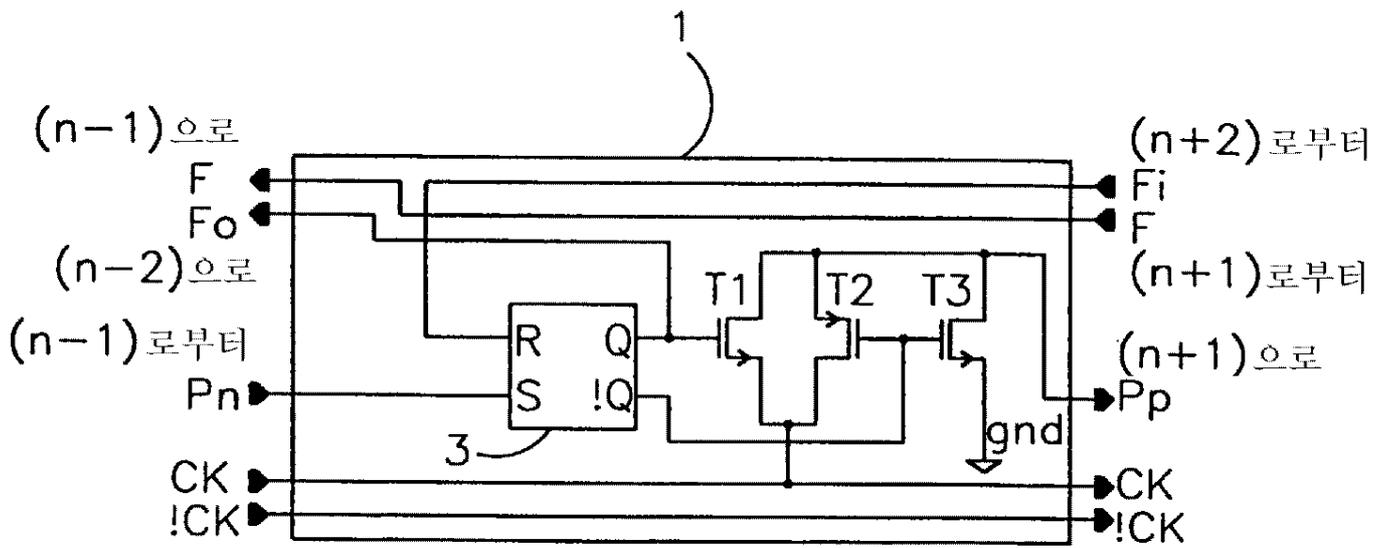




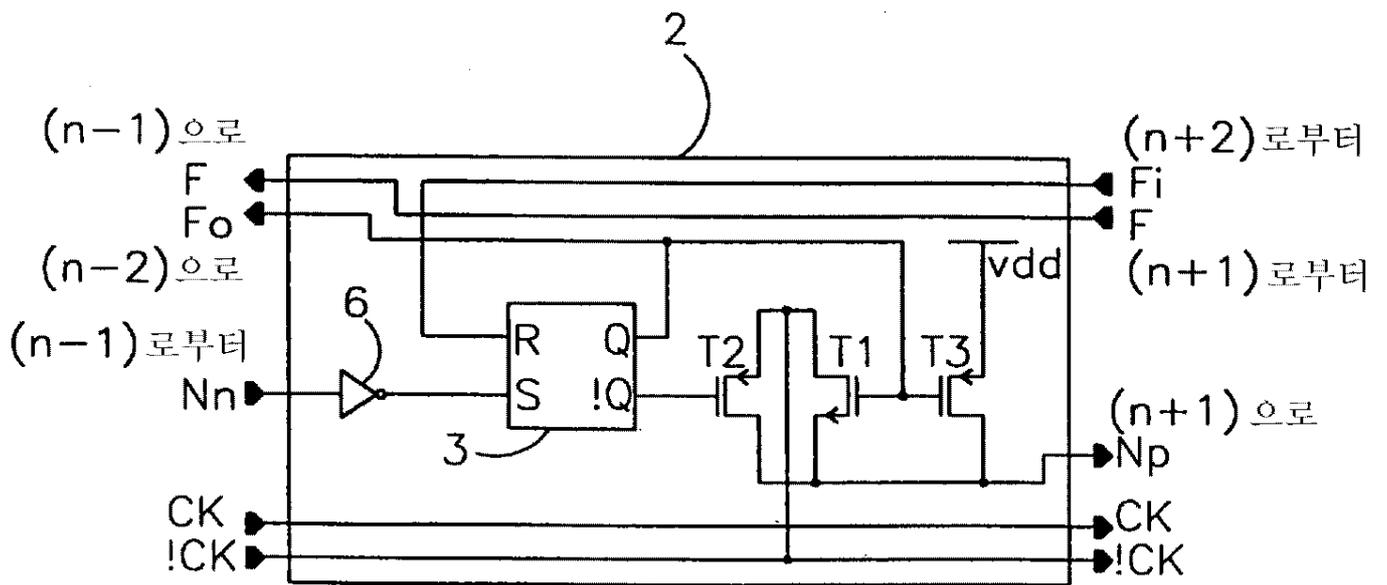
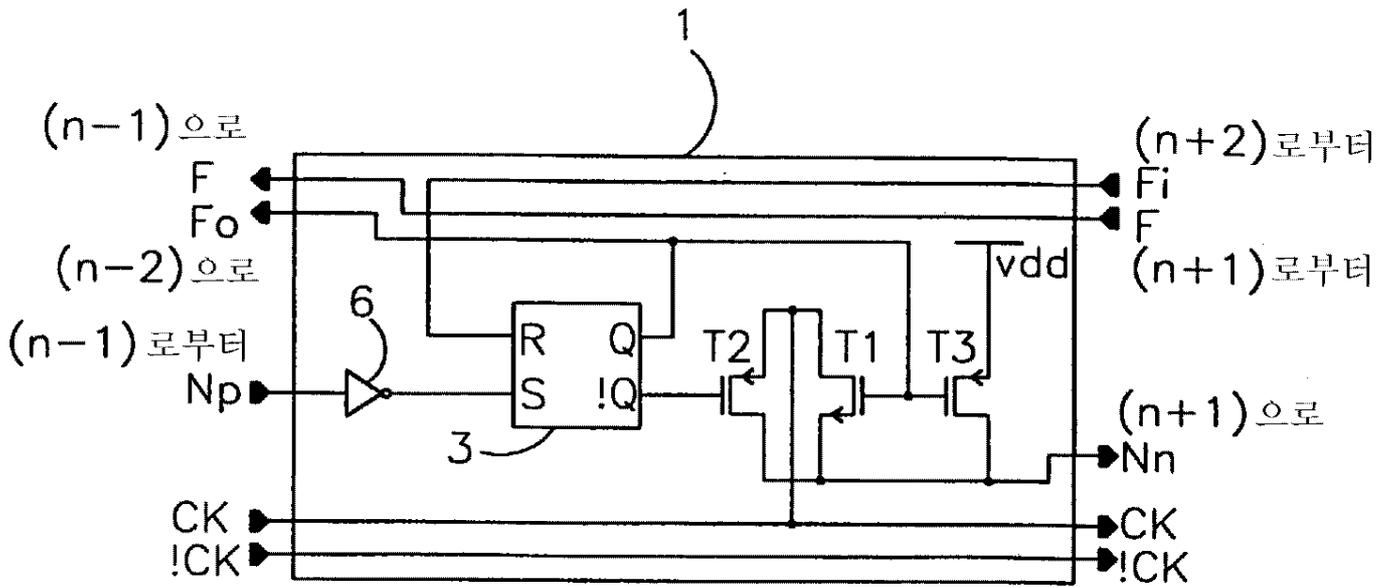
전압



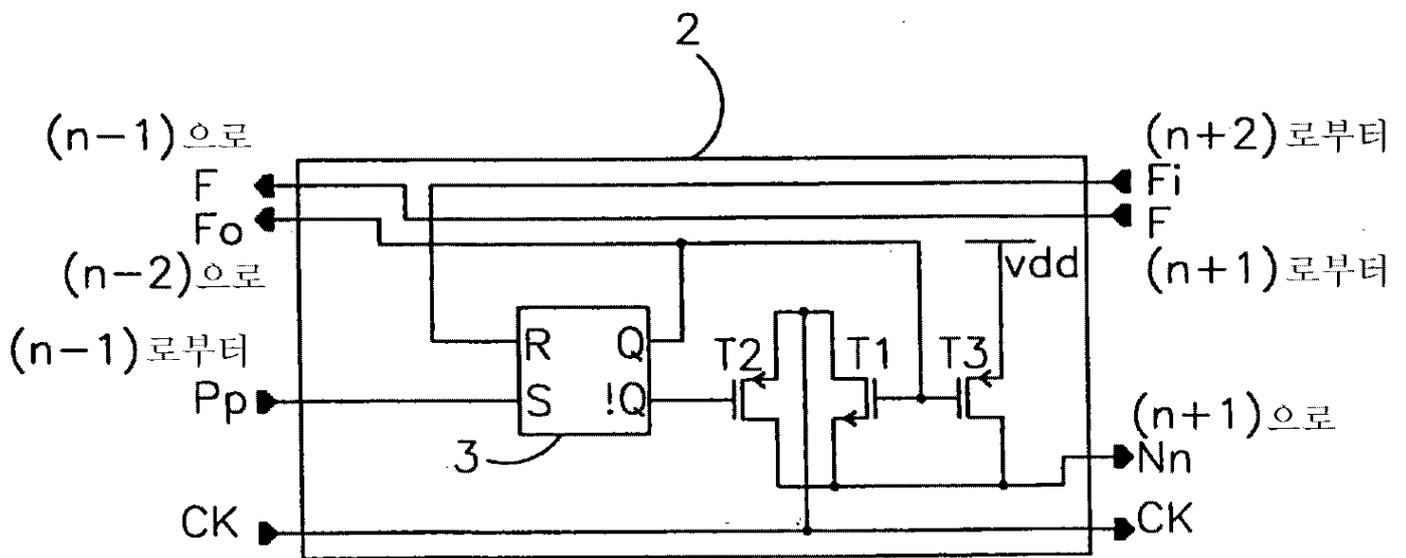
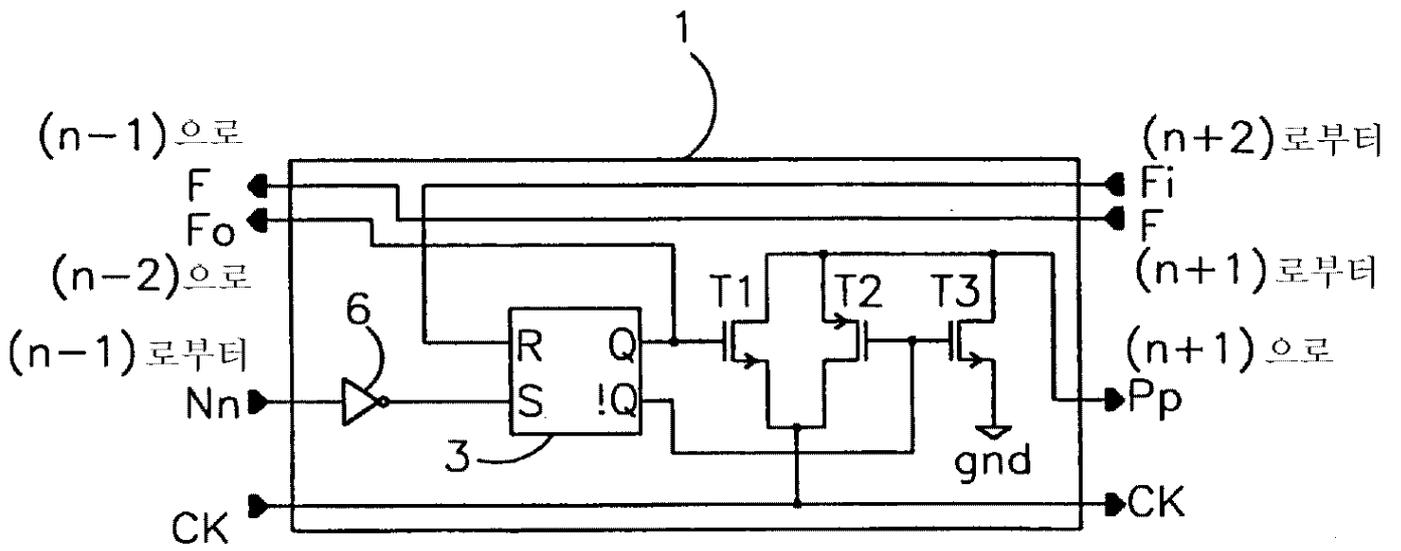
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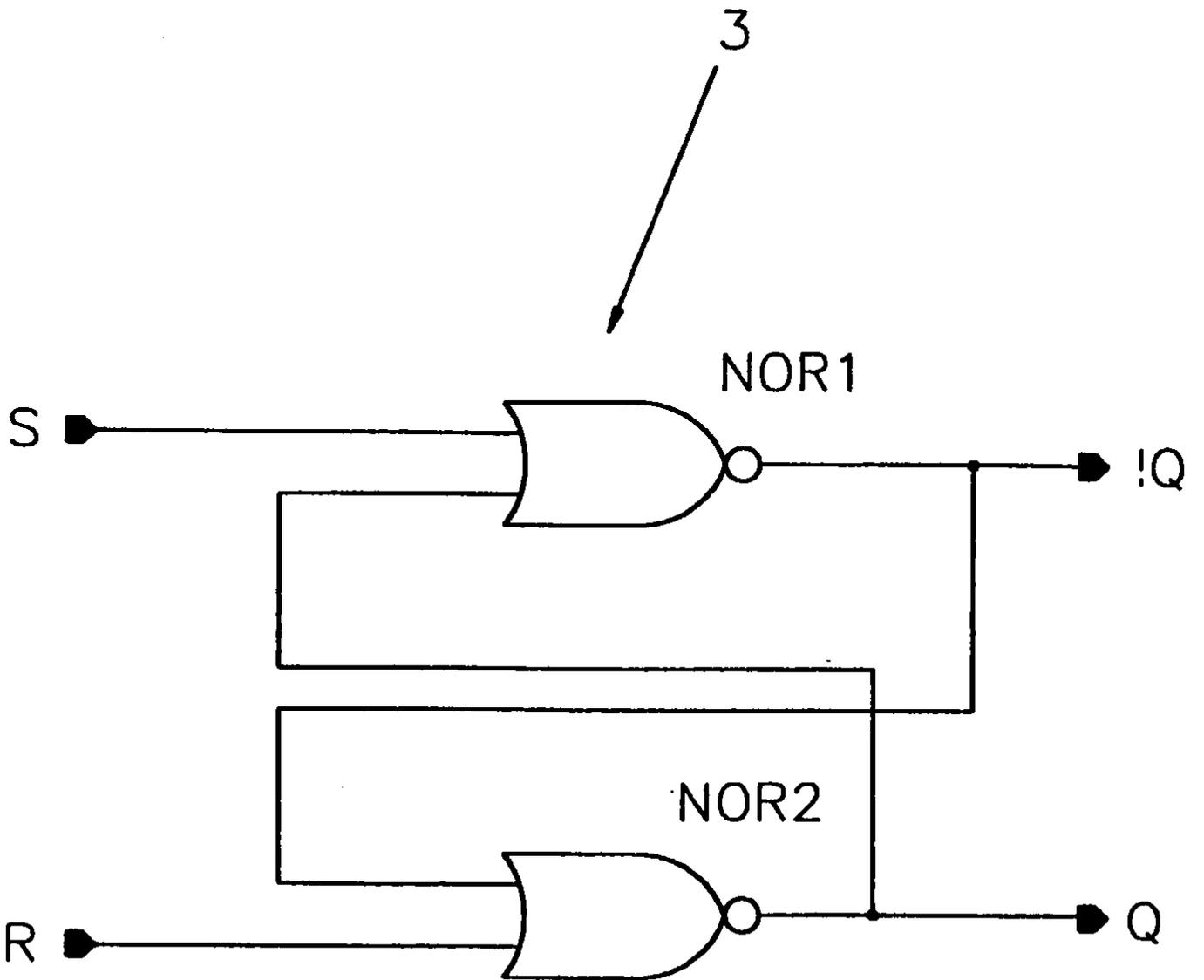


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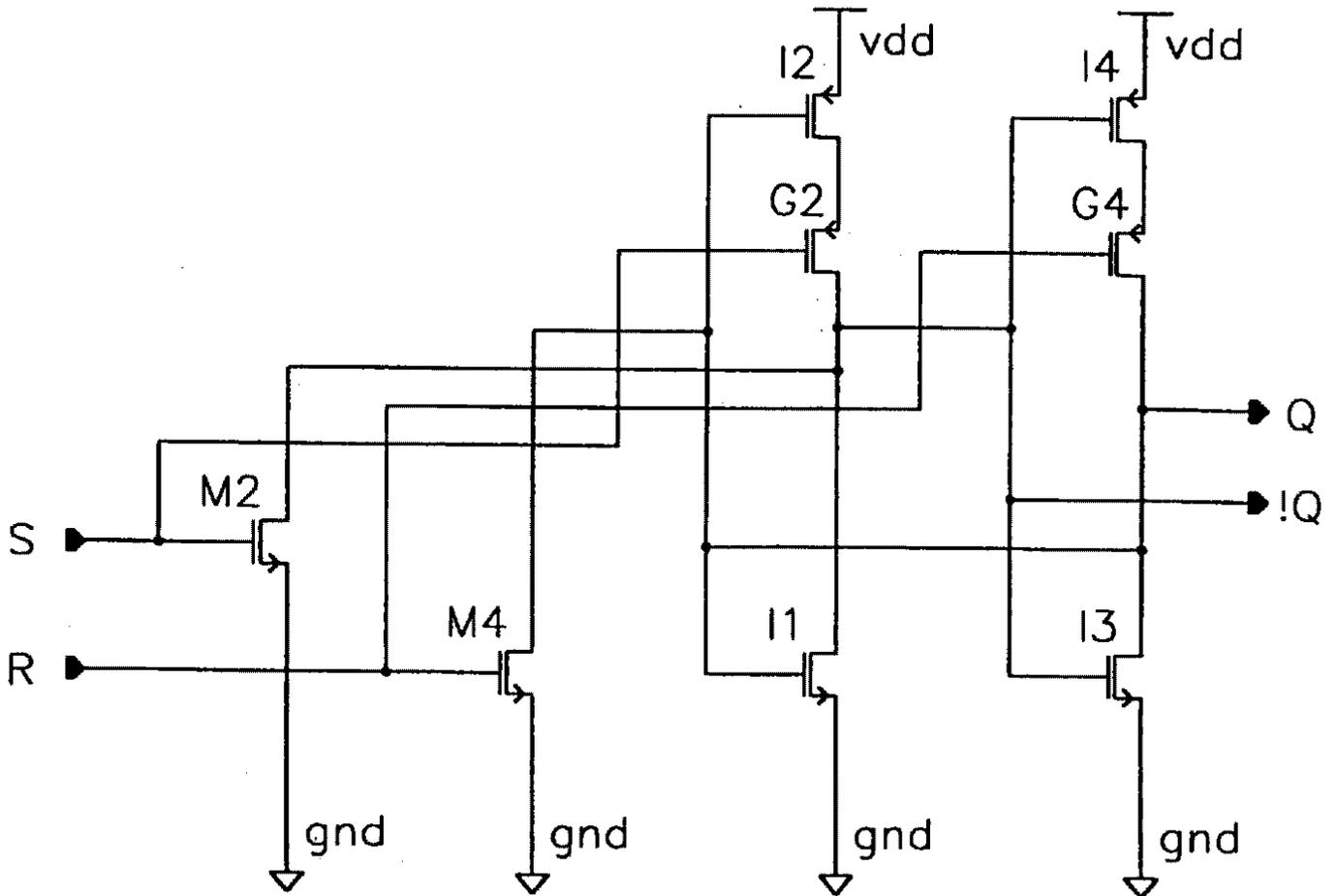
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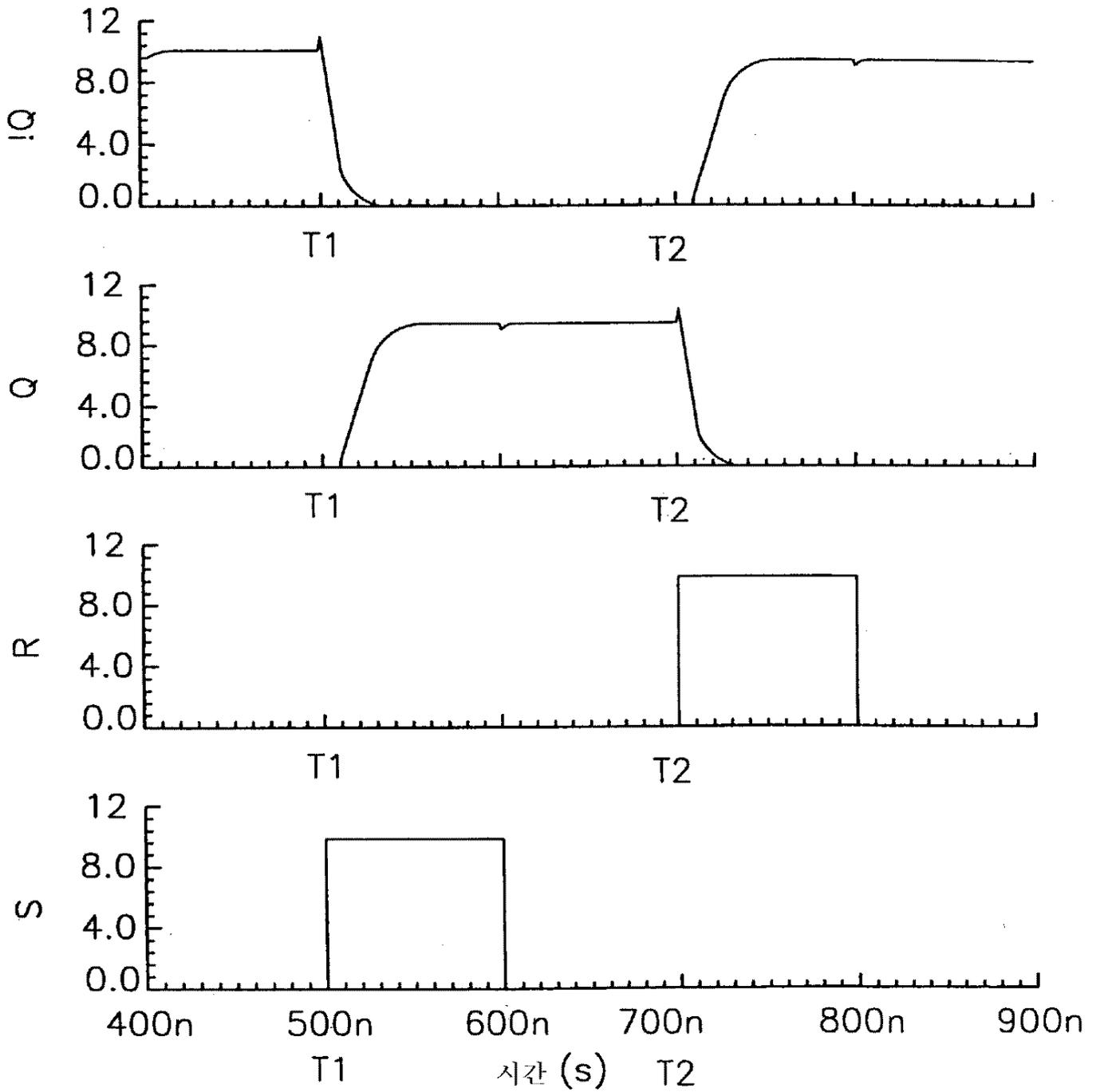


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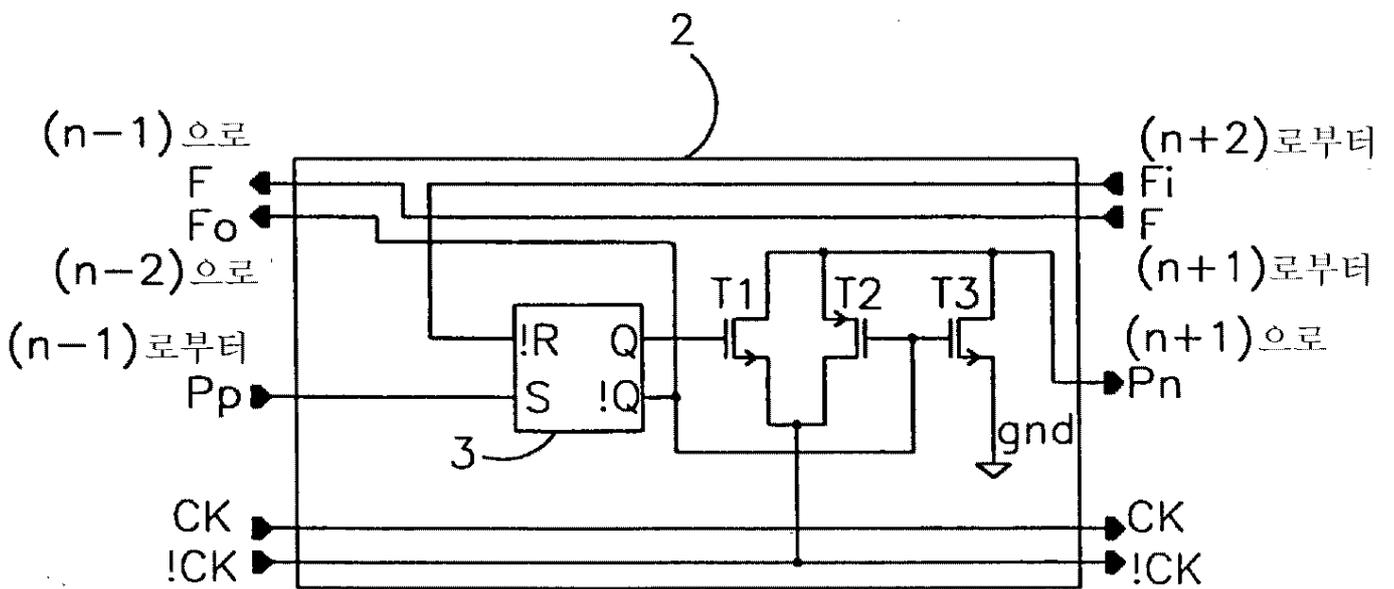
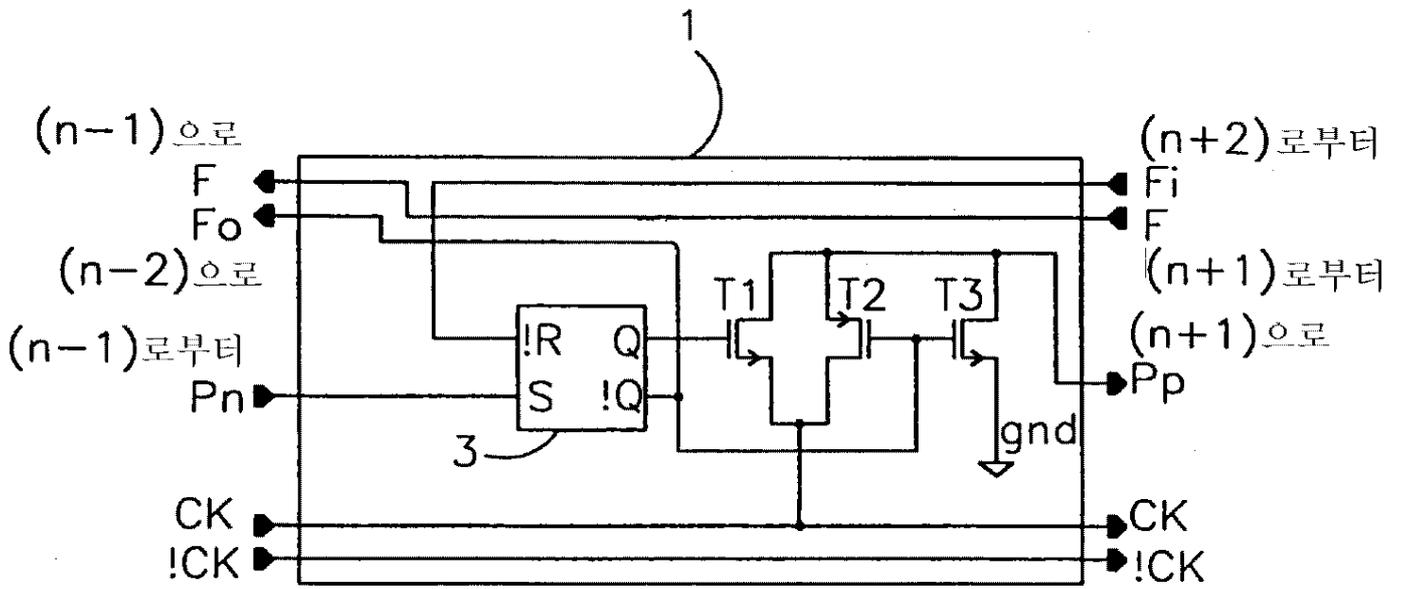
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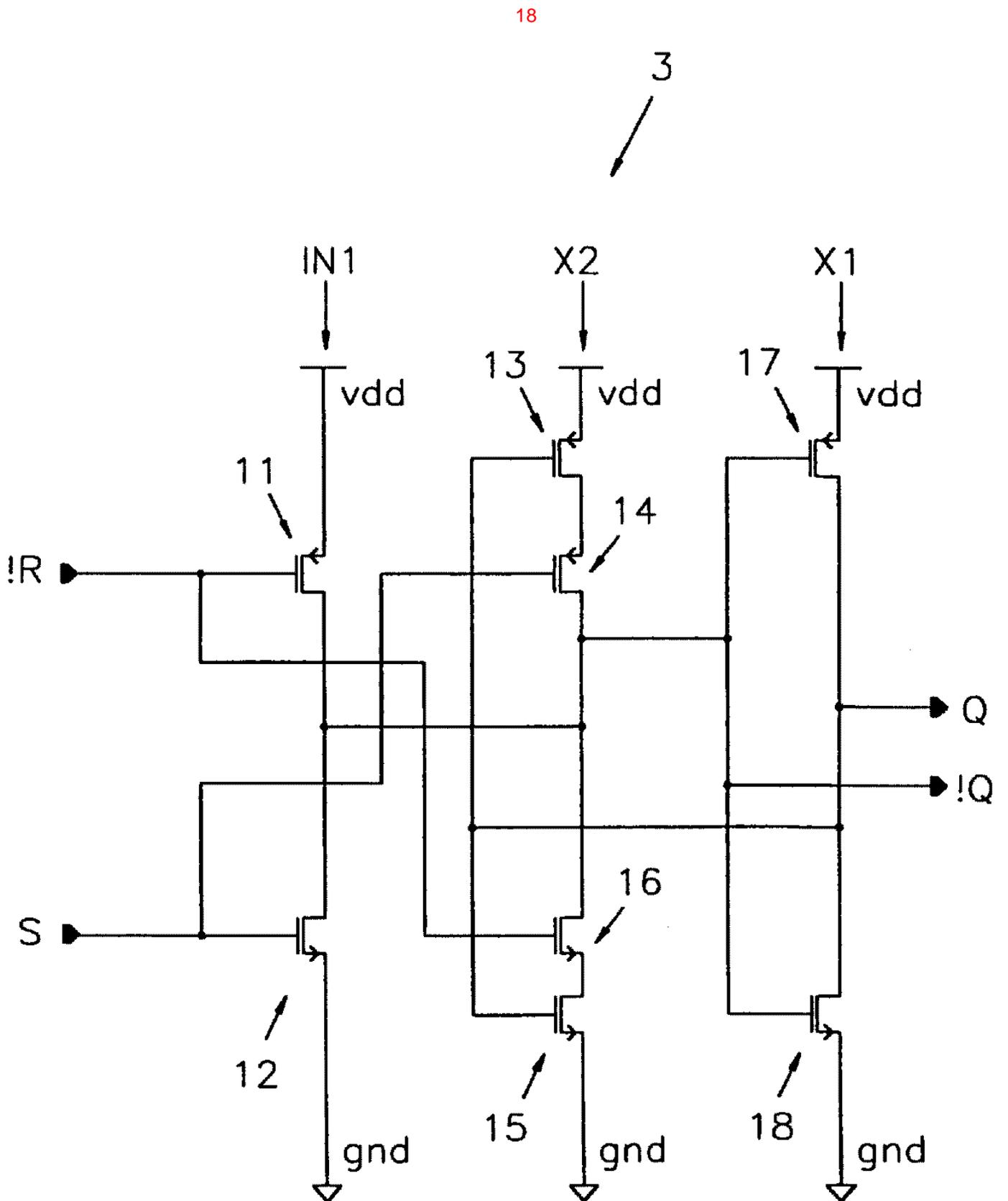


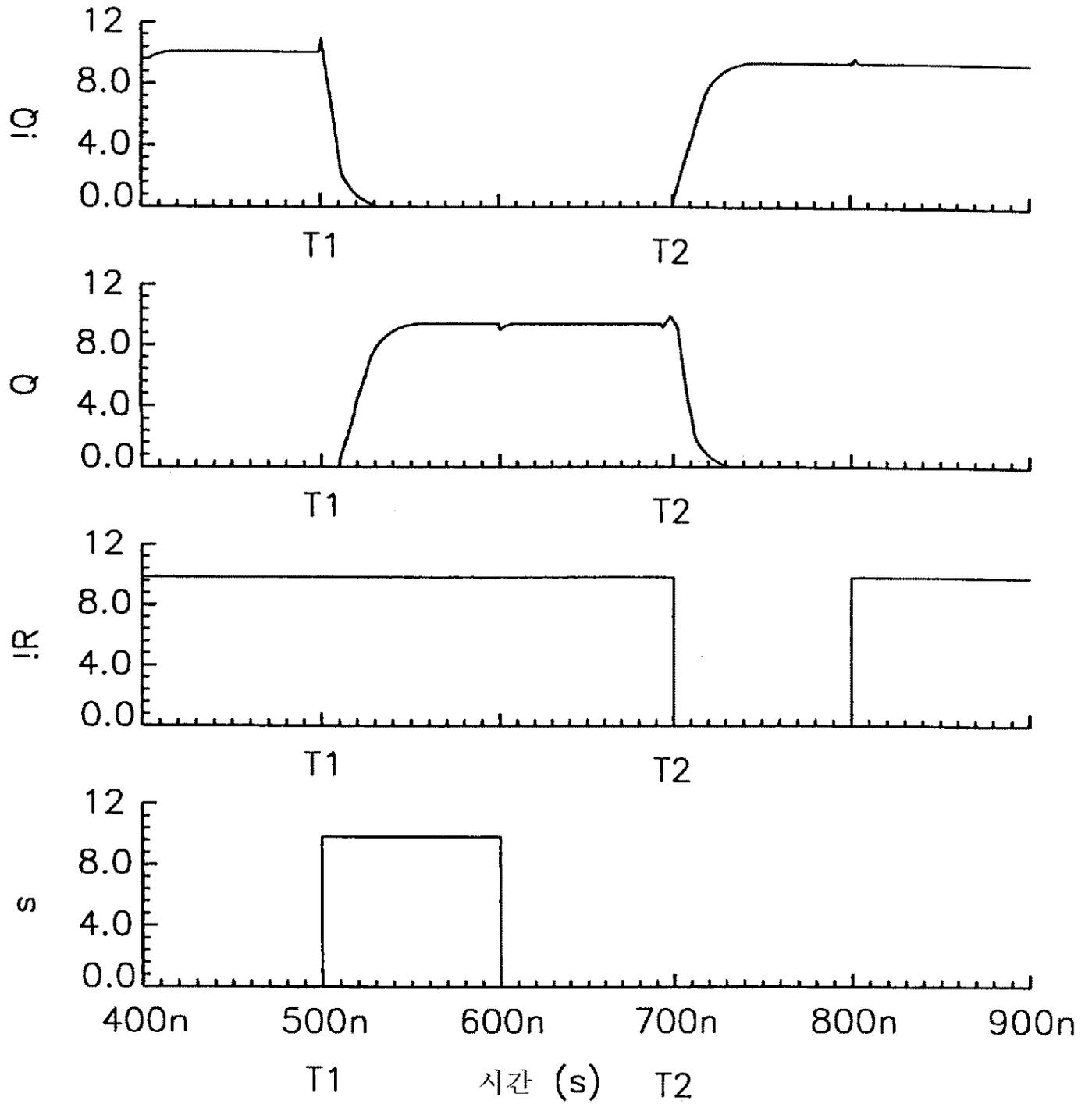
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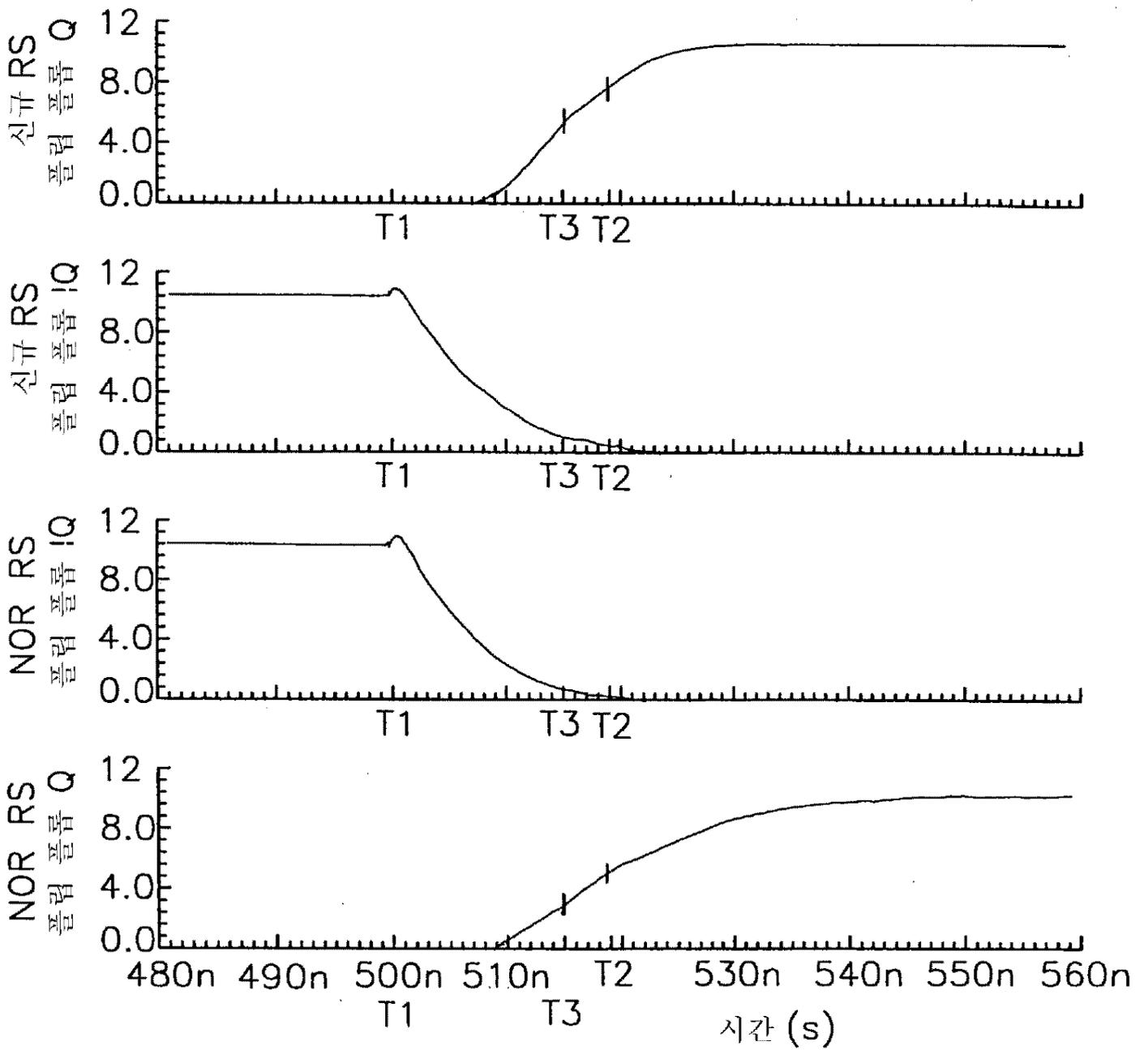
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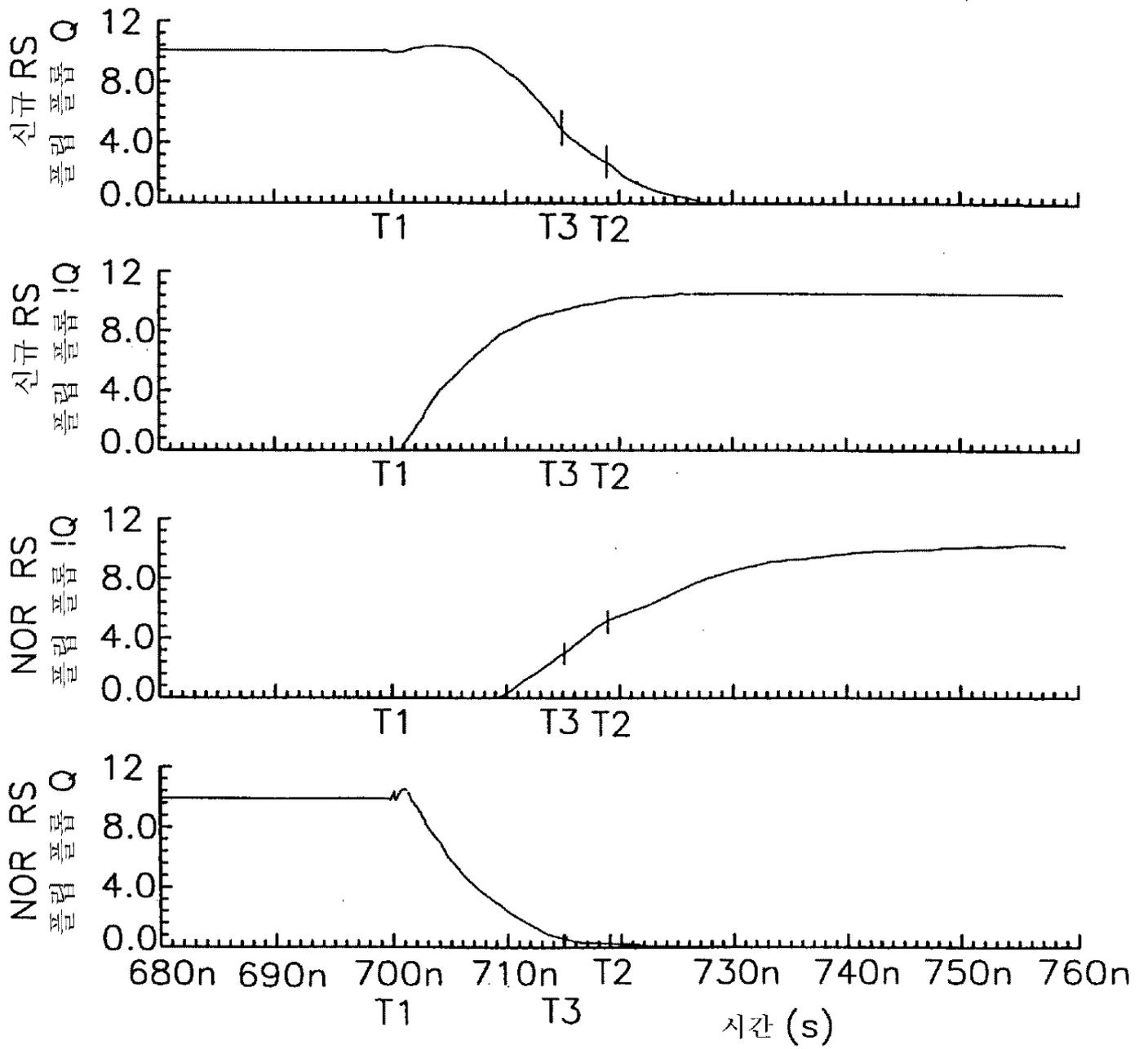


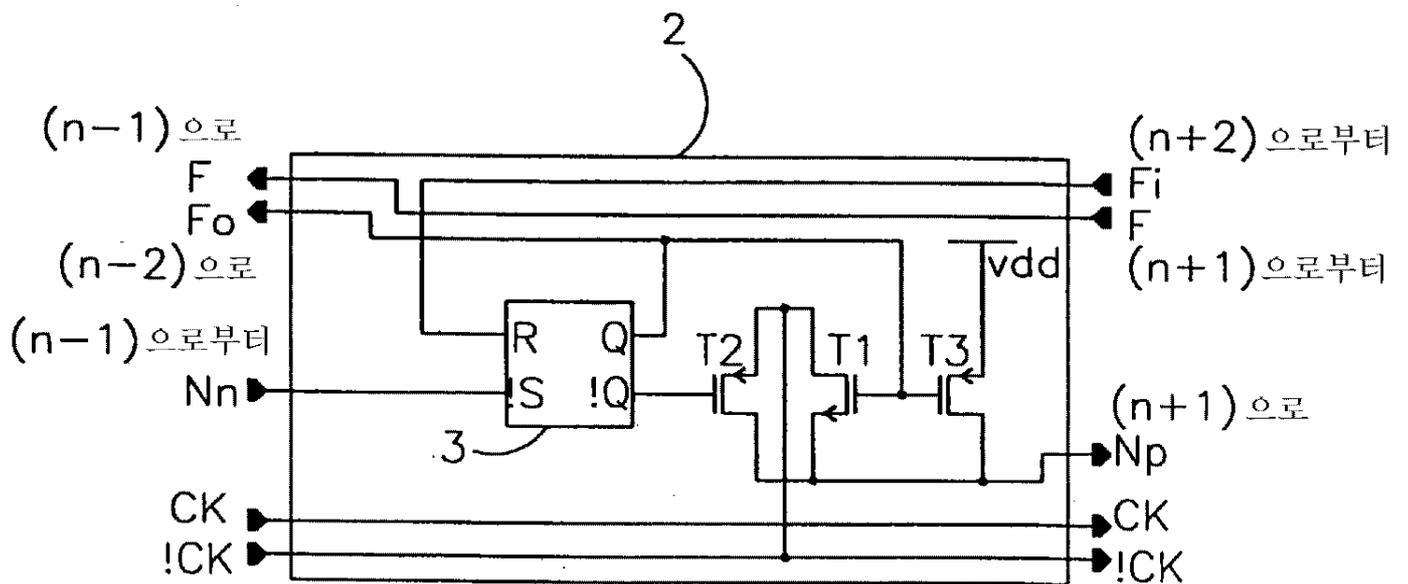
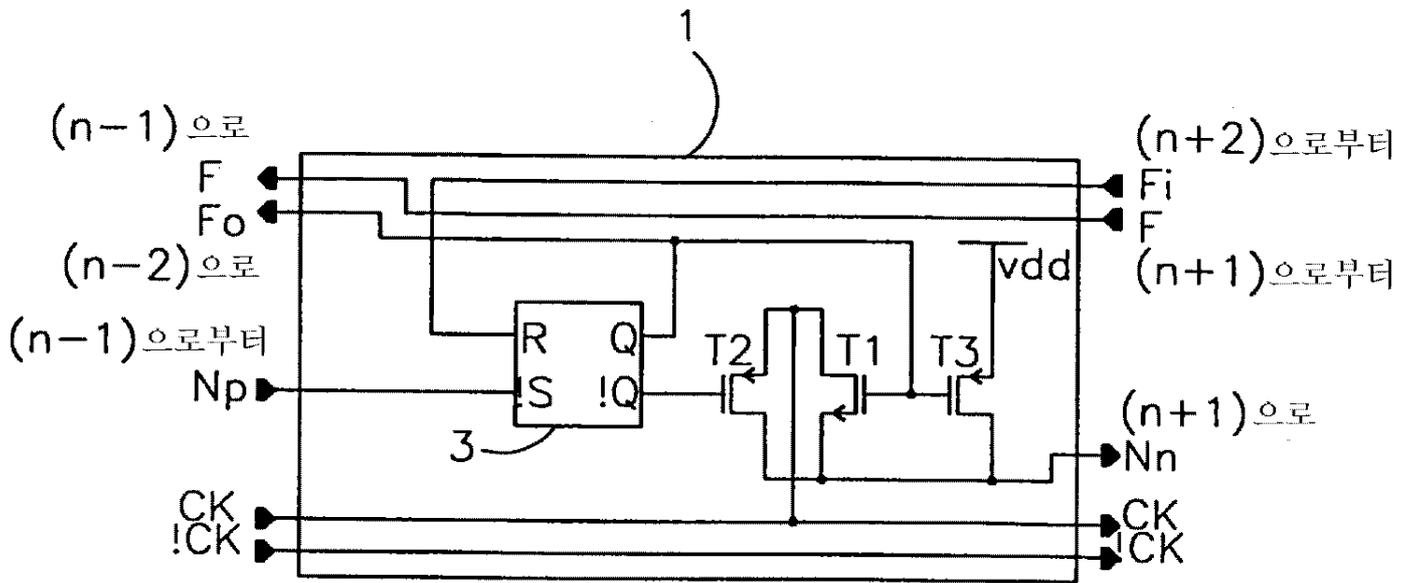


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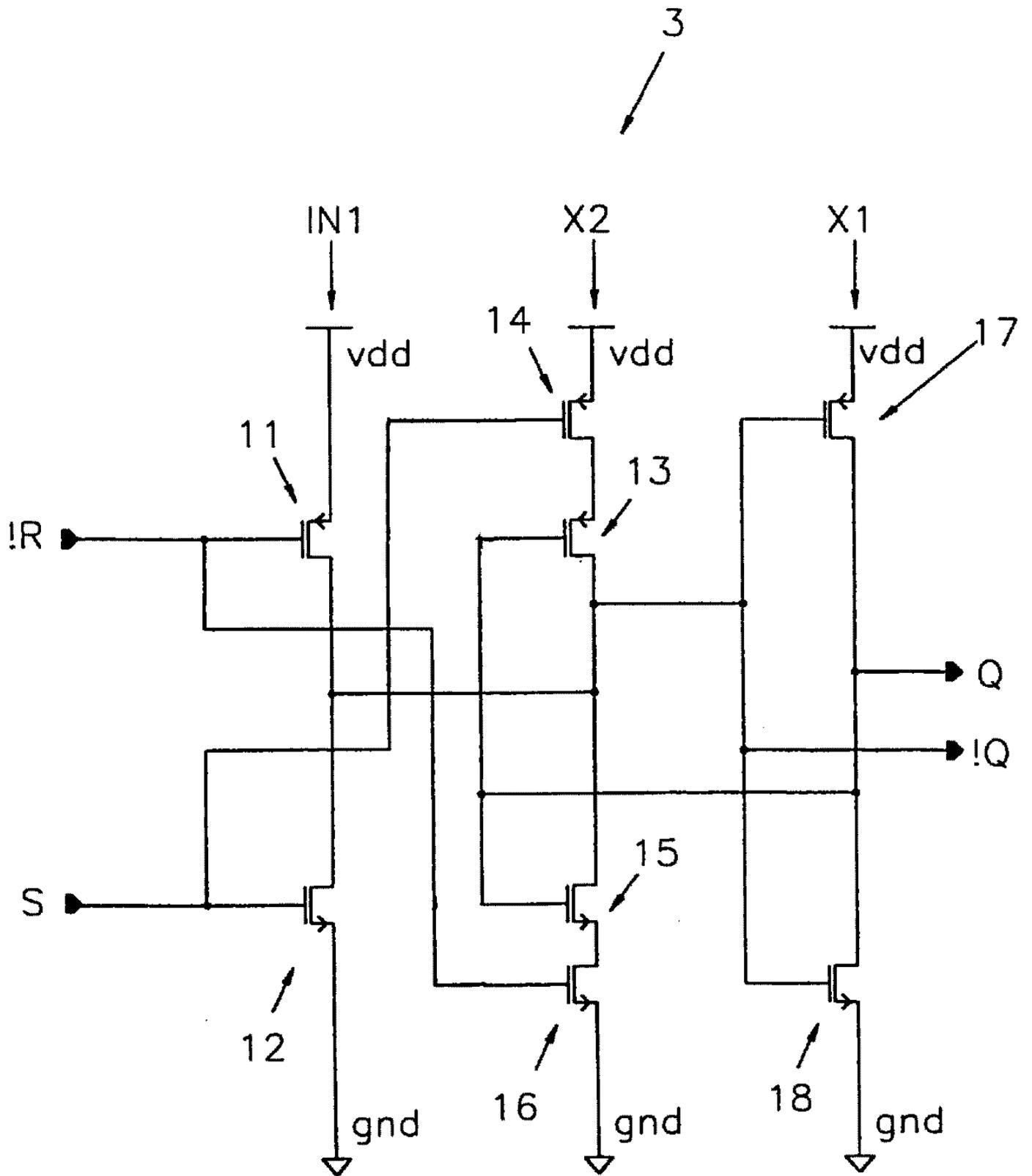
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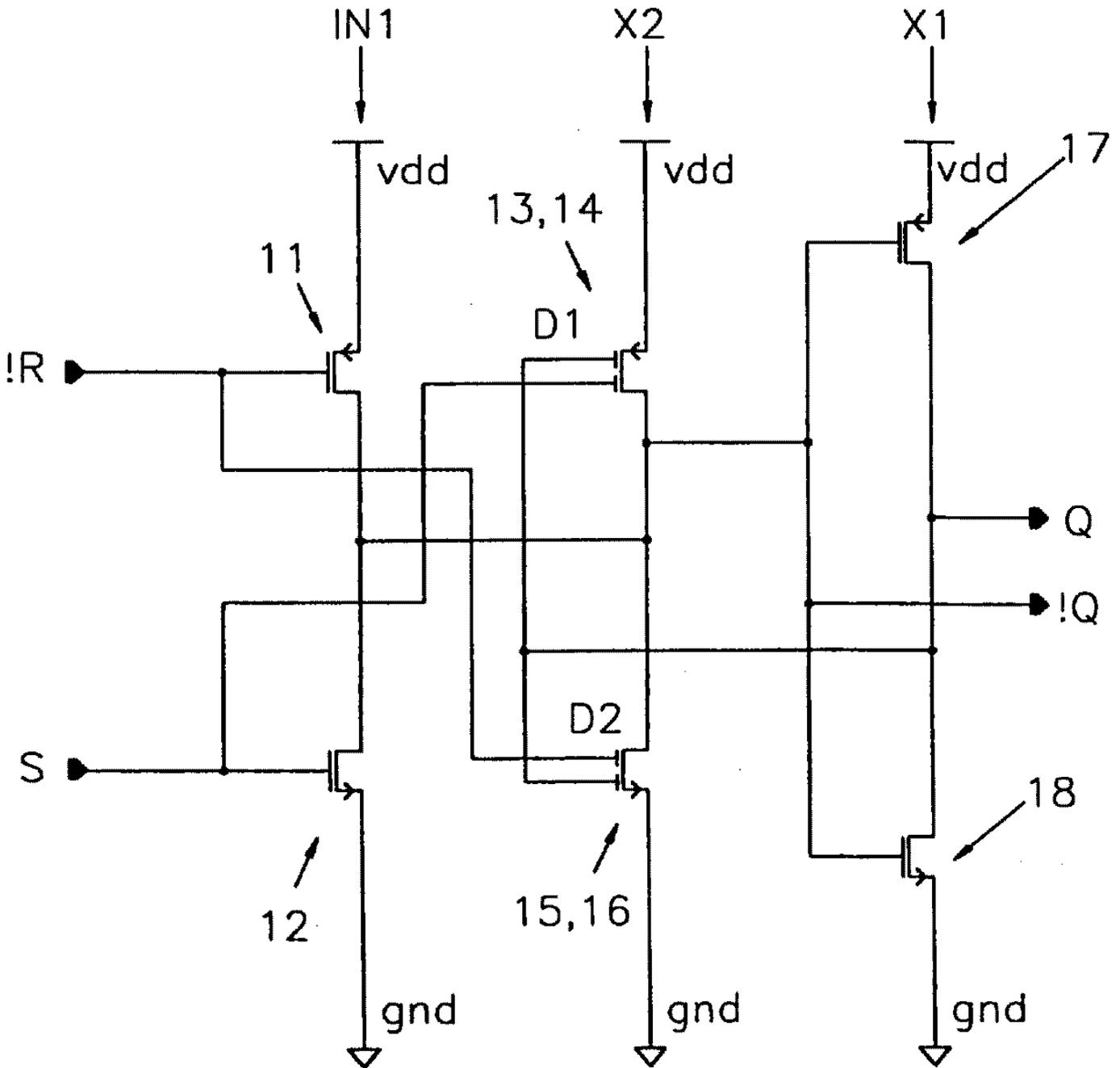


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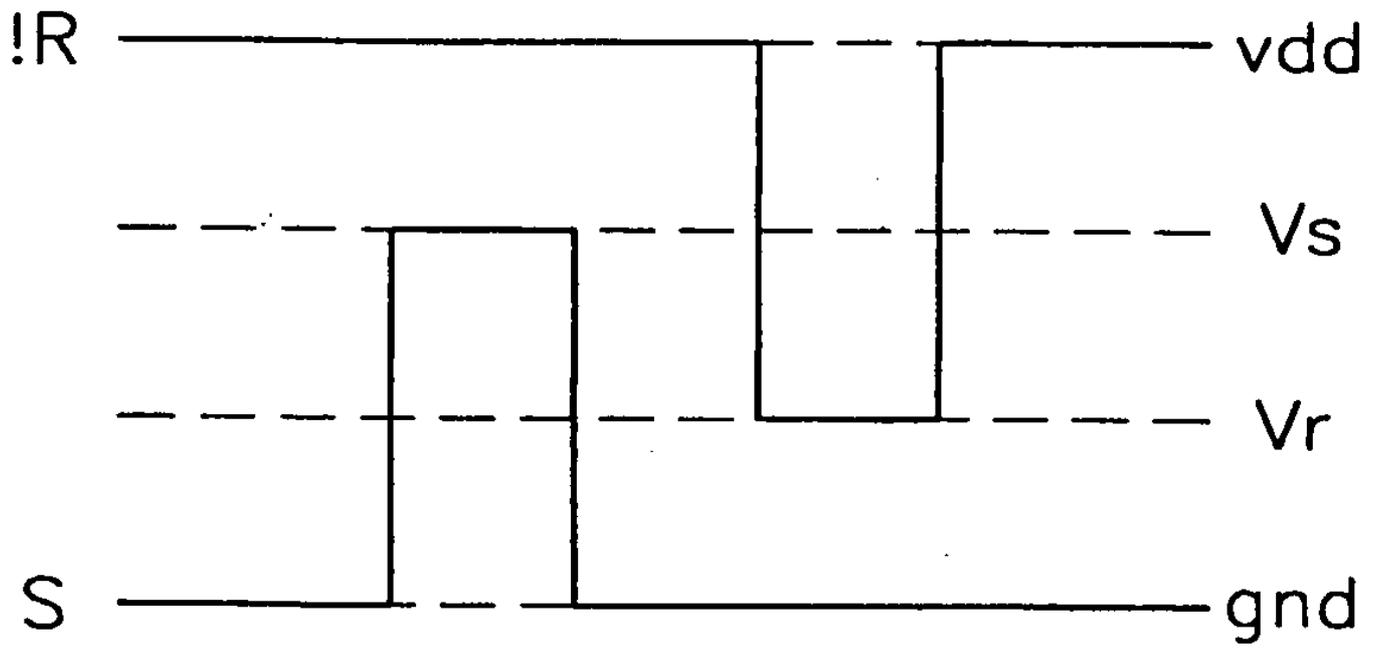


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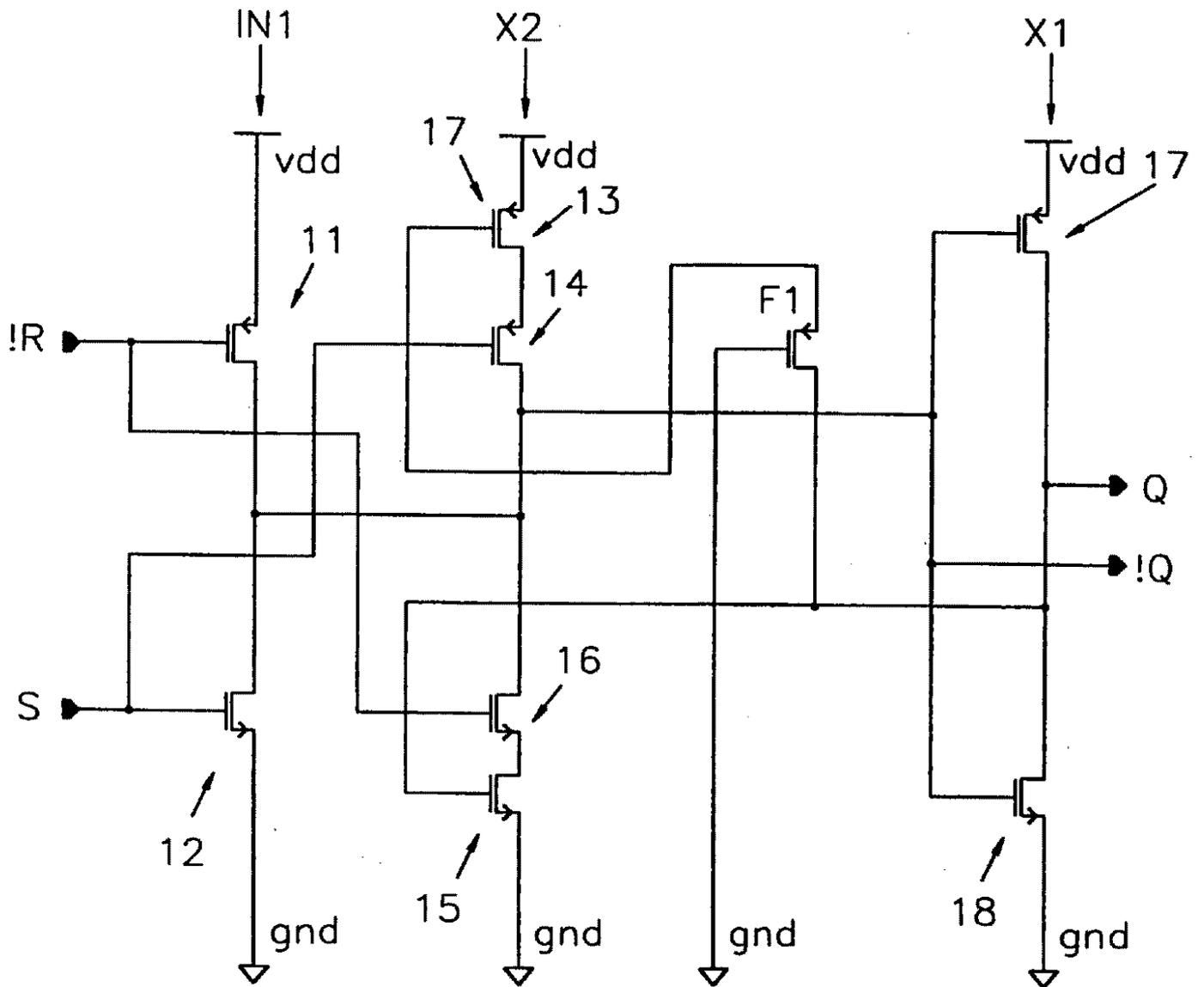


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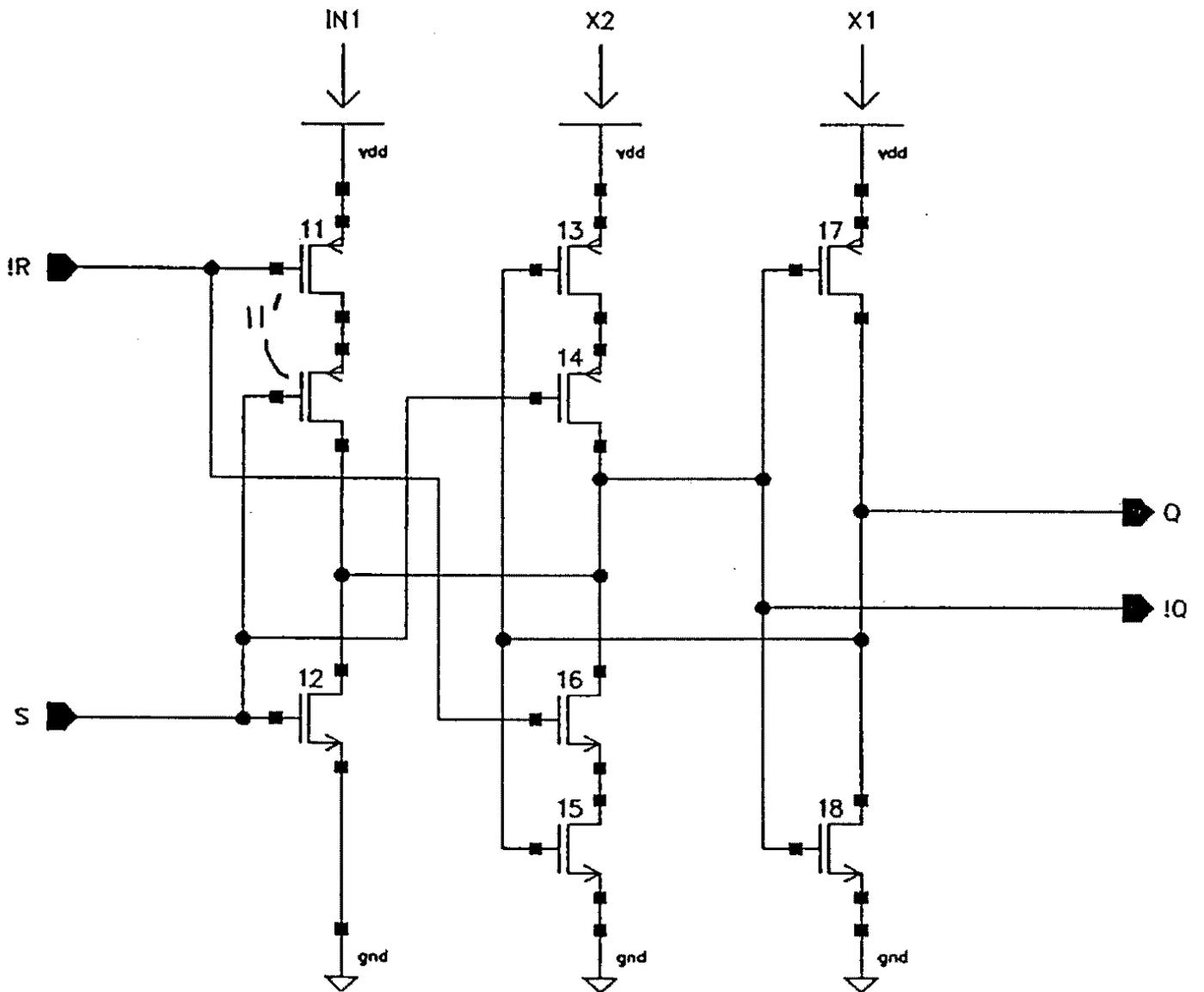
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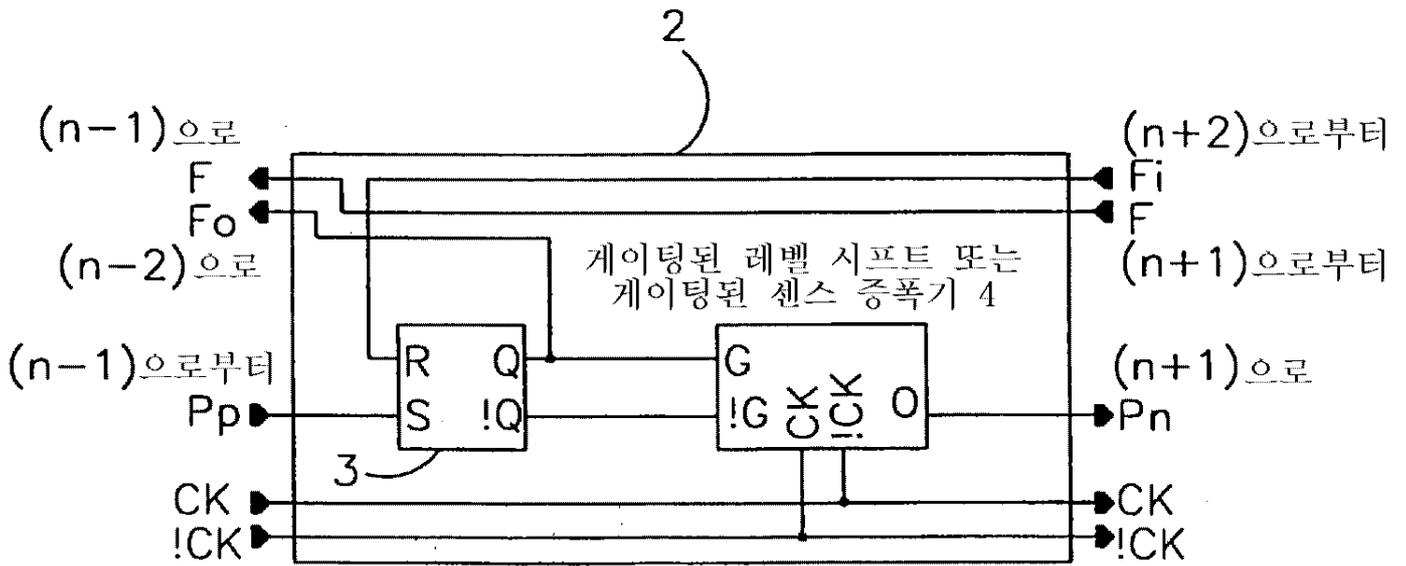
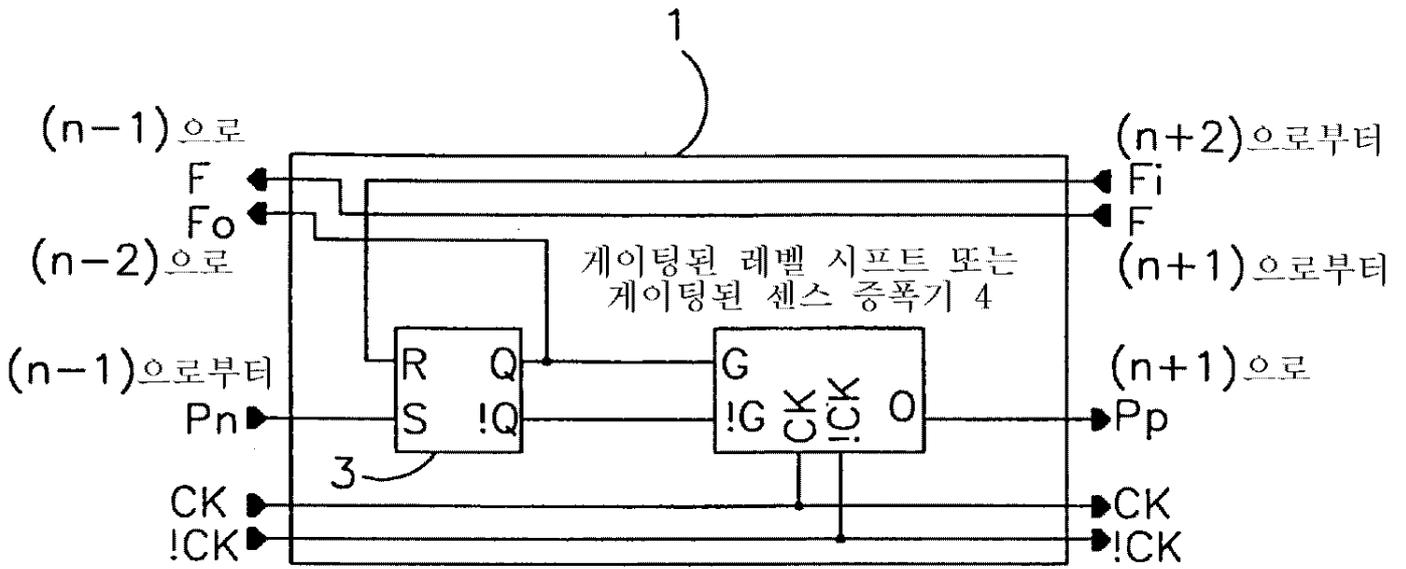


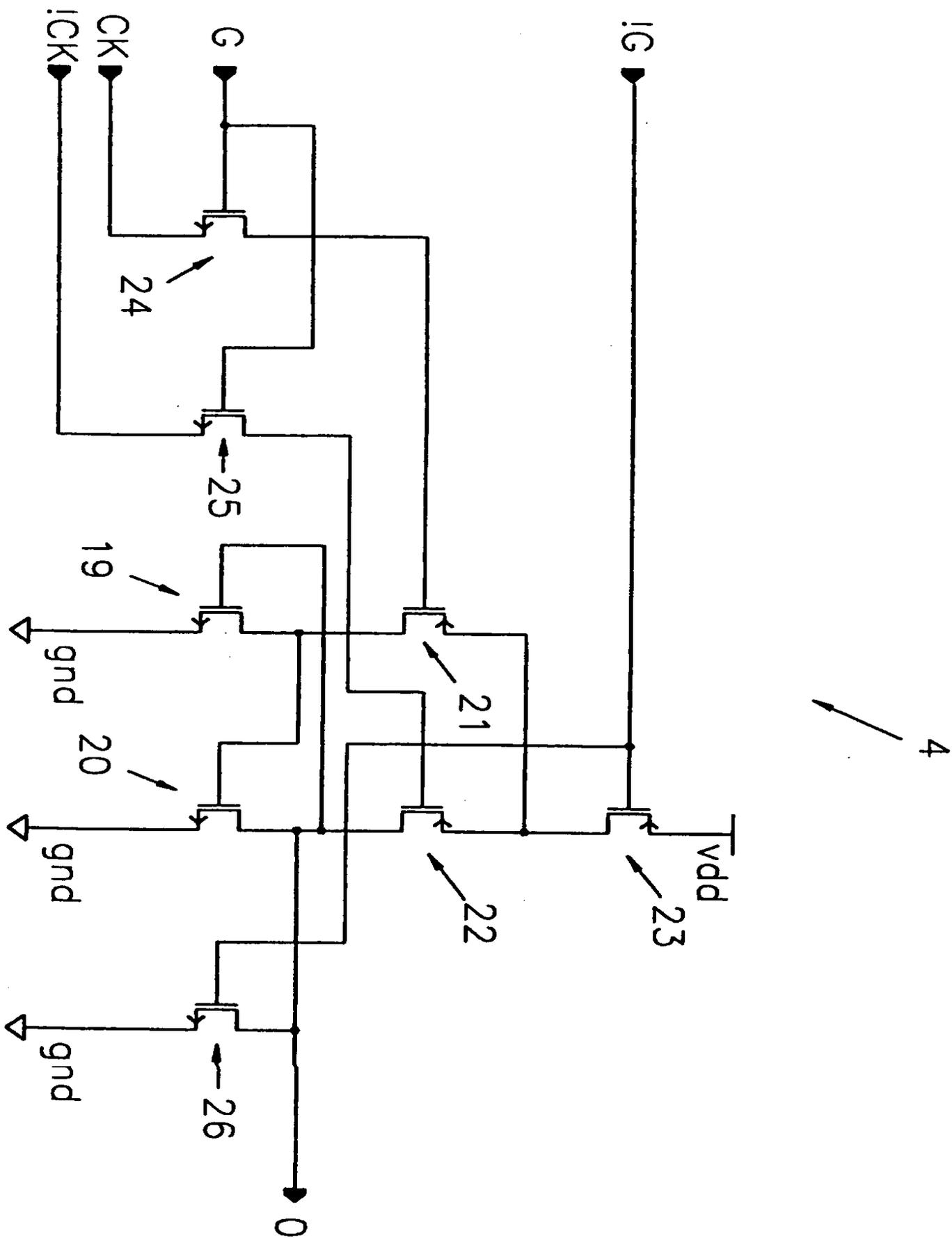
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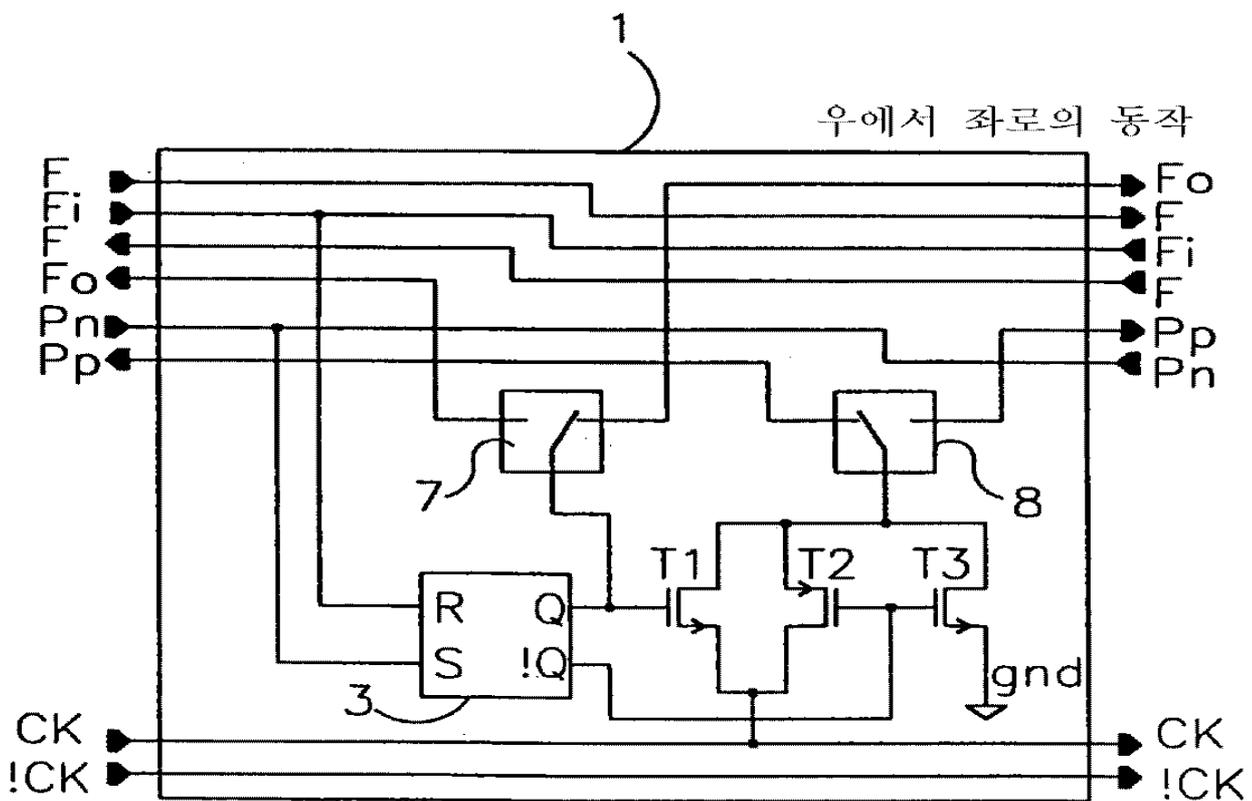
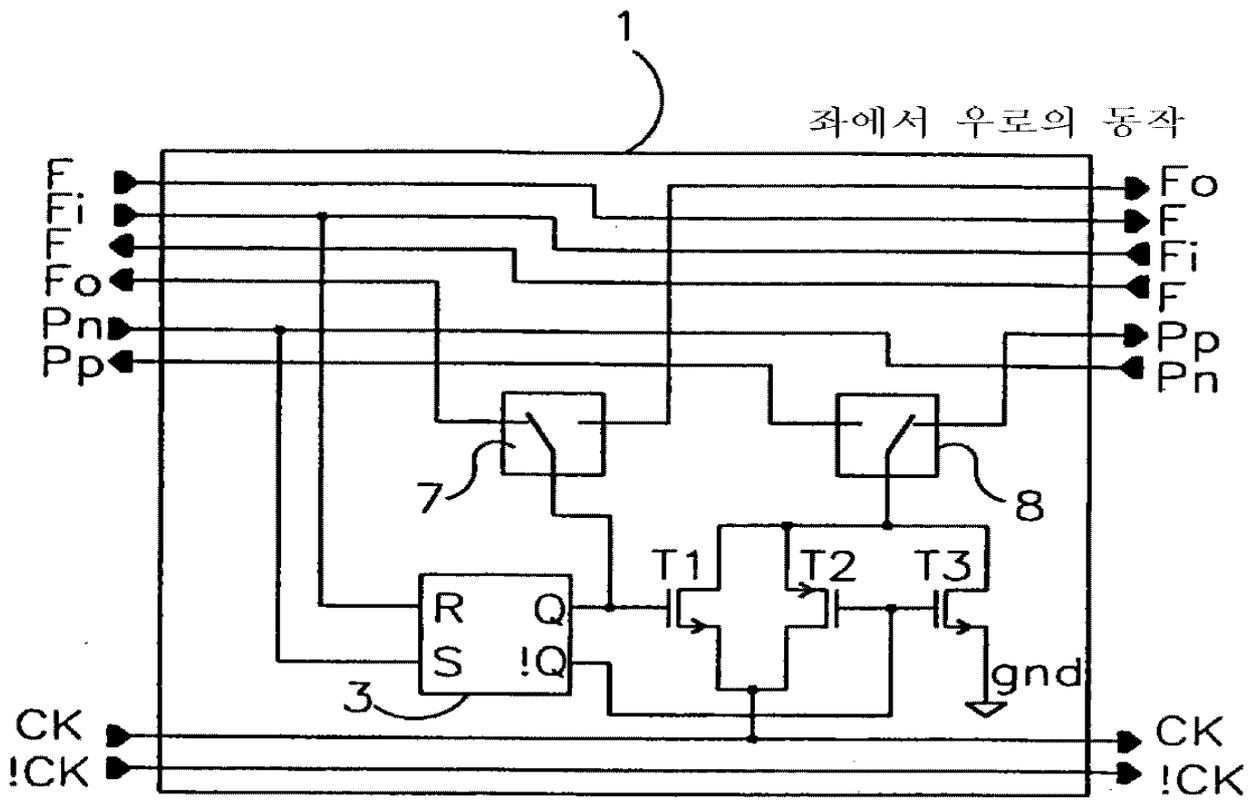


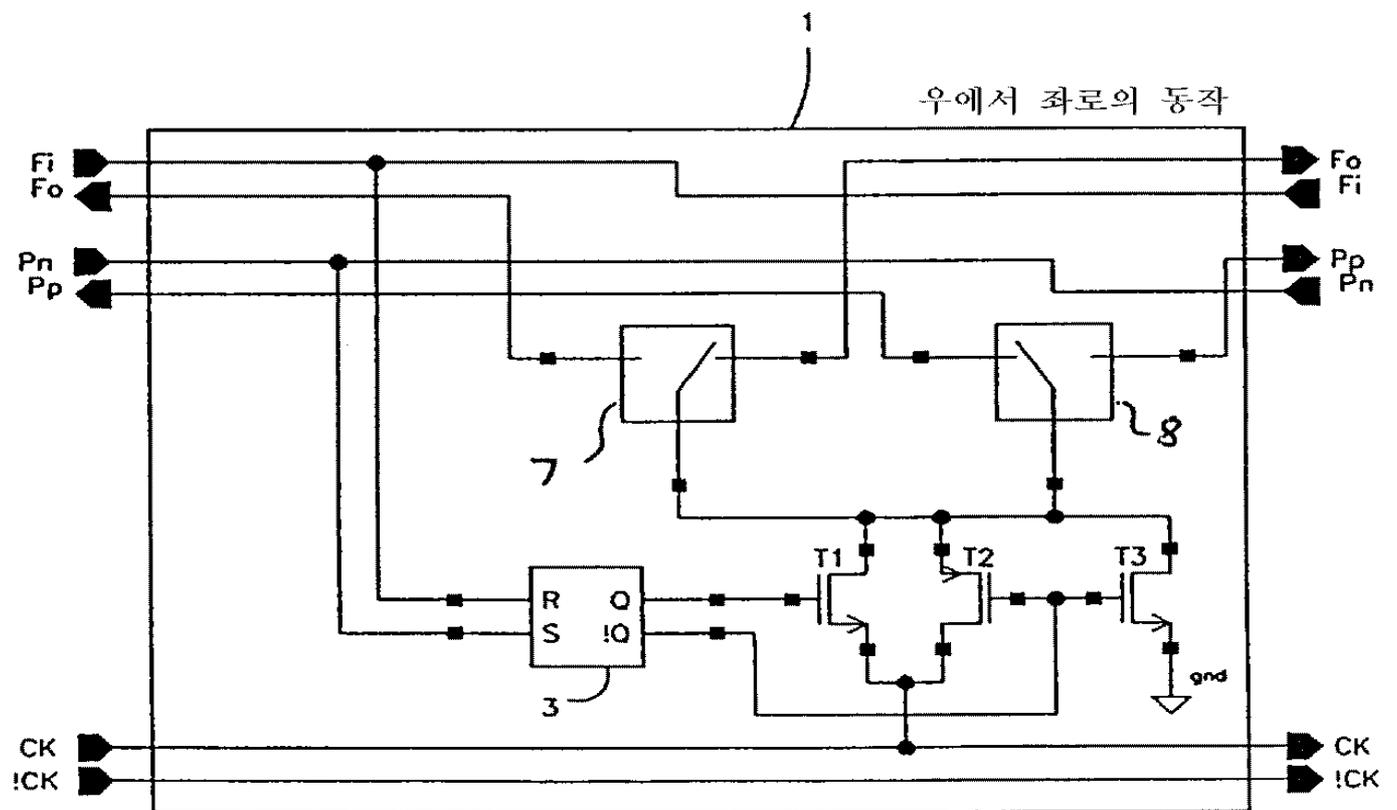
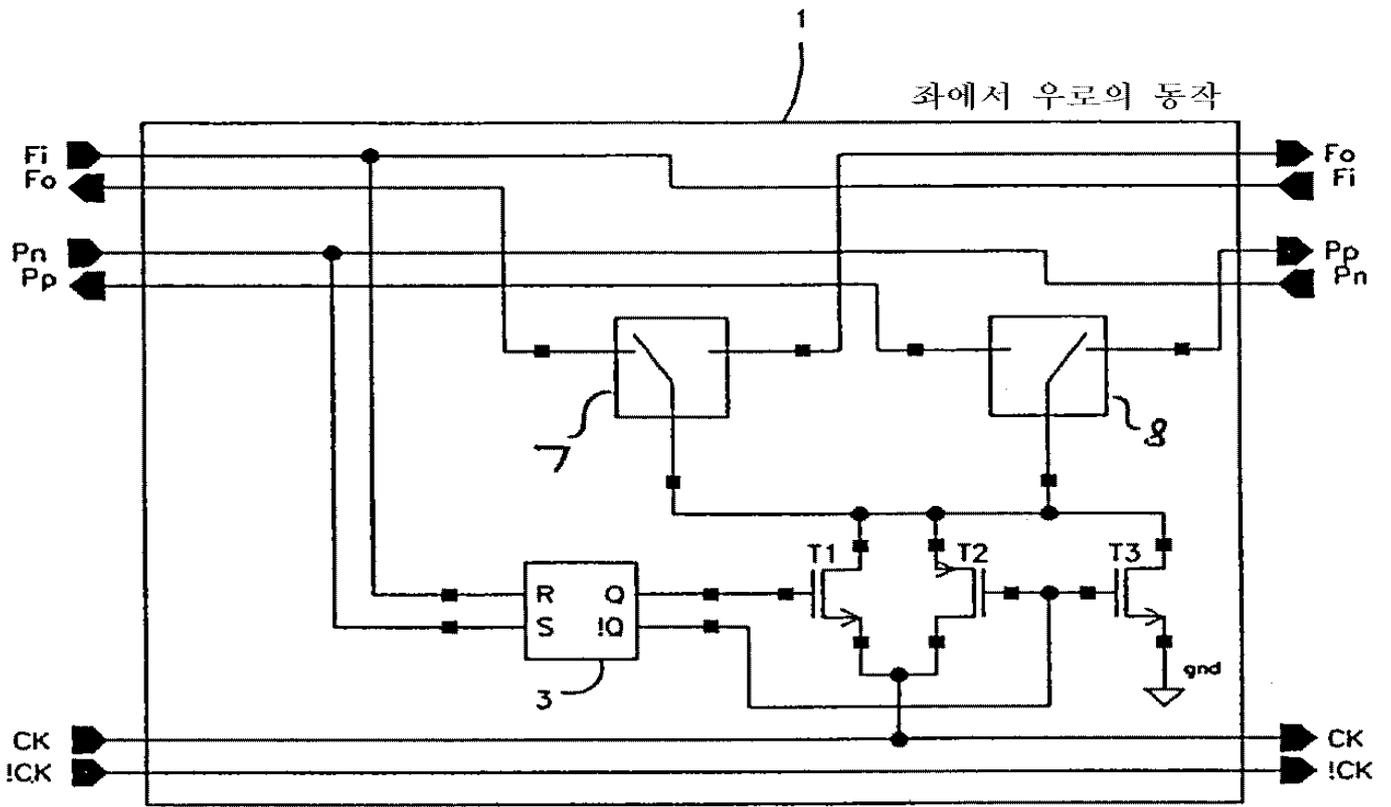
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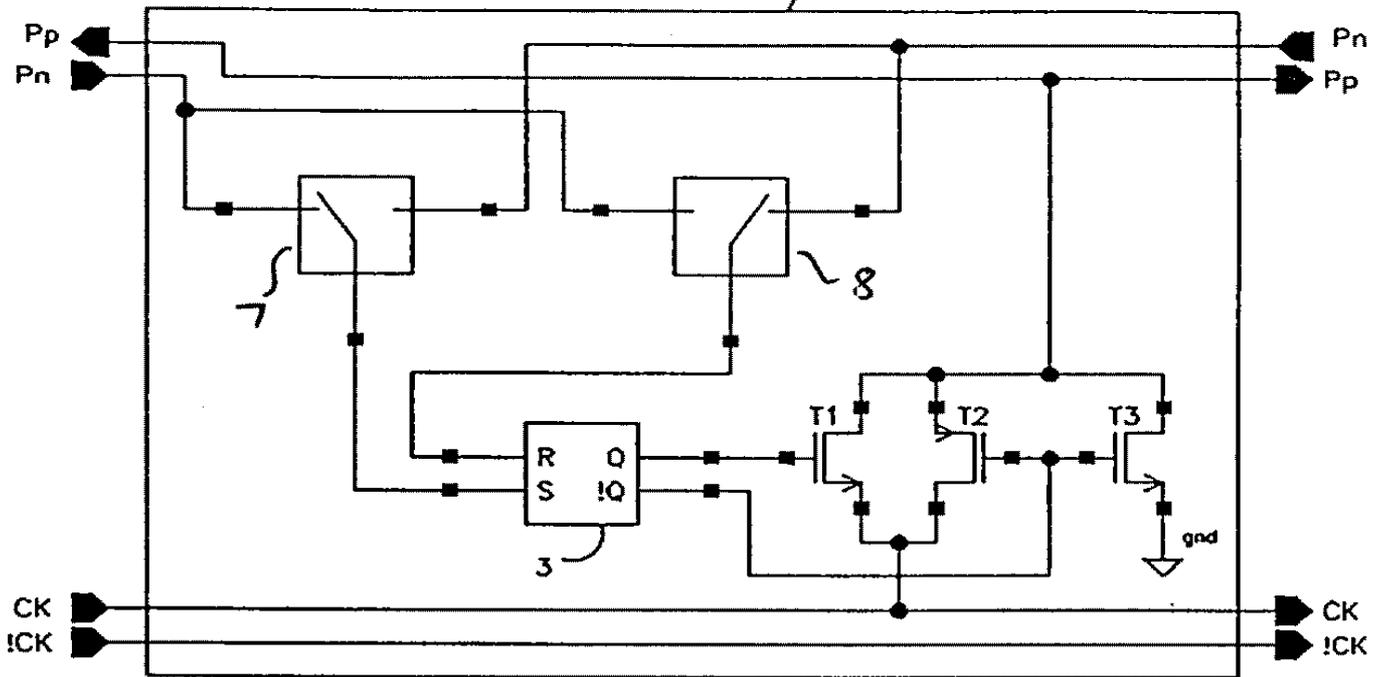




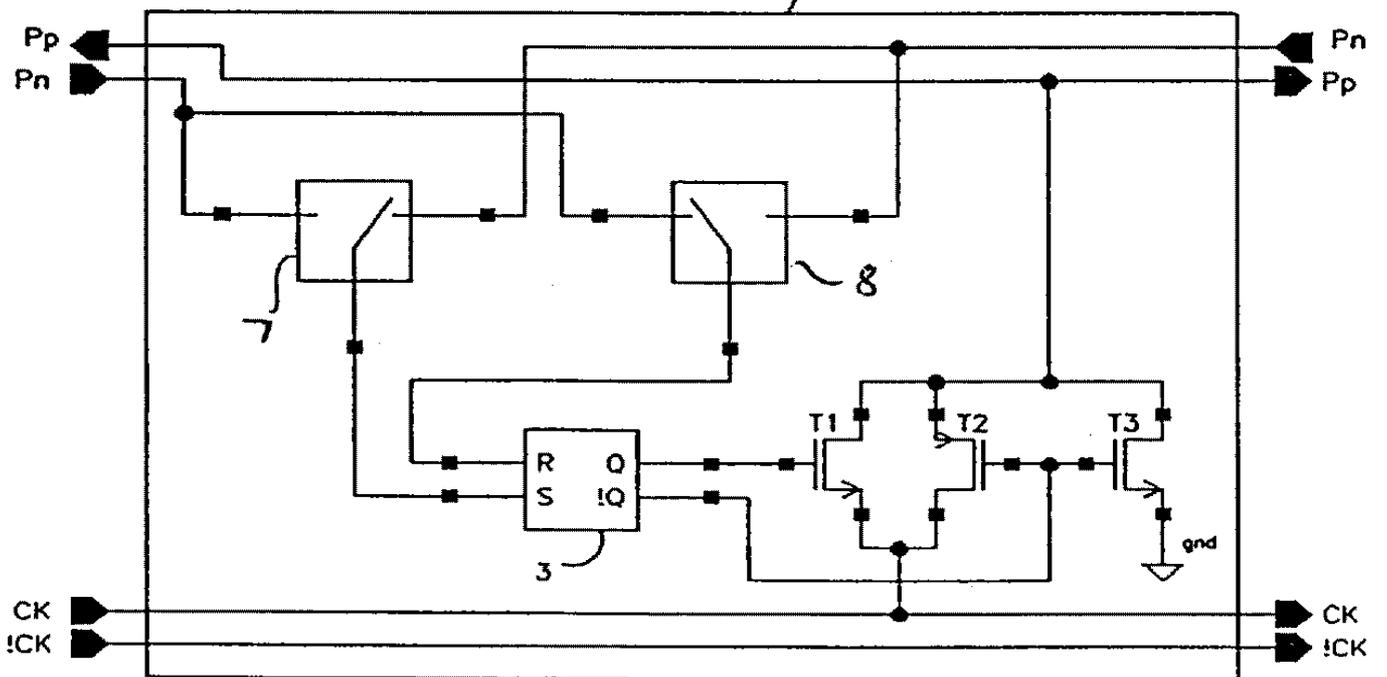




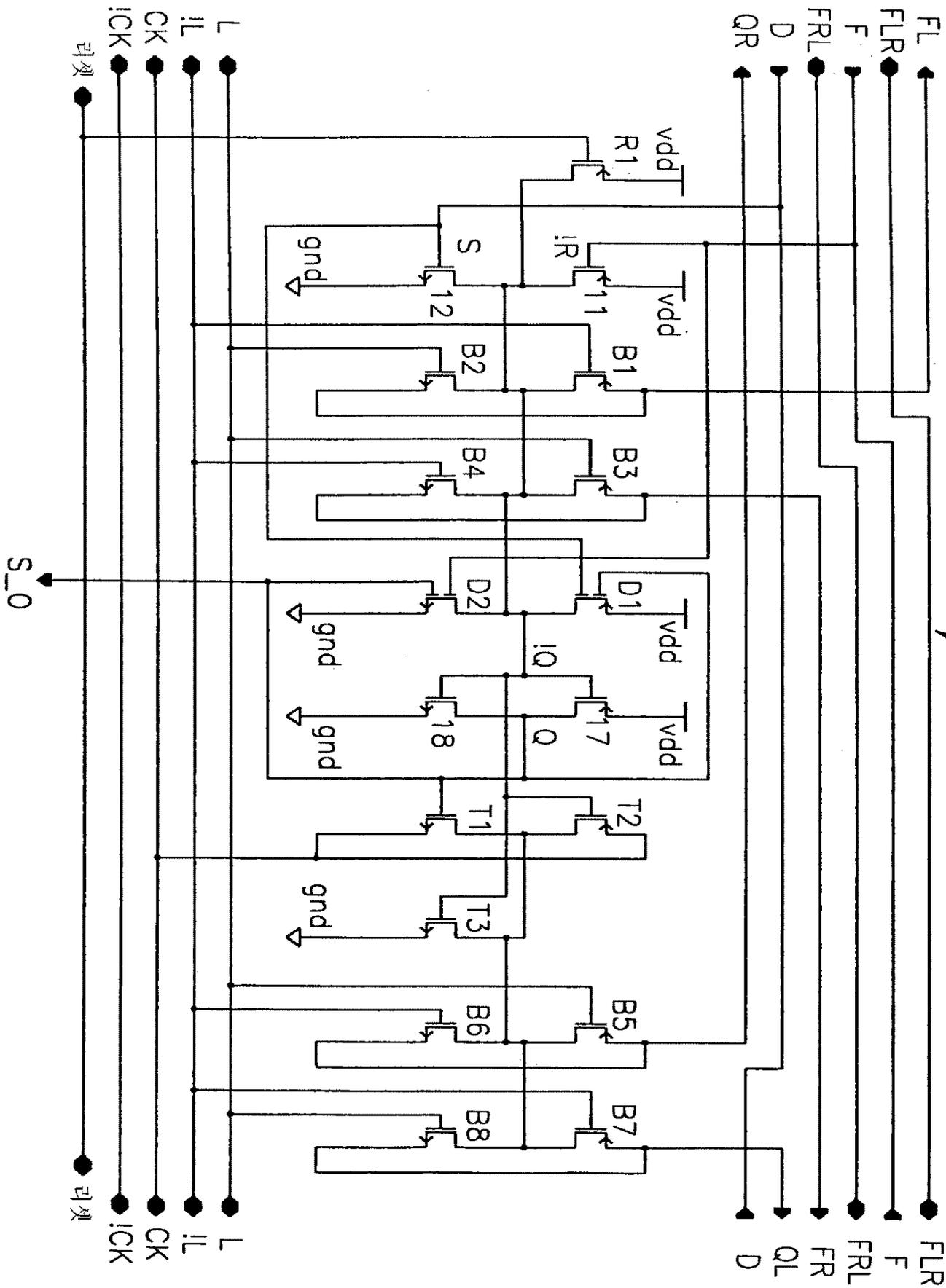
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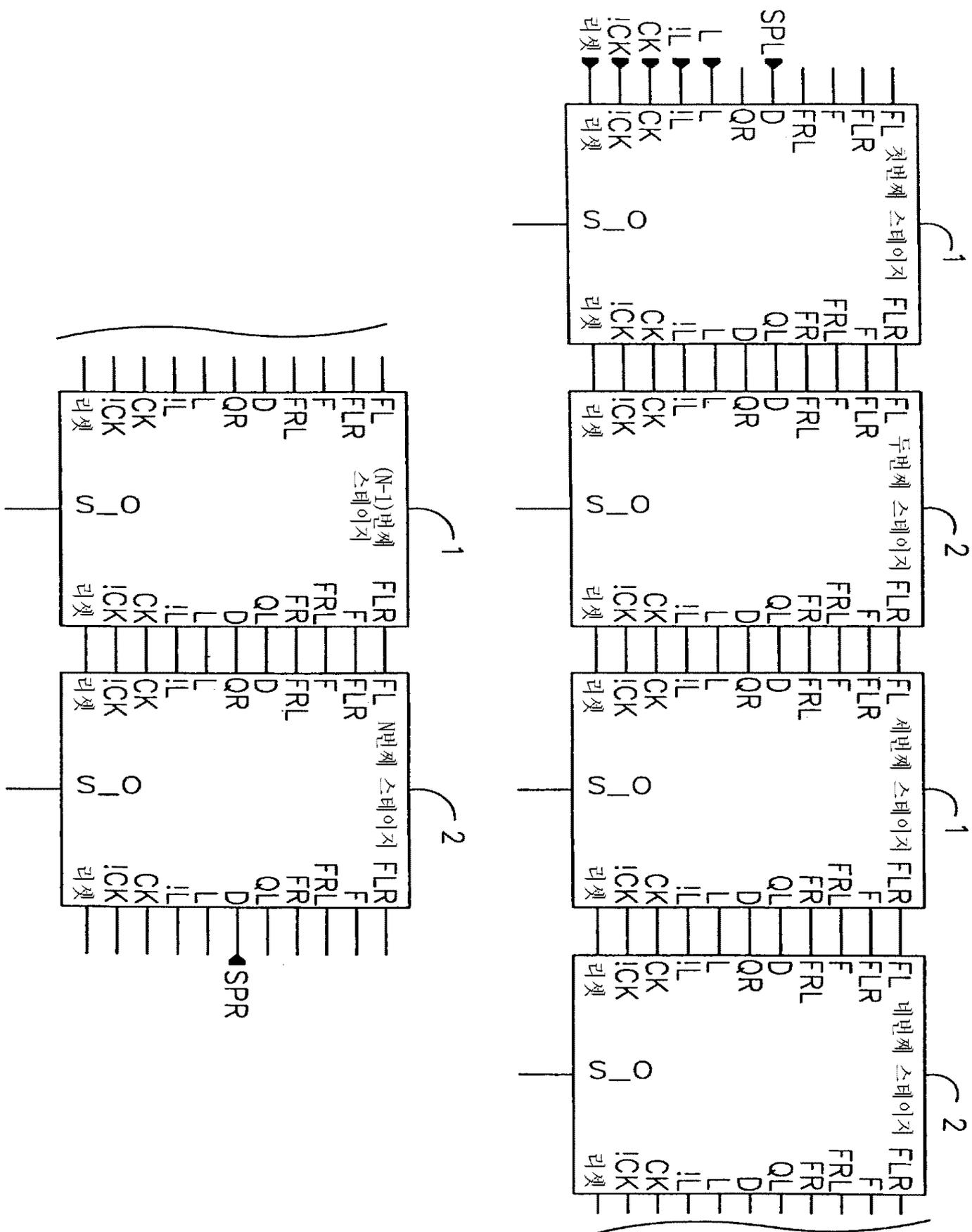


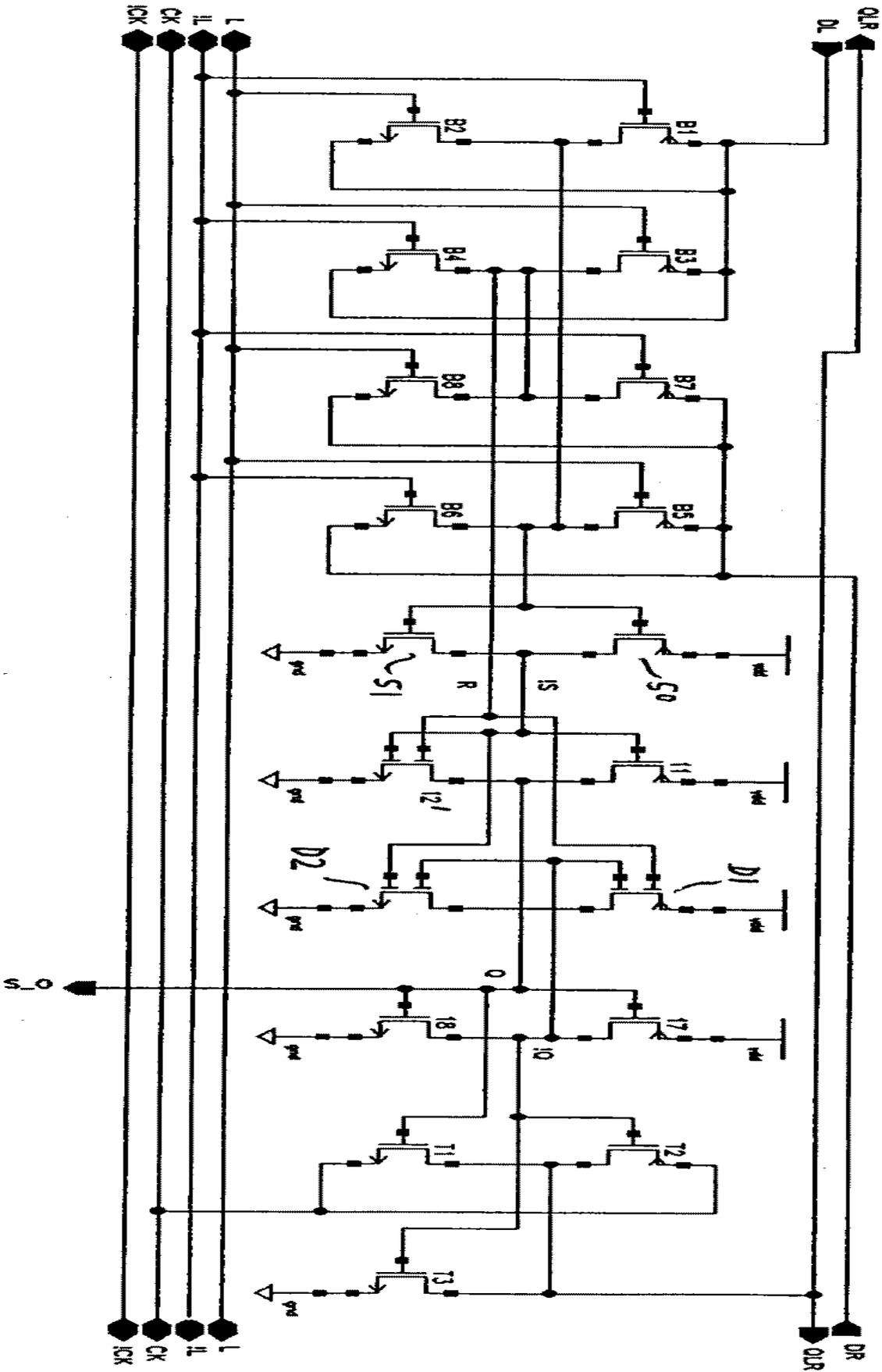
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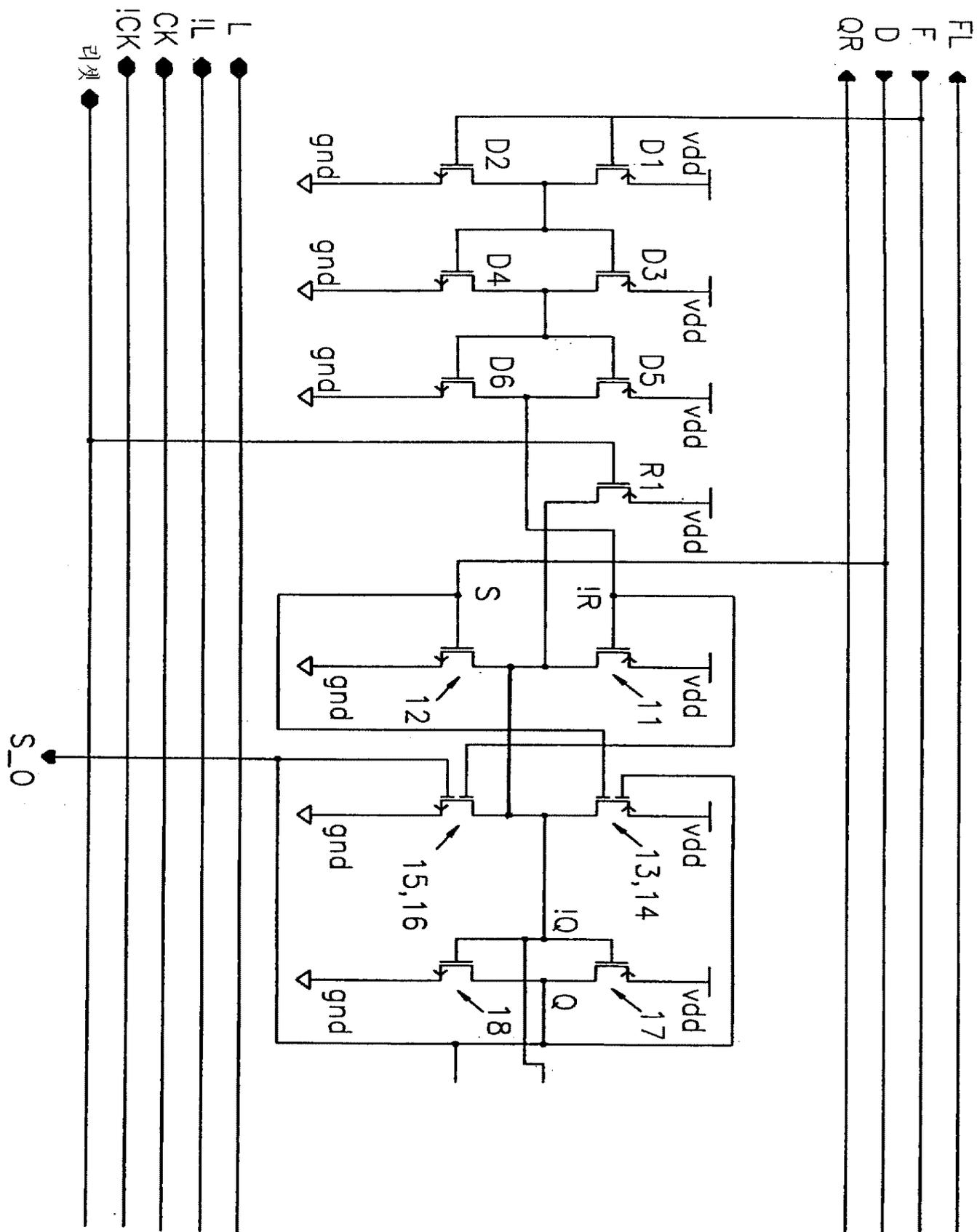




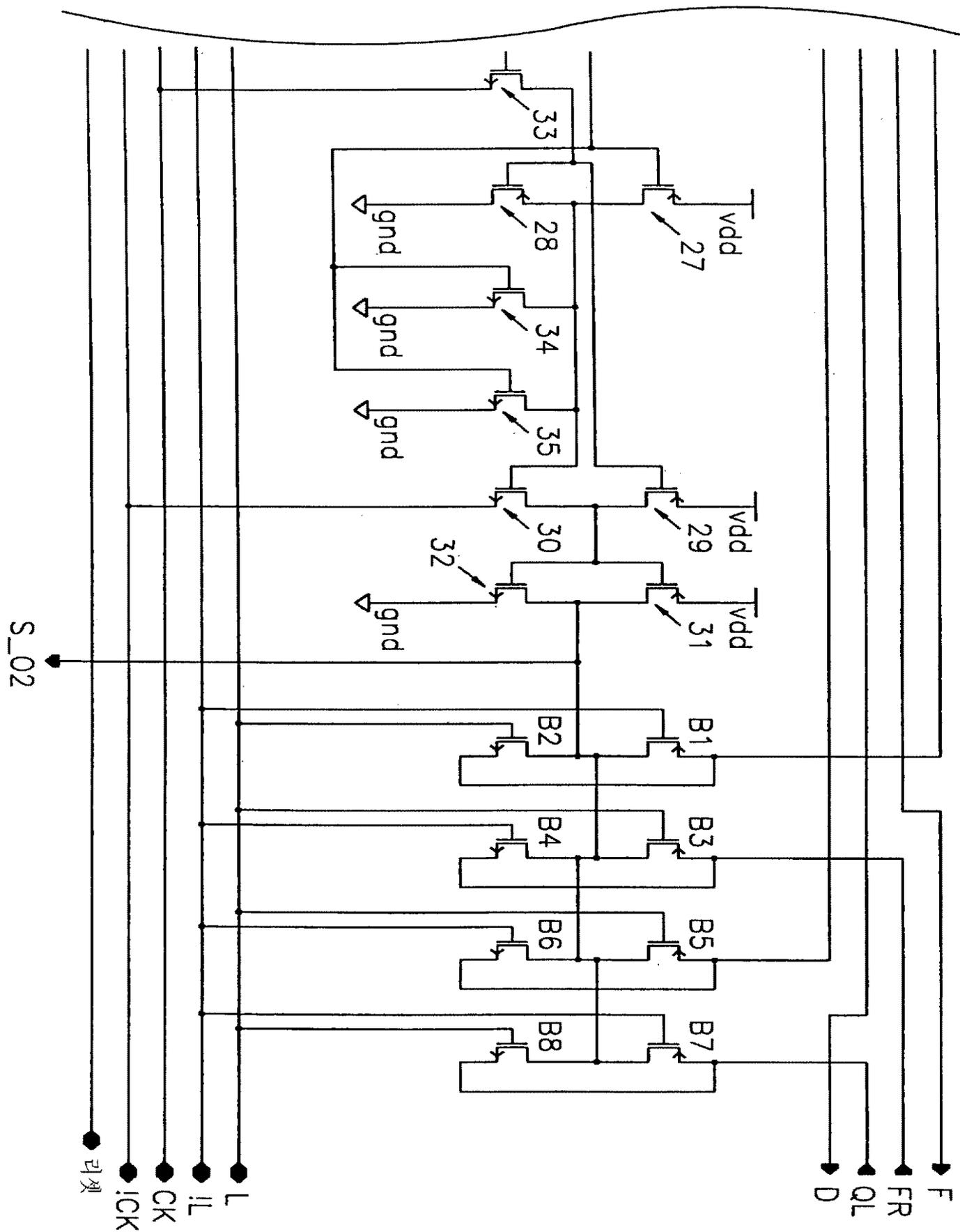




39a



39b



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