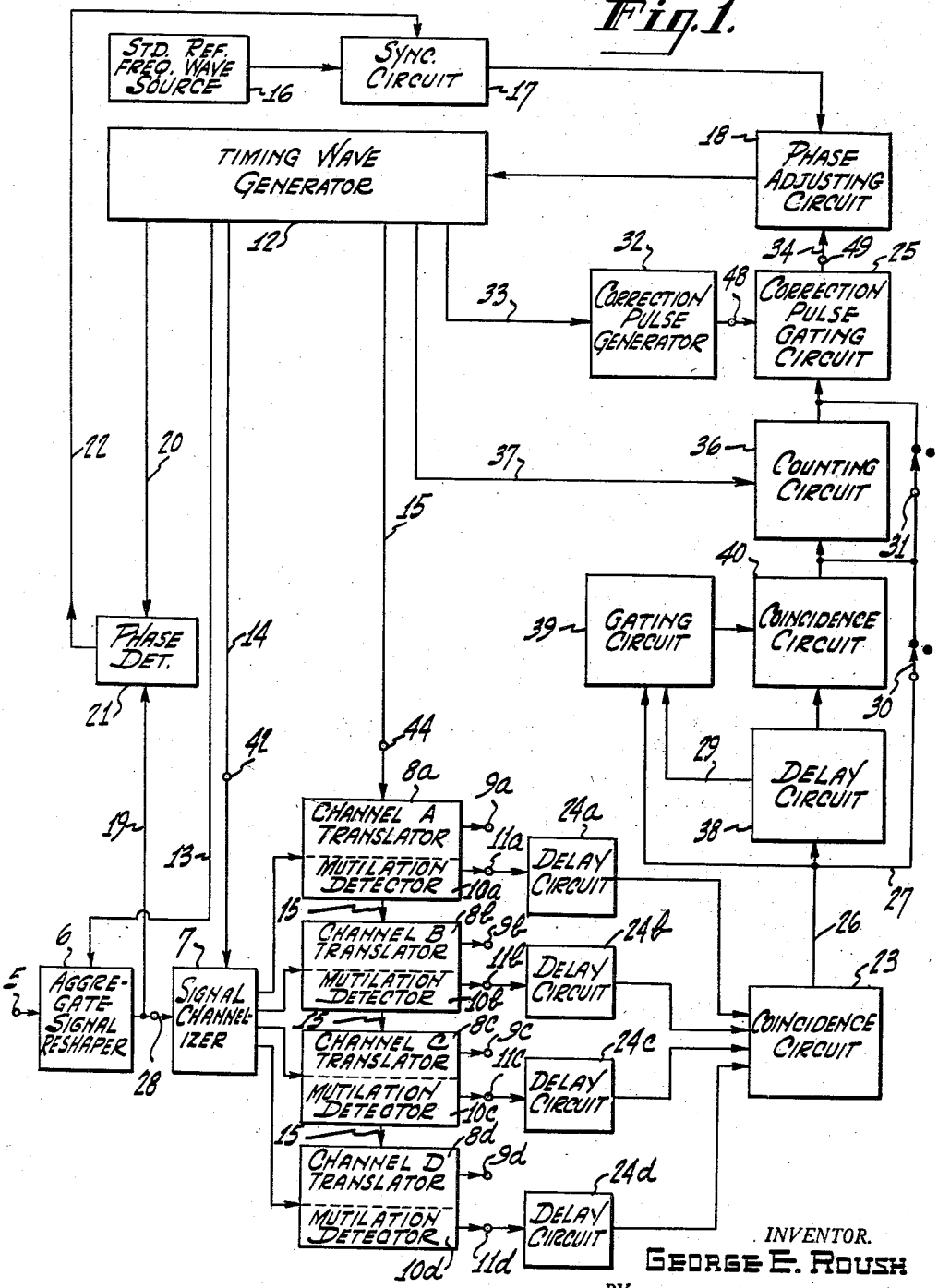
Aug. 5, 1958 G. E. ROUSH 2,846,502

AUTOMATIC PHASING FOR SYNCHRONOUS RADIO TELEGRAPH SYSTEMS

Filed Sept. 29, 1955 2 Sheets-Sheet 1

Fig. 1.



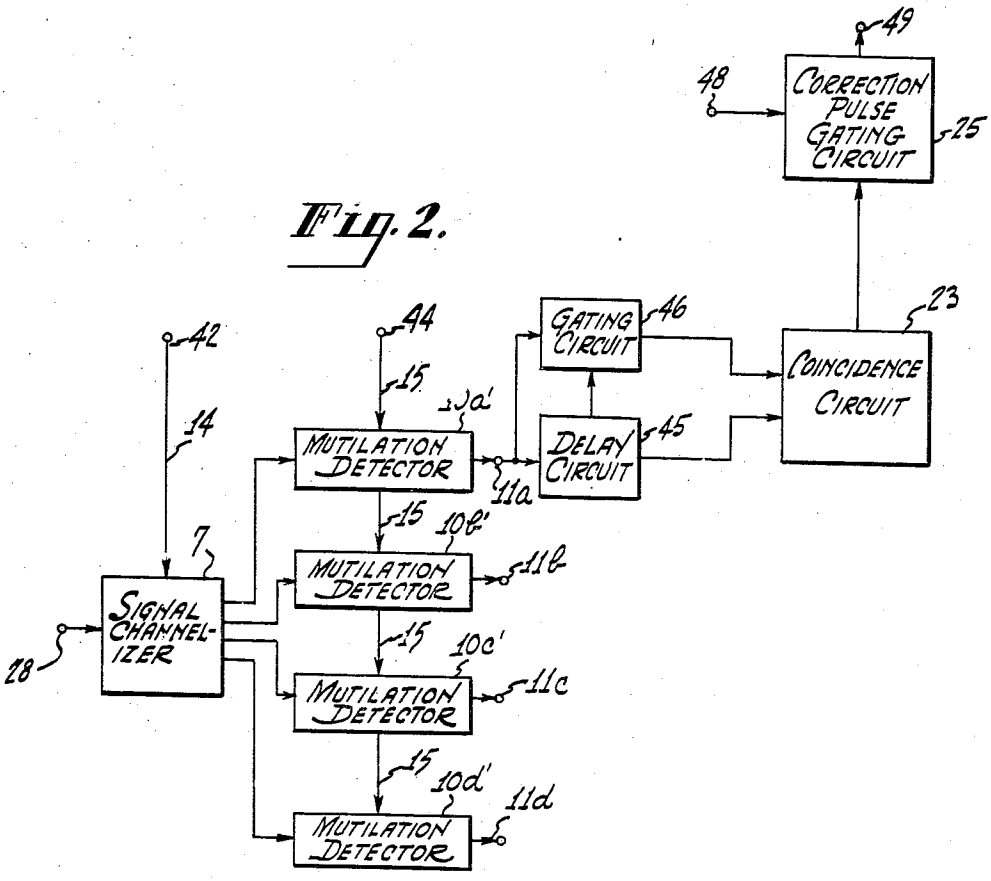
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Filed Sept. 29, 1955 2 Sheets-Sheet 2

Fig. 2.



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2,846,502

AUTOMATIC PHASING FOR SYNCHRONOUS RADIO TELEGRAPH SYSTEMS

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Application September 29, 1955, Serial No. 537,321

11 Claims. (Cl. 178—50)

The invention relates to synchronous radio telegraph systems, and it particularly pertains to arrangements for automatically phasing the receiving terminal apparatus of a synchronous multiplex radio telegraph system with received signals.

Printing telegraph equipment operates in response to electric energy appearing at discrete energy levels for the duration of discrete time intervals. At the present time, two discrete energy levels, defining a "bistatic" signalling system, are used in radio telegraph and wire line telegraph systems. The discrete time intervals are defined in the art as signal elements and the energy level thereof will be defined as the static nature of the signal element. This nomenclature will be found more convenient than the descriptive definitions given above and is free from the ambiguity and limitations of the designations "mark" and "space."

Because radio wave transmission paths are subject to atmospheric noise, radio telegraph systems may suffer seriously from distortion of the elements of the code characters to such degree that the energy level of one or more of the discrete time intervals may be mistaken for the other level at the receiving apparatus. Such distortion is referred to as mutilation, and a false character resulting from such distortion is termed a mutilated character. Such mutilation of a character may prevent the proper interpretation of a message containing the false character, and can be serious in the transmission of coded-word messages.

The recognition of a mutilated character has been made possible by using a "protected" or a "parity" code. A protected code in the strict sense comprises a fixed number of signal elements representing each character of the intelligence to be transmitted and a fixed ratio of signal elements of one nature to the total number of signal elements in each character of a polystatic code signal. Since the number of elements in each character is fixed, the ratio between elements of one nature and the elements of opposite nature in a bistatic code signal is also fixed. One known protected code, given by way of example, is the 7-unit telegraph code in which the ratio of marking to spacing elements is 3 to 4. A "parity" code is a limited form of protected code in which an even number of signal elements of one nature is always present but the ratio of elements of one nature to the other is not necessarily fixed. Usually a parity code is made up by adding an extra element to all characters of an existing code, and the extra element is made to be of the one nature when the number of elements of that nature in the existing code character is odd. One known parity code, given as an example only, is made by adding an extra element to the 5-unit teleprinter code. Unless specifically otherwise noted, the term protected code as used hereinafter will be construed as including the parity code, since the operation of the circuit arrangement according to the invention is substantially the same for either type.

Although means are known for determining the occurrence of mutilation and for automatically requesting a repetition of the transmission of a character until the proper character is printed, unless the transmitting and receiving terminal apparatus be operating strictly in phase, the continued transmission of successive characters of a message is impossible. In time division multiplex radio telegraph systems, phase slippage will cause mutilation of a greater number of messages than in simplex systems. It has been suggested that receiving terminal apparatus of radio telegraph systems be automatically phased with the incoming telegraph signal wave in response to synchronizing pulses positioned or poled to enable both synchronizing and phasing functions to be performed automatically, for example, in the manner of the start and stop pulses of wire line printing telegraph equipment. However, the disadvantages of generating, transmitting and receiving special synchronizing pulses outweigh any advantage which might accrue therefrom.

A system for automatically phasing a synchronous multiplex radio telegraph system in which the signal elements constituting the characters of one channel of communication are inverted with respect to the signal elements forming characters in the other channels has been disclosed in copending U. S. patent application Ser. No. 407,198, filed February 1, 1954, by Anthony Liguori, now U. S. Patent No. 2,769,857, issued November 6, 1956. This arrangement is capable of excellent results when used with such a radio telegraph system. The inversion of the signal elements forming the characters in one channel with respect to the signal elements forming characters in the other channels of a multiplex signal has been used extensively in electro-mechanically operated radio telegraph systems to ensure the proper distribution of the channels at the receiver. However, with present day electronic and magnetic telegraph signal handling equipment it is often unnecessary and undesirable to invert the signal elements of the characters transmitted over any channel of a multiplex radio telegraph system.

Phasing is an exacting requirement encountered in time division radio telegraph communications system. The problem is many-sided. First, there is the requirement of initial phasing on startup; then there is the problem of maintaining phase during operation; and finally, in the event of a slip in phase, there is the desirability of ascertaining this condition quickly and restoring the system to the normal phase relationship. Systems for automatically synchronizing a locally generated timing wave, upon which the timing of the various functions of the receiving terminal apparatus is based, with the received telegraph signal wave are known. For example, there is the system shown and described in U. S. Patent 2,716,158, issued August 23, 1955, to Eugene R. Shenk, Aruthur E. Canfora and Philip E. Volz. This system has phase adjusting circuitry interposed between a source of standard reference waves and a timing wave generator to shift the phase of the standard reference waves in small increments and, thereby, synchronize the locally generated timing wave with the received wave. Such systems are phased by forcing the synchronizing circuitry of the apparatus to shift the phase in response to manual operation of a control device, usually a simple push-button switch. The phase of the locally generated timing wave is shifted in increments large relative to the shift normally produced by the automatic synchronizing circuitry until the proper phase relationship is established, as indicated by electric phase indicating means or observation of clear text on teleprinting apparatus associated with the receiving terminal apparatus.

Phasing by such means requires special operating procedure for establishing the correct phase relationship on startup. This requires that the operating personnel must

be specially trained to work with the equipment and because the method is a "brute force" method, there is apt to be considerable time lost in establishing the proper phase relationship between the transmitting and receiving apparatus. Also, there must be some means for continuously checking the phase relationship. This requirement may be met by having an operator check the message text on the teleprinters to see that it is continuously intelligible. Where the printer apparatus is located at a distance from the receiving terminal apparatus, the requirement is usually met by having an operator continually or periodically observe a phasing indicator device; usually in the form of simple glow lamp indicators. This means must also be used where cryptographic text, which is not intelligible to the operators, is transmitted. This arrangement usually involves the loss of appreciable time because one operator is responsible for a number of sets of terminal apparatus and a slip in phase of any one piece of apparatus is so infrequent that for most of the time the use of only a few operators is justified. When such a slip in phase does occur, however, messages are incorrectly received. Such messages, and the time of delivery thereof, of course, are of great importance to the addressee, and the loss of considerable circuit time spent in asking for and receiving a repetition of the garbled message is undesirable. Furthermore, when there is a slip in phase, the transmitting and receiving apparatus are rephased according to the special procedure established for phasing on startup, and no less amount of time is lost in correcting for a slip in phase than is lost in phasing on startup.

An object of the invention is to provide an improved circuit arrangement for a synchronous multiplex telegraph system using a protected code to automatically phase the receiving terminal apparatus with the signals received by the apparatus.

Another object of the invention is to provide an improved circuit arrangement for a synchronous multiplex telegraph system using a protected code to automatically phase the receiving terminal apparatus with the signals received by the apparatus on startup and to automatically rephase the apparatus when a slip in phase occurs.

A further object of the invention is to provide a novel circuit arrangement for automatically maintaining the proper phase relationship between a base timing wave of telegraph receiving terminal apparatus and a signal wave received by the apparatus in response to the operation of mutilation detectors arranged to indicate the reception of mutilated characters in a protected code.

A feature of the invention is that automatic phasing of receiving terminal apparatus with the signals received by the apparatus may be obtained whether or not signal elements forming characters in any channel are inverted with respect to the signal elements forming characters in the other channels without any change in the structure of the receiving terminal apparatus according to the invention.

According to the invention, a circuit arrangement for automatically phasing the receiving terminal apparatus of a synchronous multiplex radio telegraph system may be interposed in otherwise conventional receiving terminal apparatus responsive to a protected code. The multiplex protected code signal received by the terminal apparatus is applied to an aggregate signal reshaper which operates to shape the signal. Assuming that the multiplex signal includes a train of individual signal elements expressing a plurality of intelligence characters, the signal is, thereafter, applied to a signal channelizing circuit arrangement which assigns the signal elements of each of the characters to separate message channels in a predetermined manner. The elements of the characters belonging to a particular one of the message channels included in the multiplex signal are assigned to a single one of the message channels and so on. In the case of character sequential transmission, no separation of the signal elements of a character is necessary, the characters as a whole being separated and distributed to the respective message channels by the operation of the signal channelizer in a predetermined manner. A separate code translating circuit arrangement is included in each of the message channels. The code translating arrangement may operate to convert, for example, a character expressed in a seven element protected code into the corresponding character as expressed in a conventional five element telegraph code, or merely to transfer the signal to the message printing telegraph equipment or other utilization circuits in a customary manner.

The aggregate signal shaper, signal channelizer and translating circuit arrangements are operated in response to timing waves applied thereto from a timing wave generator. The timing wave generator is operated in response to a signal fed to the generator from a source of standard reference frequency wave over a path including a phase adjusting circuit, and operates to establish the proper timing functioning of the receiving terminal apparatus.

According to the invention, a mutilation detecting arrangement is interposed in the translating circuitry of at least one of the message channels. When a mutilated or erroneous character, as expressed in the protected code, is received, as determined by too few or too many signal elements of one nature in a character, the mutilation detecting arrangement of the message channel over which the mutilated character is carried operates to develop a control current hereinafter termed an error signal, providing an indication of the mutilated character. Upon an indication of mutilation in a predetermined number of the channels, it may be assumed that the receiving terminal apparatus is out of phase with the received multiplex signal and that the mutilations are not due to equipment failure, electrical interference in the radio path, and so on. The assumption, of course, must take into consideration the practical factors involved in the operation of a particular telegraph system. The error signals from the mutilation detecting arrangements are applied to a coincidence circuit. The coincidence circuit is arranged to operate in a predetermined manner in response to error signals to apply correction currents to the phase adjusting circuitry operating in the timing wave generator. In some applications, it may be considered desirable to receive error signal indications of mutilated characters in succession in the same message channel before an out of phase relationship is assumed to exist, and the phase correcting circuit of the invention is placed in operation. The invention provides means whereby the phase correction can be made to follow any assumption considered valid under the circumstances. The invention can also be adapted to operate when a predetermined number of mutilated characters are received in a given time or when mutilated characters are received on each of a predetermined number of message channels at any one time. The circuit arrangement of the invention operates in these situations to advance or retard the phase of the reference wave applied to the timing wave generator and, therefore, the phase of the timing waves applied to the receiving terminal apparatus from the timing wave generator. By controlling the phase of the timing waves generated by the timing wave generator in this manner, the proper phase relationship can be established and maintained between the receiving terminal apparatus of the telegraph system and a multiplex protected code signal received by the apparatus.

Circuitry incorporating the invention will be described in detail with reference to the accompanying drawing in which;

Figure 1 is a functional diagram of multiplex radio telegraph receiving terminal apparatus embodying the invention; and

Figure 2 is a functional diagram of a modification of the apparatus shown in Figure 1.

The circuit arrangement of the invention is not limited to any one particular code or system of synchronous multiplex telegraph transmission, and is described in connection with a four channel multiplex telegraph system operating in response to a protected code. The message signals carried over the respective channels may be combined in time division multiplex fashion in any known manner. Character sequential transmission may be used in which every other character is inverted. On the other hand, the signal elements of the characters of the respective message signals may be intermixed forming a train of signal elements arranged in a predetermined relationship. An important feature of the invention is the fact that the signal elements of a message channel need not be inverted with respect to the signal elements in any other channel. Furthermore, the circuit arrangement to be described is not dependent for operation on a particular type or types of components for performing the required functions. In the interest of clarity and conciseness, however, the invention will be described with reference to examples of conventional circuitry employing electron discharge devices and associated elements, although it should be understood that transistor, semiconductor and magnetic circuitry may be used with equally good results by those skilled in the art.

Referring to Figure 1, there is shown a functional diagram of a circuit arrangement according to the invention. An incoming aggregate multiplex telegraph signal is applied to input terminals **5**. The signal elements of the multiplex signal are arranged in a protected code, for example, a seven element code in which the ratio of mark-to-space signal elements in each character is three to four. The multiplex signal is applied from the input terminals **5** to an aggregate signal repeater or reshaper **6** which shapes the signal, the signal, thereafter, being applied to a signal channelizer **7**. The aggregate signal reshaper **6** and signal channelizer **7** are of conventional design known in the art and, in themselves, form no part of the invention. The signal channelizer **7** operates to separate the signal elements of the multiplex signal for assignment to separate message channels in accordance with the type of aggregation employed in the telegraph system. In the example shown in Figure 1, the signal elements are assigned to the four message channels A, B, C and D included in the multiplex signal. The signal elements carried over the separate message channels A, B, C and D are applied to translating arrangements **8***a*, **8***b*, **8***c* and **8***d*, respectively, which are individual to the respective message channels. The translator circuits **8***a*–**8***d* may operate to convert the seven element protected code signals applied to their input circuits into conventional five element printing code signals. The converted signals are presented by the translator circuits **8***a*–**8***d* at terminals **9***a*–**9***d*, respectively, for application to telegraph printing equipment or other utilization circuits, not shown, and which form no part of the invention.

The aggregate signal reshaper **6**, signal channelizer **7**, and the translator circuits **8** are operated in the proper time relationship by a plurality of timing waves obtained from a timing wave generator **12**. The timing wave generator **12** is connected to the aggregate signal reshaper **6** by connections indicated by the functional lead **13**, to the signal channelizer **7** by connections indicated by the functional lead **14**, and to the translator circuits **8** by connections indicated by the functional lead **15**. The timing wave generator **12** is driven by a standard reference wave from a source **16** by way of connections including a synchronizing circuit **17** and a phase adjusting circuit **18**. Before phasing may be effected, the receiving terminal aparatus must first be synchronized. That is, the transitions of the element rate timing waves must coincide substantially with the transitions of the received telegraph signal. To do this, the incoming signal, at the output circuit of signal reshaper **6** is compared by connections indicated by the functional lead **19** with the locally generated base timing wave, obtained from the timing wave generator **12** by connections indicated by the functional lead **20**, in a phase detector circuit **21**. Depending on the relative phase relationship of the applied waves, the phase detector circuit **21** provides zero output for the in-phase condition and output proportional to phase difference and direction. The output of the phase detector **21** is applied by way of connections indicated by the functional lead **22** to the synchronizing circuit **17**, which, for example, may be a binary reciproconductive circuit, interposed in the operating circuit of the timing wave generator **12** between the source of reference wave **16** and the phase adjusting circuit **18**. The synchronizing circuit **17** operates to adjust the phase of the wave or reference signal applied to timing wave generator **12** in either direction in steps small relative to the adjustment provided by the operation of the phase correcting circuit according to the invention. The source **16** may be in the form shown and disclosed in U. S. Patent 2,706,785, issued April 19, 1955, to Philip B. Volz, for Low Frequency Standard Generator. The translating arrangements **8***a*–**8***d* are known in the art. One arrangement that can be used is shown and described in copending U. S. patent application Ser. No. 361,979, filed June 16, 1953, on behalf of James S. Harris for Code Conversion System, now U. S. Patent 2,724,739, issued November 22, 1955, and another is described and shown in copending U. S. patent application Ser. No. 375,995, for Reversible Electronic Code Translators, filed August 24, 1953, on behalf of Arthur E. Canfora, Anthony Liguori, Eugene R. Shenk and Hajime J. Kishi, now U. S. Patent 2,744,955, issued May 8, 1956. Examples of electronic circuitry of the remaining portions of the circuit arrangement shown in Figure 1, which have been described thus far, can be found in detail in U. S. Patent 2,716,158 supra.

The term "reciproconductive circuit" as employed herein is construed to include all regenerative dual controlled electron flow path device circuit arrangements in which conduction alternates in one or the other device. Examples of such devices are the high vacuum and gaseous electron discharge devices, the transistor and in some instances the semi-conductor and the para-magnetic switching structure. The monostable reciproconductive circuit, which requires one triggering pulse to switch from stable state of conduction to the unstable reciprocal state and which restores itself after an interval of time, is occasionally referred to as a monostable multivibrator, as in U. S. Patent 2,716,158, and often referred to as a "trigger circuit." The bistable reciproconductive circuit, referred to as a bistable multivibrator in U. S. Patent 2,716,158, is one having two degrees of equilibrium and which requires two triggering pulses; one to switch from one stable state to the other stable state and the other to restore the circuit to its original condition. This type of reciproconductive circuit comprises two distinct types. One type, the "lockover" reciproconductive circuit, has two trigger input terminals and requires triggering at alternate terminals to reverse the state of conduction, whereas the other type, the "binary" reciproconductive circuit, has a single terminal and the conductivity is reversed upon each application of triggering potential to the one terminal.

According to the invention, the phase adjusting circuit **18** is arranged to advance the phase of the base timing wave applied to the timing wave generator **12** in steps of time duration corresponding to a signal element in response to correction pulses generated in response to phase error signals indicating that the receiving terminal apparatus is out of phase with the incoming signal. The phase adjusting circuit **18** may be a "binary" reciproconductive circuit arranged much in the same manner as the synchronizing circuit **17** according to the teachings in U. S. Patent 2,716,158 hereinbefore mentioned. Alternatively, it may be arranged in accordance with the teach-

ings in U. S. Patent 2,714,627, issued August 2, 1955, to Eugene R. Shenk and Philip E. Volz for Electronic Multiplex Telegraph Receiving Terminal Apparatus. In some instances, it is suggested that a single phase adjusting circuit may be used both for synchronizing and phasing. This is possible where the circuit constants do not differ too greatly between the values required for small phase changes for synchronizing and the larger phase changes for phasing the signal received with the generated base timing wave. The error signals which are used to control phase adjusting circuit **18** through circuitry to be described are obtained from circuitry known to the art as "mutilation" detectors or "validity" checking circuits. A mutilation detector is connected to each channel of communication and is arranged to produce an output whenever the ratio of the number of signal elements of one nature to the number of signal elements of another nature differs from the established ratio for the protected code under consideration. Such detectors are known in the art. For example, there is the validity checking circuit shown and described in U. S. Patent 2,688,050, issued August 31, 1954, to James S. Harris. Such arrangements are used in the present telegraph art to cause a teleprinter to print a special character indicating that the character transmitted was not received in proper form or to initiate the operation of automatic equipment for requesting repetition of the character originally transmitted until it is received in proper form. Although mutilation detectors or validity checking circuits provide output only when the ratio of signal elements of a character is other than normal ratio, in contradistinction to the operation of cotranslating circuits which operate only when the proper ratio exists, the basic circuitry of the two circuits have much in common. Therefore, it is conventional in practice to combine code translating and multilation detecting circuitry in one physical structure. For example, the validity checking circuit shown in U. S. Patent 2,688,050, hereinbefore mentioned, may be interconnected with a code translator constructed according to the teachings of U. S. patent application Ser. No. 361,979, filed June 16, 1953, on behalf of James S. Harris and entitled Code Conversion System, supra. Another example of a combined code translator and mutilation detector is shown and described in the copending U. S. patent application Ser. No. 375,995, for Reversible Electronic Code Translators, filed August 24, 1953, on behalf of Arthur E. Canfora, Anthony Liguori, Eugene R. Shenk and Hajami J. Kishi, supra.

Whether or not the code translator circuit and the mutilation detector circuit are combined, channelized signals from the signal channelizing circuit **7** are applied to mutilation detecting circuits **10***a*, **10***b*, **10***c* and **10***d* to present an error signal at terminals **11***a*, **11***b*, **11***c*, and **11***d*, respectively, in the event that an improper ratio exists. The error signals are then applied over separate paths to a coincidence circuit **23** which is arranged to produce an output only upon error signals being present in a plurality of these paths. In the arrangement shown in the hereinbefore mentioned copending application Ser. No. 375,995, a steady output voltage is obtained from the mutilation detecting circuit. Therefore, control signals from the various mutilation detecting circuits would be applied simultaneously to the coincidence circuit **23** when mutilated characters are discovered at the same time in a plurality of the message channels A, B, C and D. It is possible, however, to make use of mutilation detectors found in code translators known in the art which develop a pulse output. If such circuits are used, it is necessary to use some type of storage means to ensure the simultaneous application of the control signals to the coincidence circuit **23**. Delay circuits **24***a*, **24***b*, **24***c* and **24***d* can be individually inserted in the paths between the respective mutilation detecting circuits **10***a*, **10***b*, **10***c*, **10***d* and the coincidence circuit **23**. The delay circuits may be simple monostable multivibrators or reciproconductive circuits such as are found in U. S. Patent 2,671,132, which was issued to Eugene R. Shenk and Anthony Liguori on March 2, 1954. A coincidence circuit suitable for use in the arrangement shown in Figure 1 may also be found in this patent.

The circuit arrangement according to the invention, shown in Figure 1, operates on the assumption that a single mutilated character occurring on any one of the message channels A, B, C or D at any one time is not the result of an improper phasing condition. Similarly, a number of mutilated characters occurring in succession on a single channel or intermittently without any order on a plurality of the message channels A, B, C and D are assumed to result from factors other than improper phasing. Such mutilated characters may result from equipment failure, electrical interference in the radio path and so on. It is assumed that, when a mutilated character is discovered on more than one message channel at any one time, an improper phase relationship exists between the telegraph receiving terminal apparatus and the incoming multiplex signal. In this situation, the mutilation detectors **10***a*–**10***d* in the translator indicate these mutilated characters by applying error signals simultaneously to the coincidence circuit **23**. As is understood in the art, the coincidence circuit **23** operates in response to at least two error signals simultaneously applied thereto to produce a coincidence output signal. The coincidence circuit **23** may include a vacuum tube, a transistor, a diode, or a magnetic circuit biased in a manner preventing the operation of the circuit except upon the simultaneous application thereto of a plurality of control signals from the mutilation detecting circuits **10***a*–**10***d*.

The coincidence output signal, which indicates that phasing correction is necessary, is applied from the output of the coincidence circuit **23** to a correction pulse gating circuit **25** over a path indicated by the functional leads **26** and **27** and including the closed contacts of switches **30** and **31**. Timing waves occurring at the local timing rate are obtained from the timing wave generator **12** by means of connections indicated by the functional lead **33** and applied to a correction pulse generator **32**. The correction pulse generator **32** is synchronized by the timing waves applied thereto from the timing wave generator **12** to apply correction pulses to the correction pulse gating circuit **25**. The correction pulse gating circuit **25** operates in response to the coincidence output signal from the coincidence circuit **23** to pass the correction pulses to the phase adjusting circuit **18** over a path indicated by the functional lead **34**. The correction pulse generator **32** may be a simple bistable reciproconductive circuit or a chain of such circuits, such as are found in the U. S. Patents 2,714,627 and 2,716,158 hereinbefore mentioned. However, other types of arrangements known in the art may be used. It is only necessary that a pulse or pulses be produced from the output of the correction pulse generator **32** at a local timing pulse rate which is determined according to the particular application of the circuit arrangement of the invention. The pulse rate is such that the operation of the correction pulse generator **32** and correction pulse gating circuit **25** are synchronized with the operation of the remaining circuit components of the receiving terminal apparatus. The correction pulse gating circuit **25** may be any of the simple gating circuits found in the above-identified U. S. patents and copending applications.

The phase adjusting circuit **18** in response to the correction pulses from the correction pulse gating circuit **25** alters the phase of the standard reference wave obtained from the source **16** and applied to the timing wave generator **12**. The phase of the reference wave is advanced or retarded, preferably the former, by a predetermined amount to produce the base reference waves. In practice,

this predetermined amount is equal to the amount required to step the phase by one signal element spacing, the phase adjustment always being made in the same direction, that is, either always retarding or always advancing. The phase of the timing waves supplied by the timing wave generator 12 to the telegraph receiving terminal apparatus including the signal channelizer 7 is stepped a similar amount. The automatic phasing control circuit of the invention continues to hunt for the correct phase relationship by stepping the phase of the standard reference wave so long as a coincidence output signal appears in the output circuit of coincidence circuit 23. When a coincidence output signal no longer appears, indicating proper phase relationship, the phasing control circuit ceases hunting and the telegraph receiving terminal apparatus continues to operate in normal manner under the control of the synchronizing circuit, previously described.

In certain applications, it may be desirable to limit the operation of the phase correcting circuit of the invention. The phase correcting circuit, as thus far described, operates in response to each coincidence of error signals from the mutilation detecting circuits 10, as indicated by the output of the coincidence circuit 23, to alter the phase of the timing waves supplied by the timing wave generator 12. The proper phase is re-established, but several characters of the signals carried over channels A, B, C and D may be lost as the phase of the timing waves is altered, if automatic request and repitition equipment is not used. It may be felt desirable, therefore, to sacrifice some degree of accuracy and to operate the circuit of the invention only after a number of coincidence pulses have been developed, indicating a serious phase misalignment. A single coincidence pulse, while indicating a phase misalignment, may be due to a temporary condition and the loss of characters during phase correction may be unwarranted. The switch 31 is opened, and the coincidence pulses passing to the correction pulse gating circuit 25 are applied to a counting circuit 36, the counting circuit 36 being connected in parallel with the switch 31. The counting circuit 36 is arranged to count the coincidence pulses and to cause the correction pulse gating circuit 25 to apply correction pulses to the phase adjusting circuit 18 only after a predetermined count has been established. A timing wave is applied by connections indicated by the functional lead 37 to the counting circuit 36 from the timing wave generator 12 to reset the counting circuit 36. The counting circuit 36 operates in accordance with the timing wave only after a predetermined number of coincidence pulses have occurred during a predetermined time interval to cause a correction pulse to be applied from the correction pulse gating circuit 25 to the phase adjusting circuit 18. The counting circuit 36 may be in the form of a chain of bistable reciproconductive circuits as found in the previously mentioned U. S. patents. Other forms of counting circuits, such as the step-wave generating and counting circuit also are known.

Another arrangement may also be used to determine the desired number of coincidence pulses before the correction pulse generator 32 is connected to the phase adjusting circuit 18. The switch 31 is closed, effectively removing the counting circuit 36 from the phase correcting circuit Switch 30 is opened, and the coincidence output signal from the coincidence circuit 23 which is arranged to supply a pulse output signal is applied to a delay circuit 38 which may be a simple monostable multivibrator or other known form of delay circuit and which may be of the same construction as the delay circuits 24. The delay circuit 38 is arranged to delay the application of the coincidence output signal until the time for the next coincidence output signal to appear. At the time the delay circuit 38 is actuated, a gating circuit 39 is also set to pass the next coincidence output signal directly to a coincidence circuit 40 by connections indicated by the functional lead 29. The coincidence circuit 40 may be of the same construction as coincidence circuit 23. Following the second coincidence output signal, the delay circuit 38 passes the first coincidence output signal to the coincidence circuit 40. The output of the delay circuit 38 is insufficient to operate the coincidence circuit 40. However, the gating circuit 39 operates to pass the second coincidence output signal directly to the coincidence circuit 40. The coincidence circuit 40 operates in response to the two applied signals to apply a coincidence output signal to the correction pulse gating circuit 25. The automatic phasing circuitry of the invention operates, thereafter, in exactly the same manner already described. Although only one delay circuit 38 is shown, a plurality of such delay circuits with different time constants may be used. For example, a second delay or storage circuit, not shown, having a lesser storage period may be set in readiness for a further coincidence output signal from the coincidence circuit 23 by the operation of the delay circuit 38. The second delay circuit will present its output signal to the coincidence circuit 40 and simultaneously trigger the gating circuit 39 for direct application of a final coincidence output signal from the coincidence circuit 23 to the coincidence circuit 40. The further operation of the phasing circuitry of the invention is again the same as already described.

A further arrangement could be used in a circuit in which the code translator circuits 8 are arranged to produce a pulse output from the mutilation detectors. A counting circuit, not shown, can be used in place of the coincidence circuit 23. The delay circuits 24 are removed and the output signals of the mutilation detectors are applied directly to the counting circuit. When the mutilation detectors are arranged to produce steady output signals, pulse generating circuits known in the art, and which may be simple differentiating circuits followed by monostable reciproconductive circuits, can be inserted in each of the output paths of the mutilation detectors in place of the delay circuits 24, the pulse generating circuits operating to apply pulse signals indicative of an improper phase relationship to the counting circuit. The counting circuit in each case is reset by a timing signal from the timing wave generator 12 and operates to apply a control signal in response to a predetermined count to the correction pulse gating circuit 25. Switches 30 and 31 are both closed and the circuit of the invention will operate in response to the output signal from the counting circuit to correct the phase relationship between the telegraph receiving terminal apparatus and the incoming signal applied to terminals 5 in the manner described above.

It has been assumed in the discussion of the invention in connection with Figure 1 that an improper phase relationship is to be indicated by a plurality of output signals simultaneously applied from the mutilation detectors 10 to the coincidence circuit 23. In practice, an improper phase relationship is generally indicated by three or more mutilation signals appearing simultaneously at the input of the coincidence circuit 23. However, the appearance of only two mutilation signals is in most occurrences also due to an improper phase relationship and the circuit of the invention shown in Figure 1 is designed to operate in response to this condition. A feature of the invention, however, is that it is not limited to the particular arrangement shown in Figure 1. Referring to a Figure 2, there is shown a functional diagram of a modification of the structure outlined in Figure 1. It may be assumed that an improper phase relationship is indicated by a plurality of mutilation or error signals appearing in succession on the output path of one of the mutilation detectors 10.

As shown in Figure 2, the incoming aggregate multiplex signal appearing at the terminals 28 is applied to the signal channelizer 7. The necessary timing waves are applied at the terminals 42 and 44 of the functional leads 14 and 15, respectively, as in the arrangement of Figure 1. The signal channelizer 7 operates to separate the signal elements contained in the multiplex signal and

to apply them to the mutilation detecting circuits **10***a*′–**10***d*′, if not to code translating circuits **8** as well, in accordance with the type of transmission employed. The error detecting circuit **10***a*′ connected to message channel A is arranged to produce an error signal in response to the reception of each mutilated character over message channel A and apply that error signal by means of terminals **11***a* to a delay circuit **45**. The time constant of the delay circuit **45** is such that a first error signal caused by a mutilated character appearing on message channel A causes the delay circuit **45** to be activated. A gating circuit **46** is readied by the activation of delay circuit **45** and operates upon the application of a second error signal, due to the appearance of a second mutilated character on message channel A immediately following the first mutilated character, to pass the signal indicative of the second mutilated character to the coincidence circuit **23**. The delay circuit **45** operates to simultaneously apply the delayed signal indicative of the first mutilated character to the coincidence circuit **23**. The coincidence circuit **23** depelops a coincidence output signal which is applied to the correction pulse gating circuit **25** to gate correction pulses appearing at the correction pulse terminals **48** to the phase adjusting circuit **18** at terminals **49**, the phase correcting circuit of the invention operating in the manner previously described. The output signal of the delay circuit **45** is insufficient to operate the coincidence circuit **23**. An output signal from both the delay circuit **45** and the gating circuit **46** must be applied simultaneously to the coincidence circuit **23** to cause the coincidence circuit **23** to operate. The arrangement shown in Figure 2, therefore, operates on the assumption that two mutilated characters appearing in succession over a single message channel are indicative of an improper phase relationship.

Additional delay circuits may be inserted in the output path of the mutilation detector **10***a*′ and arranged so that a larger predetermined number of signals from the mutilation detector **10***a*′ must occur before coincidence signals are applied to the coincidence circuit **23**. The phase correcting circuit of the invention may be adapted in this manner to operate in response to any predetermined number of mutilated characters appearing in succession over message channel A. While the phase correcting circuitry is shown in Figure 2 as being operated in association with the mutilation detecting circuit **10***a*′, it is to be understood that any one of the mutilation detecting circuits **10***a*′–**10***d*′ could be used in the manner described.

Many combinations of the arrangements shown in Figures 1 and 2 are available for use in particular applications of the invention. The arrangement used depends on the assumption made as to the most adequate arrangement in a particular application to reveal a condition of improper phase relationship between a telegraph receiving terminal apparatus and an incoming multiplex signal. For example, a delay arrangement such as is shown in Figure 2 can be inserted in the output circuits of each of mutilation detectors **10***a*–**10***d* of the arrangement shown in Figure 1. The output signals of the coincidence circuits associated with each of the delay circuits would be applied to a final coincidence circuit, the coincidence output signal from the final coincidence circuit being applied to the correction pulse gating circuit **25**. In this arrangement, a predetermined number of mutilated characters would have to appear in succession on at least two of the message channels A, B, C or D at the same time before the final coincidence circuit would be operated to apply a coincidence output signal to the correction pulse gating circuit **25**. The assumption would be, of course, that a predetermined number of mutilated characters appearing in succession on a plurality of message channels A, B, C and D at a given time are indicative of an out-of-phase condition in the operation of the telegraph receiving terminal apparatus. Other embodiments and modifications will be suggested to those skilled in the art.

The invention claimed is:

1. An electronic circuit arrangement for automatically phasing a received bistatic aggregate signal wave of the type including a train of signal elements expressing a plurality of intelligence characters in multiplex fashion with a timing wave locally generated in a receiving apparatus, each of said characters being constituted by a predetermined ratio of said signal elements of one static nature to the number of said signal elements in each of said characters as a whole, said circuit comprising a signal channelizer, means for applying said received wave to said signal channelizer, a timing wave generator included in said receiving apparatus and coupled to said signal channelizer, said timing wave generator producing said timing wave, a phase adjusting circuit, a source of standard reference wave, means for applying said reference wave from said source to said timing wave generator over a path including said phase adjusting circuit, said timing wave generator being operated in response to said reference wave to apply said timing wave to said signal channelizer, said signal channelizer being operated in response to said timing wave to distribute said signal elements according to said characters among a plurality of channels in a predetermined manner, a plurality of utilization circuits, means for individually and electrically connecting said channels to said utilization circuits, a separate counting circuit included in each of said channels and arranged to count the number of said signal elements of said one static nature in each character appearing on said respective channels, each of said counting circuits producing a control signal whenever a count other than a predetermined count is obtained, means for operating said phase adjusting circuit in response to the occurrence of a control signal in the output circuit of more than one of said counting circuits at a given time to alter the phase of said reference wave applied to said timing wave generator from said source, said timing wave being varied in phase with respect to said reference wave and into a predetermined phase relationship with said received wave.

2. An electronic circuit arrangement for automatically phasing a received bistatic aggregate signal wave of the type including a train of signal elements expressing a plurality of intelligence characters in multiplex fashion with a timing wave locally generated in a receiving apparatus, each of said characters being constituted by a predetermined ratio of said signal elements of one static nature to the number of said signal elements in each of said characters as a whole, said circuit comprising a signal channelizer, means for applying said received wave to said signal channelizer, a timing wave generator included in said receiving apparatus and coupled to said signal channelizer, said timing wave generator producing said timing wave, a phase adjusting circuit, a source of standard reference wave, means for applying said reference wave from said source to said timing wave generator over a path including said phase adjusting circuit, said timing wave generator being operated in response to said reference wave to apply said timing wave to said signal channelizer, said signal channelizer being operated in response to said timing wave to distribute said signal elements according to said characters among a plurality of channels in a predetermined manner, a plurality of utilization circuits, means for individually and electrically connecting said channels to said utilization circuits, a separate counting circuit included in each of said channels and arranged to count the number of said signal elements of said one static nature in each character appearing on said respective channel, each of said counting circuits producing a control signal whenever a count other than a predetermined count according to said ratio is obtained, a coincidence circuit coupled to each of said

counting circuits and functioning in response to the simultaneous application of a control signal from more than one of said counting circuits to produce a coincidence output signal, means for operating said phase adjusting circuit in response to said coincidence output signal to alter the phase of said reference wave applied to said timing wave generator from said source, said timing wave being varied in phase with respect to said reference wave and into a predetermined phase relationship with said received wave.

3. An electronic circuit arrangement for automatically phasing a received bistatic aggregate signal wave of the type including a train of signal elements expressing a plurality of intelligence characters in multiplex fashion with a timing wave locally generated in a receiving apparatus, each of said characters being constituted by a predetermined ratio of said signal elements of one static nature to the number of said signal elements in each of said characters as a whole, said circuit comprising a signal channelizer, means for applying said received wave to said signal channelizer, a timing wave generator included in said receiving apparatus and coupled to said signal channelizer, said timing wave generator producing said timing wave, a phase adjusting circuit, a source of standard reference wave, means for applying said reference wave from said source to said timing wave generator over a path including said phase adjusting circuit, said timing wave generator being operated in response to said reference wave to apply said timing wave to said signal channelizer, said signal channelizer being operated in response to said timing wave to distribute said signal elements according to said characters among a plurality of channels in a predetermined manner, a plurality of utilization circuits, means for individually and electrically connecting said channels to said utilization circuits, a separate counting circuit included in each of said channels and arranged to count the number of said signal elements of said one static nature in each character appearing on said respective channels, each of said counting circuits producing a control signal whenever a count other than a predetermined count according to said ratio is obtained, a coincidence circuit coupled to the output circuit of each of said counting circuits, said coincidence circuit being arranged to operate in response to the simultaneous application of a control signal from more than one of said counting circuits to produce a coincidence output signal, a correction pulse gating circuit coupled to said coincidence circuit and to said phase adjusting circuit, means including a correction pulse generator for applying timing pulses to said correction pulse gating circuit from said timing wave generator, said correction pulse gating circuit being operated by said timing pulses and in response to each coincidence output signal produced by said coincidence circuit to apply a correction pulse to said phase adjusting circuit, said phase adjusting circuit being operated in response to each correction pulse produced by said correction pulse gating circuit to alter the phase of said reference wave applied to said timing wave generator from said source, said timing wave being varied in phase with respect to said reference wave and into a predetermined phase relationship with said received wave.

4. An electronic circuit arrangement for automatically phasing a received bistatic aggregate signal wave of the type including a train of signal elements expressing a plurality of intelligence characters in multiplex fashion with a timing wave locally generated in a receiving apparatus, each of said characters being constituted by a predetermined ratio of said signal elements of one static nature to the number of said signal elements in each of said characters as a whole, said circuit comprising a signal channelizer, means for applying said received wave to said signal channelizer, a timing wave generator included in said receiving apparatus and coupled to said signal channelizer, said timing wave generator producing said timing wave, a phase adjusting circuit, a source of standard reference wave, means for applying said reference wave from said source to said timing wave generator over a path including said phase adjusting circuit, said timing wave generator being operated in response to said reference wave to apply said timing wave to said signal channelizer, said signal channelizer being operated in response to said timing wave to distribute said signal elements according to said characters among a plurality of channels in a predetermined manner, a plurality of utilization circuits, means for individually and electrically connecting said channels to said utilization circuits, a separate counting circuit included in each of said channels and arranged to count the number of said signal elements of said one static nature in each character appearing on said respective channels, each of said counting circuits producing a control signal whenever a count other than a predetermined count according to said ratio is obtained, a coincidence circuit coupled to the output circuit of each of said counting circuits, said coincidence circuit being arranged to operate in response to the simultaneous application of a control signal from more than one of said counting circuits to produce a coincidence pulse output signal, a correction pulse gating circuit coupled to said phase adjusting circuit, means including a correction pulse generator for applying a first train of timing pulses to said correction pulse gating circuit from said timing wave generator, a counting circuit coupled to said correction pulse gating circuit and to said coincidence circuit, means for applying a second train of timing pulses from said timing wave generator to said last-mentioned counting circuit, said last-mentioned counting circuit being operated in response to a predetermined number of said coincidence output signals received from said coincidence circuit to apply a signal to said correction pulse gating circuit, said correction pulse gating circuit being operated by said first train of timing pulses in response to each signal received from said last-mentioned counting circuit to apply a correction pulse to said phase adjusting circuit, said phase adjusting circuit being operated in response to each correction pulse received from said correction pulse gating circuit to alter the phase of said reference wave applied to said timing wave generator from said source, whereby said timing wave is varied in phase with respect to said reference wave and into a predetermined phase relationship with said received wave.

5. An electronic circuit arrangement for automatically phasing a received bistatic aggregate signal wave of the type including a train of signal elements expressing a plurality of intelligence characters in multiplex fashion with a timing wave locally generated in a receiving apparatus, each of said characters being constituted by a predetermined ratio of said signal elements of one static nature to the number of said signal elements in each of said characters as a whole, said circuit comprising a signal channelizer, means for applying said received wave to said signal channelizer, a timing wave generator included in said receiving apparatus and coupled to said signal channelizer, said timing wave generator producing said timing wave, a phase adjusting circuit, a source of standard reference wave, means for applying said reference wave from said source to said timing wave generator over a path including said phase adjusting circuit, said timing wave generator being operated in response to said reference wave to apply said timing wave to said signal channelizer, said signal channelizer being operated in response to said timing wave to distribute said signal elements according to said characters among a plurality of channels in a predetermined manner, a plurality of utilization circuits, means for individually and electrically connecting said channels to said utilization circuits, a separate counting circuit included in each of said channels and arranged to count the number of said signal elements of said one static nature in each character appearing on said respective channels, each of said counting cir-

cuits producing a control signal whenever a count other than a predetermined count according to said ratio is obtained, a coincidence circuit coupled to the output circuit of each of said counting circuits, said coincidence circuit being arranged to operate in response to the simultaneous application of a control signal from more than one of said counting circuits to produce a coincidence output signal, a delay circuit coupled to said coincidence circuit, a gating circuit coupled to said delay circuit and to said coincidence circuit, a second coincidence circuit coupled to said gating circuit and to said delay circuit, said delay circuit being operated in response to a predetermined number of said coincidence output signals to apply a coincidence output signal to said second coincidence circuit and to cause said gating circuit to simultaneously apply a final coincidence output signal to said second coincidence circuit, a correction pulse gating circuit coupled to said second coincidence circuit and to said phase adjusting circuit, said second coincidence circuit being operated in response to the simultaneous application of said coincidence output signals from said gating circuit and said delay circuit to apply a second coincidence output signal to said correction pulse gating circuit, means including a correction pulse generator for applying timing pulses to said correction pulse gating circuit from said timing wave generator, said correction pulse gating circuit being operated by said timing pulses and in response to each of said second coincidence output signals to apply a correction pulse to said phase adjusting circuit, said phase adjusting circuit being operated in response to each correction pulse to alter the phase of said reference wave applied to said timing wave generator from said source, said timing wave being varied in phase with respect to said reference wave and into a predetermined phase relationship with said received wave.

6. An electronic circuit arrangement for automatically phasing a received bistatic aggregate signal wave of the type including a train of signal elements expressing a plurality of intelligence characters in multiplex fashion with a timing wave locally generated in a receiving apparatus, each of said characters including seven signal elements arranged in a ratio of three signal elements of marking condition to four signal elements of spacing condition, said circuit comprising a signal channelizer, means for applying said received wave to said signal channelizer, a timing wave generator included in said receiving apparatus and coupled to said signal channelizer, said timing wave generator producing said timing wave, a phase adjusting circuit, a source of standard reference wave, means for applying said reference wave from said source to said timing wave generator over a path including said phase adjusting circuit, said timing wave generator being operated in response to said reference wave to apply said timing wave to said signal channelizer, said signal channelizer being operated in response to said timing wave to distribute said signal elements according to said characters among a plurality of chanels in a predetermined manner, a code translating circuit included in each of said channels and operated to convert said seven signal element characters into five signal element code characters, a pluarlity of utilization circuits, means for individually applying said five signal element code characters from said code translating circuits to said utilization circuits, a separate counting circuit included in each of said translating circuits and arranged to count the number of said signal elements of said marking condition in each seven signal element characters appearing on said respective channels, each of said counting circuits producing a control signal whenever a count of other than three signal elements of said marking condition is obtained, a coincidence circuit coupled to the output circuit of each of said counting circuits, said coincidence circuit being arranged to operate in response to the simultaneous application of a control signal from more than one of said counting circuits to produce a coincidence output signal, a correction pulse gating circuit coupled to said coincidence circuit and to said phase adjusting circuit, means including a correction pulse generator for applying timing pulses to said correction pulse gating circuit from said timing wave generator, said correction pulse gating circuit being operated by said timing pulses and in response to each concidence output signal produced by said coincidence circuit to apply a correction pulse to said phase adjusting circuit, said phase adjusting circuit being operated in response to each correction pulse produced by said correction pulse gating circuit to alter the phase of said reference wave applied to said timing wave generator from said source, said timing wave being varied in phase with respect to said reference wave and into a predetermined phase relationship with said received wave.

7. An electronic circuit arrangement for automatically phasing a received polystatic aggregate signal wave of the type including a train of signal elements representative of a plurality of intelligence characters in multiplex fashion with a timing wave locally generated in receiving apparatus, said signal elements of different static natures being arranged in each of said characters in a predetermined manner, said circuit comprising a signal channelizer, means for applying said received wave to said signal channelizer, a timing wave generator for producing said timing wave included in said receiving apparatus and coupled to said signal channelizer, control means for operating said timing wave generator to apply said timing wave to said signal channelizer, said signal channelizer being operated in response to said timing wave to distribute said signal elements according to said characters among a plurality of channels in a predetermined manner, a plurality of utilization circuits, means for individually and electrically connecting said channels to said utilization circuits, a separate counting circuit included in at least a first and second one of said channels and arranged to count the number of said signal elements of one static nature in each character appearing on said respective first and second channels, said counting circuits each producing an error signal whenever a count other than a predetermined count is obtained, means connected to each of said counting circuits and functioning in response to the occurrence of an error signal in the output circuits of both of said counting circuits in a given time relationship to operate said control means to alter the operation of said timing wave generator, said timing wave generator being operated by said control means to vary the phase of said timing wave into a predetermined phase relationship with said received wave.

8. An electronic circuit arrangement for automatically phasing a received polystatic aggregate signal wave of the type including a train of signal elements expressing a plurality of intelligence characters in multiplex fashion with a timing wave locally generated in receiving apparatus, each of said characters being constituted by a predetermined ratio of said signal elements of one static nature to the number of said signal elements in each of said characters as a whole, said circuit comprising a signal channelizer, means for applying said received wave to said signal channelizer, a timing wave generator for producing said timing wave included in said receiving apparatus and coupled to said signal channelizer, a phase adjusting circuit, a source of standard reference wave, means for applying said reference wave from said source to said timing wave generator over a path including said phase adjusting circuit, said timing wave generator being operated in response to said reference wave to apply said timing wave to said signal channelizer, said signal channelizer being operated in response to said timing wave to distribute said signal elements according to said characters among a plurality of channels in a predetermined manner, a plurality of utilization circuits, means for individually and electrically connecting said channels to said utilization circuits, a separate ratio determining circuit included in at least a first and second one of said chan-

nels and arranged to determine the ratio of said signal elements of said one static nature to the signal elements of another static nature in each character appearing on said respective first and second channels, said ratio determining circuits each producing a control signal whenever a ratio other than said predetermined ratio is determined, means connected to each of said ratio determining circuits and functioning in response to the occurrence of a control signal in the output circuits of both of said ratio determining circuits at the same time to operate said phase adjusting circuit to alter the phase of said reference wave applied to said timing wave generator from said source to cause said timing wave to be varied into a predetermined phase relationship with said received wave.

9. An electronic circuit arrangement for automatically phasing a received polystatic aggregate signal wave of the type including a train of signal elements representative of a plurality of intelligence characters in multiplex fashion with a timing wave locally generated in receiving apparatus, said signal elements of different static natures being arranged in each of said characters in a predetermined manner, said circuit comprising a signal channelizer, means for applying said received wave to said signal channelizer, a timing wave generator for producing said timing wave included in said receiving apparatus and coupled to said signal channelizer, control means for operating said timing wave generator to apply said timing wave to said signal channelizer, said signal channelizer being operated in response to said timing wave to distribute said signal elements according to said characters among a plurality of channels in a predetermined manner, a plurality of utilization circuits, means for individually and electrically connecting said channels to said utilization circuits, a separate counting circuit included in each of said channels and arranged to count the number of said signal elements of one static nature in each character appearing on said respective channels, said counting circuits each producing an error signal whenever a count other than a predetermined count is obtained, means connected to each of said counting circuits and functioning in response to the occurrence of an error signal in the output circuit of more than one of said counting circuits at a given time to operate said control means to alter the operation of said timing wave generator, said timing wave generator being operated by said control means so as to vary the phase of said timing wave into a predetermined phase relationship with said received wave.

10. An electronic circuit arrangement for automatically phasing a received polystatic aggregate signal wave of the type including a train of signal elements representative of a plurality of intelligence characters in multiplex fashion with a timing wave locally generated in receiving apparatus, each of said characters being constituted by a predetermined ratio of said signal elements of one static nature to the number of said signal elements in each of said characters as a whole, said circuit comprising a signal channelizer, means for applying said received wave to said signal channelizer, a timing wave generator for producing said timing wave included in said receiving apparatus and coupled to said signal channelizer, control means for operating said timing wave generator to apply said timing wave to said signal channelizer, said signal channelizer being operated in response to said timing wave to distribute said signal elements according to said characters among a plurality of channels in a predetermined manner, a plurality of utilization circuits, means for individually and electrically connecting said channels to said utilization circuits, a separate counting circuit included in each of said channels and arranged to count the number of said signal elements of said one static nature in each character appearing on said respective channels, said counting circuits each producing an error signal whenever a count other than a predetermined count is obtained, a coincidence circuit connected to each of said counting circuits and functioning in response to the occurrence of an error signal in the output circuit of more than one of said counting circuits at a given time to operate said control means to alter the opertion of said timing wave generator so as to vary the phase of said timing wave into a predetermined phase relationship with said received wave.

11. An electronic circuit arrangement for automatically phasing a received bistatic aggregate signal wave of the type including a train of signal elements expressing a plurality of intelligence characters in multiplex fashion with a timing wave locally generated in a receiving apparatus, each of said characters including seven signal elements arranged in a given ratio of three signal elements of marking condition to four signal elements of spacing condition, said circuit comprising a signal channelizer, means for applying said received wave to said signal channelizer, a timing wave generator for producing said timing wave included in said receiving apparatus and coupled to said signal channelizer, control means for operating said timing wave generator to apply said timing wave to said signal channelizer, said signal channelizer being operated in response to said timing wave to distribute said signal elements according to said characters among a plurality of channels in a predetermined manner, a plurality of utilization circuits, means for individually and electrically connecting said channels to said utilization circuits, a separate ratio determining circuit included in each of said channels and arranged to count the number of said signal elements of said marking condition in each character appearing on said respective channels, said ratio determining circuits each producing a control signal whenever a ratio other than said given ratio is determined, means connected to each of said ratio determining circuits and functioning in response to the occurrence of a control signal in the output circuit of at least two of said ratio determining circuits at the same time to operate said control means to alter the operation of said timing wave generator, said timing wave generator being operated by said control means to vary the phase of said timing wave into a predetermined phase relationship with said received wave.

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