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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6: G01R 1/073, 1/067, 31/316

A3

(11) International Publication Number:

WO 97/43656

(43) International Publication Date:

20 November 1997 (20.11.97)

(21) International Application Number:

PCT/US97/08604

(22) International Filing Date:

15 May 1997 (15.05.97)

(30) Priority Data:

60/005,189	17 May 1996 (17.05.96)	US
PCT/US96/08107	24 May 1996 (24.05.96)	wo
(34) Countries for v	which the regional or	
international a	application was filed: U	JS et al.
60/020,869	27 June 1996 (27.06.96)	US
60/024,405	22 August 1996 (22.08.96)	US
60/024,555	26 August 1996 (26.08.96)	US
60/030,697	13 November 1996 (13.11.96)	
60/032,666	13 December 1996 (13.12.96)	US
60/034,053	31 December 1996 (31.12.96)	US
08/784,862	15 January 1997 (15.01.97)	US
08/788,740	24 January 1997 (24.01.97)	US
08/802,054	18 February 1997 (18.02.97)	US
08/819,464	17 March 1997 (17.03.97)	US
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- (81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

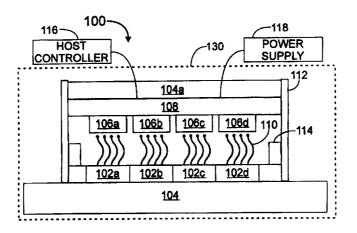
Published

With international search report.

Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(88) Date of publication of the international search report: 12 March 1998 (12.03.98)

(54) Title: WAFER-LEVEL BURN-IN AND TEST



(57) Abstract

Techniques for performing wafer-level burn-in and test of semiconductor devices include a test substrate having active electronic components such as ASICs mounted to an interconnection substrate or incorporated therein, metallic spring contact element effecting interconnections between the ASICs and a plurality of devices-under-test (DUTs) on a wafer-under-test (WUT), all disposed in a vacuum vessel so that the ASICs can be operated at temperatures independent from and significantly lower than the burn-in temperature of the DUTs. The spring contact elements may be mounted to either the DUTs or to the ASICs, and may fan out to relax tolerance constraints on aligning and interconnecting the ASICs and the DUTs. A significant reduction in interconnect count and consequent simplification of the interconnection substrate is realized because the ASICs are capable of receiving a plurality of signals for testing the DUTs over relatively few signal lines from a host controller and promulgating these signals over the relatively many interconnections between the ASICs and the DUTs. The ASICs can also generate at least a portion of these signals in response to control signals from the host controller. Physical alignment techniques are also described. Micromachined indentations on the front surface of the ASICs ensure capturing free ends of the spring contact elements. Micromachined features on the back surface of the ASICs and the front surface of the interconnection substrate to which they are mounted facilitate precise alignment of a plurality of ASICs on the support substrate.

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Inter. Inal Application No PCT/US 97/08604

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According to	o International Patent Classification (IPC) or to both national classifica	ion and IPC
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X Fur	ther documents are listed in the continuation of box C.	X Patent family members are listed in annex.
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	6 January 1998	1 5. 01. 98.
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	NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, East (431-70) 340-3016	Iwansson, K

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А	see abstract see page 5, line 50 - page 6, line 7 see page 7, line 7 - line 22; claim 2; figures 3,5,6 see page 10, line 24 - line 51	7,13,16, 17
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PCT/US 97/08604

Box I C	Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)
This Intern	national Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:
1.	Claims Nos.: because they relate to subject matter not required to be searched by this Authority, namely:
	Claims Nos.: because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
з. 🔲 с	Claims Nos.: because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).
Box II	Observations where unity of invention is lacking (Continuation of item 2 of first sheet)
This Inter	national Searching Authority found multiple inventions in this international application, as follows:
see	continuation sheet
1. X	As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
	As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3.	As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4.	No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
Remark	The additional search fees were accompanied by the applicant's protest. X No protest accompanied the payment of additional search fees.

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FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

- 1. claims 1-15,17-32,41-46,51-60: method for providing test signals to a DUT over common few lines as part of the wafer burn in and test
- 2. claims 16,33-40:

method for burning in semiconductor devices maintaining the DUT and the test substrate at different independent temperatures

3. claims 47,48:

performing burn-in with the DUT and the test substrate diposed in vacuum

4. claims 49,50:

method for aligning a plurality of electronic components to an interconnection substrate

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