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[54] **INFORMATION CONTROL IN A PROCESSING SYSTEM**
7 Claims, 1 Drawing Fig.

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[50] **Field of Search** 340/172.5

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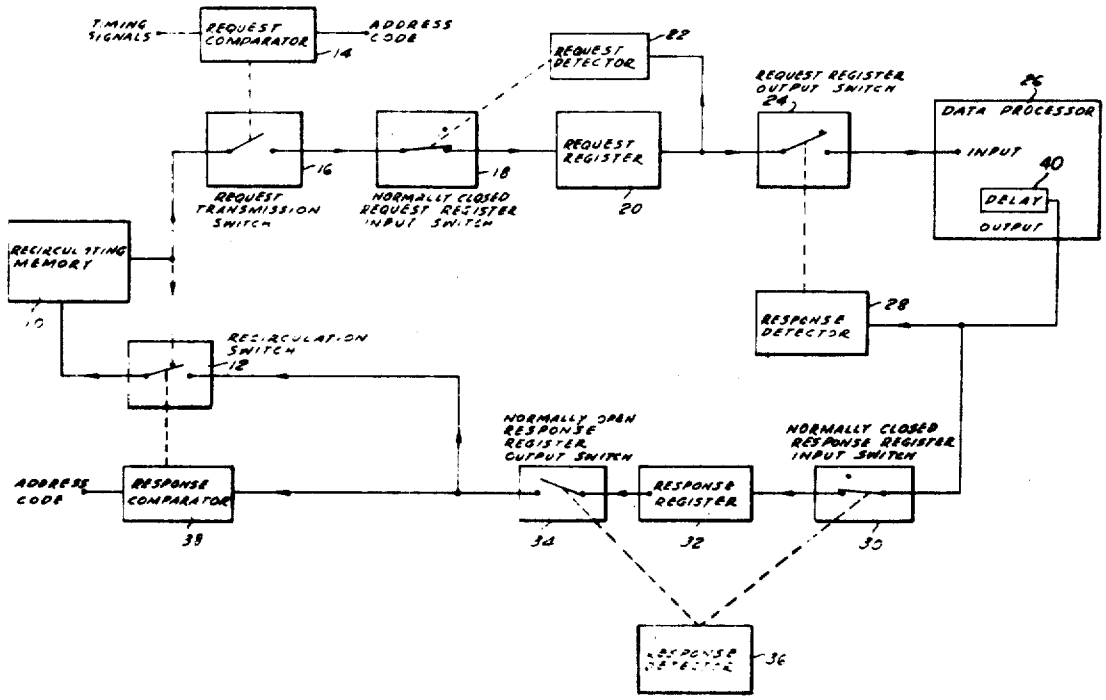
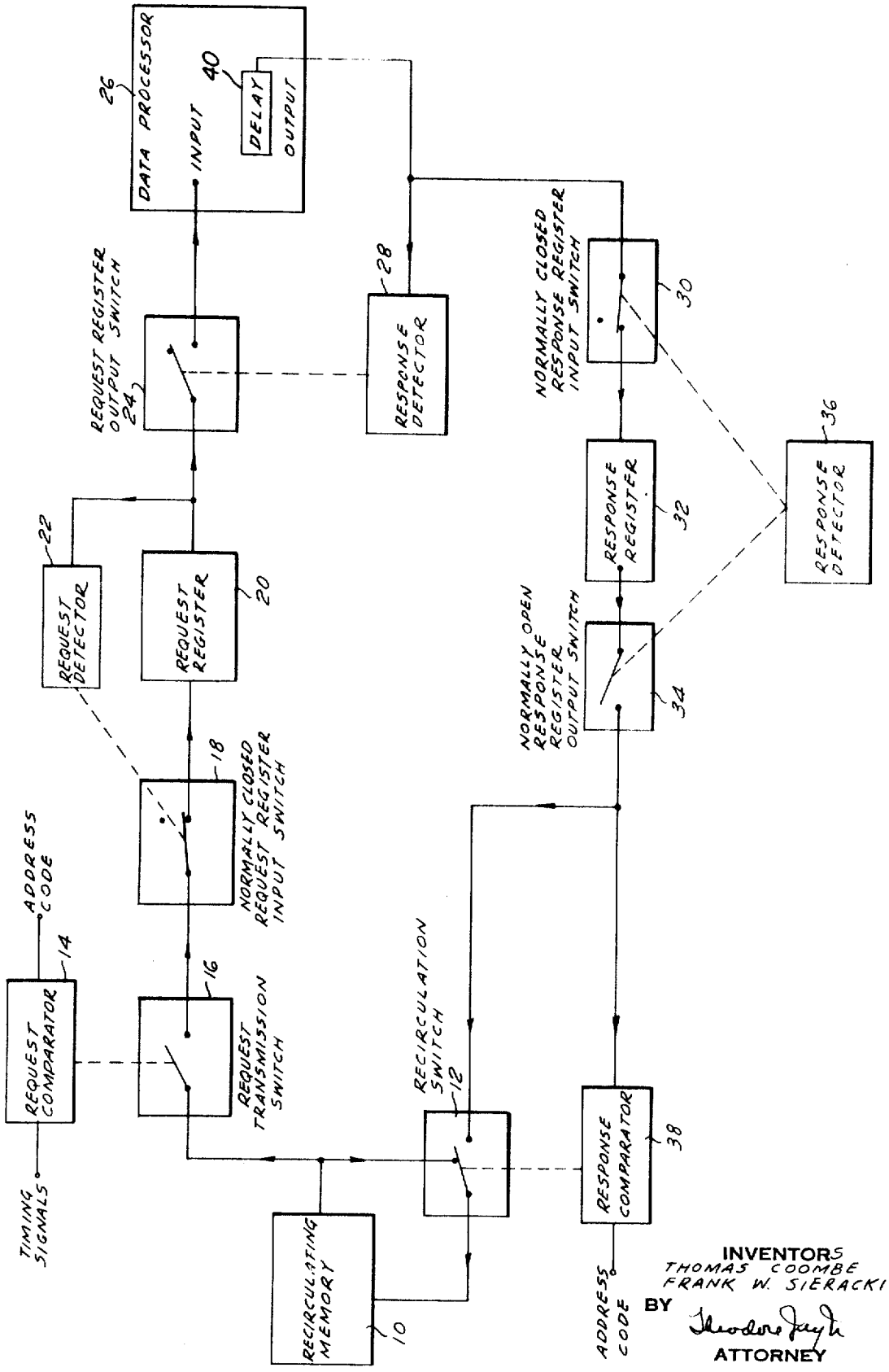
ABSTRACT: Information, such as stock market transactions, stored in a common memory, is to be displayed visually by a plurality of remotely disposed video monitors. The displays of the various monitors can be totally independent in content, but partial or complete duplication is possible. Each monitor has a keyboard associated therewith whereby the memory can be interrogated for certain specific information to be displayed by the corresponding monitor. To this end, interrogations or requests are supplied sequentially into the memory. The requests are then read out of the memory into a data processor which generates answers. The answers are fed back into the memory and then read out from the memory to the various monitors at which the requests originated.





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INFORMATION CONTROL IN A PROCESSING SYSTEM

CROSS-REFERENCES TO RELATED APPLICATIONS

Our copending application entitled "Information Storage and Display System" filed Mar. 28, 1969, Ser. No. 822,755, now Pat. No. 3,555,523, discloses apparatus wherein stock market transactions or other information stored in a single memory is to be displayed visually by a plurality of remotely disposed video monitors. The information can take the form of alphanumeric characters. The displays of the various monitors can be totally independent in content from each other but partial or complete duplication is possible.

BACKGROUND OF THE INVENTION

The apparatus disclosed in the above reference patent application cooperates with keyboards associated with each of the monitors whereby the memory can be interrogated for certain specific embodiments to be displayed by a corresponding monitor. To this end, requests or interrogations are supplied sequentially into the memory. The requests are read out of the memory into a data processor which generates answers. The answers are fed back into the memory and then read out from the memory to the various monitors at which the requests originated.

Our invention is directed toward apparatus which cooperates with the memory to feed requests out of the memory to a data processor and to feed answers back from the processor into the memory.

SUMMARY OF THE INVENTION

The memory is of the recirculation type wherein information in the series-bit, series-character form is recirculated past an output terminal. A recirculation switch, associated with the memory and included in the recirculation loop, has one position at which recirculation can be interrupted and old information selectively erased, while new information is inserted in the memory to replace the erased old information. The recirculation switch has a second position as which recirculation ensues, and no new information is inserted.

The recirculating information is disposed in time slots which have been preassigned to individual monitors. To insure that the requests forwarded from the memory to the data processor and the answers forwarded from the data processor to the memory are properly timed, i.e., that each answer is supplied only to the monitor at which the request originated, information transfers between the memory and the processor ensue under the control of timing of synchronization pulses. Each group of time slots is assigned a different address code uniquely identifying the monitor with which it is associated.

These address codes, in proper timing, are supplied sequentially to a request comparator. The comparator also receives timing signals which are in correspondence with the memory timing and identify in turn each time slot group as it appears at the output terminal of the memory. When an address code supplied to the comparator is in time coincidence with corresponding timing pulses identifying the group of slots associated with the address code, the comparator closes a request transmission switch and any request in the group of time slots is read out of the memory and passes in series-bit, series-character format through a normally closed request register input switch into a request register. When sufficient information has accumulated in the request register to the request register to indicate that a proper request can be forwarded to the processor, a request detector, coupled to the output of the request register, momentarily opens the request register input switch, thus momentarily preventing any additional data from being supplied to the register. The information then stored in the register passes out to the request register output switch. When the output switch is closed, the request is supplied to the input of the data processor which

generates an answer thereto. When this switch is open, no request are supplied to the processor.

A response detector receives answers from the output of the processor. When an answer is received by the response detector, the request register output switch is closed. When no answer is received this switch remains open. Proper timing between entry of answer requests into the processor and read out of answers from the processor is thus ensured. Consequently, arrival of a request at the processor is synchronized with the read out of an answer to another request from the processor.

The answers appearing at the output of the processor pass through a normally closed response register input switch to a response register. When sufficient information has accumulated in the response register to indicate that a proper answer can be forwarded to the memory, a response detector coupled to the output of the response register momentarily opens the response register input switch, thus momentarily preventing any additional data from being supplied to the register. The information then stored in the register passes out to the response register output switch which is controlled by the response detector to be opened when the response register input switch is closed and vice versa.

When the response register output switch is closed, the answer in the register passes therethrough and is supplied to both the recirculation switch and the response comparator. The address codes are also supplied to the comparator. The address codes are also supplied to the comparator. When an address code arrives at the response comparator in time coincidence with the same code in an answer, the comparator closes the recirculation switch, interrupting recirculation and entering the answer in the proper time slot in the memory.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawing illustrates a block diagram of one embodiment of my invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawing, a series-bit, series-character format recirculating memory **10**, for example a magnetostrictive delay line, is adapted to cooperate with recirculation switch **12**. When the switch is in the position shown, the output of the memory is fed back for recirculation to the input of the memory. Suitable amplification and pulse reshaping circuitry is normally used in such feedback connection.

When the switch **12** is in the opposite position, recirculation is interrupted and old information selectively erased, while new information is inserted. Switch **12** is the functional equivalent of the conventional pair of reverse acting read-in and erase gates.

The recirculating information is disposed in time slots which has been preassigned to individual monitors. The information in each slot appears in proper time sequence at the normally open request transmissions switch **16**. Timing signals developed elsewhere but designating sequentially each group of time slots identifying each monitor are supplied to one input of request comparator **14**.

Different address codes are preassigned to each of the monitors and are supplied in proper sequential timing to a second input of comparator **14**. When coincidence occurs, and only when it occurs, comparator **14** closes switch **16** and information is read out of the memory and passes through a normally closed request register input switch **18** into the request register **20**. This process insures that requests forwarded from the memory to the data processor and answers forwarded from the data processor to the memory are properly times to insure that each answer is supplied only to the monitor at which the request originated. An alternative process is to insert the appropriate address code in each group of time slots and to supply these codes from the memory to the first input of comparator **14** in place of the timing signals.

While a mechanical connection is shown between comparator **14** and switch **16**, it will be understood that switch **16** is a gate which is opened or closed upon receipt of signals from the output of the comparator which indicate noncoincidence or coincidence respectively.

The request register **20** has a number of stages into which information is entered. A proper request will cause a selected number of stages to contain information. For example, each bit of request data can enter the first stage and be transferred to the next stage upon receipt of the next bit until the last stage is filled. At this point, request detector **22**, detecting this condition, sends a control signal to the normally closed request register input switch **18** (which is typically a gate) to open same momentarily whereby additional data is momentarily blocked from entry into the register **20**.

The information then stored in the register **20** is then available for transmission at the request register output switch **24** which is typically a gate opened and closed by signals from the response detector **28**. When switch **24** is closed, the request is supplied to the input of data processor **26**. After a necessary delay in processing symbolized by delay box **40**, an answer is generated and appears at the output of processor **26**.

Response detector **28** receives these answers. Whenever an answer is received, detector **28** develops a signal which closes switch **24**. In the absence of such answer, switch **24** is held open. Obviously, because of the delay between supply of a request to the processor and the production of an answer to the request, the detector cannot close switch **24** to pass a request therethrough when an answer to this request is obtained from the processor. The purpose of the detector is to maintain proper timing so that any request can pass through switch **24** only when any answer is supplied to the detector **28**; i.e., arrival of any request at the input of the processor is synchronized with the read out of an answer to another request from the processor.

Answers from the processor are also supplied through normally closed responses register input switch **30** to a response register **32**. Register **32**, switch **30** and response detector **36** operates together in the same manner as register **20**, switch **18** and detector **22**, whereby when sufficient information has been accumulated in register **32** to indicate that a proper answer can be forwarded to the memory, switch **30** is momentarily opened to prevent additional data from being supplied to register **32**. Response register output switch **34**, which typically is a gate acting in reverse sense to that gate representing switch **30**, is controlled by detector **36** to be open when switch **30** is closed and vice versa.

Thus with switch **30** and switch **34** closed, an answer is transferred to switch **12** and also to a first input of response comparator **38**. The address codes supplied to the second input of comparator **14** are also supplied to the second input of comparator **38**. When an address code is in coincidence with an answer associated with the same monitor, comparator **38** places switch **12** in position to interrupt recirculation and to enter the answer in the proper time slot group in the memory.

While we have discussed out invention with particular reference to the drawings, out protection is to be limited only by the terms of the claims which follow:

What we claim is:

1. An information processing system adapted to cooperate with a memory and a data processor and comprising:

a. first means coupled to said memory and having first and second mutually exclusive states, said first means permitting entry of new information into the memory when in the first state and blocking such entry when in the second state, said first means being normally in the second state;

b. second means having an input at which request data can be received and an output at which the received request data is released, said second means including means for preventing new request data from being received until completed earlier request data has been released;

c. third means interposed between the output of the memory and the input of the second means, said third means being operable to establish a path through which request data in the memory passes to said second means in response to a first predetermined condition at the input thereto;

d. fourth means interposed between the output of said second means and the input of said processor, said fourth means having a first state during which request data passes to the input of said processor and a second state during which request data cannot so pass, said fourth means being normally in said second state;

e. fifth means coupled between said fourth means and the output of the processor and operable to place said fourth means in said first state only when processed data appears at the output of the processor;

f. sixth means having an input coupled to the output of the processor at which processed data can normally be received and an output at which processed data will normally not be released, said sixth means including means for permitting release of processed data which has been received and simultaneously preventing additional processed data from being received in response to the presence of processed data in said sixth means; and

g. seventh means couple between the output of the sixth means and said first means for transferring processed data to said first means, said seventh means being operable to place said first means in said first state only when a second predetermined condition exists at the input thereto.

2. An information processing system adapted to cooperate with a memory, a plurality of monitors and a data processor, said monitors submitting request in series character format from said memory, said system passing said requests from said memory to the input of said processor and passing responses from the output of said processor to said memory, each request having data associated therewith which identifies the particular monitor at which a request originates, each response having data associated therewith which identifies the particular monitor to which a response is directed, said memory having an output at which all request appear in time sequence and an input to which all responses are supplied in time sequence, said system comprising:

a. first means having a first state at which response supplied thereto will be presented at the input of said memory for entry and having a second state at which responses will not be presented, said states being mutually exclusive, said first means being normally in said second state;

b. second means having a first state during which requests are received and accumulated character by character and having a second state during which the reception of requests is prevented and a completed request is released character by character, said second means including means operable to establish the second state of said second means when an accumulated request is complete and otherwise being operable to establish the first state;

c. third means coupled between the output of the memory and the input of the second means and operable to compare monitor identification data supplied sequentially thereto with request appearing sequentially at the memory output and to permit a request to be supplied to the second means only when the identification data associated with a monitor arrives at the third means in coincidence with a request associated with the same monitor;

d. fourth means interposed between the input and output of said processor and said second means and operable to permit a request to be supplied to the input of the processor only when a response appears at the output of the processor;

e. fifth means coupled to the output of the processor and having a first state during which responses from the processor are received and accumulated character by character and having a second state during which recep-

tion of responses is prevented and a completed response released character by character, said fifth means including means for establish the second state of said fifth means when an accumulated response is complete and otherwise being operable to establish the first state;

f. sixth means coupled between said fifth means and said first means for transferring responses thereto, said sixth means being operable to compare monitor identification data supplied sequentially thereto with the responses and to place said first means in its first state only when identification data associated with a monitor arrives at the sixth means in coincidence with a response associated with the same monitor.

3. A system as set forth in claim 2 wherein said memory is a recirculating memory and wherein all requests and responses are transferred between memory and processor in serial bit-serial character format.

4. A system as set forth in claim 3 wherein said second means includes:

a request register for accumulating requests,

a request register input switch connected in series between said third means and the request register and having a closed condition corresponding to said first state of the second means and an open condition corresponding to said second state of the second means, and

a request detector coupled to the request register and the request register input switch and operable to cause the request register input switch to be in the open condition when the request register contains a complete request and otherwise being operable to cause the request register input switch to be in the closed condition.

5. A system as set forth in claim 4 wherein said fifth means includes:

a response register for accumulating responses,

a response register input switch connected in series between the output of the processor and the response register and having a normally closed condition and an open condition and

a response register output switch connected in series between the response register and said sixth means and having a normally open condition and a closed condition, and

a response detector coupled to the response register, the response register input switch, and the response register output switch, said response detector being operable to cause the response register input switch to be in the open condition and the response register output switch to be in the closed condition when the response register contains a complete response and otherwise being operable to cause the response register input switch to be in the closed condition and the response register output switch to be in the open condition.

6. A system as set forth in claim 5 wherein said fourth means includes;

a request register output switch connected in series between said second means and the input of the processor and having an open condition and a closed condition, and

a response detector coupled to the output of the processor and the request register output switch, said response detector being operable to cause the request register output switch to be closed condition only when a response appears at the output of the processor and otherwise being operable to cause the request register output switch to be in the open condition.

7. A system as set forth in claim 6 wherein said first means includes a recirculation switch connected to said memory and to said fifth means and having a first condition corresponding to the first state of the first means during which responses supplied thereto from the fifth means are entered at the input of the memory and having a second condition corresponding to the second state during which the output of the memory is connected to the input of the memory.