

[54] **LINE PRINTER TIME SHARED ELECTRONICS**

2,919,967 1/1960 Schwertz.....101/93 C X
 3,442,206 5/1969 Sugimoto.....101/93 C

[75] Inventors: **Richard F. Elmhurst, Largo; John S. Farina; David C. Davis, Jr., both of Clearwater; William A. Elmhurst, Largo, all of Fla.**

Primary Examiner—Gareth D. Shaw
Assistant Examiner—Paul R. Woods
Attorney—Ronald T. Reiling and Fred Jacob

[73] Assignee: **Honeywell Information Systems, Inc., Waltham, Mass.**

[57] **ABSTRACT**

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A time-shared electronic control system for use with hammer-actuated continuously rotating-type drum-printers, for selectively driving print hammers to impact intermediate recording media upon the drum. Information indicative of the position of the drum is serially compared with information available for printing during a print-cycle equivalent to the travel-time of the drum from one row of characters to an adjacent row, and upon attaining correspondence of information, emitting and storing an electronic signal indicative of the column for printing during that print-cycle.

[21] Appl. No.: **146,215**

[52] U.S. Cl. **340/172.5, 101/93 C**

[51] Int. Cl. **G06f 3/12**

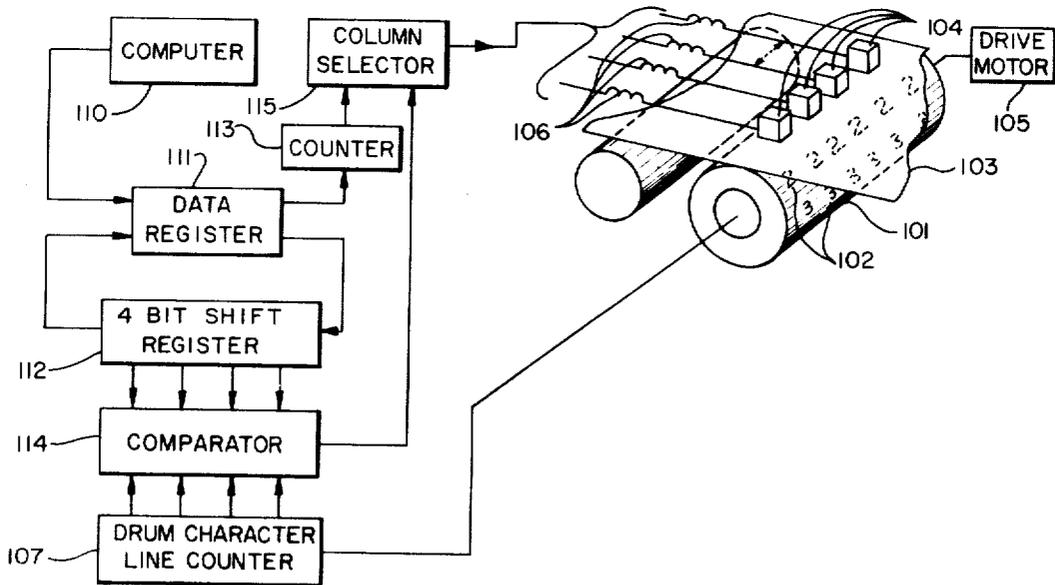
[58] Field of Search **340/172.5; 101/93 C**

[56] **References Cited**

UNITED STATES PATENTS

3,406,381 10/1968 Peyton340/172.5

19 Claims, 9 Drawing Figures



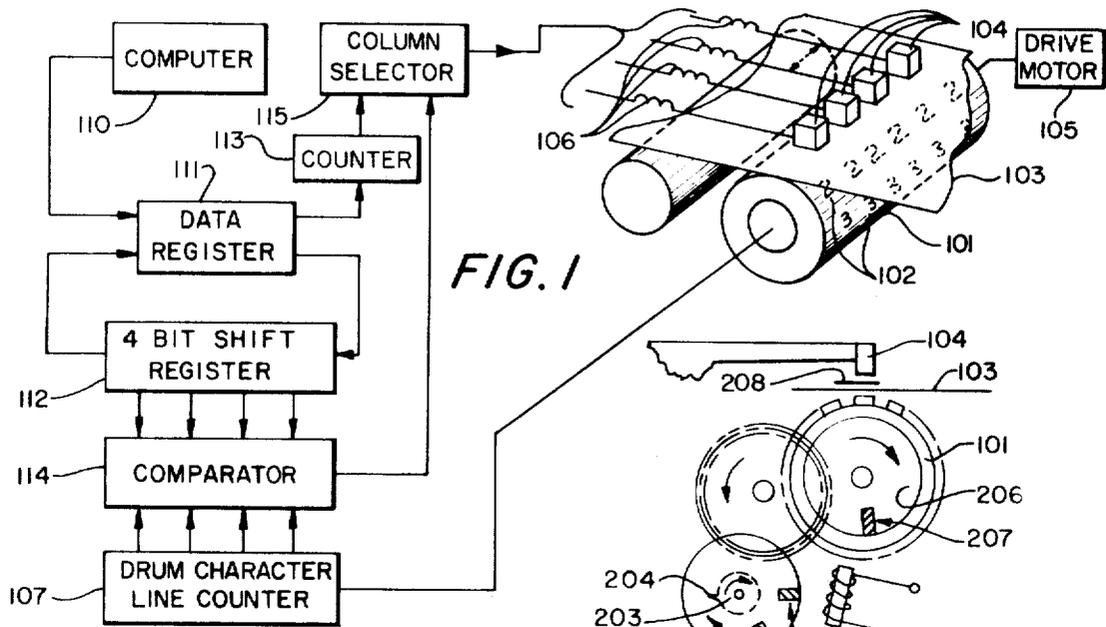


FIG. 1

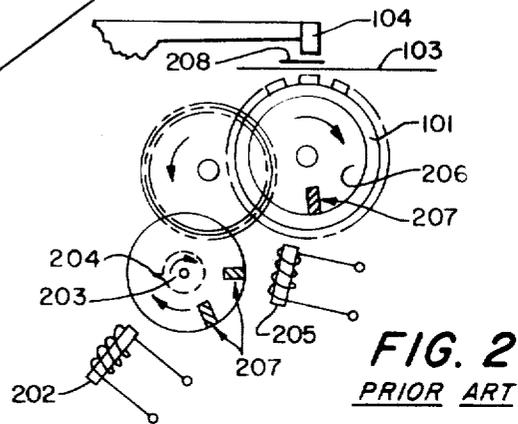


FIG. 2
PRIOR ART

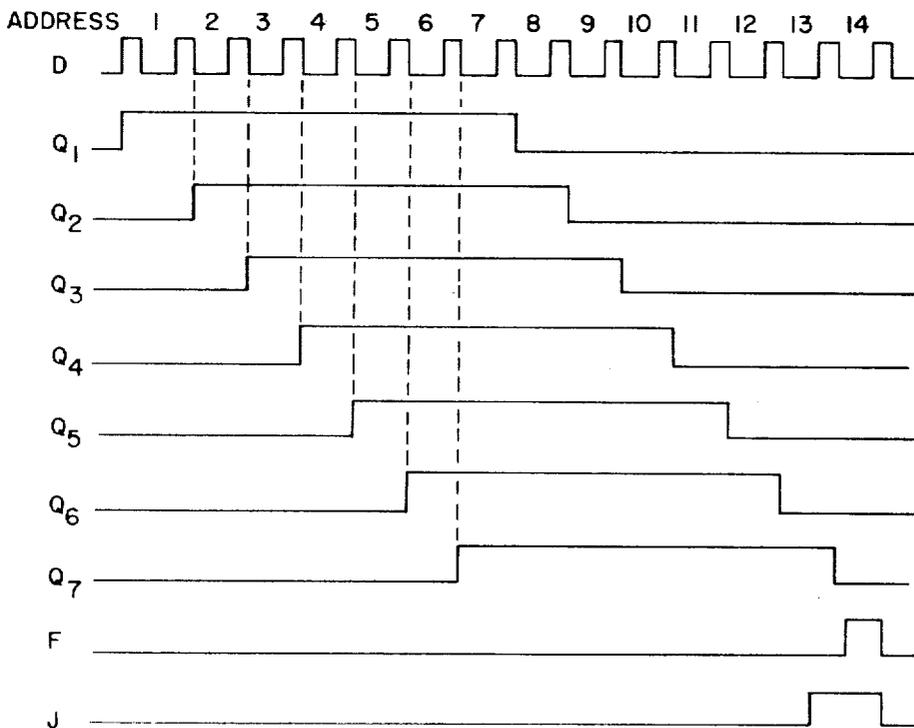


FIG. 5

INVENTORS
 RICHARD F. ELMHURST
 JOHN S. FARINA
 DAVID C. DAVIS, JR.
 WILLIAM A. ELMHURST
 BY *Walter S. Pransky*
 ATTORNEY

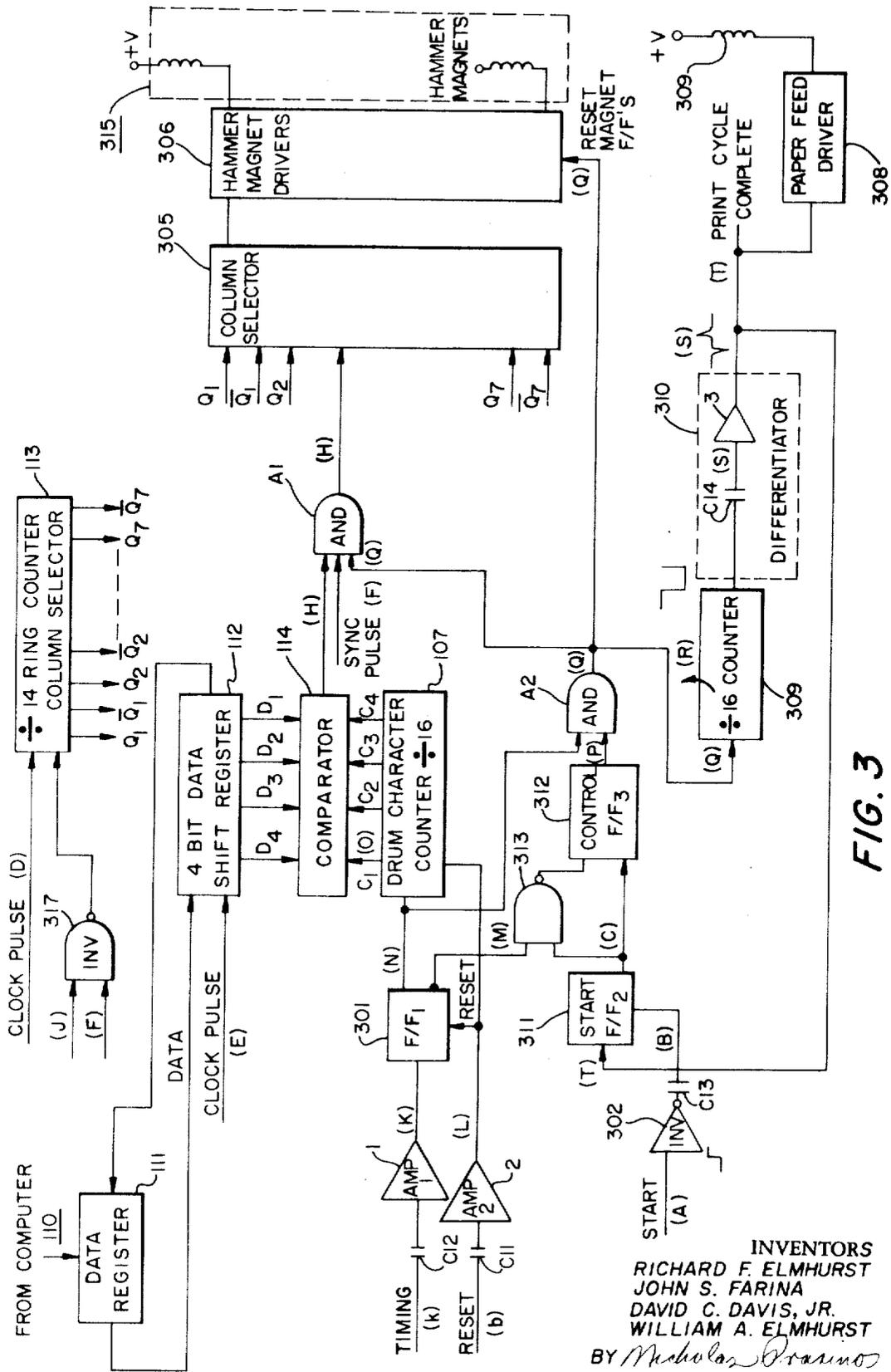


FIG. 3

INVENTORS
 RICHARD F. ELMHURST
 JOHN S. FARINA
 DAVID C. DAVIS, JR.
 WILLIAM A. ELMHURST
 BY *Nicholas Pransino*
 ATTORNEY

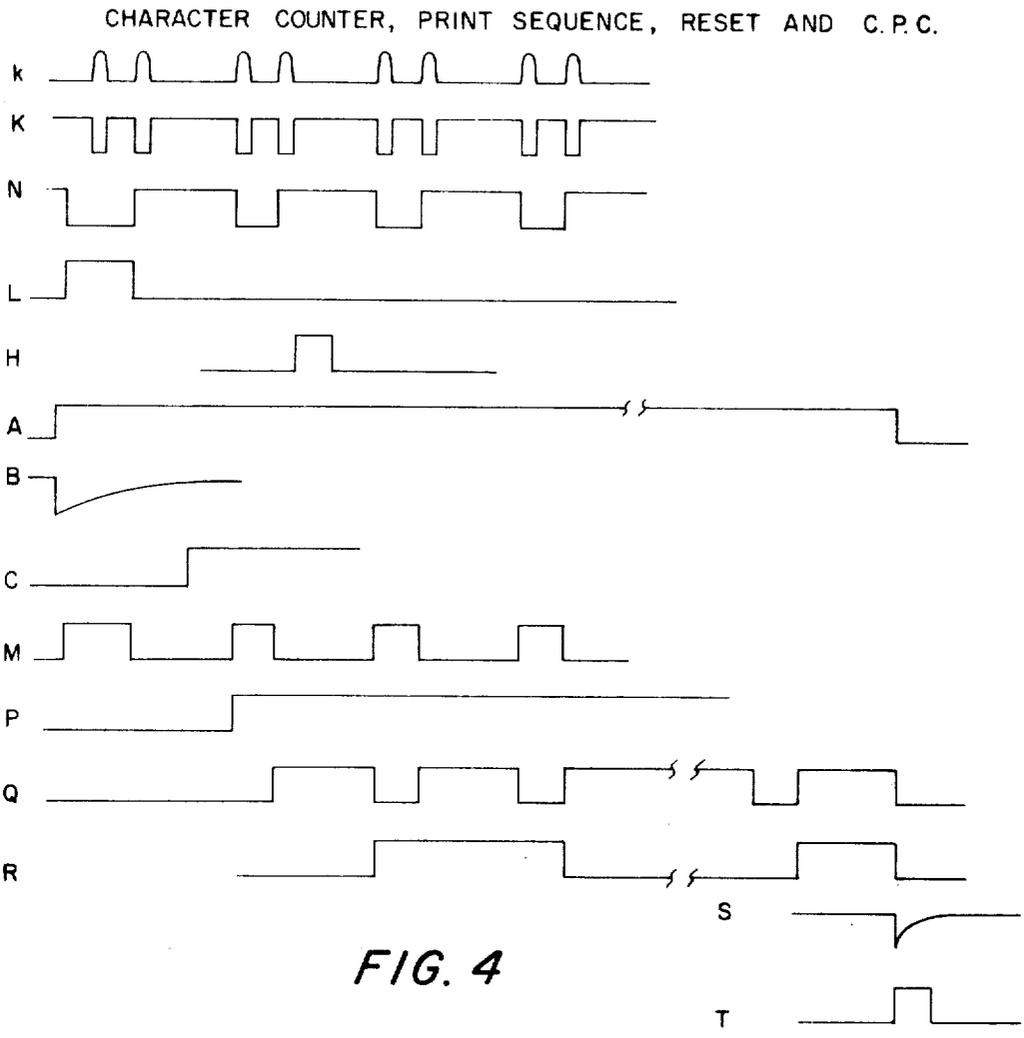
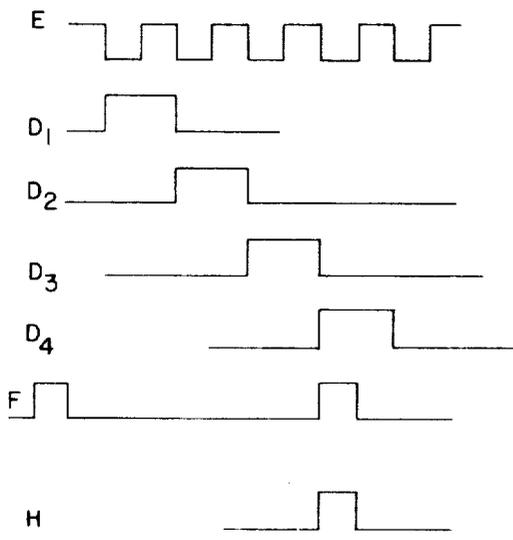


FIG. 4



DATA SHIFT, COMPARE
6 SET TRIGGER F/F'S

FIG. 6

INVENTORS
RICHARD F. ELMHURST
JOHN S. FARINA
DAVID C. DAVIS, JR.
WILLIAM A. ELMHURST

BY *Nicholas P. Prinos*
ATTORNEY

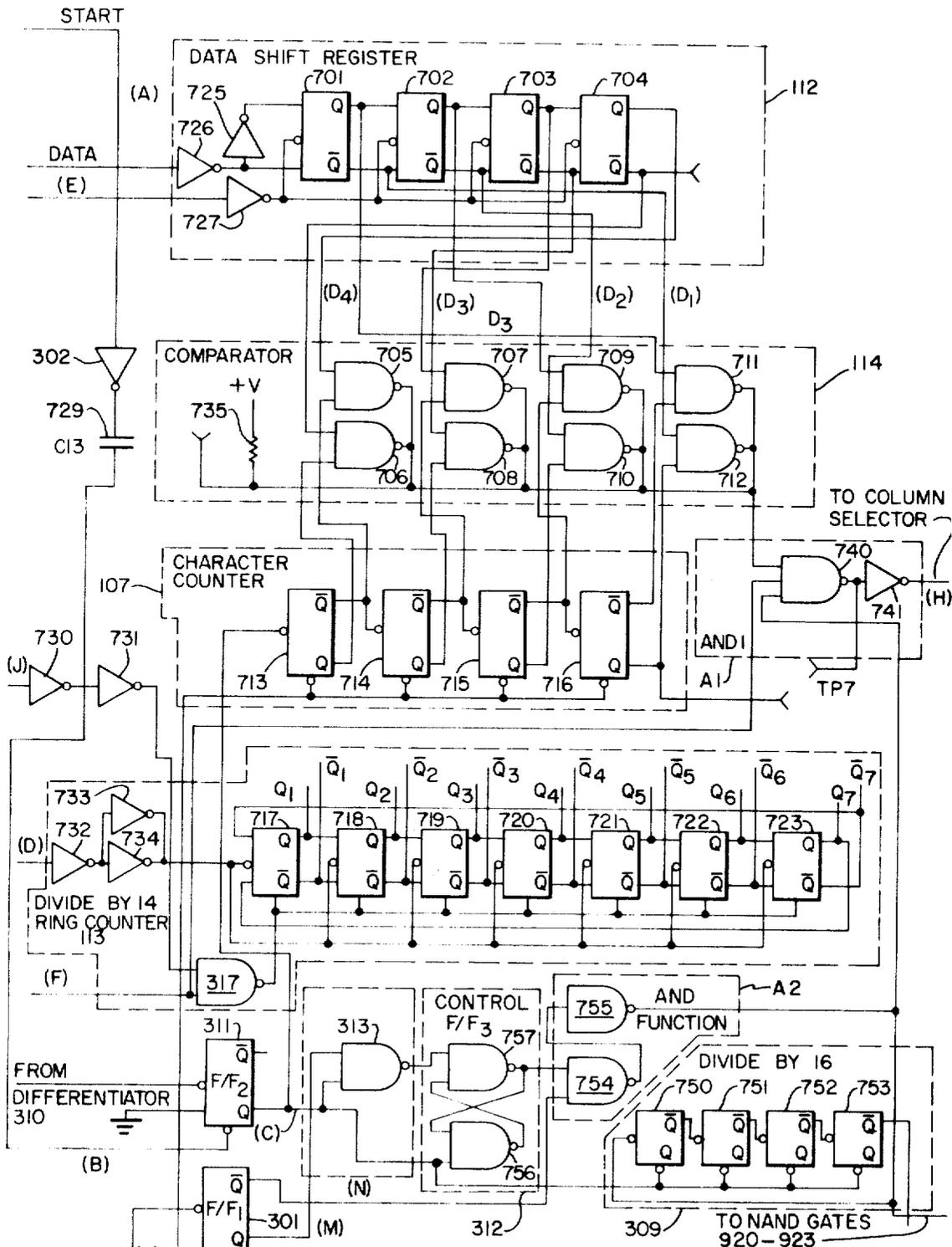


FIG. 7

INVENTORS
 RICHARD F. ELMHURST
 JOHN S. FARINA
 DAVID C. DAVIS, JR.
 WILLIAM A. ELMHURST

BY *Michael J. ...*
 ATTORNEY

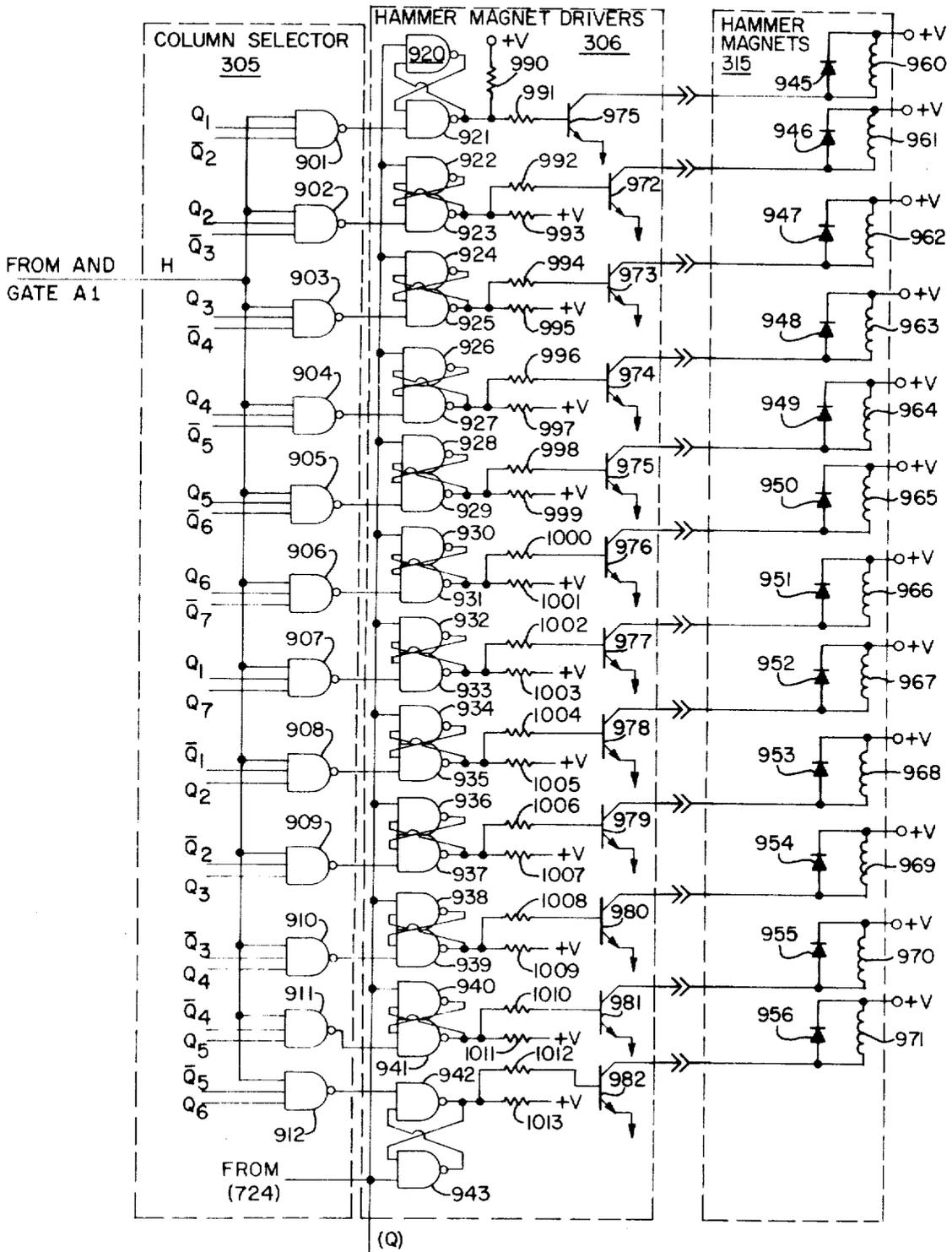


FIG. 9

INVENTORS
RICHARD F. ELMHURST
JOHN S. FARINA
DAVID C. DAVIS, JR.
WILLIAM A. ELMHURST
BY *Walter D. Davis*
ATTORNEY

LINE PRINTER TIME SHARED ELECTRONICS

BACKGROUND OF THE INVENTION

1. Field of the Invention:

This invention relates to rotary type multi-column impact printers, and more particularly to an improved electronic control system for actuating selected columns of print-hammers in response to data representing the characters of a row upon a rotating drum selected to be printed during a print-cycle interval.

2. Description of the Prior Art:

Rotary type multi-column impact printers for printing a line of characters stored in a buffer memory, in binary or other computer compatible code, is well known in the art. Printers of this type are comprised generally of a rotating drum having an assortment of type on its periphery, which is arranged in an array of columns and rows. Each row consists of that number of like characters required for printing out a complete line of type. Print hammers are generally associated with each column of type and cooperate with the type to print, on a recording medium interposed between the hammers and the type, those characters in preselected columns of any row of type presented to the hammers in spaced printing position relationship. (See U.S. Pat. to F. V. Thiemann No. 3,128,693 and L. Rosen et al No. 2,805,620 for typical prior art devices.)

Typical control circuitry for prior art rotary impact printers comprise generally temporary storage devices for storing, in a binary or other code, a line of information to be printed out. (See U.S. Pat. to G. I. Shimabukuro No. 3,088,401 and U.S. Pat. to R. J. Furlong et al No. 3,196,404 for typical prior art temporary storage devices utilized in connection with rotary impact printers.) Information in temporary storage is printed out in response to control circuitry which identifies the column and row of the print wheel, and provides signals for actuating selected hammers in an appropriate sequence. In some prior art control systems the selection process is effected by providing a plurality of storage means each one associated with one of the hammers for storing the coded information to be printed out. Decoding means for decoding the stored information identifies the appropriate hammer to be actuated. In other prior art devices subscanning devices are utilized to read out buffer (temporary storage) characters in correspondence with the mechanical alignment of the moving rows of characters with print positions. (See U.S. Pat. to V. C. Martin No. 3,192,854 and U.S. Pat. to T. G. Brown No. 3,013,119.) In still other prior art control systems "each of the character code combinations stored in a memory must be examined by comparing it against the output of a code generator which provides a code combination corresponding to the print row character next moving into printing position. For each true decoding comparison, an indication is stored in a buffer which has a storage position corresponding to each print hammer, i.e. to each space of the print line. After the entire memory has thus been examined for a given data character and the necessary information has been stored in the buffer, the latter is read out to energize the appropriate print hammers when the corresponding character row is in printing position." (Column I, lines 46-56. U.S. Pat. to A. J. Deerfield No. 3,193,802.)

Such complexity and multiplicity of mechanical and electrical components of these devices has invited attempts to simplify the structure and number of parts necessary to effect the desired object. Toward this end U.S. Pat. to Sims No. 3,332,343 and U.S. Pat. to Wasserman No. Re. 26,240 disclose devices which reduce the number of impact hammers by "making one hammer span more than one column of type." The U.S. Pat. to Belson No. 3,461,796 discloses time-sharing of driver electronics. Although a significant reduction of parts and greater simplicity is thus achieved by the device disclosed in U.S. Pat. No. 3,461,796, it still requires driver electronic circuits equal to at least half the number of hammers, i.e. one driver circuit shares two hammers.

Some other U.S. Pat. Nos. relating to rotary printers for use with computer printouts have the following numbers: 2,799,222; 3,024,723; 3,120,801; 3,140,470; 3,158,090; 3,167,002; 3,229,626; 3,247,788; 3,285,165.

What is needed is further simplification wherein the electronic control system for energizing each solenoid driving each print hammer is time shared by solenoid of each print hammer.

SUMMARY OF THE INVENTION

The invention herein disclosed comprises a time-shared electronic control system for selectively driving print hammers of a rotary type impact printer, causing the hammers to impinge upon intermediate recording media between the hammers and the rotating drum. A print drum generates timing signals which reset and also increment the state of a drum line counter. Characters are engraved on the periphery of the drum with respect to an initial point in a manner such that the character binary-coded-decimal (BCD) code agrees with the alpha numeric code of the print data. Thus the drum line counter indicates not only which row is in a printing position but it also indicates the actual character to be printed.

A line of data to be printed out is temporarily stored in a first register and is shifted continuously for a period equal to one revolution of the drum, through a second shift register capable of storing one data character. The relative columnar position of each character in its row is provided by a ring counter, which counts the number of characters in a line as the line is shifted through the second shift register. During the time interval that is required for the drum to travel from one row to an adjacent row all the characters stored in the first shift register available for printing have been compared with the information stored in the drum line counter indicative of the characters on the drum which are in a print-ready position; the identity of those columns in which a match was established is stored for print-out upon the appropriate print signal being given.

OBJECTS

It is an object, therefore, of the instant invention to provide improved line printer time-shared electronics.

It is another object of the invention to provide a simple and inexpensive time-shared electronic control system for selectively driving print hammers of rotary type impact printers.

It is still another object of the invention to provide a time-shared electronics control system for selectively driving print hammers of rotary impact printers, that is simple in construction, and economical to service and maintain.

It is still a further object of the invention to provide a time-shared electronics control system for selectively driving print hammers of rotary type impact printers that is reliable in operation.

It is yet another object of the invention to provide a time-shared electronics control system for selectively driving print hammers of rotary type impact printers requiring a minimum of components.

It is yet another further object of the invention to provide time-shared electronics control system for selectively driving print hammers of rotary type impact printers, that can take advantage of large scale integration (LSI).

Other objects and advantages of the invention will become apparent from the following description of a preferred embodiment of the invention when read in conjunction with the drawings contained herewith.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an overall block diagram of a system employing the invention.

FIG. 2 is a schematic illustration of a prior art device utilized for generating timing pulses in synchronism with the print drum.

FIG. 3 is a detailed block-schematic diagram of a system employing the invention.

FIG. 4 is a timing diagram showing the timing of certain signals in the drum character counter, print sequence, and reset area.

FIG. 5 is a timing diagram showing the sequencing of the divide by 14 ring counter utilized in the invention.

FIG. 6 is a timing diagram showing the timing of certain signals in the data shift and compare areas.

FIG. 7 is a schematic illustration of a logic block diagram showing details of certain components of a preferred embodiment of the invention.

FIG. 8 is a schematic illustration of a logic block diagram showing details of further components of a preferred embodiment of the invention.

FIG. 9 is a schematic illustration of a logic block diagram showing details of still further components of a preferred embodiment of the invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

General

FIG. 1 is a block diagram of an exemplary system utilizing the instant invention. The system shown is a rotary type multi-column impact printer which may be typical of the type disclosed by Wasserman in U.S. Pat. No. 3,024,723.

Referring to FIG. 1, a conventional rotary printer having a drum constantly rotating about its axis and having upon its periphery a font of characters 102 arranged in an array of columns and rows, has an intermediate medium 103 which may be impact sensitive paper, interposed between print hammers 104. Each print hammer corresponds to a character column of a line in print-ready position. There may be as many columns of type as is required by the system to print out a complete line consisting of a predetermined number

of characters; and concomittantly there are as many hammers as there are columns of type, each hammer cooperating with its associated character to effect a print out of recording medium 103. The medium 103 moves intermittently between the rotating drum 101 driven by motor 105, and especially aligned hammers 104. Hence the recording medium 103 remains stationary for a cycle sufficient to complete the printing of one line of characters, and then moves to its new position of one line of characters ready for printing another complete line of characters on the recording medium 103. Print hammers 104 may be pivoted from a suitable support (not shown) and each print hammer can strike against the record medium when its appropriate coil 106 is energized. This apparatus is well known in the art and is typically exemplified by U.S. Pat. to L. Rosen et al No. 2,805,620.

Cooperating with drum 101 is a prior art device schematically illustrated in FIG. 2. Two timing signals are generated by the device of FIG. 2: one, a pair of timing signals from a detecting head 202, correspond to one rotation of a ratchet shaft 203 mounted on detecting wheel 204; hence this signal corresponds to the time interval for one row of characters to pass under the hammer 104. The other signal, the reset signal from detecting head 205 corresponds to one complete rotation of the print drum 101. The signals are generated electromagnetically by magnetic flux from a magnetic material such as ferrite chips 207 buried in detecting wheels 204 and 206 respectively. For a fuller description of the generation of typical timing signals see copending U.S. Pat. application Ser. No. 34,934 filed on 5/6/70 and assigned to the same assignee as the instant invention.

Referring again to FIG. 1, a computer 110 transfers a line or row of data which is to be printed-out on a record medium 103, to a data shift register 111. Timing signals from a typical device shown on FIG. 2 are supplied through a drum character line counter 107. Each timing signal supplied by detecting head 202 changes the stage of the drum character line counter 107 in relation to the reset signal supplied by detecting head 205. The reset signal is indicative of the position on the drum when the row of zero characters is in correspondence with the print hammers 104. Hence, the state of the drum character line-counter 107 at any one given time period of a complete revolution of the drum 101 is indicative of the row of characters which are in corresponding alignment with the print hammers 104.

During the time interval required for the drum 101 to rotate from one row of characters positioned in corresponding relationship to the print hammers, so as to bring an adjacent row of characters on the drum in corresponding alignment with the print hammers all the data stored in data register 111 is shifted serially bit by bit and character by character through four bit shift register 112. This shifting process continues until all the row of characters on the drum 101 has passed beneath the hammers 104 and the drum has made a complete revolution; whereupon a new line of data to be printed out is presented to register 111 by computer 110. During the same time interval wherein the drum rotates from one row of characters to another and wherein one complete line of characters in data register 111 are circulated through four bit shift register 112, a counter

113, counts each character after it is shifted in four-bit shift register 112; this count, therefore, is indicative of the relative columnar position of each character in the line which is to be printed on recording medium 103. Also the character count in counter 113 is indicative of the column of a print hammer which corresponds to a similarly numbered column of that particular character contained in the four bit register 112, at that particular instant. For example, each character presented to data register 111 for print-out on record medium 103 has a one to one correspondence with each print hammer 104. To select the appropriate print hammers for print out during the printing cycle, a comparison is made in comparator 114 between the contents of drum character line counter 107 and the contents of four bit shift register 112. When a match is detected the information contained in counter 113 gates the output of comparator 114 to the appropriate storage location in column selector 115. Hence the information stored in column selector 115 is indicative of the number of the column of that character below said print hammer, to be printed out during print time.

Thus the line printer time-shared electronics drive system performs the following basic functions:

1. Receives the data to be printed.
2. Receives timing signals from the print drum which indicates the position of the print drum.
3. Compares the data to be printed with the position of the print drum.
4. If a comparison match occurs, sets the trigger magnet RS flip-flop (to be hereinafter described in greater details). The appropriate column is selected by a ring counter to correspond with the address location of the input data.
5. Controls the feed paper and take up paper for both pre-upspace and post-upspace paper.
6. Generates an end of print signal.

Receive Data — Referring now to FIG. 3, input data is received synchronously with a master clock (not shown) by data register 111. The data is shifted continuously through a four bit shift register 112 by clock pulses (E). (See also FIG. 6 for timing diagram.) A total of four shifts occur within an address time, prior to compare time. In this manner a four-bit character is completely shifted into the four bit shift register at compare time. During compare time the contents of the four bit shift register 112 is compared with the contents of the drum character counter 107 in a comparator 114. If the contents of the shift register 112 matches the contents of the drum character counter 107, the comparator 114 generates an output signal (H).

Receive Timing Signals From The Print Drum To Determine The Position Of The Drum — As hereinbefore described the print drum generates two timing signals (k) for each row of characters on the print drum. A total of 16 rows of characters are engraved on the print drum although more or less may be engraved. Normally, the characters in the preferred embodiment of the invention are 0-9 plus other desired characters for a total of 16 different characters. The print drum also generates a reset signal for each revolution of the print wheel. The reset signal occurs when the first row of characters, which consists of all zeros, is beneath the print hammer. The reset signal (L) (see also FIG. 4) resets the character-counter 107 to a zero state which

character-counter is then incremented once for every two timing signals (k). A flip-flop 301 receives the timing signals (k) which have been shaped and amplified by capacitor C12 and amplifier 1, and produces one output pulse (N) for every two input pulses (K). Hence the flip-flop 301 is used to divide a total of 32 signals generated for every revolution of the print drum by 2, to produce 16 pulses (N) per drum revolution, and apply the signals (N) to the input of the drum character binary counter 107. In this manner, the shift register 107 which is the drum character-counter, contains a binary number corresponding to the position of the print wheel relative to the print hammers i.e. which row of type characters is beneath the print hammers. Characters are engraved on the wheel in a manner such that the character-counter code agrees with a code of the print data received from the computer; this minimizes control electronics and eliminates the necessity for a code generator to convert the data to a drum position code.

Table I below shows the code arrangement.

TABLE I
CHARACTER CODE TABLE

Character Counter Code				Print Character and Row Number
C ₄	C ₃	C ₂	C ₁	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
				Any symbols may be assigned to these rows.
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

NOTE: (Code for symbols would correspond to position of symbols on the print drum.)

It will be understood that a minimum of logic is required if the location of the character on the print drum is related to the BCD code of the input data. For example, the code for the input number 6 is 0110 and the character 6 is engraved on the sixth row on the print drum.

Referring again to FIG. 3 and 4 a reset signal (1) is generated for each complete revolution on the print drum and is shaped and amplified by capacitors C11 and amplifier 2 respectively to produce a signal (L) which is used to reset the flip-flop 301 and the drum character counter 107.

Compare Data To Be Printed With The Contents Of The Character Counter — The compare function is performed by the comparator 114 which consists of 8 NAND gates arranged in an exclusive OR configuration to be later more fully described. The comparator compares the character stored in the drum character-counter 107 with the character momentarily stored in the four-bit shift register 112, and when a match occurs, a signal output (h) is applied to AND gate A1. A pulse signal (F) is also applied to AND gate A1 which occurs when a full character has been shifted to four bit

shift register 112 (see FIG. 6) and is a necessary coincident pulse together with pulse (h) and (Q) to enable AND GATE A1.

Set, Output Flip-Flops For Printing — The data signal (H) is applied to all input gates 901-912 of FIG. 9 in the column selector 305. Also connected to the input of NAND gates 901-912 are signals from a seven stage ring counter 113 which generates signals corresponding to the address of the input data. The ring counter is synchronized to the address locations by signal (J) and sync pulse (F). As seen on FIG. 5 when these two signals are coincident the ring counter 113 is reset to a 0 state. The operational sequence of the ring counter 113 is pictorially described by the timing diagram of FIG. 5. The ring counter 113 is delayed one bit from the input data. By delaying the ring counter by one bit the comparator output is sampled at the midpoint of the data address rather than during the last bit of the address. Because of this feature, the operation is not affected by minor signal delays. Signals $Q_1, \bar{Q}_1, Q_2, \bar{Q}_2, \dots, Q_7, \bar{Q}_7$ from the ring counter 113 are also applied to NAND gates 901-912 of column selector to enable the gates that correspond to input data. For example, if a 5 located at address 2 of data register 111 is to be printed, then the comparator 114 will produce an output when a character counter 107 contains a BCD 5 during compare of address 2. During that time interval the appropriate gate corresponding to a column assigned to address 2 will be turned on.

This sequence is best described by examining in detail the condition of the various signals and logic blocks during the period of compare. This will be done by using the example of printing a 5 in column 2 which corresponds to the data in address 2. The character counter 107 and data register 111 will contain a stage of 5 in a BCD code 0101. The column selector will be in such a state that flip-flop 718 signal Q_2 will be a logic 1 and the \bar{Q}_3 signal of flip-flop 719 will be a logic 1. The time relationship of this state is shown on FIG. 5. FIG. 6 shows the timing which occurs within an address time. Compare time occurs at the time when signal (H) which is derived from AND gate A1 is in a logic 1 state. Signal (H) is applied to all gates 901-912. Gate 902 is the only gate enabled due to the state of the column selector 113 which applies Q_2 and \bar{Q}_3 signals both of which are logic one (1) to gate 902. The coincidence of signals Q_2, \bar{Q}_3 and H causes only the output of NAND gate 902 to assume a logic 0 state. The output of 902 is applied to NAND gate 923 which is arranged with NAND gate 922 in an RS flip-flop configuration required to "hold" and "store" the short compare command for a period of time sufficient for the print hammer to engage and print. The logic 0 signal applied to gate 923 causes the output of gate 923 to assume a logic one state which causes the voltage and the junction of resistors 992 and 993 to change from 0 volts to approximately 4 volts. This causes current to flow through resistor 992 to the base of NPN transistor 972. Transistor 972 is connected to trigger magnet 961 in a common-emitter switch configuration. Current into the base of transistor 927 causes the collector junction to conduct current which flows through magnetic 961 which activates the magnet 961. The hammer magnet 961 activated will engage the print hammer 104 in column 2 which strikes against recording medium 103, causing a 5 to be printed.

Feed and Take-Up Paper — The paper feed and take-up solenoid 319 are driven by a paper feed driver which is activated by a print complete signal (T).

Generate An End Of Print Signal — A print cycle signal (T) is generated by the counter 309 which merely informs the logic that 16 characters have passed beneath the print hammers after the start of the print cycle which indicates that 1 full revolution of the print drum has occurred and is the signal which commands paper to be up-spaced and informs the computer that a line of printing has been completed. A differentiator 310 comprised of capacitor C14 and an amplifier 3, differentiates the signal and applies it through the paper feed driver and start flip-flop 311 to stop the printing process. The print cycle is initiated by an external signal (A) which is driven by an external computer device. (A print cycle is defined as the entire print sequence that occurs between start signal (A) and a print cycle complete signal (T).) Inverter 302 and capacitor C13 invert and differentiate the start signal (A). (See above cited copending U.S. Pat. application, Ser. No. 34,934 for details for one typical technique.) The resulting signal (B) is applied to start flip-flop 311 which is deactivated causes signal (C) to change from a logic 0 to a logic 1 which in turn activates control flip-flop 312. The control flip-flop 312 prevents the starting of start sequence in a middle of a timing pulse. The control flip-flop 312 thereto synchronizes the start signal which may occur at any random time with respect to the timing signals from drum 101. This is accomplished by gating signal C, which is derived from an external source and is asynchronous to the print timing, and signal (M) which is synchronously derived from the printer. These signals are gated by NAND gate 313, the output of which activates the control flip-flop 312 when the output of NAND gate 313 changes to a logic zero state (low). The gating of these two signals assures that control flip-flop 312 will be activated during the period when the signal (M) is a logic one and not when signal (M) is a logic 0 which is the period during which printing occurs. This timing sequence of this synchronizing means is shown in FIG. 4. Control flip-flop 312 being activated goes high, to generate a voltage signal P. It will be observed that both the voltage signal P from control flip-flop 312 and a voltage signal M from timing flip-flop 301 are applied to AND gate A2 in order to generate a trigger signal Q; thus the print cycle cannot proceed until both the signals are coincident. The trigger signal Q is applied to AND gate A1, the reset magnet flip-flops 920-943 of hammer magnet drivers 306, and to the divide by 16 counter 309. The trigger signal therefore synchronizes the magnet driver 306 with the position of the characters beneath the print hammer. The trigger signal Q is also utilized to drive counter 309 which indicates when a complete revolution of the drum 101 was occurred, by the counting of each row of characters on the drum until a total of 16 counts, for this embodiment, have occurred. The trigger signal Q from four-stage binary counter 309 is applied to differentiator 310 comprised of a capacitor C14 and an amplifier 3, to generate a print cycle complete signal T. The print cycle complete signal T in turn drives a paper feed driver 308 which causes the paper to be advanced 1 full row. Furthermore, the print cycle complete signal T also feeds back to flip-flop 311 resetting the flip-flop thus signifying the entire print cycle is complete to this point.

Description Of The Timing Diagrams — Referring to FIG. 4 the timing signal (k) is derived from the print drum 101 and is a low amplitude signal which is applied to amplifier 1 which in turn amplifies it, generating an amplified signal (K) which is used to drive the logic.

In addition to the (K) signal we have a (1) signal, shown in FIG. 3 but not shown on FIG. 4, which is the reset signal from the print drum. There is one (1) signal for each complete revolution of the drum. The (1) signal is applied to capacitor C11 and to amplifier 2 to shape and amplify the signal and differentiate it to obtain signal (L) which is utilized to reset flip-flop 301 and drum counter 107. The amplified reset signal L resets the drum character counter 107, which requires an initial setting of 0000 to correspond with the zero row of characters on the print drum 101. The signal M and N are generated by flip-flop 301 in response to timing signals, as hereinbefore described; the print drum 101, with its associated logic, generates 32 pulse signals, in this embodiment, for each revolution of the drum; however since there are only 16 rows of characters for this particular embodiment, it is required that half the number of these timing signals be applied to the logic. Hence flip-flop 301 divides every two (K) signals into one M and N output signal respectively. It will be noted that the (N) signal is the complement of the M signal. The M and N signals are the primary timing signals. The (N) signal increments the drum character counter 107 which keeps track of the location of the print drum and generates the trigger signal (Q) while the (M) signal is used to synchronize the activation of the control flip-flop 312. Signal (0) is a signal in the drum character counter shown on FIG. 3 as the first stage of the drum character counter 107. Signal (0) changes stage for every input of the timing signal (N). Other signals in the drum character counter 107, which are not shown, are simply binary count-down signals from the signal (0).

Signals (A,B,C,P,Q,R,S and T) on FIG. 4 pertain to the print cycle, and shown the sequence of signals that occur from the start print cycle to the completion of print. Signal (A) is an externally generated signal that indicates that the print cycle is ready to begin by going from a logic 0 to a logic 1. Signal (B) is the differential signal of signal (A) which is applied to flip-flop 311 to indicate that the system is ready to start printing. Flip-flop 311 in turn generates signal (C) which is the actual start of the print cycle signal. When signal (C) is high coincident with signal (M) control flip-flop 312 is activated by NAND gate 313 to generate the print signal (P). When the signal (P) is generated the actual print cycle begins and continues until a total of 16 prints has occurred during one full revolution of the print drum beneath the print hammers. The signal (P) applied coincidentally with signal (N) to AND GATE A2 generates signal (Q) which is applied to AND gate A1, to magnet flip-flops of magnetic hammer driver 306, and divide by 16 counter 309. Internal of the divide by 16 counter 309 is a signal (R) which represents the counting sequence which occurs as internal to the divide by 16 counter. After a total of 16 counts have occurred by the divide by 16 counter 309, then signal (S) is generated which is then differentiated, shaped and amplified to generate print cycle complete signal (T) which indicates that a complete revolution of the drum has occurred. Signal (T) is generated from signal (S) by

the action of capacitor C14 and shaping amplifier 3 which are arranged as a differentiator. Signal T drives the paper feed driver 308 in order to increment or up-space the record medium 103 by one line in order to print the next row.

Referring now to FIG. 5, there is shown timing signals which advance the count of the ring counter 113 which counts the address location. In this particular embodiment there are a total of 14 address locations, and therefore a divide by 14 ring counter is used although the invention need not be so limited. The ring counter 113 is advanced in its state by clock pulses (D). The outputs of the ring counter 113 are signals (Q₁) through (Q₇). The signals (Q₁) through (Q₇) and their corresponding complements (\bar{Q}_1) through (\bar{Q}_7) are the signals that are presented to the column selector 305. The ring counter 113 is synchronized to the address location by signal (J) and sync pulse (F). Signals (J) and (F) are derived externally from a computer 110 and is synchronized with the timing of the input data.

Referring now to FIG. 6, the data shift, compare and set-trigger flip-flop sequence signals will be discussed. External clock pulses (E), shift in data sequentially to the four bit data shift register 112. Signals D1 through D4 illustrate the state of each flip-flop of the shift register as data is serially shifted therein. When a complete word has been shifted into the four bit shift register, a signal (F) occurs signifying that point in time when the word is ready to be compared with the word in the drum character counter 107. Upon comparison of the word in four bit shift register 112, and the word in drum character counter 107 within the comparator 114, and upon the occurrence of a match between these two words a signal (h) is generated and is applied to AND gate A1.

Discussion Of Detailed Drawings — Referring to FIG. 7 details are shown in four-bit data shift register 112, comparator 114, drum character counter 107, divide by 14 ring counter 113, and divide by 16 counter 309, and their arrangement and interconnections with other cooperating logic circuitry.

Four bit data shift register 112 comprises four J-K flip-flops 701-704 connected in series, although other store devices such as magnetic cores may be utilized in an appropriate connection to form a shift register (Typical RS and JK flip-flops, with their truth tables are to be found on page 37 of a book entitled "Introduction to Digital Computer Design" by Herbert S. Sobel published in 1970 by Addison - Wesley Publishing Company). The character counter 107 is also comprised of 4 JK flip-flops. Each flip-flop represents a stage of the character with flip-flop 713 representing the first stage and so on to the 4th stage. Also the position of flip-flop is accorded a weight in accordance with a BCD code. Thus flip-flop 713 has a weight of $2^0 = 1$, flip-flop 714 a weight of $2^1 = 2$, flip-flop 715 a weight of $2^2 = 4$, and flip-flop 716 a weight of $2^3 = 8$. The comparator 114 is comprised generally of NAND gates 705 through 712. The inputs of the NAND gates 705-712 are operatively connected to the Q and \bar{Q} terminals of flip-flops 701-704 and also flip-flops 713-716 so that when high signals occur on the flip-flops of register 112 and high signals also occur on corresponding flip-flops of register 107, the corresponding NAND gates to

which these flip-flops are coupled, are enabled. For example, it will be noted that the Q and \bar{Q} terminals of flip-flop 716 are coupled to the inputs of NAND gates 712 and 711 respectively. Also the other set of input terminals for gates 711 and 712 are coupled to the Q and \bar{Q} terminals of flip-flop 701 respectively. Hence when the Q terminals of flip-flop 701 and 716 are high and the \bar{Q} terminals of flip-flops 701 and 716 are low then NAND gate 711 and 712 will be high. When this condition results for all flip-flops a match occurs. Upon the occurrence of a match a signal is applied to the input of AND gate A1.

Data to the four bit shift register 116 is applied through inverters 725 and 726. The clock pulse (E) is applied to the four bit shift register 112 or the toggle of each flip-flop 701-704 through inverter 727.

Divide by 14 ring counter 113 is also comprised of JK flip-flops 717 through 723 coupled in series. The \bar{Q} terminal of flip-flop 723 is then coupled into the Q terminal of flip-flop 717, whereas the Q terminal of 723 is coupled to the \bar{Q} terminal of flip-flop 717; thus completing the ring counter. The (D) signal is applied to the toggle of each JK flip-flop 717-723 through inverter 732, and inverters 733 and 734 coupled in parallel. The (J) signal is applied to NAND gate 317 via inverters 730 and 731; whereas the (F) signal is applied to NAND gate 317 and to AND gate A1 which is comprised of NAND gate 740, whose output is coupled to the input of an inverter 741. The $Q_1, Q_1, \dots, Q_7, Q_7$ signals from the Q \bar{Q} terminals of each flip-flop of ring counter 113 are applied to the inputs of NAND gates 901-912 in pre-selected patterns. For example Q_1, \bar{Q}_2 is applied to the inputs of NAND gate 901; Q_2, \bar{Q}_3 is applied to the inputs of NAND gate 902 and so on.

Divide by 16 counter 309 is comprised of four JK flip-flops 750 through 753. The \bar{Q} terminal of one flip-flop is coupled to the toggle terminal of a succeeding flip-flop. Hence \bar{Q} terminal of flip-flop 750 is coupled to the toggle terminal of flip-flop 751, and so on. Also the output terminal of AND gate A2 is coupled to toggle terminal of flip-flop 750. AND gate A2 is comprised of 2 NAND gates 754 and 755, wherein the output of NAND gate 754 is coupled to the input of NAND gate 755. NAND gate 754 has also inputs from the Q terminal of flip-flop 301 and the output terminal of control flip-flop 312. Control flip-flop 312 is comprised of 2 NAND gates 756 and 757 coupled so as to form an RS flip-flop i.e., the output terminal of NAND gate 757 is coupled to an input terminal of NAND gate 756 and the output terminal of NAND gate 756 is coupled to an input terminal of NAND gate 757. Furthermore another input terminal of NAND gate 757 is coupled to the output of NAND gate 313; still another input terminal of NAND gate 756 is coupled to an input terminal of NAND gate 313 and also to the Q terminal of flip-flop 311. Flip-flop 301 has its toggle input coupled to the output of amplifier 1 and its Q terminal coupled to an input of NAND gate 313 whereas its \bar{Q} terminal is coupled to an input of NAND gate 754. Therefore as hereinbefore described outside signal (A) initiates the print cycle. The signal (A) is differentiated through inverter 302 and capacitor C13 and applied to flip-flop 311; thus Q terminal of flip-flop 311 assumes its high state and is not applied to an input of NAND gate 313. When a coincident signal (M) is also applied to NAND

gate 313, NAND gate 313 generates a low signal at its output which is then applied to the input of NAND gate 757 of control flip-flop 312. The high signal from Q terminal of flip-flop 311 is also applied to the input of NAND gate 756 of control flip-flop 312. If control flip-flop 312 is in such a state so that NAND gate 756 generates a high output signal which is then applied to the input of NAND gate 757, the output state of NAND gate 757 is high. This high output of NAND gate 757 is applied to an input terminal of NAND gate 754, and when there is a coincident high signal (N) also applied to NAND gate 754, it generates a low output signal which in turn is applied to NAND gate 755 which in turn generates a high output signal which is then applied to the input of NAND gate 920 - 943 of column selector 305, and also to the toggle of flip-flop 750, of divide by 16 counter 309.

The ring counter 113 is arranged to produce the set of pulses as described in FIG. 5. The counter has a total of 14 different states and is self recycling. Pulses are shifted by the clock pulse D which is derived from the computer and is synchronized with the input data which is shifted into register 112. The shifting sequence is best described by understanding the means to change from one state to the following state. Beginning with the address 1 state in which the Q output of flip-flop 717 is a logic one; all other Q outputs for flip-flops 718-723 are logic 0. Flip-flop 718 changes state during the next negative excursion of signal D due to the fact that Q_1 of 717 is applied to the set input of 718 which conditions 718. Successive stages 719-723 operate similarly. Q_1 of 717 is reset to zero during the next negative excursion of D signal following the condition in which Q_7 of 723 is positive. This is accomplished by connecting Q_7 of 723 to the reset input of 717. The Q_2 signal goes negative in the same manner. Selection of the particular address is accomplished simply through a two line decoding means by NAND gates 901 to 912. For example, address 2 is decoded by applying Q_2 from 718 and \bar{Q}_3 from 719 to NAND gate 902. Hence, NAND gate 902 is enabled during address 2 time. If signal H is positive (logic 1) during address 2 time, then NAND gate 902 output becomes negative (logic 0). Printing in turn is effected by setting RS flip-flop consisting of gates 922 and 923 which drives transistor 972 and hammer solenoid 961.

Referring now to FIG. 8, amplifier 1 comprises a transistor 803 having its collector coupled with plus voltage +V through resistor 816 and having its emitter coupled to ground. The base of transistor 803 is coupled to plus voltage +V through voltage dropping resistors 814 and 815 and also coupled to ground through diode 840. A capacitor 841 by-passes unwanted RF energy commonly referred to as electrical noise to ground. The small signal (k) to be amplified is applied to the base of transistor 803 at junction 842. The amplified signal (K) is abstracted at the collector terminal of transistor 803 at junction 843. Amplifier 2 is similar to amplifier 1 and operates in a similar manner with the exception that an additional reset stage has been added, which stage inverts the reset signal 1. Once again transistor 802 has its collector coupled to a plus voltage +V through resistor 813 and its emitter coupled to ground. Similarly the transistor 801 has its collector coupled to a plus voltage +V to transistor 812 and its

emitter coupled to ground. Also the collector of resistor 801 is coupled to base of transistor 802. The base of transistor 801 is coupled through resistors 810 and 811 to a plus voltage +V and is also coupled to ground to a diode 829. A capacitor coupled to the base and ground filters out any unwanted RF signals. A reset signal (1) to be amplified is applied to the base of transistor 801 at junction 860. This signal is amplified through transistor 801 and is abstracted by the collector circuit at junction 861 and is applied to the base of transistor 802 which is then amplified once again and abstracted at junction 862 of the collector circuit of transistor 802, which signal is then further amplified and inverted in inverters 827 and 828. Inverters 827 and 828 not only invert the signal but also apply additional gain to the circuitry in order to drive the several flip-flops.

The differentiator 310 is comprised of an inverter amplifier 825 whose input is coupled to a capacitor 826 and a resistor 824; the output of inverter 825 is coupled to flip-flop 311 (see FIG. 7) and also to the input of the paper feed driver 308.

Paper feed driver 308 comprises a transistor 807 whose base is coupled to the output of the differentiator 310 through resistor 823, and whose emitter is coupled to ground. The collector of transistor 807 is coupled to another transistor, resistor, capacitor circuit comprised as follows: A transistor 805 has its emitter coupled to ground through resistor 821, its collector coupled to a plus voltage +V through resistor 819, and its base coupled to the collector of transistor 804. Transistor 804 also has its collector coupled to a plus voltage +V and to resistor 817, and its emitter coupled to ground. The base of transistor 804 is coupled to a plus voltage +V through resistors 822 and 818. The base of transistor 804 is also coupled to the collector of transistor 805 through resistor 822, capacitor 870 and diode 880. The emitter of transistor 805 is further coupled to the base of transistor 806 whose emitter is coupled to ground and whose collector is coupled to the input circuit of paper feed solenoid 309.

The paper feed driver 308 receives an input print cycle complete signal (T), through the base of transistor 807 thus activating the circuitry consisting of transistors 804, 805 and 806. The circuit once activated by transistor 807 drives a high current signal at the collector of transistor 806 which in turn activates the paper feed solenoid to up-space the paper. The time period of this pulse is controlled by capacitor 870 and resistor 818. When a capacitor 870 is fully charged transistor 804 turns on thus current flows in the collector of transistor 804. Since the collector 804 is coupled to the base of transistor 805, transistor 805 is turned off; hence transistor 806 is also turned off which will then remove the high current from the paper feed solenoid 308.

Referring now to FIG. 9 column selector 305 is comprised of a series of NAND gates 901 through 912 each gate having 3 input terminals. On one of the input terminals of each one of the gates the signal (H) is applied. The other 2 input terminals of each gate are coupled in pre-selected manner to the Q_n \bar{Q}_n terminals of the flip-flop of divide by 14 ring counter 113. For example, NAND gate 902 has one of its input terminals coupled to the Q_n terminal of flip-flop 718 and another

of its input terminals to the \bar{Q}_n terminal of flip-flop 719. Similarly the other NAND gates of the column selector 305 are coupled to flip-flops of divide by 14 ring counter 113. The output terminal of each NAND gate 901 through 912 are coupled respectively to hammer magnet drivers 306 — one hammer magnet driver for each NAND gate 901 through 912. Hammer magnet drivers 306 are comprised of a series of NAND gates 920 through 943, each pair of NAND gates coupled to perform the functions of an RS flip-flop. For example NAND gates 920 and 921 are coupled such that the output of NAND gate 920 is coupled to an input of NAND gate 921 and the output of NAND gate 921 is coupled to an input of NAND gate 920. Furthermore one input of NAND gate 920 is coupled to the output of AND gate A2. The other input of NAND gate 921 is coupled to the output of NAND gate 901.

Similarly the remaining NAND gates of hammer magnet drivers 306 are associated with a NAND gate from column selector 306. The output of each pair of NAND gates are coupled to transistors 975 through 982. For example NAND gates 920 and 921 which form RS flip-flop are coupled to transistor 975. Transistor 975 has its base coupled to the output of the RS flip-flop formed by NAND gate 920 and 921 through resistor 991. The base of transistor 975 is also coupled to a plus voltage through resistor 990. The emitter of transistor 975 is coupled to ground whereas the collector is coupled through a solenoid 960 of one hammer magnet. The hammer magnet 960 is also coupled in parallel to a diode 945. This scheme is repeated through transistors 975 to 982 and through solenoids 960 through 971.

As hereinbefore described, when data is in the four bit shift register 112, which corresponds to a particular address of NAND gates 901 through 912, then that particular address of the NAND gate of column selector 305 will be activated. For example, when address 2 as shown on FIG. 5 is in the data shift register 112, Q_2 \bar{Q}_3 will be positive, and if at that point in time is a match between the data in shift register 112, and the data in drum counter 107, the output of NAND gate 902 will be low or negative. (This is true because when the inputs to a NAND gate are all positive then the output is negative or low.) Similarly other addresses may be thus selected during the time that it takes one row of characters on the drum 101 to move to the next row. The hammer magnet drivers are activated at an instant in time depending on the state of the Q_n signal; the signal Q_n is normally a logic 0 and is applied to the input of each of the flip-flops comprised of NAND gates 920 through 943. When it is time to activate the hammer magnets the reset signal (Q) is released and the selected low input signals are presented to each of the reset flip-flops, at the proper sequence as determined by the column selector 305. When any of the NAND gates 901 through 911 associated with a particular reset flip-flop comprised of pairs of NAND gates 920 through 943 is low at the output, that particular flip-flop will generate a high signal at its output. The associated transistor or transistors coupled to the selected NAND gates will become conductive, thus energizing the selected solenoid or solenoids causing the print hammers to be activated and impinge on the record medium 103.

Having shown and described one embodiment of the invention, those skilled in the art will realize that many variations and modifications can be made to produce the described invention and still be within the spirit and scope of the claim of invention.

What is claimed is:

1. A time shared electronic system for selectively driving a plurality of impact hammers of a rotary type multi-column impact printer with the hammers operatively associated with a print-drum rotationally supported for rotation about its axis having a font of characters engraved on its periphery the characters arranged in an array of columns and rows, the plurality of print hammers disposed in spatial one to one correspondence with the characters of a row when passing a print-ready position, the print hammers also movably supported for selectively striking a recording medium when disposed between the print hammers and the corresponding engraved characters, said time-shared electronic system comprising:
 - a. data shift-register means for receiving a coded information to be printed on the recording medium;
 - b. shift-register means coupled to said data shift-register means for receiving bit by bit and character by character the coded information shifted out of said data shift-register means and reapplying them bit by bit and character by character to said shift-register means;
 - c. drum character line-counter means responsive to the rotating print drum as each row of characters thereon reaches print-ready position for identifying the row of characters on the print drum that is in print-ready position for printing on the recording medium;
 - d. and comparator means coupled to said shift-register means and to said drum character line-counter means for comparing the coded information in said shift-register means with the coded information in said drum character line-counter means.
2. The time-shared electronic system as recited in claim 1 wherein said data shift-register means, said shift-register means, said drum character line-counter means and said comparator means statically store the coded information.
3. A time-shared electronics system as recited in claim 2 including column selector means coupled to said data register means and to said comparator means for selecting the column of a row in print-ready position when a match is found between the coded information in said shift-register means and said drum character line-counter means.
4. A time-shared electronic system as recited in claim 3 including first storage means for storing the identity of the column selected by said column selector means.
5. A time-shared electronic system as recited in claim 1 wherein all of the coded information in said data shift-register means to be printed on the recording medium are shifted bit by bit and character by character once through said shift-register means during a time interval equal to a time interval of rotation of the drum from one row of type to an adjacent row of type on the drum.

6. A time-shared electronic system as recited in claim 5 wherein all of the characters of a line to be printed on the recording medium in said data shift-register means are shifted through said shift-register means during one complete revolution of the print-drum for as many times as there are rows of characters on the print-drum.

7. A time-shared electronic system as recited in claim 6 including first magnetic signal generating means coupled to said drum character line-counter means for generating electronic timing signals each time that a row of characters passes by the print-ready position.

8. A time shared electronic system as recited in claim 7 including second magnetic signal generating means coupled to said drum character line counter means for producing an electronic reset signal to reset said drum character line counter means to zero each time a complete revolution of the print-drum occurs relative to the print-ready position and wherein the information in said drum character line counter means corresponds at any instant to the information engraved in the row of type on the print-drum in print-ready position during the same instant and wherein the corresponding information in said drum character line-counter means and the engraved row of type at any instant is in binary form in said drum character line-counter means and in decimal form in the engraved row of type on the print drum.

9. A rotary type multi-column impact printer comprising:

- a. a print-drum rotationally supported for rotation about its axis having a font of characters engraved on its periphery arranged in an array of columns and rows;
- b. a plurality of print-hammers disposed in spatial one to one correspondence with the characters of a row when passing a print-ready position, said print-hammers movably supported for selectively striking a recording medium when disposed between said print-hammers and said corresponding engraved characters;
- c. first flip-flop shift-register means for receiving a line of coded information for printing on the recording medium;
- d. second flip-flop shift-register means coupled to said first flip-flop shift-register means for serially receiving coded information from said first register means, serially shifting the coded information through said second shift-register means, and serially applying the coded information directly back into said first shift-register means;
- e. first flip-flop character line-counter means responsive to the row position of the characters relative to said print-hammers position, for identifying the row of characters on the print-drum that is in print-ready position for printing on the recording medium;
- f. comparator means coupled to said second flip-flop shift-register means and to said first flip-flop character line-counter means for comparing the coded information on said second flip-flop shift-register means with the code information in said first flip-flop character line-counter means;

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g. and first flip-flop ring-counter means responsive to said first flip-flop shift-register means for identifying the column of a row of characters in print-ready position, when a match is found between said second flip-flop shift-register means and said first flip-flop character line-counter means.

10. A rotary type multi-column impact printer as recited in claim 9 wherein said flip-flop ring-counter means is delayed one bit from the input coded information.

11. A rotary type multi-column impact printer as recited in claim 9 including first magnetic signal generating means coupled to said first flip-flop character line-counter means for generating electronic timing signals whenever a row of characters on the print-drum passes the print-ready position, second magnetic signal generating means coupled to said first flip-flop character line-counter means for producing an electronic reset signal to reset said first character line-counter means to an initial state whenever a complete revolution of the print-drum occurs relative to the print-ready position, and first reset flip-flop means responsive to said first magnetic signal generating means for dividing every two signals generated by said first magnetic signal generating means into one signal for incrementing said first flip-flop character line-counter means and another trigger signal which is the complement of said one signal.

12. A rotary type multi-column impact printer as recited in claim 11 further including start flip-flop means coupled to said first reset flip-flop means and responsive to externally generated start signals for generating a start print cycle signal.

13. A rotary type multi-column impact printer as recited in claim 12 further including control flip-flop means coupled to said start flip-flop means and to said first reset flip-flop means for synchronizing the externally generated start signals to occur synchronously with a timing pulse.

14. A rotary type multi-column impact printer as recited in claim 12 further including AND gate means coupled to said control flip-flop means, to said first reset flip-flop means and to said comparator means for generating a signal when a match is obtained between the coded information in said second flip-flop shift-register means and the information in said first flip-flop character line-counter means, coincidentally with the application of said trigger signal and a sync signal to the input terminals of said AND gate means.

15. A rotary type multi-column impact printer as recited in claim 9 further including column selector means coupled to said first flip-flop ring-counter means and to said comparator means for selecting the column of a row of characters in print-ready position when a match is found between the coded information in said second flip-flop shift-register means and said first flip-flop character line-counter means, hammer magnet

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means operatively associated with said plurality of print-hammers for causing said plurality of print-hammers to selectively strike the recording medium when disposed between said print-hammers and said corresponding engraved characters, and hammer magnet driver means coupled to said column selector means and to said hammer magnet means for selectively energizing said hammer magnet means.

16. A rotary type multi-column impact printer as recited in claim 15 wherein said column selector means is comprised of a plurality of column selector NAND gate means each having at least three input terminals adapted to receive an (H) signal on one of its first input terminal, a (Q_n) signal on its second input terminal and a (\bar{Q}_n) signal on its third input terminal.

17. A rotary type multi-column impact printer as recited in claim 15 wherein said hammer magnet driver means are comprised of a plurality of magnet driver flip-flop means coupled each to each to said column selector NAND gate means for selectively storing the column identity selected by said selector means, and transistor switch-means coupled each to each to said magnet driver flip-flop means and to said hammer magnet means for selectively switching said hammer magnet means to the on-state.

18. A rotary type multi-column impact printer as recited in claim 16 wherein there are at least twelve column selector NAND gate means and the (Q_n , \bar{Q}_n) signal associated with each NAND gate are as follows:

NAND Gate Identity	Pattern of Q_n, \bar{Q}_n Signals
1	Q_1, \bar{Q}_1
2	Q_2, \bar{Q}_2
3	Q_3, \bar{Q}_3
4	Q_4, \bar{Q}_4
5	Q_5, \bar{Q}_5
6	Q_6, \bar{Q}_6
7	Q_1, \bar{Q}_7
8	\bar{Q}_1, Q_7
9	\bar{Q}_2, Q_2
10	\bar{Q}_3, Q_3
11	\bar{Q}_4, Q_4
12	\bar{Q}_5, Q_5

19. A rotary type multi-column printer as recited in claim 9 wherein the coded information that may appear in said first flip-flop character line-counter means corresponding to the characters engraved on said print wheel has the following corresponding code:

First Flip-Flop Character Line Counter Code	Print Drum Character and Row Number
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 1 1 1	Blank

* * * * *

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