



(51) International Patent Classification:

H01L 21/285 (2006.01) H01L 21/67 (2006.01)
H01L 21/768 (2006.01) H01L 21/677 (2006.01)
H01L 21/02 (2006.01)

(21) International Application Number:

PCT/US2024/035186

(22) International Filing Date:

24 June 2024 (24.06.2024)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

63/524,092 29 June 2023 (29.06.2023) US

(71) Applicant: **APPLIED MATERIALS, INC.** [US/US];
3050 Bowers Avenue, Santa Clara, California 95054 (US).

(72) Inventors: **WU, Liqi**; 3050 Bowers Avenue, Santa Clara,
California 95054 (US). **WANG, Rongjun**; 3050 Bowers
Avenue, Santa Clara, California 95054 (US). **LIU, Feng Q.**;
3050 Bowers Avenue, Santa Clara, California 95054 (US).
ZHU, Qihao; 3050 Bowers Avenue, Santa Clara, California
95054 (US). **LU, Jiang**; 3050 Bowers Avenue, Santa Clara,
California 95054 (US). **THOMPSON, David**; 1743 El Co-

do Way, San Jose, California 95124 (US). **TANG, Xianmin**;
3050 Bowers Avenue, Santa Clara, California 95054 (US).

(74) Agent: **SEACH, JR., Stephen A.**; Servilla Whitney LLC,
33 Wood Avenue South, Suite 830, Iselin, New Jersey
08830 (US).

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG,
KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY,
MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA,
NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO,
RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH,
TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS,
ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, CV,
GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST,
SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ,
RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ,
DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT,
LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE,

(54) Title: BOTTOM-UP GAP FILL PROCESSES FOR SEMICONDUCTOR SUBSTRATES

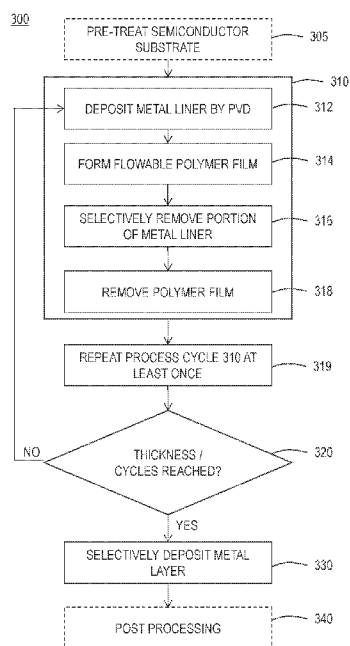


FIG. 3A

(57) Abstract: Embodiments of the disclosure relate to methods of selectively depositing a metallic material after forming a flowable polymer film to protect a substrate surface within a feature. A first metal liner is deposited by physical vapor deposition (PVD). The flowable polymer film is formed on the first metal liner on the bottom. A portion of the first metal liner is selectively removed from the top surface and the at least one sidewall. The flowable polymer film is removed. In some embodiments, the cycle of depositing a metal liner, forming a flowable polymer film, removing a portion of the metal liner, and removing the flowable polymer film is repeated at least once. A metal layer is deposited on the plurality of metal liners (e.g., first metal liner and the second metal liner) and the metal layer is free of seams or voids.

SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN,
GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

BOTTOM-UP GAP FILL PROCESSES FOR SEMICONDUCTOR SUBSTRATES

TECHNICAL FIELD

- 5 **[0001]** Embodiments of the present disclosure pertain to methods of selective deposition facilitated by a flowable polymer. More particularly, embodiments of the disclosure are directed to methods of selectively depositing a metal after use of a flowable polymer to protect a substrate surface within a feature.

BACKGROUND

- 10 **[0002]** Gap fill processes are integral to several semiconductor manufacturing processes. A gap fill process can be used to fill a gap (or feature) with an insulating or conducting material. For example, shallow trench isolation, inter-metal dielectric layers, passivation layers, dummy gate, are all typically implemented by gap fill processes.

- 15 **[0003]** As device geometries continue to shrink (e.g., critical dimensions < 20 nm, < 10 nm, and beyond) and thermal budgets are reduced, defect-free filling of spaces becomes increasingly difficult due to the limitations of conventional deposition processes.

- 20 **[0004]** Physical vapor deposition (PVD) processes have been widely used for liner or gap fill applications. However, it remains a challenge to deposit high sidewall coverage PVD films without causing overhang due to continuous scaling. Both overhang and low sidewall coverage limit the effectiveness of chemical vapor deposition (CVD) or atomic layer deposition (ALD) gap fill or filling a feature entirely by PVD. The effectiveness of CVD or ALD is also limited for gap fill or filling a feature entirely by PVD when there is a liner deposited prior to gap fill due to overhang and low sidewall coverage.

- 25 **[0005]** Processes for selective metal gap fill, such as tungsten fill, have been implemented wherein tungsten can be selectively deposited on a tungsten seed layer. Unfortunately, these processes require a minimum seed layer thickness. Known PVD processes can provide the necessary seed layer thickness, but the selective tungsten fill process will deposit tungsten material on any exposed seed layer. Additionally, there

are no known selective metal deposition methods on metal or metal silicide without causing damage to the underlying metal or metal silicide.

[0006] Accordingly, there is a need for methods to protect the metal or metal silicide within a feature in order to enable bottom-up fill by selective deposition processes.

5 SUMMARY

[0007] One or more embodiments of the disclosure are directed to a method manufacturing a semiconductor device. The method comprises: depositing a first metal liner by physical vapor deposition (PVD) on a semiconductor substrate surface with at least one feature formed thereon. The at least one feature has at least one opening at
10 a top surface with an opening width, at least one sidewall, and a bottom. The at least one feature extends a feature depth from the top surface to the bottom. The first metal liner forms on the top surface, on the at least one sidewall, and on the bottom. The method comprises forming a first flowable polymer film on the first metal liner within the at least one feature. The first flowable polymer film forms on the first metal liner on the
15 bottom and has a polymer depth less than the feature depth. The method comprises selectively removing at least a portion of the first metal liner from the top surface and the at least one sidewall. The method comprises removing the first flowable polymer film to expose the first metal liner on the bottom of the at least one feature. The method comprises depositing a second metal liner by physical vapor deposition (PVD) on the
20 top surface of the at least one feature, and on the remaining portion of the first metal liner on the at least one sidewall and on the bottom. The method comprises selectively depositing a metal layer on the first metal liner and the second metal liner to fill the at least one feature.

[0008] Additional embodiments of the disclosure are directed to a method of
25 manufacturing a semiconductor device. The method comprises depositing a first metal liner comprising tungsten (W) by physical vapor deposition (PVD) on a semiconductor substrate surface with at least one feature formed thereon. The at least one feature has at least one opening at a top surface with an opening width, at least one sidewall, and a bottom. The at least one feature comprises an overhang or an undercut within the
30 opening width, and the at least one feature extends a feature depth from the top surface to the bottom. The first metal liner forms on the top surface, on the overhang or the

undercut, on the at least one sidewall, and on the bottom. The method comprises forming a first flowable polymer film on the first metal liner within the at least one feature. The first flowable polymer film forms on the first metal liner on the bottom and has a polymer depth less than or equal to the feature depth. The method comprises
5 selectively removing at least a portion of the first metal liner from the top surface and the at least one sidewall. The method comprises removing the first flowable polymer film to expose the first metal liner on the bottom of the at least one feature. The method comprises depositing a second metal liner comprising tungsten (W) by physical vapor deposition (PVD) on the top surface of the at least one feature, on the overhang or the
10 undercut, and on the remaining portion of the first metal liner on the at least one sidewall and on the bottom. The method comprises selectively depositing a metal layer on the first metal liner and the second metal liner to fill the at least one feature.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] So that the above recited features of the present disclosure can be understood
15 in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this disclosure and are therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective embodiments.

20 [0010] The embodiments as described herein are illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references indicate similar elements.

[0011] FIG. 1A illustrates a cross-sectional view of a semiconductor substrate according to the prior art;

25 [0012] FIG. 1B illustrates a cross-sectional view of a semiconductor substrate according to the prior art;

[0013] FIG. 1C illustrates a cross-sectional view of a semiconductor substrate according to the prior art;

30 [0014] FIG. 2A illustrates a process flow diagram of a method according to one or more embodiments;

- [0015] FIG. 2B illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;
- [0016] FIG. 2C illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;
- 5 [0017] FIG. 2D illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;
- [0018] FIG. 2E illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;
- [0019] FIG. 2F illustrates a cross-sectional view of a semiconductor substrate
10 according to one or more embodiments;
- [0020] FIG. 2G illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;
- [0021] FIG. 2H illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;
- 15 [0022] FIG. 3A illustrates a process flow diagram of a method according to one or more embodiments;
- [0023] FIG. 3B illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;
- [0024] FIG. 3C illustrates a cross-sectional view of a semiconductor substrate
20 according to one or more embodiments;
- [0025] FIG. 3D illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;
- [0026] FIG. 3E illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;
- 25 [0027] FIG. 3F illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;
- [0028] FIG. 3G illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;
- [0029] FIG. 3H illustrates a cross-sectional view of a semiconductor substrate
30 according to one or more embodiments;
- [0030] FIG. 3I illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;

[0031] FIG. 3J illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;

[0032] FIG. 3K illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments; and

5 [0033] FIG. 4 is a schematic top-view diagram of an example multi-chamber processing system according to one or more embodiments.

DETAILED DESCRIPTION

[0034] Before describing several exemplary embodiments of the disclosure, it is to be understood that the disclosure is not limited to the details of construction or process
10 steps set forth in the following description. The disclosure is capable of other embodiments and of being practiced or being carried out in various ways.

[0035] The term "about" as used herein means approximately or nearly and in the context of a numerical value or range set forth means a variation of $\pm 15\%$ or less, of the numerical value. For example, a value differing by $\pm 14\%$, $\pm 10\%$, $\pm 5\%$, $\pm 2\%$, $\pm 1\%$,
15 $\pm 0.5\%$, or $\pm 0.1\%$ would satisfy the definition of about.

[0036] As used in this specification and the appended claims, the term "substrate" or "wafer" refers to a surface, or portion of a surface, upon which a process acts. It will also be understood by those skilled in the art that reference to a substrate can refer to only a portion of the substrate unless the context clearly indicates otherwise.
20 Additionally, reference to depositing on a substrate can mean both a bare substrate and a substrate with one or more films or features deposited or formed thereon.

[0037] A "substrate" as used herein, refers to any substrate or material surface formed on a substrate upon which film processing is performed during a fabrication process. For example, a substrate surface on which processing can be performed
25 include materials such as silicon, silicon oxide, strained silicon, silicon on insulator (SOI), carbon doped silicon oxides, amorphous silicon, doped silicon, germanium, gallium arsenide, and any other materials such as metals, metal nitrides, metal alloys, and other conductive materials, depending on the application. Substrates include, without limitation, semiconductor wafers. Substrates may be exposed to a pretreatment
30 process to polish, etch, reduce, oxidize, hydroxylate, anneal and/or bake the substrate surface. In addition to film processing directly on the surface of the substrate itself, in

the present disclosure, any of the film processing steps disclosed may also be performed on an under-layer formed on the substrate as disclosed in more detail below, and the term "substrate surface" is intended to include such under-layer as the context indicates. Thus, for example, where a film/layer or partial film/layer has been deposited
5 onto a substrate surface, the exposed surface of the newly deposited film/layer becomes the substrate surface.

[0038] As used herein, the term "substrate surface" refers to any substrate surface upon which a layer may be formed. The substrate surface may have one or more features formed therein, one or more layers formed thereon, and combinations thereof.
10 The shape of the feature can be any suitable shape including, but not limited to, peaks, trenches, holes and vias (circular or polygonal). As used in this regard, the term "feature" refers to any intentional surface irregularity. Suitable examples of features include but are not limited to trenches, which have a top, two sidewalls and a bottom extending into the substrate, vias which have one or more sidewall extending into the
15 substrate to a bottom and slot vias.

[0039] As used in this specification and the appended claims, the term "selectively" refers to a process which acts on a first surface with a greater effect than another second surface. Such a process would be described as acting "selectively" on the first surface over the second surface. The term "over" used in this regard does not imply a
20 physical orientation of one surface on top of another surface, rather a relationship of the thermodynamic or kinetic properties of the chemical reaction with one surface relative to the other surface.

[0040] The term "on" indicates that there is direct contact between elements. The term "directly on" indicates that there is direct contact between elements with no
25 intervening elements.

[0041] As used in this specification and the appended claims, the terms "precursor," "reactant," "reactive gas" and the like are used interchangeably to refer to any gaseous species that can react with the substrate surface.

[0042] Embodiments of the disclosure advantageously provide methods for
30 selectively depositing polysilicon after use of a flowable polymer to protect a substrate surface within a feature. One or more embodiments advantageously provide for the removal of a metallic material from the field and sidewalls of a feature without removal

of a flowable polymer from the bottom surface of the substrate. The remaining flowable polymer has a smooth surface. Further embodiments advantageously provide methods for selectively depositing a metallic gap fill in a bottom-up fashion. More particularly, embodiments advantageously provide methods for bottom-up metal gap fill that is free
5 of seams or voids.

[0043] The embodiments of the disclosure are described by way of the Figures, which illustrate processes and substrates in accordance with one or more embodiments of the disclosure. The processes, schemes, and resulting substrates shown are merely illustrative of the disclosed processes, and the skilled artisan will recognize that the
10 disclosed processes are not limited to the illustrated applications.

[0044] In the following description, numerous specific details are set forth in order to provide a thorough understanding of embodiments. It will be apparent to one skilled in the art that embodiments may be practiced without these specific details. In other instances, well-known aspects are not described in detail in order to not unnecessarily
15 obscure embodiments. Furthermore, it is to be understood that the various embodiments shown in the accompanying drawings are illustrative representations and are not necessarily drawn to scale.

[0045] FIGS. 1A–1C illustrate cross-sectional views of a semiconductor substrate according to the prior art. In FIG. 1A, an incoming semiconductor device 10 includes a
20 feature 11 having an opening 12 with an opening width 75. The opening 12 is formed in a top surface 15 of the device 10. The feature 11 also has one or more sidewall 14 and extends a feature depth D from the top surface 15 to a bottom 16. The one or more sidewalls 14 include an overhang or undercut 20 near the top surface 15 of the opening 12.

[0046] In one or more embodiments, the device 10 illustrated is comprised of a material 19 on a material 18. Those skilled in the art will recognize that the top surface 15, sidewall 14, and bottom 16 may each be comprised of one or more similar or different materials. For example, the lower portion of sidewall 14 may be formed from a first material while the upper portion of the same sidewall 14 (e.g., the overhang or
30 undercut 20) may be comprised of a second material. Similarly, a thin layer may be deposited on the top surface 15 without forming an appreciable portion of the sidewall 14. In one or more embodiments, the bottom 16 may be comprised of a different

material than the sidewall 14. In one or more embodiments, the material 18 comprises silicon nitride (SiN). In one or more embodiments, the material 19 comprises silicon oxide (SiOx).

5 [0047] In FIG. 1B, a metal liner 30 is deposited on the top surface 15, the overhang or undercut 20, the sidewall 14, and the bottom 16 using a conventional PVD process. In FIG. 1C, a metal material 40 is deposited on the metal liner 30 to fill the feature 11 by a conventional CVD process. As shown in the illustrated embodiment, the metal material 40 includes a seam in the center as the metal material 40 forms from the sidewall and meets in the center. As used herein with reference to a substrate feature,
10 the term "center" refers to a region that includes a middle portion of the opening width and a middle portion of the depth of the feature, and is not a fixed point. As shown in the illustrated embodiment, the metal material 40 also includes a plurality of voids (denoted by the ovals in FIG. 1C). The seam and the voids in the metal material 40 may lead to a higher line resistance and/or an open circuit, i.e., device failure or defects.

15 [0048] FIGS. 1A–1C illustrate the PVD liner related overhang and weak sidewall coverage issues for feature gap fill. If the incoming structure, such as device 10 has an overhang or undercut 20, it will further amplify the PVD liner overhang and weak sidewall coverage issues. As a result, conformal CVD gap fill, such as the metal material 40, would have 1) many sidewall voids due to discontinuous liner (e.g., metal liner 30),
20 and 2) a center seam due to amplified overhang or undercut. Without intending to be bound by theory, it has been found that the seam and voids can merge and form open lines, which would cause device failure. Subsequent processing, such as a chemical mechanical planarization (CMP) process also will attack the metal liners (e.g., metal liner 30) from the seam and voids, causing device failure. As such, sidewall thickness
25 and overhang are limiting factors to extend PVD processing to structure having a critical dimension less than or equal to 15 nm or 10 nm nodes and beyond.

[0049] Referring to the Figures, the disclosure relates to methods 100 and 300 of selective deposition of a gap fill material. FIG. 2A illustrates a process flow diagram of a selective deposition method 100 in accordance with one or more embodiments of the
30 present disclosure. FIGS. 2B–2H depict a device 200 having a substrate surface with at least one feature formed therein during processing according to one or more embodiments of the present disclosure. FIG. 3A illustrates a process flow diagram of a

selective deposition method 100 in accordance with one or more embodiments of the present disclosure. FIGS. 3B–3K depict a device 1000 having a substrate surface with at least one feature formed therein during processing according to one or more embodiments of the present disclosure. FIG. 4 is a schematic top-view diagram of an example multi-chamber processing system for performing the methods according to one or more embodiments.

[0050] FIG. 2B illustrates a semiconductor device 200 with a substrate surface. As identified above, the substrate surface refers to the exposed surface of the substrate upon which a process may be performed. The substrate surface has at least one feature 210 formed therein. While only one feature is shown in the Figures, one skilled in the art will recognize that a plurality of features will each be affected by the disclosed methods in a similar manner.

[0051] The at least one feature 210 has an opening 212 with an opening width 205. The opening 212 is formed in a top surface 215 of the device 200. The feature 210 also has one or more sidewall 214 and extends a feature depth D from the top surface 215 to a bottom 216. The one or more sidewalls 214 include an overhang or undercut 230 near the top surface 215 of the opening 212. The overhang or undercut 230 may have any suitable shape. Stated differently, the overhang or undercut 230 may be any suitable shape such that the sidewall 214 does not vertically extend from the top surface 215 to the bottom 216. While the present disclosure is described with respect to incoming substrates having an overhang or undercut, the skilled artisan will appreciate that the disclosed processes can be implemented on substrates that do not have an overhang or undercut and extend vertically entirely from top surface to bottom.

[0052] In one or more embodiments, the device 200 illustrated in FIGS. 2B–2H is comprised of a material 221 on a material 220. In one or more embodiments, each of the materials (material 220 and material 221) comprise a dielectric material. Those skilled in the art will recognize that the top surface 215, sidewall 214, and bottom 216 may each be comprised of one or more similar or different materials. For example, the lower portion of sidewall 214 may be formed from a first material while the upper portion of the same sidewall 214 (e.g., the overhang or undercut 230) may be comprised of a second material. Similarly, a thin layer may be deposited on the top surface 215 without forming an appreciable portion of the sidewall 214. In one or more embodiments, the

bottom 216 may be comprised of a different material than the sidewall 214. In one or more embodiments, the material 220 comprises silicon nitride (SiN). In one or more embodiments, the material 221 comprises silicon oxide (SiOx). In one or more embodiments, each of the material 220 and the material 221 comprises silicon nitride (SiN). In one or more embodiments, each of the material 220 and the material 221 comprises silicon oxide (SiOx).

[0053] In one or more embodiments, the opening width 205 of the opening 212 is less than or equal to about 50 nm, less than or equal to about 30 nm, less than or equal to about 20 nm, less than or equal to about 10 nm, or less than or equal to about 7 nm. In one or more embodiments, the opening width 205 is in a range of about 8 nm to about 20 nm.

[0054] In one or more embodiments, the feature depth D of the feature 210 is greater than or equal to about 5 nm, greater than or equal to about 10 nm, greater than or equal to about 20 nm, greater than or equal to about 50 nm, greater than or equal to about 60 nm, greater than or equal to about 75 nm, greater than or equal to about 100 nm, greater than or equal to about 200 nm, greater than or equal to about 300 nm, greater than or equal to about 400 nm, or greater than or equal to about 450 nm. In one or more embodiments, the feature depth D is in a range of about 5 nm to about 500 nm. In one or more embodiments, the feature depth D is in a range of about 10 nm to about 300 nm. In one or more embodiments, the feature depth D is in a range of about 60 nm to about 100 nm.

[0055] As used herein, the term "feature" means any intentional surface irregularity. Suitable examples of features include but are not limited to trenches or vias which have a top, two sidewalls and a bottom, peaks which have a top and two sidewalls. Features can have any suitable aspect ratio (ratio of the depth of the feature to the width of the feature). In one or more embodiments, the aspect ratio of the at least one feature 210 is greater than or equal to about 1:1, 5:1, 10:1, 15:1, 20:1, 25:1, 30:1, 35:1, or 40:1.

[0056] For simplicity, reference will be made to parts of the feature 210 illustrated in FIG. 2B while referring to FIGS. 2C–2H. For example, the device 200 shown in FIG. 2C will be referred to as having a bottom 216. For clarity of the illustrations provided, the reference numerals of the parts of feature 210 are not shown in FIGS. 2C–2H.

[0057] Referring to FIGS. 2A–2H, in one or more embodiments, the method 100 begins with optional operation 105 to pre-treat the substrate. The pre-treatment at operation 105 can be any suitable pre-treatment known to the skilled artisan. Suitable pre-treatments include, but are not limited to, pre-heating, cleaning, soaking, native
5 oxide removal, or deposition of a contact layer (e.g., titanium silicide (TiSi)), or capping layers (e.g., TiSiN). In one or more embodiments, a layer such as titanium silicide or titanium silicon nitride (TiSiN), or other metal silicide is deposited at operation 105 to form a silicide contact.

[0058] The skilled artisan will recognize that the disclosed processes are not limited
10 to the silicide contact and liner/gap fill applications. Generally, front-end of line (FEOL) refers to the first portion of integrated circuit fabrication, including transistor fabrication, middle of line (MOL) connects the transistor and interconnect parts of a chip using a series of contact structures, and back-end of line (BEOL) refers to a series of process steps after transistor fabrication through completion of a wafer. One or more
15 embodiments of the disclosure are directed to methods of forming devices that are useful for one or more FEOL, MOL, and/or BEOL processes known to the skilled artisan.

[0059] An exemplary device 200 is shown in FIG. 2B after optional operation 105. Those skilled in the art will recognize that the disclosed processes may be performed on different materials and/or that the illustrated layers may be arranged in different
20 ways.

[0060] The method 100 continues with cycle 110. The cycle 110 forms at least one metal liner at the bottom 216 of at least one feature 210 of the device 200. The cycle 110 includes a series of operations which are each performed in sequence and may be repeated. Some of the operations are optional within each cycle. A given optional
25 operation may be performed during each cycle, periodically (every other, every fifth, or every hundredth cycle), as needed based on predetermined parameters, or even not at all.

[0061] As shown in FIG. 2C, the cycle 110 begins with operation 112. At operation 112, a first metal liner 240 is deposited on the top surface 215, on the overhang or undercut 230, on the at least one sidewall 214, and on the bottom 216 of the at least
30 one feature 210. The first metal liner 240 has a bottom thickness on the bottom 216 and a top thickness on the top surface 215 and/or a sidewall thickness on the sidewall

214. The metallic material of the first metal liner 240 may comprise any suitable material known to the skilled artisan. In some embodiments, the first metal liner 240 comprises one or more of tungsten (W), molybdenum (Mo), ruthenium (Ru), or cobalt (Co). In some embodiments, the first metal liner 240 comprises tungsten (W). In one or more
5 embodiments, the first metal liner 240 comprises an alloy of one or more of tungsten (W), molybdenum (Mo), ruthenium (Ru), or cobalt (Co).

[0062] The first metal liner 240 may be deposited by any suitable method. In one or more embodiments, the first metal liner 240 is deposited by physical vapor deposition (PVD). In these embodiments, as shown in FIG. 2C, the sidewall thickness is less than
10 the top thickness and the bottom thickness. In one or more embodiments, the top thickness is greater than the bottom thickness.

[0063] Those skilled in the art will recognize that the disclosed methods may begin with a first metal liner 240 already formed, and the device 200 is then provided. As used in this specification and the appended claims, the term "provided" means that the
15 substrate is made available for processing (e.g., positioned in a processing chamber).

[0064] The cycle 110 continues with operation 114. As shown in FIG. 2D, at operation 114, a flowable polymer film 250 is formed on the first metal liner 240 within the feature 210 of the device 200. The polymer film 250 has a polymer thickness less than or equal to the feature depth D. Stated differently, as a flowable film (described below), the
20 polymer film 250 is contained entirely within the feature 210 and is not present on the top surface 215 of the device 200. Accordingly, in this regard, the polymer may be described as having a "thickness" or may interchangeably be described as having a "depth." Stated differently, the polymer "thickness" is measured in a Z-direction within the feature 210 of the device 200, such that the thickness/depth is less than or equal to feature depth
25 D. In one or more embodiments, the polymer film 250 has a thickness in a range of about 1 nm to about 50 nm, or in a range of about 1 nm to 10 nm, or in a range of about 2 nm to about 5 nm. In some embodiments, the thickness of the polymer film 250 is in a range of from 1% to 99%, or in a range of from 1% to 80%, or in a range of from 2% to 20% of the depth D of the at least one feature 210.

30 [0065] In the disclosed methods, processing parameters and reactants may be selected to limit conformality of deposited materials, which may allow the deposited material to better fill features on the substrate. A flowable material is one which, under

the proper conditions, will flow by gravity to the low point of a substrate surface and/or by capillary action to narrow CD spaces of trenches or other features.

[0066] In one or more embodiments, forming the polymer film at operation 114 comprises exposing the surface to one or more monomers.

5 [0067] In some embodiments, the one or more monomers comprise, consist essentially of, or consist of a single monomer selected from the group consisting of a methyl group, a methacrylate group, a styrene group, a benzyl alcohol group, a benzyl chloride group, an aldehyde group, and an amine group. In some embodiments, the one or more monomers consist of a single monomer selected from the group consisting
10 of a methyl group, a methacrylate group, a styrene group, a benzyl alcohol group, a benzyl chloride group, and an aldehyde group.

[0068] In one or more embodiments, the monomers comprise, consist essentially of, or consist of a single, bi-functional monomer, with each functional group in the bi-functional monomer being different. In this way, one functional group of a monomer
15 molecule will react with the other functional group of a different monomer molecule. Those skilled in the art may recognize this as an "A" polymer.

[0069] In one or more embodiments, the one or more monomers comprise, consist essentially of, or consist of one or more of amines with bi-functional groups, aldehydes with bi-functional groups, ketones with bi-functional groups, and alcohols with bi-
20 functional groups.

[0070] In one or more embodiments, the monomers comprise, consist essentially of, or consist of two monomers, such as two bi-functional monomers, each functional group being the same. In this way the functional groups of one monomer react with the functional groups of a second monomer. Those skilled in the art may recognize this as
25 an "AB" polymer.

[0071] In one or more embodiments, the one or more monomers comprise, consist essentially of, or consist of three monomers, wherein two of the monomers independently comprise one or more of an amine with a single functional group, an aldehyde with a single functional group, a ketone with a single functional group, or an
30 alcohol with a single functional group, and at least one of the monomers is independently selected from the group consisting of amines with bi-functional groups, aldehydes with bi-functional groups, ketones with bi-functional groups, and alcohols

with bi-functional groups. Those skilled in the art may recognize this as an "ABC" polymer.

[0072] In one or more embodiments, the flexible monomers used for producing the selective protection polymer film 250 are capable of forming oligomers in a higher percentage during polymerization compared with stiff monomers. Thus, in one or more 5 embodiments, the polymerization process is through monomer, oligomer, and polymer stages. The polymer formation depends on its local concentration of monomers. In one or more embodiments, A and B monomers are used, which can only bond between A and B, not between A's or B's. Therefore, during the purge and pumping stage, the A concentration is greatly reduced, especially on the field/wall areas 214, 215. In this 10 case, when B monomers come in, it only forms oligomers on the field/wall areas 214, 215 with very low concentration of A monomer. Due to pumping and purge efficiency difference between field/wall 214, 215 and bottom 216 of the feature 210, the A monomer concentration in the bottom 216 of the feature 210 is higher compared with 15 the concentration on the field/wall 214, 215. Since A monomer concentration is higher at the bottom 216 of the feature 210, it forms higher molecular number oligomer or polymer with incoming B monomers. These oligomers and polymers will continually grow with process cycles at bottom 216 of the feature 210. In one or more embodiments, a lower molecular weight B monomer is used, when it forms B-A-B oligomer on field/wall 20 214, 215 with low concentration of A, it is still volatile compared with higher oligomers formed at bottom 216 of the feature 210, B-A-B-A-B, etc., which decreases the amount of polymer residue on field/wall 214, 215 as much as possible.

[0073] A benzene ring has an electrical advantage to activate the aldehyde functional group during bonding with amine. When two aldehyde groups are in the 1,4 positions 25 of a benzene ring, the monomer is a stiff or rigid monomer. When the monomer reacts with 1,4-diaminobenzene, it forms a stiff polymer with a rough surface in the feature.

[0074] Accordingly, in one or more embodiments, if two aldehyde groups are in the 1,3 positions of benzene, which is a flexible monomer, a flexible polymer film 250 with is formed. The flexible polymer film 250 has a lower glass transition temperature 30 compared with a film formed from a stiff polymer. Thus, in one or more embodiments, a polymer film 250 is advantageously formed having a smooth polymer surface,

flexibility, and a lower glass transition temperature (T_g), especially when the T_g is below the process temperature.

[0075] In one or more embodiments, when a flexible monomer is used, the opportunity to form oligomers, such as ABAB or ABABAB, is increased. Flexible monomers also make possible a smooth surface in the feature 210 with easy packing and packing density. Flexible monomers also reduce polymer residue on field/wall 214, 215 area due to the oligomers volatility and flowability into the feature. By this improvement, the residue of polymer on field 215 and on the sidewall 214 is eliminated, enhancing process efficiency. In one or more embodiments, the semiconductor device quality is improved when there is substantially no residue or no residue on the field 215 and wall 214 areas.

[0076] Without intending to be bound by theory, it is thought that the polymer that is formed and deposited as the polymer film 250 has the flexibility to fill the bottom 216 of the feature 210. In one or more embodiments, the polymer has liquidity during deposition and further processing.

[0077] As stated previously, the polymer film 250 is flowable. In order to control the "flowability" of the resulting polymer film 250, it has been found that it is necessary to control the size of the resulting oligomers.

[0078] Accordingly, in one or more embodiments, the formation of the polymer film 250 is performed on a substrate maintained at a temperature in a range of 0 °C to 400 °C. In some embodiments, the substrate is maintained at a temperature in a range of 30 °C to 400 °C.

[0079] Further, other process parameters may be controlled during the formation of the polymer film 250. Examples of parameters which may be controlled include, but are not limited to processing chamber pressure, monomer selections, the use of an inert diluent or carrier gas, partial pressures of monomers, pulse sequence of monomers, and pause periods to permit flow of the polymer material.

[0080] After forming the flowable polymer film 250 at operation 114, the cycle 110 continues with operation 116. As shown in FIG. 2E, at operation 116, at least a portion of the first metal liner 240 is selectively removed. In one or more embodiments, the first metal liner 240 is selectively removed from the top surface 215, the overhang or undercut 230, and a portion of the at least one sidewall 214. The first metal liner 240 is

removed from the top surface 215 without substantially affecting any material beneath the polymer film 250. As used in this regard, a process which does not “substantially affect” material layers does not cause any decrease in volume, thickness, or composition. One skilled in the art will recognize that the polymer film 250 is acting as
5 an etch stop layer during the removal of a portion of the first metal liner 240.

[0081] In one or more embodiments, operation 116 also removes a portion of the first metal liner 240 from the sidewall 214. In specific embodiments, operation 116 removes a portion of the first metal liner 240 that is deposited on the sidewall 214 of the material 221 (e.g., silicon oxide (SiOx)). In specific embodiments, operation 116 removes a
10 portion of the first metal liner 240 that is deposited on the sidewall 214 of the material 220 (e.g., silicon nitride (SiN)). In one or more embodiments, operation 116 removes a portion of the first metal liner 240 that is deposited on the sidewall 214 of the material 220 (e.g., silicon nitride (SiN)) and a portion of the first metal liner 240 that is deposited on the sidewall 214 of the material 221 (e.g., silicon oxide (SiOx)). In one or more
15 embodiments, any portion of the first metal liner 240 which is present on sidewall 214 below the upper surface of the polymer film 250, such as on the material 220 (silicon nitride (SiN)), for example, may remain intact without being removed.

[0082] In one or more embodiments, the selective removal of the portion of the first metal liner 240 at operation 116 is performed on a substrate maintained at a
20 temperature in a range of 100 °C to 400 °C.

[0083] In one or more embodiments, the selective removal of the first metal liner 240 is performed by exposing the substrate surface to a fluorine-based plasma or a chlorine-based plasma. Any suitable fluorine-based plasma or chlorine-based plasma known to the skilled artisan that selectively removes the first metal liner 240 may be used.

25 **[0084]** In one or more embodiments, the selective removal of the first metal liner 240 at operation 116 is performed by exposing the substrate surface to NF₃ radicals. In one or more embodiments, the substrate is maintained at a temperature in a range of 80 °C to 150 °C.

30 **[0085]** In one or more embodiments, the selective removal of the first metal liner 240 at operation 116 is performed by exposing the substrate surface to a chlorine-containing gas or an alkylchloride gas. In some embodiments, the alkylchloride gas includes, but is not limited to, methylchloride, 2-chloropropane, or 1,2-dichloroethane. In one or more

embodiments, the substrate is maintained at a temperature in a range of 80 °C to 150 °C.

[0086] The cycle 110 continues with operation 118. As shown in FIG. 2F, at operation 118, the polymer film 250 is removed to expose the remaining portion of the first metal liner 240, e.g., the portion of the first metal liner 240 on the bottom 216
5 beneath the polymer film 250. In one or more embodiments, the removal of the polymer film 250 is complete and leaves substantially no residue or no residue.

[0087] In one or more embodiments, the polymer film 250 is removed by exposing the substrate surface to a hydrogen (H₂) plasma treatment. In one or more
10 embodiments, the polymer film 250 is removed by exposure to a thermal O₂ environment at an elevated temperature.

[0088] In one or more embodiments, the removal of the polymer film 250 is performed by exposing the substrate surface to one or more of a thermal process or a hydrogen (H₂) plasma treatment. In one or more embodiments, after removing the first metal liner
15 240 from the top surface 215 and sidewall 214, the polymer film 250 can be removed thermally by heating it to 350 °C to 500 °C under vacuum. In other embodiments, after removing the first metal liner 240 from the top surface 215 and sidewall 214, the polymer film 250 may also be removed by hydrogen (H₂) plasma at temperature in a range of from 100 °C to 300 °C for a time period in a range of from 2 seconds to 30 seconds.

[0089] In one or more embodiments, the removal of the polymer film 250 at operation
20 118 comprises a first step including exposing the substrate surface to hydrogen (H₂) plasma and oxygen (O₂) plasma and a second step including exposing the substrate surface to hydrogen (H₂) plasma only.

[0090] The first step may be performed at a chamber pressure in a range of from
25 about 1 Torr to about 10 Torr, for example, about 5 Torr, at a flow rate of the hydrogen (H₂) plasma in a range of from about 1000 sccm to about 10000 sccm, for example, 6000 sccm and a flow rate of the oxygen (O₂) in a range of from about 100 sccm to about 1000 sccm, for example, 300 sccm.

[0091] The second step may be performed at a chamber pressure in a range of from
30 about 10 Torr to about 50 Torr, for example, about 20 Torr, at a flow rate of the hydrogen (H₂) plasma in a range of from about 10 sccm to about 10000 sccm.

[0092] The polymer removal process of operation 118 may be performed in a processing chamber, such as a Volta® CVD/ALD chamber available from Applied Materials of Santa Clara, Calif.

[0093] After removing the polymer film 250, at operation 118 shown in FIG. 2F, the cycle 110 continues with operation 119. At operation 119, a second metal liner 260 is deposited on the top surface 215, on the overhang or undercut 230, on the at least one sidewall 214, and on the remaining portion of the first metal liner 240 on the bottom 216 of the at least one feature 210. The second metal liner 260 may be deposited by the same or similar process as the deposition of the first metal liner 240, operation 112 shown in FIG. 2C. The metallic material of the second metal liner 260 may comprise any suitable material known to the skilled artisan. In some embodiments, the second metal liner 260 comprises one or more of tungsten (W), molybdenum (Mo), ruthenium (Ru), or cobalt (Co). In some embodiments, the second metal liner 260 comprises tungsten (W). In some embodiments, each of the first metal liner 240 and the second metal liner 260 comprises one or more of tungsten (W), molybdenum (Mo), ruthenium (Ru), or cobalt (Co). In some embodiments, each of the first metal liner 240 and the second metal liner 260 comprises tungsten (W).

[0094] In one or more embodiments, the first metal liner 240 and the second metal liner 260 form a continuous layer. One or more of the layers deposited on the substrate or substrate surface may be continuous. As used herein, the term "continuous" refers to a layer that covers an entire exposed surface without gaps or bare spots that reveal material underlying the deposited layer.

[0095] In some embodiments, the first metal liner 240 does not form a continuous layer. In some embodiments, the second metal liner 260 does not form a continuous layer.

[0096] In one or more embodiments, at the end of cycle 110, the surface of the first metal liner 240/second metal liner 260 does not contain any contaminants or residues of the polymer film 250. Specifically, in one or more embodiments, there are no carbon or oxygen residues on the surface of the first metal liner 240/second metal liner 260. In one or more embodiments, when the method 100 includes repeated cycles 110 (see below), there are no contaminants or residues between amounts of first metal liner 240/second metal liner 260 deposited in subsequent cycles. In one or more

embodiments, when the method 100 includes the deposition of a metal layer 270 (see below), there are no contaminants or residues between the first metal liner 240/second metal liner 260 and the metal layer 270.

[0097] In one or more embodiments, the monomers are selected so as not to contain any oxygen atoms which may oxidize the surface of the first metal liner 240/second metal liner 260 during removal of the polymer film 250.

[0098] The method 100 continues to decision point 120. At point 120, the substrate is evaluated to determine whether or not first metal liner 240/second metal liner 260 has reached a predetermined thickness or a predetermined number of cycles 110 have been performed. If the conditions are met, the method 100 continues to operation 130. If the conditions are not met, the method 100 returns to the beginning of cycle 110 with operation 112. In those embodiments in which the cycle 110 is repeated to form additional material, those skilled in the art will appreciate that operation 112 is often performed to deposit the requisite additional metal material (e.g., the first metal liner 240/second metal liner 260). In one or more embodiments, the predetermined thickness is in a range of from about 1 nm to about 20 nm, or in a range of from about 2 nm to about 10 nm.

[0099] In one or more unillustrated embodiments, one or more of the first metal liner 240 or the second metal liner 260 may be optionally etched. In one or more embodiments, one or more of the first metal liner 240 or the second metal liner 260 is etched to remove the portions of the first metal liner 240 or the second metal liner 260, respectively, which extend up the sidewall 214. When etched, one or more of the first metal liner 240 or the second metal liner 260 is also thinned on the bottom 216 of the feature 210. Accordingly, one skilled in the art will recognize that one or more of the first metal liner 240 or the second metal liner 260 may be deposited to a greater bottom thickness than desired in a final product to provide for sacrificial material which will be removed when etching the metal material from the sidewall 214.

[00100] The method 100 includes operation 130 after depositing the second metal liner 260 at operation 119 shown in FIG. 2G. In FIG. 2H, at operation 130, a metal layer 270 is selectively deposited on the first metal liner 240/second metal liner 260. The metal layer 270 may be deposited by any suitable deposition process known to the skilled artisan such that the metal layer 270 forms selectively to the surface of the first

metal liner 240/second metal liner 260 over other substrate surface materials. In one or more embodiments, selectively depositing the metal layer 270 comprises chemical vapor deposition (CVD). The selective deposition process provides a gapfill material comprising the metal layer 270 which is formed in a bottom-up fashion without lateral deposition from the sidewall 214. Advantageously, the substrate that is processed according to method 100 has fewer voids in the metal layer 270 and a smaller seam in the center than the substrate processed according to the prior art shown in FIGS. 1A–1C. In one or more embodiments, the metal layer 270 is deposited without forming any voids within the metal layer 270. Accordingly, the substrate that is processed according to method 100 has a lower volume of voids/seams in the metal layer 270 than the substrate processed according to the prior art shown in FIGS. 1A–1C.

[00101] The method 100 may end after operation 130 (selectively depositing the metal layer 270), or it may continue with optional post processing at optional operation 140. The optional post-processing operation 140 can be, for example, a process to modify film properties (e.g., annealing or plasma treatment), a further film deposition process (e.g., additional ALD or CVD processes) to grow additional films, or a further etch process to form a desired predetermined device architecture. In one or more embodiments, the optional post-processing operation 140 can be a process that modifies a property of the deposited film. In one or more embodiments, the optional post-processing operation 140 comprises annealing the device 200. In one or more embodiments, annealing is performed at a temperature greater than or equal to about 300 °C, greater than or equal to about 400 °C, greater than or equal to about 500 °C, greater than or equal to about 600 °C, greater than or equal to about 700 °C, greater than or equal to about 800 °C, greater than or equal to about 900 °C or greater than or equal to about 1000 °C. The annealing environment of one or more embodiments comprises one or more of an inert gas (e.g., molecular nitrogen (N₂), argon (Ar)) or a reducing gas (e.g., molecular hydrogen (H₂) or ammonia (NH₃)) or an oxidant, such as, but not limited to, oxygen (O₂), ozone (O₃), or peroxides. Annealing can be performed for any suitable length of time. In one or more embodiments, the substrate is annealed for a predetermined time in the range of about 15 seconds to about 90 minutes, or in the range of about 1 minute to about 60 minutes.

[00102] In one or more illustrated embodiments, like references indicate similar elements, unless specified otherwise. As noted herein, the disclosure relates to methods 100 and 300 of selective deposition of a gap fill material to fill a feature formed in a substrate. FIG. 2A illustrates a process flow diagram of a selective deposition
5 method 100 in accordance with one or more embodiments of the present disclosure. FIGS. 2B–2H depict a device 200 having a substrate surface with at least one feature formed therein during processing according to one or more embodiments of the present disclosure. FIG. 3A illustrates a process flow diagram of a selective deposition method 100 in accordance with one or more embodiments of the present disclosure. FIGS. 3B–
10 3K depict a device 1000 having a substrate surface with at least one feature formed therein during processing according to one or more embodiments of the present disclosure.

[00103] For example, some of the operations of method 300 include the same or similar elements as the operations of method 100. In one or more embodiments,
15 operation 105 of method 100 and operation 305 of method 300 include optionally pre-treating the semiconductor substrate. The cycle 110 of method 100 includes depositing a first metal liner by PVD (operation 112), forming a flowable polymer film (operation 114), selectively removing a portion of the first metal liner (operation 116), removing the polymer film (operation 118), and depositing a second metal liner by PVD (operation
20 119), as described elsewhere herein. The method 100 further includes decision point 120, selectively depositing a metal layer (operation 130), and optional post-processing operation 140.

[00104] The cycle 310 of method 300 includes depositing a first metal liner by PVD (operation 312), forming a flowable polymer film (operation 314), selectively removing
25 a portion of the first metal liner (operation 316), removing the polymer film (operation 318). In some embodiments, the cycle 310 corresponds to operation 112, operation 114, operation 116, and operation 118 of cycle 110 of method 100. In method 300, operation 319 includes repeating the cycle 310 at least once, whereas operation 119 of cycle 110 of method 100 includes depositing a second metal liner by PVD. The method
30 300 further includes decision point 320, selectively depositing a metal layer (operation 330), and optional post-processing operation 340. In some embodiments, decision point 320, selectively depositing a metal layer (operation 330), and optional post-processing

operation 340 are the same operations as decision point 120, selectively depositing a metal layer (operation 130), and optional post-processing operation 140 of method 100.

[00105] FIGS. 3B–3K depict a device 1000 having a substrate surface with at least one feature formed therein during processing according to one or more embodiments of the present disclosure. The device 1000 includes the same or similar elements as the device 200 manufactured by method 100, unless indicated otherwise. As an example, at least one feature 210 of device 200 corresponds to the at least one feature 1010 of device 1000.

[00106] The at least one feature 1010 has an opening 1012 with an opening width 1005. The opening 1012 is formed in a top surface 1015 of the device 1000. The feature 1010 also has one or more sidewall 1014 and extends a feature depth D from the top surface 1015 to a bottom 1016. The one or more sidewalls 1014 include an overhang or undercut 1030 near the top surface 1015 of the opening 1012. The overhang or undercut 1030 may have any suitable shape. Stated differently, the overhang or undercut 1030 may be any suitable shape such that the sidewall 1014 does not vertically extending from the top surface 1015 to the bottom 1016.

[00107] In one or more embodiments, the device 200 illustrated in FIGS. 2B–2H is comprised of a material 221 on a material 220 and the device 1000 illustrated in FIGS. 3B–3K is comprised of a material 1021 on a material 1020. In one or more embodiments, the material 220 and the material 221 of device 200 are the same as the material 1020 and the material 1021, respectively, of the device 1000. In one or more embodiments, the material 1020 comprises silicon nitride (SiN). In one or more embodiments, the material 1021 comprises silicon oxide (SiOx). In one or more embodiments, each of the material 1020 and the material 1021 comprises silicon nitride (SiN). In one or more embodiments, each of the material 1020 and the material 1021 comprises silicon oxide (SiOx).

[00108] In one or more embodiments, the opening width 1005 of the opening 1012 is less than or equal to about 50 nm, less than or equal to about 30 nm, less than or equal to about 20 nm, less than or equal to about 10 nm, or less than or equal to about 7 nm. In one or more embodiments, the opening width 1005 is in a range of about 8 nm to about 20 nm.

[00109] In one or more embodiments, the feature depth D of the feature 1010 is greater than or equal to about 5 nm, greater than or equal to about 10 nm, greater than or equal to about 20 nm, greater than or equal to about 50 nm, greater than or equal to about 60 nm, greater than or equal to about 75 nm, greater than or equal to about 100 nm, greater than or equal to about 200 nm, greater than or equal to about 300 nm, greater than or equal to about 400 nm, or greater than or equal to about 450 nm. In one or more embodiments, the feature depth D is in a range of about 5 nm to about 500 nm. In one or more embodiments, the feature depth D is in a range of about 10 nm to about 300 nm. In one or more embodiments, the feature depth D is in a range of about 60 nm to about 100 nm.

[00110] It has been advantageously found that repeating the cycle 310 at operation 319 provides for improved bottom-up gap fill depth. More particularly, a metal layer 1080 advantageously fills the depth D of the feature 1010 with no voids or seams by repeating the cycle 310 at least once.

[00111] Advantageously, the substrate that is processed according to method 100 has fewer voids in the metal layer 270 and a smaller seam in the center than the substrate processed according to the prior art shown in FIGS. 1A–1C. Stated differently, the substrate that is processed according to method 100 has a lower volume of voids/seams in the metal layer 270 than the substrate processed according to the prior art shown in FIGS. 1A–1C. Advantageously, the substrate that is processed according to method 300 has no voids or seams in the metal layer 1080.

[00112] FIG. 4 illustrates a schematic top-view diagram of an example of a multi-chamber processing system 400 according to embodiments of the present disclosure. The processing system 400 generally includes a factory interface 402, load lock chambers 404, 406, transfer chambers 408, 410 with respective transfer robots 412, 414, holding chambers 416, 418, and processing chambers 420, 422, 424, 426, 428, 430. As detailed herein, wafers in the processing system 400 can be processed in and transferred between the various chambers without exposing the wafers to an ambient environment exterior to the processing system 400 (e.g., an atmospheric ambient environment such as may be present in a fab). For example, the wafers can be processed in and transferred between the various chambers in a low pressure (e.g., less than or equal to about 300 Torr) or vacuum environment without breaking the low

pressure or vacuum environment between various processes performed on the wafers in the processing system 400. Accordingly, the processing system 400 may provide for an integrated solution for some processing of wafers.

[00113] Examples of a processing system that may be suitably modified in accordance with the teachings provided herein include the Endura®, Producer® or Centura® integrated processing systems or other suitable processing systems commercially available from Applied Materials, Inc., located in Santa Clara, California. It is contemplated that other processing systems (including those from other manufacturers) may be adapted to benefit from aspects described herein.

10 [00114] In the illustrated example of FIG. 4, the factory interface 402 includes a docking station 440 and factory interface robots 442 to facilitate transfer of wafers. The docking station 440 is configured to accept one or more front opening unified pods (FOUPs) 444. In some examples, each factory interface robot 442 generally comprises a blade 448 disposed on one end of the respective factory interface robot 442

15 configured to transfer the wafers from the factory interface 402 to the load lock chambers 404, 406.

[00115] The load lock chambers 404, 406 have respective ports 450, 452 coupled to the factory interface 402 and respective ports 454, 456 coupled to the transfer chamber 408. The transfer chamber 408 further has respective ports 458, 460 coupled to the

20 holding chambers 416, 418 and respective ports 462, 464 coupled to processing chambers 420, 422. Similarly, the transfer chamber 410 has respective ports 466, 468 coupled to the holding chambers 416, 418 and respective ports 470, 472, 474, 476 coupled to processing chambers 424, 426, 428, 430. The ports 454, 456, 458, 460, 462, 464, 466, 468, 470, 472, 474, 476 can be, for example, slit valve openings with slit

25 valves for passing wafers therethrough by the transfer robots 412, 414 and for providing a seal between respective chambers to prevent a gas from passing between the respective chambers. Generally, any port is open for transferring a wafer therethrough. Otherwise, the port is closed.

[00116] The load lock chambers 404, 406, transfer chambers 408, 410, holding

30 chambers 416, 418, and processing chambers 420, 422, 424, 426, 428, 430 may be fluidly coupled to a gas and pressure control system (not specifically illustrated). The gas and pressure control system can include one or more gas pumps (e.g., turbo

pumps, cryo-pumps, roughing pumps), gas sources, various valves, and conduits fluidly coupled to the various chambers. In operation, a factory interface robot 442 transfers a wafer from a FOUP 444 through a port 450 or 452 to a load lock chamber 404 or 406. The gas and pressure control system then pumps down the load lock chamber 404 or 406. The gas and pressure control system further maintains the transfer chambers 408, 410 and holding chambers 416, 418 with an interior low pressure or vacuum environment (which may include an inert gas). Hence, the pumping down of the load lock chamber 404 or 406 facilitates passing the wafer between, for example, the atmospheric environment of the factory interface 402 and the low pressure or vacuum environment of the transfer chamber 408.

[00117] With the wafer in the load lock chamber 404 or 406 that has been pumped down, the transfer robot 412 transfers the wafer from the load lock chamber 404 or 406 into the transfer chamber 408 through the port 454 or 456. The transfer robot 412 is then capable of transferring the wafer to and/or between any of the processing chambers 420, 422 through the respective ports 462, 464 for processing and the holding chambers 416, 418 through the respective ports 458, 460 for holding to await further transfer. Similarly, the transfer robot 414 is capable of accessing the wafer in the holding chamber 416 or 418 through the port 466 or 468 and is capable of transferring the wafer to and/or between any of the processing chambers 424, 426, 428, 430 through the respective ports 470, 472, 474, 476 for processing and the holding chambers 416, 418 through the respective ports 466, 468 for holding to await further transfer. The transfer and holding of the wafer within and among the various chambers can be in the low pressure or vacuum environment provided by the gas and pressure control system.

[00118] The processing chambers 420, 422, 424, 426, 428, 430 can be any appropriate chamber for processing a wafer. In some embodiments, the processing chamber 420 can be capable of performing an annealing process, the processing chamber 422 can be capable of performing a cleaning process, and the processing chambers 424, 426, 428, 430 can be capable of performing epitaxial growth processes. In some examples, the processing chamber 422 can be capable of performing a cleaning process, the processing chamber 420 can be capable of performing an etch process, and the processing chambers 424, 426, 428, 430 can be capable of performing respective epitaxial growth processes. The processing chamber 422 may be a SiCoNi™

Preclean chamber available from Applied Materials of Santa Clara, Calif. The processing chamber 420 may be a Selectra™ Etch chamber available from Applied Materials of Santa Clara, Calif. The processing chamber 422 may be a Volta® CVD/ALD chamber available from Applied Materials of Santa Clara, Calif.

5 [00119] A system controller 490 is coupled to the processing system 400 for controlling the processing system 400 or components thereof. For example, the system controller 490 may control the operation of the processing system 400 using a direct control of the chambers 404, 406, 408, 416, 418, 410, 420, 422, 424, 426, 428, 430 of the processing system 400 or by controlling controllers associated with the chambers 404, 406, 408,
10 416, 418, 410, 420, 422, 424, 426, 428, 430. In operation, the system controller 490 enables data collection and feedback from the respective chambers to coordinate performance of the processing system 400.

[00120] The system controller 490 generally includes a central processing unit (CPU) 492, memory 494, and support circuits 496. The CPU 492 may be one of any form of a
15 general-purpose processor that can be used in an industrial setting. The memory 494, or non-transitory computer-readable medium, is accessible by the CPU 492 and may be one or more of memory such as random-access memory (RAM), read only memory (ROM), floppy disk, hard disk, or any other form of digital storage, local or remote. The support circuits 496 are coupled to the CPU 492 and may comprise cache, clock circuits,
20 input/output subsystems, power supplies, and the like. The various methods disclosed herein may generally be implemented under the control of the CPU 492 by the CPU 492 executing computer instruction code stored in the memory 494 (or in memory of a particular process chamber) as, for example, a software routine. When the computer instruction code is executed by the CPU 492, the CPU 492 controls the chambers to
25 perform processes in accordance with the various methods.

[00121] Other processing systems can be in other configurations. For example, more or fewer processing chambers may be coupled to a transfer apparatus. In the illustrated example, the transfer apparatus includes the transfer chambers 408, 410 and the holding chambers 416, 418. In other examples, more or fewer transfer chambers (*e.g.*,
30 one transfer chamber) and/or more or fewer holding chambers (*e.g.*, no holding chambers) may be implemented as a transfer apparatus in a processing system.

[00122] Processes may generally be stored in the memory of the system controller 1190 as a software routine that, when executed by the processor, causes the process chamber to perform processes of the present disclosure. The software routine may also be stored and/or executed by a second processor (not shown) that is remotely located
5 from the hardware being controlled by the processor. Some or all of the methods of the present disclosure may also be performed in hardware. As such, the process may be implemented in software and executed using a computer system, in hardware as, e.g., an application specific integrated circuit or other type of hardware implementation, or as a combination of software and hardware. The software routine, when executed by the
10 processor, transforms the general-purpose computer into a specific purpose computer (controller) that controls the chamber operation such that the processes are performed.

[00123] Embodiments of the disclosure are directed to a non-transitory computer readable medium. In one or more embodiments, the non-transitory computer readable medium includes instructions that, when executed by a controller of a processing
15 chamber, causes a processing chamber to perform the operations of any of the methods (e.g., method 100 and/or method 300) described herein.

[00124] Spatially relative terms, such as "beneath," "below," "lower," "above," "upper," "near," and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures.
20 It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below," or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" may encompass both an
25 orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[00125] The use of the terms "a" and "an" and "the" and similar referents in the context of describing the materials and methods discussed herein (especially in the context of
30 the following claims) are to be construed to cover both the singular and the plural, unless otherwise indicated herein or clearly contradicted by context. Recitation of ranges of values herein are merely intended to serve as a shorthand method of referring

individually to each separate value falling within the range, unless otherwise indicated herein, and each separate value is incorporated into the specification as if it were individually recited herein. All methods described herein can be performed in any suitable order unless otherwise indicated herein or otherwise clearly contradicted by context. The use of any and all examples, or exemplary language (e.g., "such as")
5 provided herein, is intended merely to better illuminate the materials and methods and does not pose a limitation on the scope unless otherwise claimed. No language in the specification should be construed as indicating any non-claimed element as essential to the practice of the disclosed materials and methods.

10 **[00126]** Reference throughout this specification to "one embodiment," "certain embodiments," "one or more embodiments" or "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in at least one embodiment of the disclosure. Thus, the appearances of the phrases such as "in one or more embodiments," "in certain
15 embodiments," "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the disclosure. In one or more embodiments, the particular features, structures, materials, or characteristics are combined in any suitable manner.

[00127] Although the disclosure herein has been described with reference to particular
20 embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present disclosure. It will be apparent to those skilled in the art that various modifications and variations can be made to the method and apparatus of the present disclosure without departing from the spirit and scope of the disclosure. Thus, it is intended that the present disclosure include modifications and
25 variations that are within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method of manufacturing a semiconductor device, the method comprising:
depositing a first metal liner by physical vapor deposition (PVD) on a
5 semiconductor substrate surface with at least one feature formed thereon, the at
least one feature having at least one opening at a top surface with an opening
width, at least one sidewall, and a bottom, the at least one feature extending a
feature depth from the top surface to the bottom, the first metal liner forming on
the top surface, on the at least one sidewall, and on the bottom;
10 forming a first flowable polymer film on the first metal liner within the at
least one feature, the first flowable polymer film forming on the first metal liner
on the bottom and having a polymer depth less than the feature depth;
selectively removing at least a portion of the first metal liner from the top
surface and the at least one sidewall;
15 removing the first flowable polymer film to expose the first metal liner on
the bottom of the at least one feature;
depositing a second metal liner by physical vapor deposition (PVD) on the
top surface of the at least one feature, and on the remaining portion of the first
metal liner on the at least one sidewall and on the bottom; and
20 selectively depositing a metal layer on the first metal liner and the second
metal liner to fill the at least one feature.
2. The method of claim 1, wherein the at least one feature comprises an overhang
or an undercut within the opening width.
- 25 3. The method of claim 1, wherein the first metal liner comprises one or more of
tungsten (W), molybdenum (Mo), ruthenium (Ru), or cobalt (Co).
4. The method of claim 1, wherein the second metal liner comprises one or more
30 of tungsten (W), molybdenum (Mo), ruthenium (Ru), or cobalt (Co).

5. The method of claim 4, wherein the first metal liner and the second metal liner are the same.
6. The method of claim 1, comprising forming the first flowable polymer film at a temperature in a range of from 30 °C to 400 °C.
7. The method of claim 1, wherein forming the first flowable polymer film comprises exposing the semiconductor substrate surface to one or more monomers.
8. The method of claim 1, comprising selectively removing the portion of the first metal liner at a temperature in a range of from 100 °C to 400 °C.
9. The method of claim 8, wherein selectively removing the portion of the first metal liner comprises exposing the semiconductor substrate surface to a fluorine-based plasma or a chlorine-based plasma.
10. The method of claim 1, wherein the first flowable polymer film is removed without substantially affecting any material beneath the first flowable polymer film.
11. The method of claim 1, wherein removing the first flowable polymer film comprises exposing the semiconductor substrate surface to one or more of a thermal process or a hydrogen (H₂) plasma treatment.
12. The method of claim 1, comprising repeating the operations of: depositing a first metal liner by PVD, forming a first flowable polymer film on the first metal liner, selectively removing at least a portion of the first metal liner from the top surface and the at least one sidewall, and removing the first flowable polymer film.
13. The method of claim 1, further comprising forming a second flowable polymer film on the second metal liner, selectively removing at least a portion of the second metal liner from the top surface and the at least one sidewall, and removing the second flowable polymer film.

14. The method of claim 13, further comprising selectively depositing a metal layer on the first metal liner and the second metal liner to fill the at least one feature.
- 5 15. The method of claim 1, wherein the feature depth is in a range of about 10 nm to about 300 nm.
16. The method of claim 14, wherein the feature depth is in a range of about 60 nm to about 100 nm.
- 10 17. The method of claim 1, wherein the polymer depth is in a range of about 1 nm to about 50 nm.
18. A method of manufacturing a semiconductor device, the method comprising:
- 15 depositing a first metal liner comprising tungsten (W) by physical vapor deposition (PVD) on a semiconductor substrate surface with at least one feature formed thereon, the at least one feature having at least one opening at a top surface with an opening width, at least one sidewall, and a bottom, the at least one feature comprising an overhang or an undercut within the opening width, the
- 20 at least one feature extending a feature depth from the top surface to the bottom, the first metal liner forming on the top surface, on the overhang or the undercut, on the at least one sidewall, and on the bottom;
- forming a first flowable polymer film on the first metal liner within the at least one feature, the first flowable polymer film forming on the first metal liner
- 25 on the bottom and having a polymer depth less than or equal to the feature depth;
- selectively removing at least a portion of the first metal liner from the top surface and the at least one sidewall;
- removing the first flowable polymer film to expose the first metal liner on the bottom of the at least one feature;
- 30 depositing a second metal liner comprising tungsten (W) by physical vapor deposition (PVD) on the top surface of the at least one feature, on the overhang or the undercut, and on the remaining portion of the first metal liner on the at least one sidewall and on the bottom; and

selectively depositing a metal layer on the first metal liner and the second metal liner to fill the at least one feature.

19. The method of claim 18, further comprising forming a second flowable polymer
5 film on the second metal liner, selectively removing at least a portion of the second metal liner from the top surface and the at least one sidewall, and removing the second flowable polymer film prior to selectively depositing the metal layer on the first metal liner and the second metal liner.
- 10 20. The method of claim 19, wherein the metal layer on the first metal liner and the second metal liner is free of seams or voids.

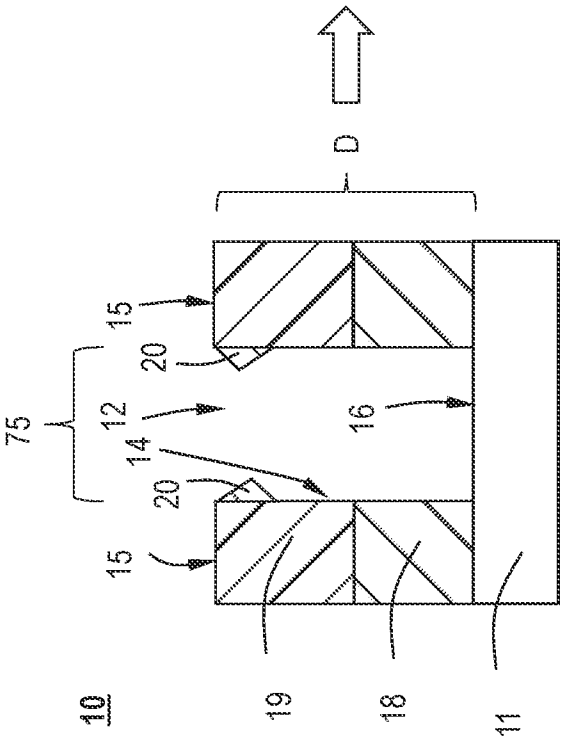


FIG. 1A
Prior Art

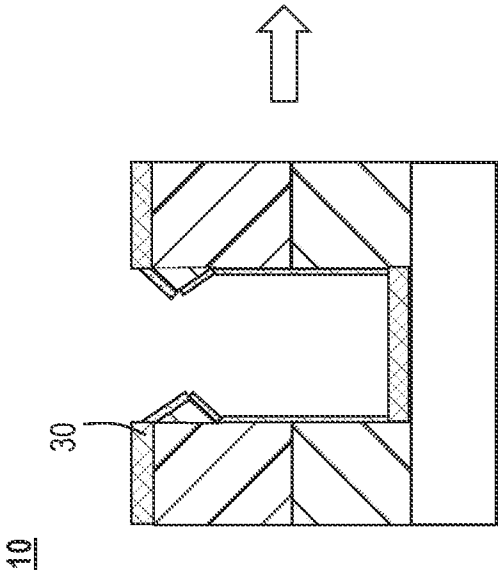


FIG. 1B
Prior Art

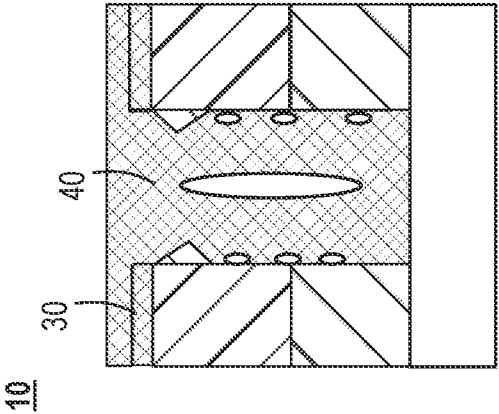


FIG. 1C
Prior Art

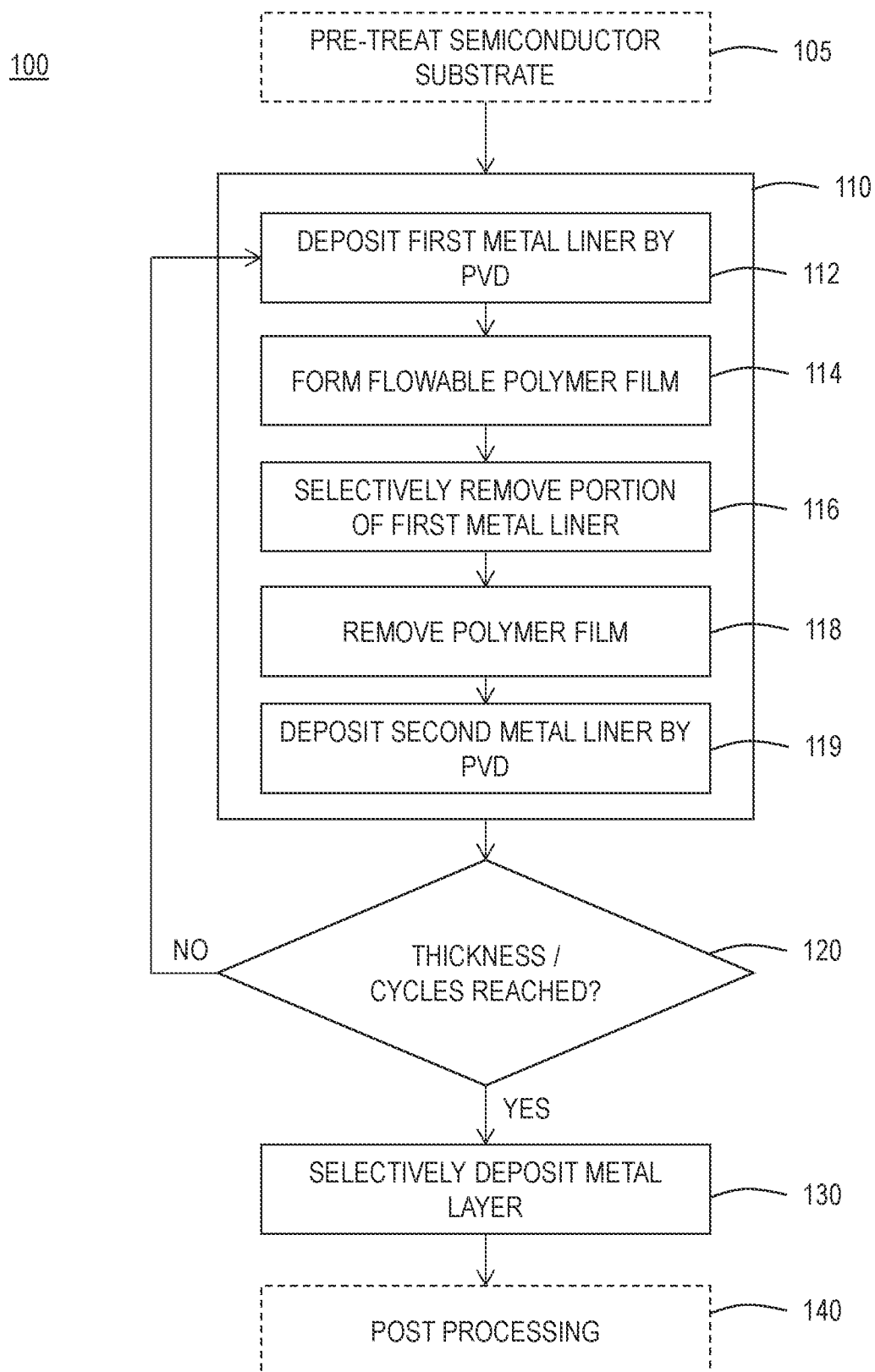


FIG. 2A

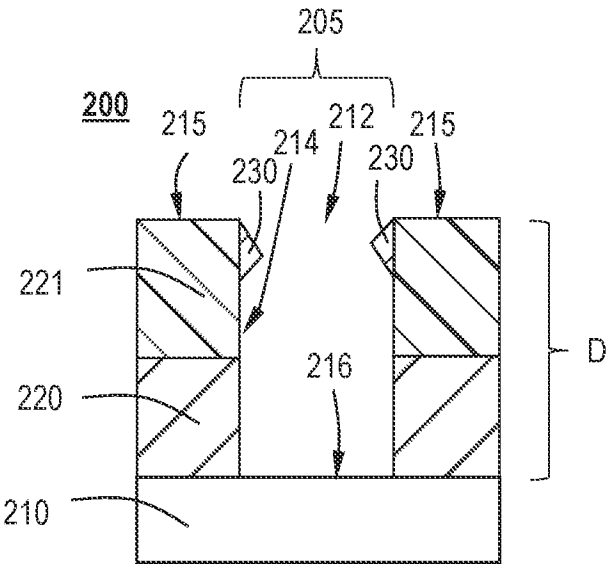


FIG. 2B

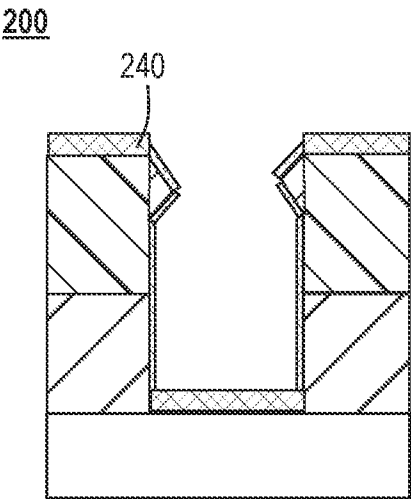
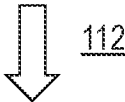


FIG. 2C

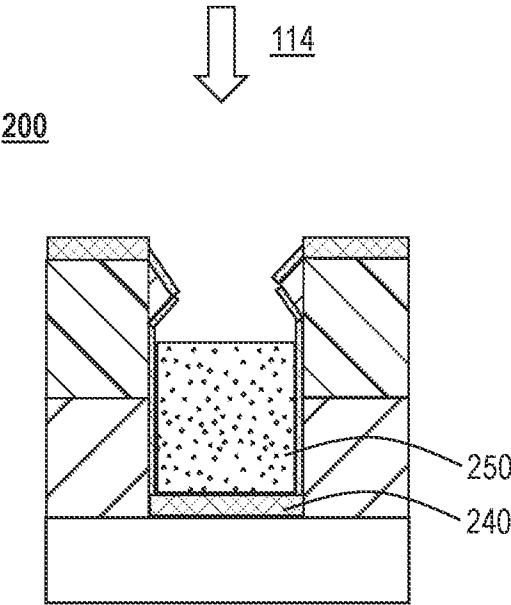


FIG. 2D

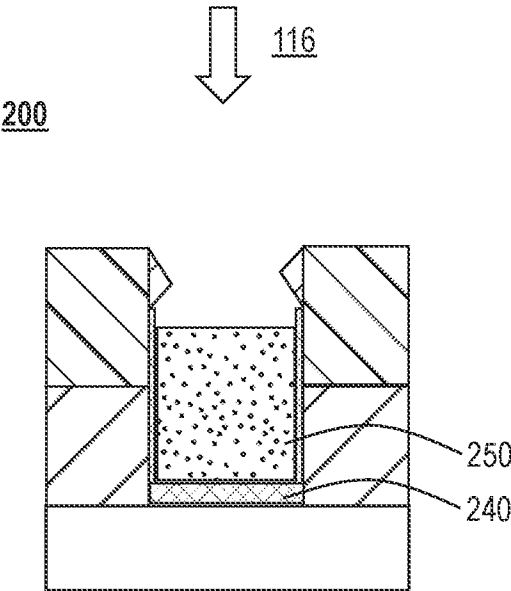


FIG. 2E

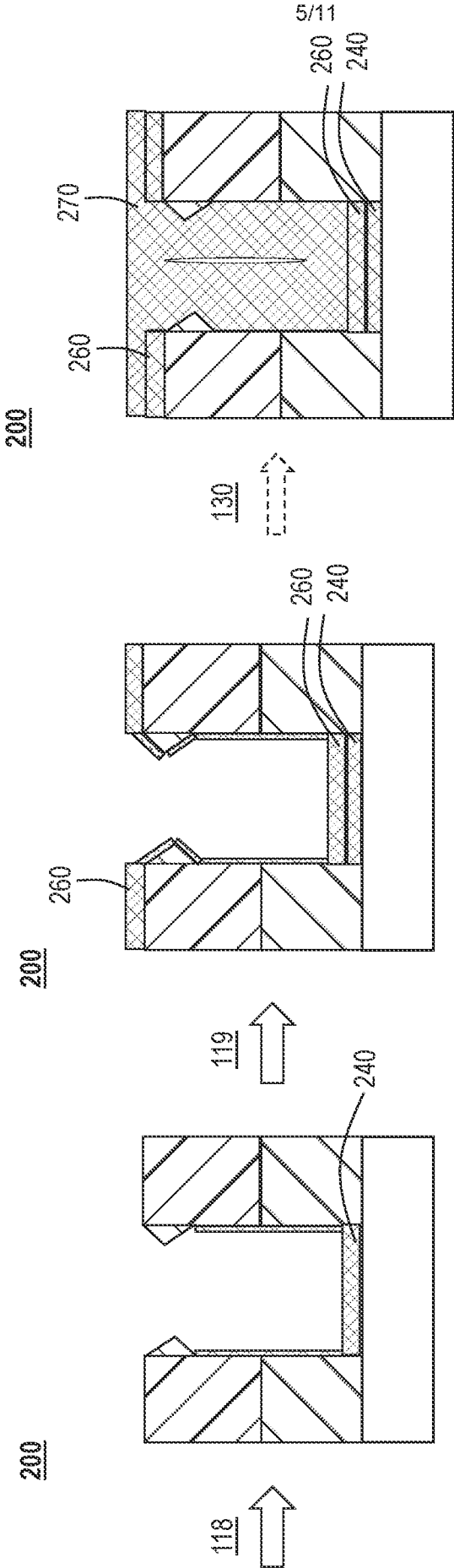


FIG. 2F

FIG. 2G

FIG. 2H

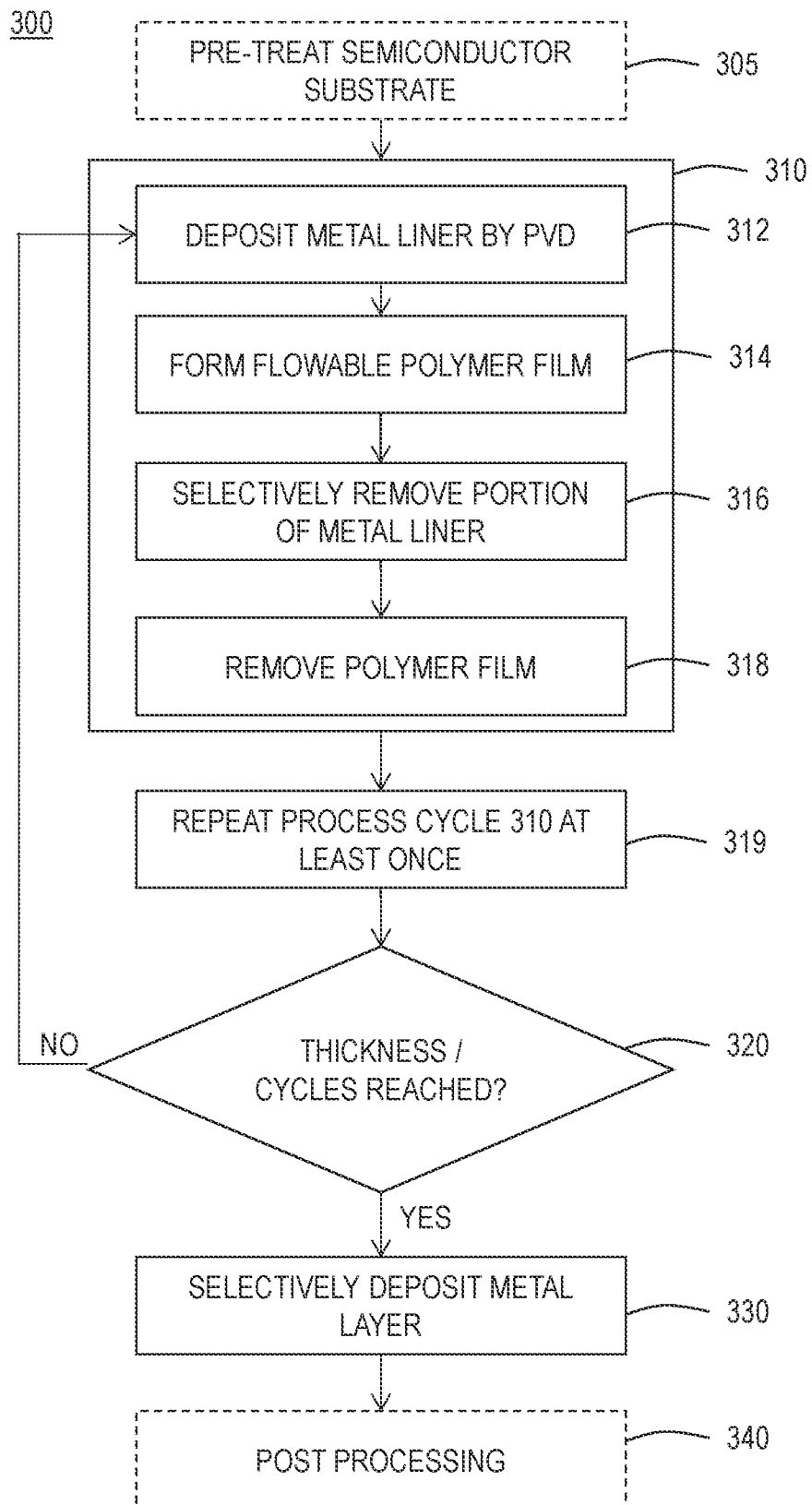


FIG. 3A

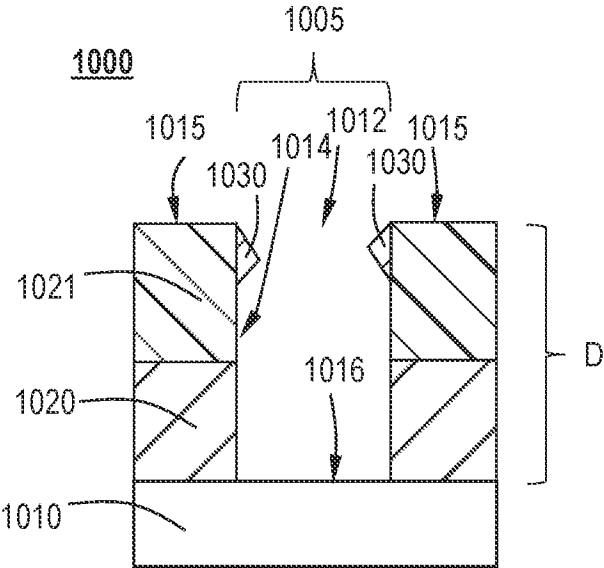


FIG. 3B

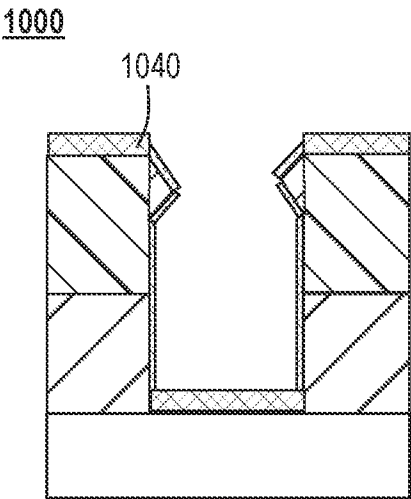
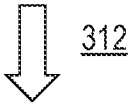


FIG. 3C

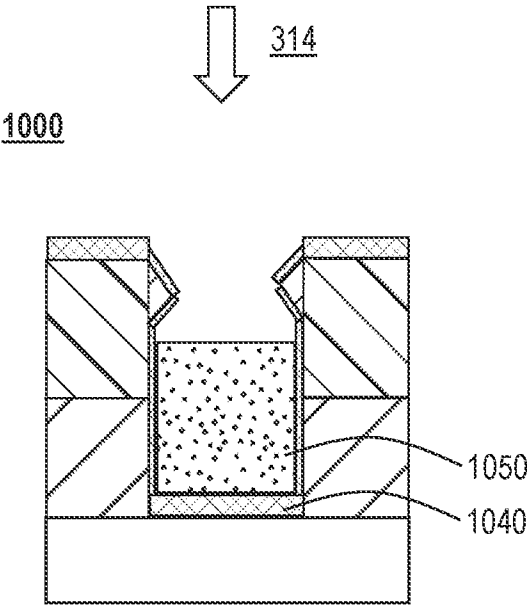


FIG. 3D

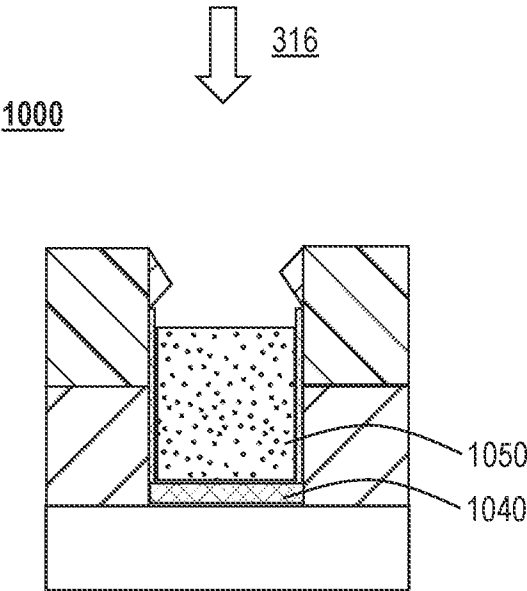


FIG. 3E

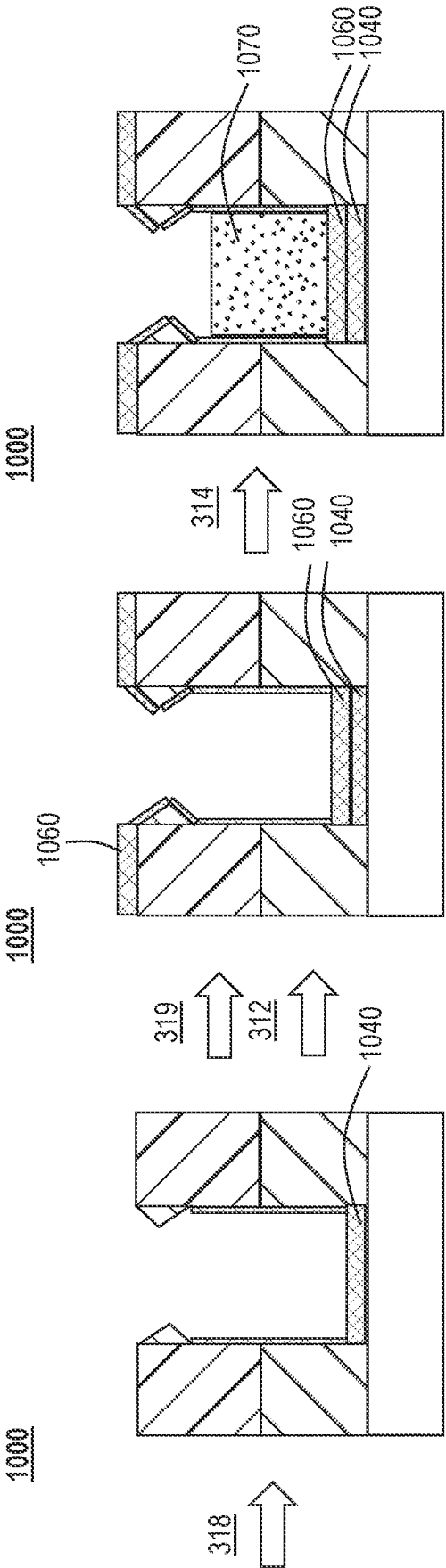


FIG. 3H

FIG. 3G

FIG. 3F

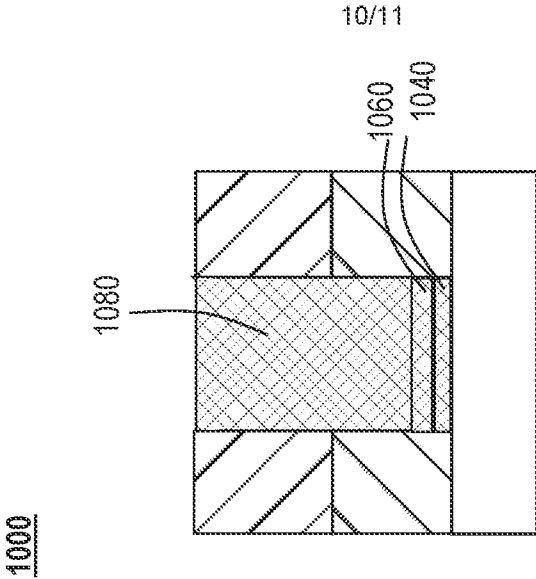


FIG. 3I

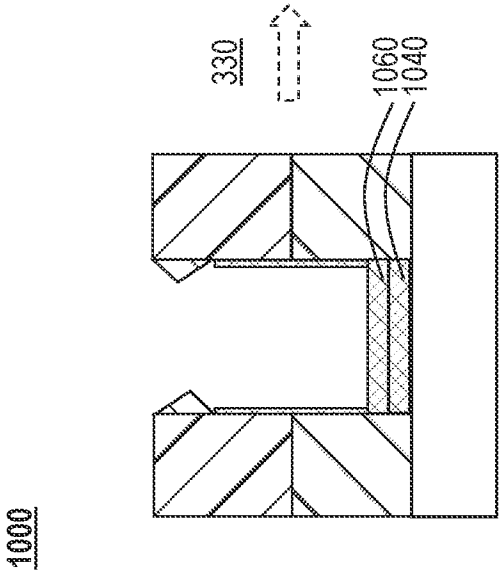


FIG. 3J

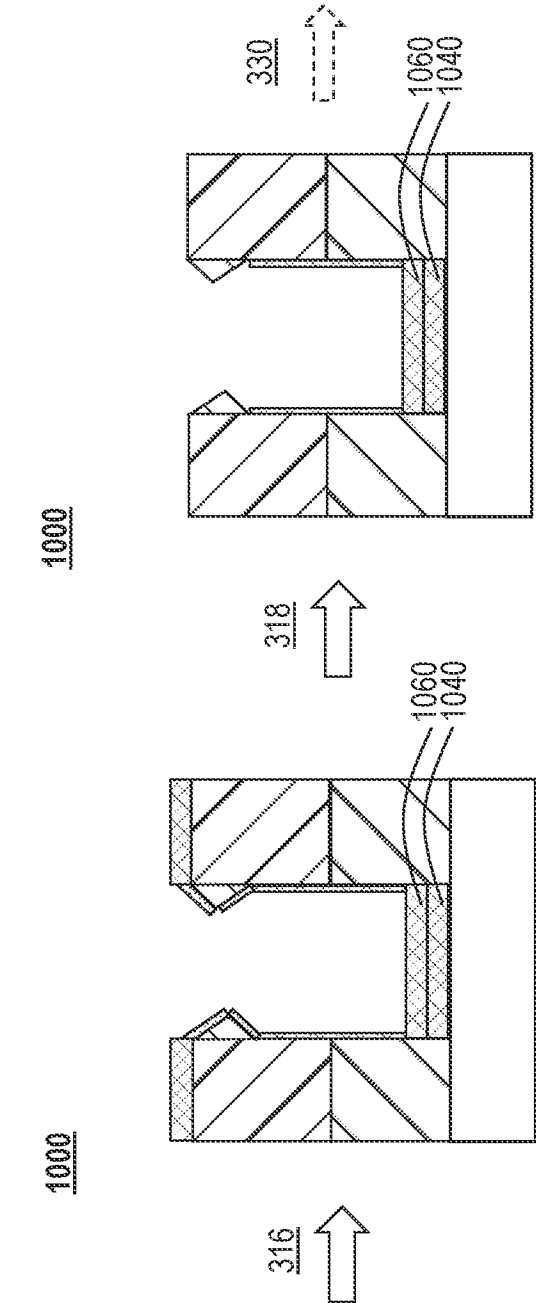


FIG. 3K

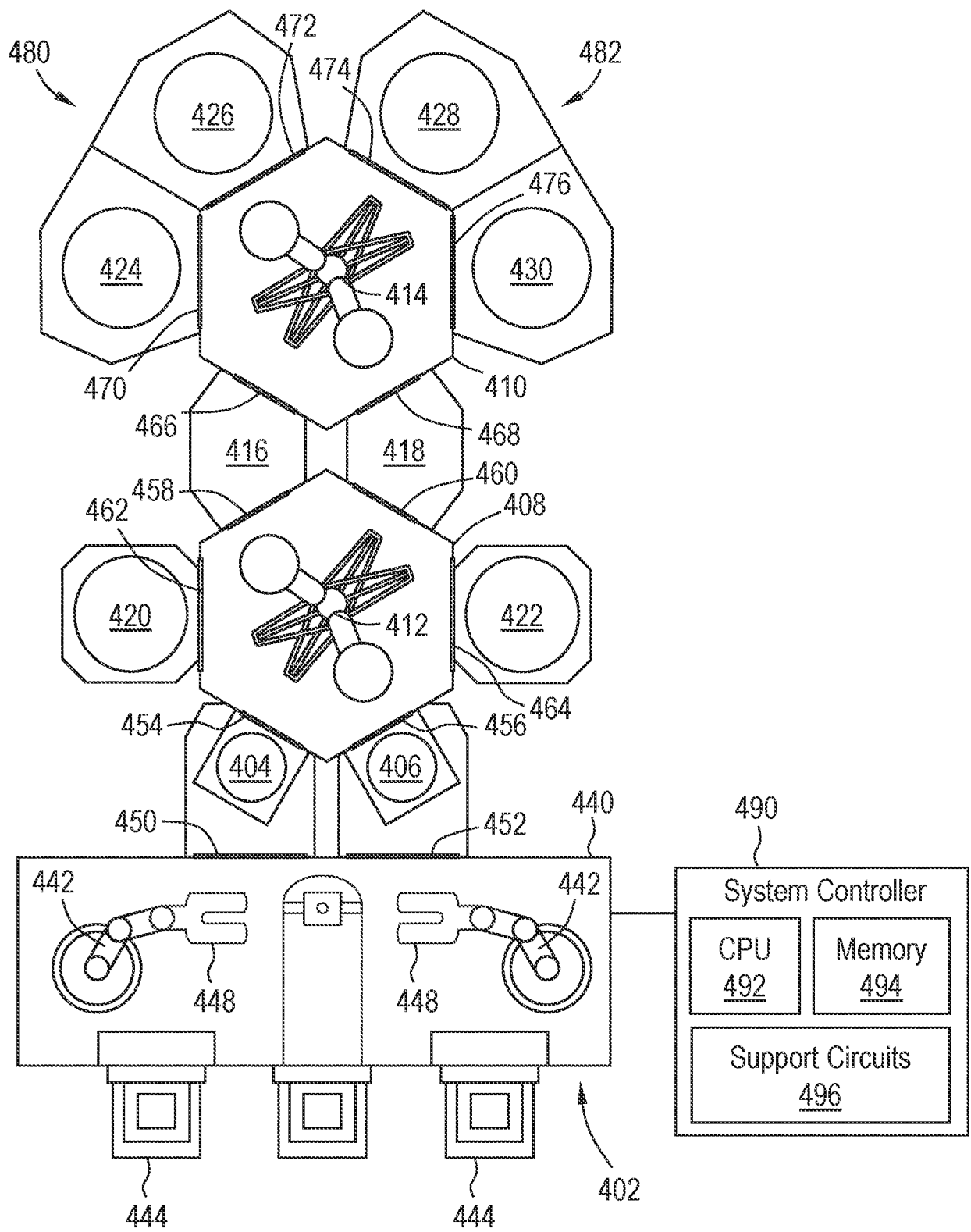
400

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2024/035186

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/285**(2006.01)i; **H01L 21/768**(2006.01)i; **H01L 21/02**(2006.01)i; **H01L 21/67**(2006.01)i; **H01L 21/677**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/285(2006.01); H01L 21/56(2006.01); H01L 21/768(2006.01); H01L 23/00(2006.01); H01L 23/522(2006.01);
H01L 23/532(2006.01); H01L 27/115(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: metal liner, flowable polymer film, metal layer, overhang, undercut

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2021-0305090 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 30 September 2021 (2021-09-30) paragraphs [0005]-[0042] and figure 11	1-20
Y	US 2009-0140429 A1 (KYU-HA LEE et al.) 04 June 2009 (2009-06-04) paragraph [0030]	1-20
Y	US 2016-0093528 A1 (LAM RESEARCH CORPORATION) 31 March 2016 (2016-03-31) paragraph [0056] and figure 1B	2,18-20
Y	US 2019-0006301 A1 (IMEC VZW) 03 January 2019 (2019-01-03) paragraph [0032]	6,8,9
A	KR 10-1579352 B1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 21 December 2015 (2015-12-21) paragraphs [0007]-[0029]	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“D” document cited by the applicant in the international application

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

10 October 2024

Date of mailing of the international search report

10 October 2024

Name and mailing address of the ISA/KR

**Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon
35208, Republic of Korea**

Facsimile No. +82-42-481-8578

Authorized officer

LEE, Kang Ha

Telephone No. +82-42-481-5687

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/US2024/035186

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)		Publication date (day/month/year)
US	2021-0305090	A1	30 September 2021	US	11244854 B2	08 February 2022
US	2009-0140429	A1	04 June 2009	KR	10-1406276 B1	27 June 2014
				KR	10-2009-0056045 A	03 June 2009
				US	7960273 B2	14 June 2011
US	2016-0093528	A1	31 March 2016	CN	105470194 A	06 April 2016
				CN	105470194 B	06 September 2019
				CN	110459503 A	15 November 2019
				CN	110459503 B	16 April 2024
				KR	10-2016-0039139 A	08 April 2016
				TW	I712107 B	01 December 2020
				US	10580695 B2	03 March 2020
				US	11901227 B2	13 February 2024
				US	2018-0277431 A1	27 September 2018
				US	2020-0185273 A1	11 June 2020
				US	2022-0102208 A1	31 March 2022
				US	9997405 B2	12 June 2018
US	2019-0006301	A1	03 January 2019	EP	3422395 A1	02 January 2019
				EP	3422395 B1	08 June 2022
				US	10418339 B2	17 September 2019
KR	10-1579352	B1	21 December 2015	KR	10-2014-0112370 A	23 September 2014
				US	2014-0264873 A1	18 September 2014
				US	2015-0311152 A1	29 October 2015
				US	9076729 B2	07 July 2015
				US	9287212 B2	15 March 2016