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GB 1531951
GB 1401281
GB 1376358
GB 1330184
GB 1260113
(58) Field of search
E2A
(71) Applicant
David Neil Sweetman, 48

(54) An Electronic Locking System

(57) An electronic locking system includes a lock and a key designed so that on inserting the key into the lock, the lock transmits to the key a lock code. The key receives this lock code and transmits to the lock a key actuating code. The lock then samples this key actuating code and is actuated only if the key actuating code is correct.

In a preferred system, it is not necessary to insert the key into the lock in order to transmit a lock code to the key. The lock and the key are operable so that the key transmits to the lock a starting code, and the lock samples the key starting code and transmits to the key a lock code only if the key starting code is correct. The key samples this lock code and transmits to the lock a key actuating code only if the lock code is correct. The lock then samples the key actuating code and is actuated only if the key actuating code is correct. The codes may be in various forms such as, for example electronic, sonic, ultrasonic or light pulses.

ERRATUM

SPECIFICATION NO 2024914A

Page 5, line 59, *after* drawings. *Start new paragraph insert*

Amendments to claim 1 filed on 17 Sept. 1979

New or amended claims:—

1. An electronic locking system comprises a lock and a key which are operable so that on inserting the key into the lock, the lock transmits to the key a digital lock code, the key receives the lock code, and transmits to the lock a key actuating code, and the lock samples the key actuating code and is actuated only if the key actuating code is correct.

THE PATENT OFFICE
18 February 1981

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(71) Applicant
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Urquhart-Dykes & Lord

(54) An Electronic Locking System

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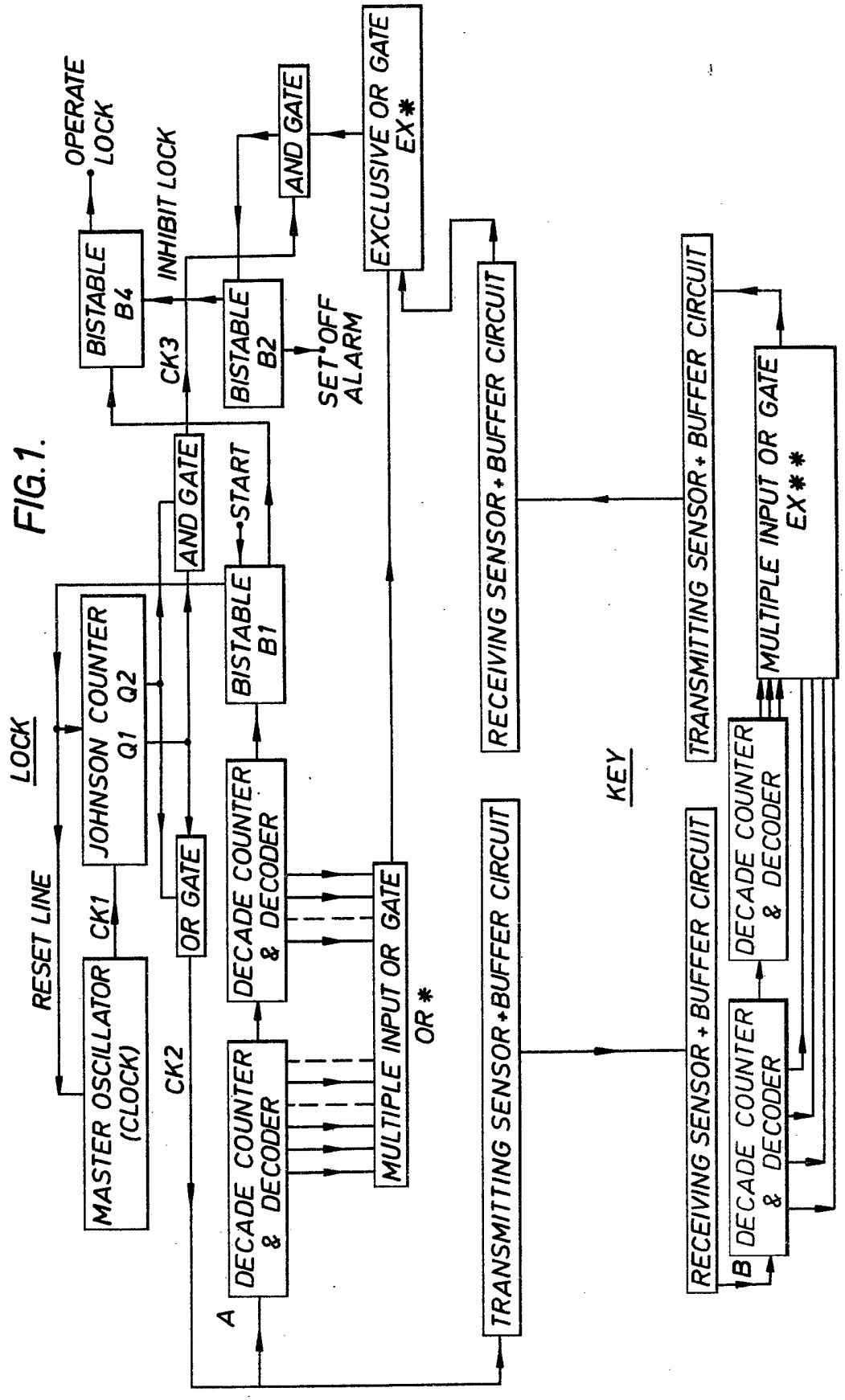
GB 2 024 914A

FIG.1.


LOCK
RESET LINE
MASTER OSCILLATOR (CLOCK)
CK1
JOHNSON COUNTER Q1 Q2
CK2
OR GATE
AND GATE
START
BISTABLE B1
CK3
INHIBIT LOCK
BISTABLE B4
OPERATE LOCK
BISTABLE B2
SET OFF ALARM
AND GATE
EXCLUSIVE OR GATE EX*
DECADE COUNTER & DECODER
A
DECADE COUNTER & DECODER
MULTIPLE INPUT OR GATE
OR *
RECEIVING SENSOR + BUFFER CIRCUIT
TRANSMITTING SENSOR + BUFFER CIRCUIT
KEY
TRANSMITTING SENSOR + BUFFER CIRCUIT
MULTIPLE INPUT OR GATE EX**
RECEIVING SENSOR + BUFFER CIRCUIT
DECADE COUNTER & DECODER
B
DECADE COUNTER & DECODER

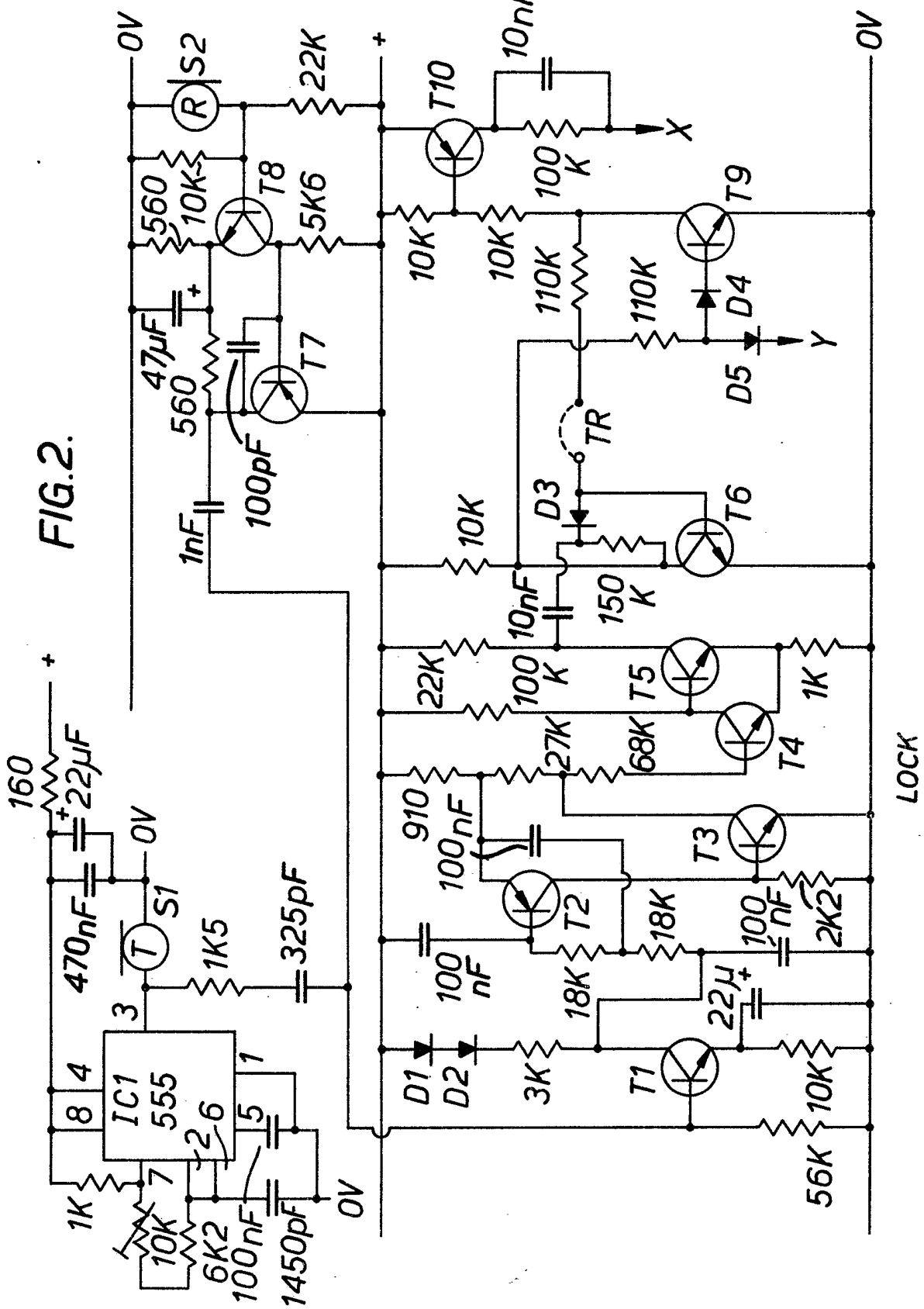

0V
S2
22K
+
10nF
T10
X
100 K
560
10K
T8
5K6
10K
10K
110K
110K
T9
D4
47µF
T7
560
100pF
D5
Y
TR
1nF
D3
T6
10K
10nF
150 K
22K
100 K
T5
1K
T4
27K
68K
910
100nF
T3
160
22µF
0V
S1
T2
18K
100 nF
2K2
470nF
1K5
325pF
100 nF
18K
22µ
3
IC1
555
4
8
1
2
6
5
7
D1
D2
3K
T1
10K
1K
10K
6K2
100nF
1450pF
0V
56K
LOCK

FIG.2.

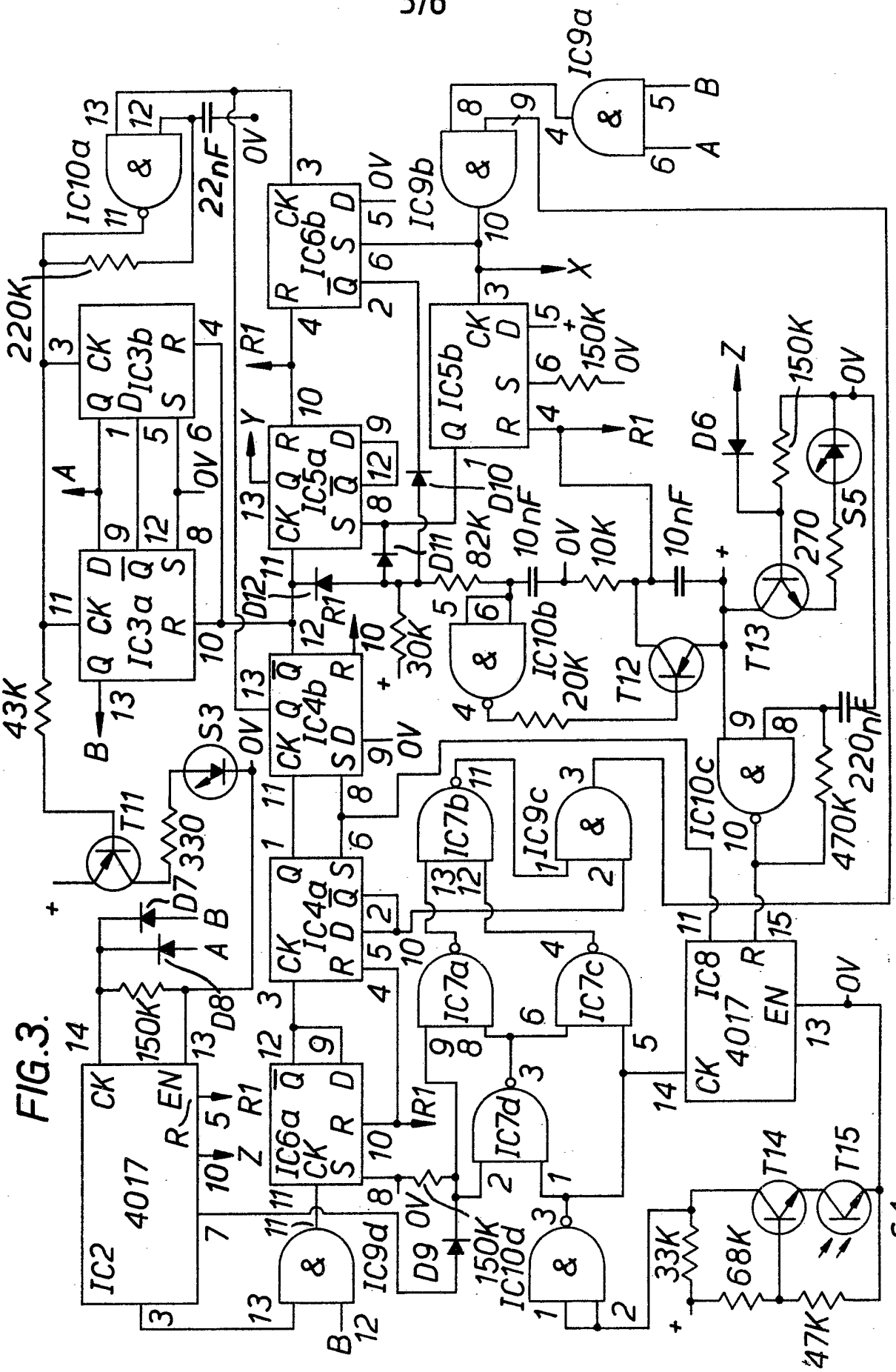

IC10a
IC9a
IC9b
IC6b
IC3b
IC5b
IC5a
IC3a
IC4b
IC4a
IC6a
IC10b
IC7b
IC9c
IC10c
IC7a
IC7c
IC7d
IC8
IC2
4017
IC9d
IC10d
220K
22nF
0V
R1
X
Y
Z
150K
10nF
82K
10K
20K
30K
43K
330
270
470K
220nF
LOCK
T11
T12
T13
T14
T15
S3
S4
S5
D6
D7
D8
D9
D10
D11
D12
A
B
33K
68K
47K

FIG.3.

FIG.4.

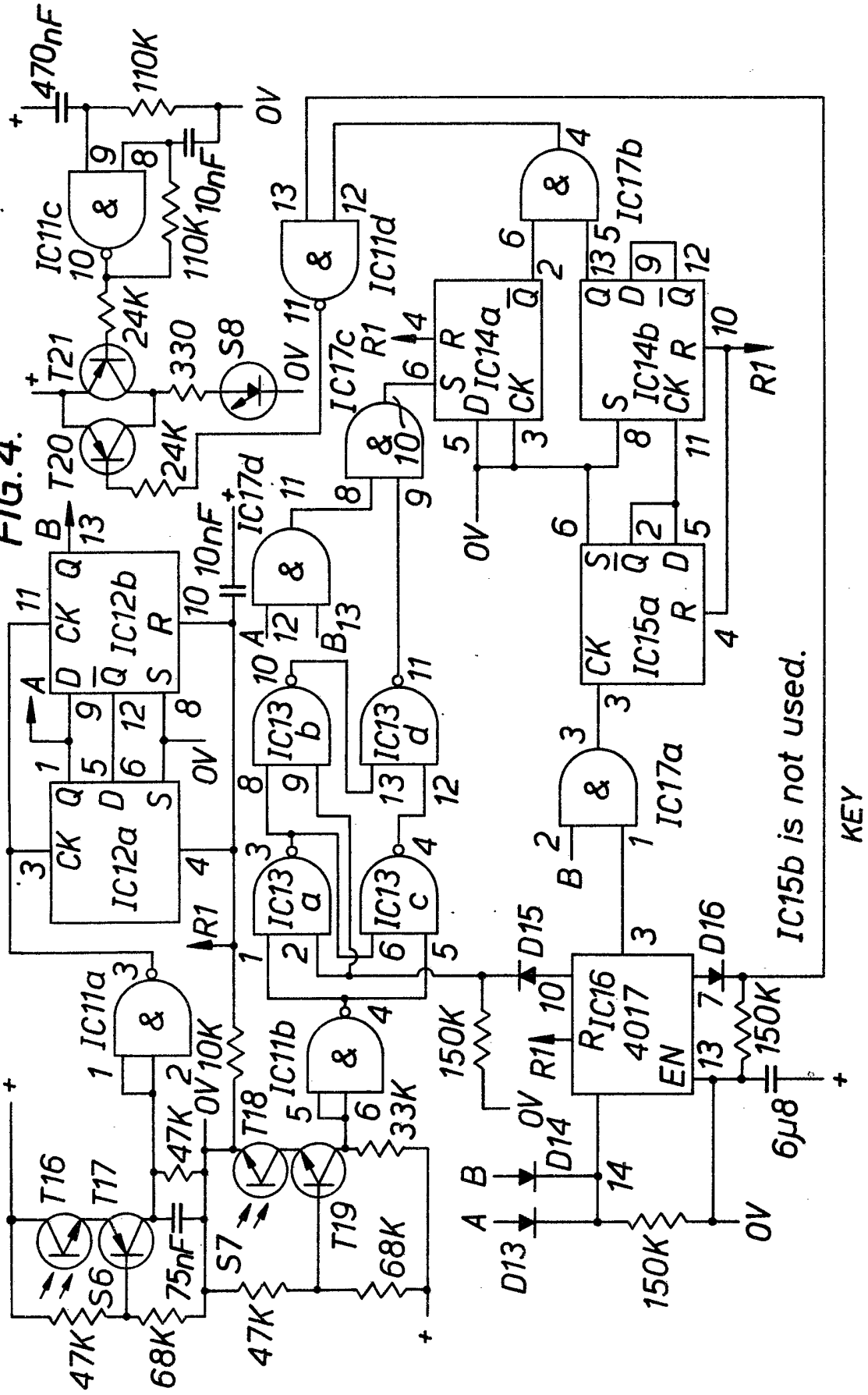
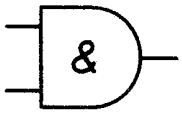
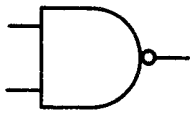

470nF
110K
0V
IC11c
10nF
24K
T21
330
S8
T20
IC11d
IC17c
IC17b
IC14a
IC14b
IC12b
IC12a
IC15a
IC13 a
IC13 b
IC13 c
IC13 d
IC11a
IC11b
IC17a
IC17d
R1
D15
D16
D14
D13
IC16 4017
150K
10K
47K
68K
33K
75nF
S6
S7
T16
T17
T18
T19
6µ8
IC15b is not used.
KEY

FIG.5.

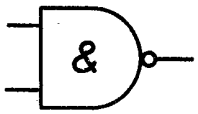
This is a CD4017 CMOS Decade Counter/Decoder, or equivalent.



This is a 1/4 CD4081 CMOS Quadruple 2 input AND gate, or equivalent.



This is a 1/4 CD4011 CMOS Quadruple 2 input NAND gate, or equivalent.



This is a 1/4 CD4093 CMOS Quadruple 2 input Schmitt NAND gate, or equivalent.

General purpose NPN transistor.

General purpose PNP transistor.

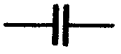
Light emitting diode.

Opto-darlington transistor.

Ultrasonic Receiving Sensor.

Ultrasonic Transmitting Sensor.

Resistor - value in ohms.



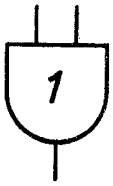
Capacitor - value in Farads.

General purpose silicon diode - eg IN914.

Trembler mechanism - normally closed.

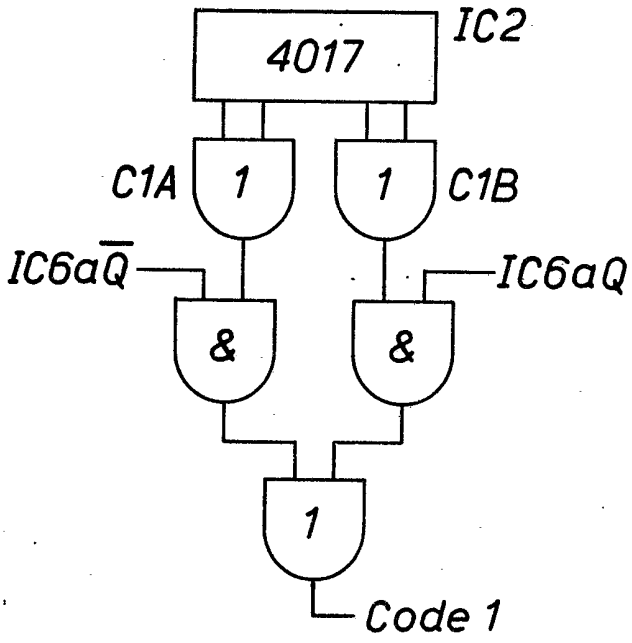
FIG.6.

This is half of a CD 4013 positive-edge triggered Dual D flip-flop.



This is an OR gate.

FIG.7.



SPECIFICATION

An Electronic Locking System

Technical Field

The present invention relates to an electronic locking system comprising a lock and a key.

In this Specification the term "lock" and "key" are each used to define electronic circuitry having a specific function. In operation the lock and key cooperate with one another to actuate the lock provided that the lock and key are correctly paired or matched.

Background Art

In a conventional lock and key system, the key is a mechanical member which is accurately shaped so as to be absolutely complementary within fine limits to the lock receiving passage. One clearly apparent disadvantage of this system is that it is relatively simple to produce an unauthorised replica of the key which will actuate the lock.

Statement of Invention

It is an aim of the invention to alleviate the aforementioned disadvantage, and according to one aspect of the invention there is provided an electronic locking system comprising a lock and a key which are operable so that on inserting the key into the lock, the lock transmits to the key a lock code, the key samples the lock code, and transmits to the lock a key actuating code only if the lock code is correct, and the lock samples the key actuating code and is actuated only if the key actuating code is correct.

According to another aspect of the invention there is provided an electronic locking system comprising a lock and a key which are operable so that the key transmits to the lock a starting code, the lock samples the key starting code and transmits to the key a lock code only if the key starting code is correct, the key samples the lock code, and transmits to the lock a key actuating code only if the lock code is correct, and the lock samples the key actuating code is actuated only if the key actuating code is correct.

In this Specification the term "code" is intended to include any form of signal which may, for example, be in the form of electronic, sonic, ultrasonic or light pulses.

Figures in the Drawings

Two embodiments of the invention will now be described by way of example with reference to the accompanying drawings in which:—

Figure 1 is a block schematic diagram of a first locking system of the invention,

Figures 2, 3 and 4 are circuit diagrams of a second locking system of the invention,

Figures 5 and 6 illustrate the circuit coding used in Figures 2, 3 and 4; and

Figure 7 is a modification of the circuit of Figure 3 to enable it to use a full code.

Detailed Description of Drawings

Referring to Figure 1, one locking system of the invention consists of a lock and key. The lock is a package of electronic circuitry which may be connected to an alarm system or a door bolt, or some similar means of allowing a particular action to take place, or not to take place, when controlled by the key.

The key is a second package of electronic circuitry; which when placed in such a position with respect to the lock unit that it controls the lock unit, and is activated; will allow the lock to check that the key is or is not coded correctly. The lock will take one action if the key is coded correctly, and a second one if it is not.

The lock unit is so designed that tampering with accessible portions of it will cause an alarm to be activated or a suitable action to be initiated.

The two-way interchange of information between the lock and the key is conveyed by optical, magnetic or mechanical means. Radio waves may also be used for the interchange of information provided certain legal conditions are satisfied.

A purely electronic version of this unit without any moving mechanical parts may be constructed, thus giving potentially far greater reliability than magnetic and locks which use moving mechanical parts.

The type of logic "building blocks" used for the lock and key is not critical, but will probably consist of CMOS Complementary Metal Oxide Silicon logic integrated circuits for minimum power consumption. Discrete components are also used as well as integrated circuits. Mechanical construction is in no way critical, except to ensure that the sensors of the lock and key are properly aligned in use.

A master oscillator (clock) is switched on by the insertion of the key, due to bistable B1 changing state; the change of state of B1 also allowing a two-bit (Johnson) counter to start counting. A stream of pulses is thus produced (CK1). The frequency of CK1 is only limited by the frequency response of the sensors, and the maximum usable frequency of the logic used. CK1 feeds the two-bit Johnson counter whose outputs are gated to produce two more clock pulse trains CK2 and CK3. CK2 is generated by OR-gating together the two Q outputs of the counter, giving a 3:1 mark-space ratio. CK3 is generated by AND-gating together the two Q outputs of the counter. CK2 is used to feed the buffering circuit for the lock transmitting sensor, and also feeds one or more decade counters connected in cascade. The carry output from the final decade counter feeds B1 to stop the clock and reset the two-bit counter.

Thus the sequence of events is as follows:—

On inserting the key into the lock, the bistable B1 is set (changes its state to a logical '1' from a logical '0'). This starts the master oscillator, and allows the Johnson two-bit counter to count. E.G. with one decade counter, there are 37 CK1 pulses, s,

10 CK2 and CK3 pulses, and the decade counter counts 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, (the 10th CK2 pulse in fact resets the decade counter fron 9 to 0). The transmitting sensor is also actuated 10 times.

The decade counters commonly available give the numbers from 0 to 9 in the form of a binary code. Devices called BCD/Decimal decoders convert this code back into decimal, i.e. they have 10 output connections, and each connection corresponds to one of the numbers from 0 to 9. By cascading several decade counters connected to BCD/Decimal decoders in series, several decades may be counted and decoded for driving lamp bulbs, displays or other purposes, as in this idea.

The code in the lock is generated by feeding the outputs of the decade counters into BCD/Decimal decoders, and then arbitrarily selecting some of these outputs which are then fed to a diode-resistor OR gate. Thus a set of pulses will be produced every time the key is inserted into the lock, and the number and time between each pulse will be set up by the number and connection points of the diode-resistor OR gate, e.g. with one decade counter connected to its BCD/Decimal decoder and the diodes of the gate connected to outputs 2, 5, 7, 9 of the decoder 4 output pulses will be produced at the second, fifth, seventh and ninth CK2 pulse fed into the counter. In the diagram, the diode-resistor OR gate is called OR*. The pulse train thus generated from the output of OR* is the code, and by changing the number of diodes constituting the OR gate and their connection points, a very large number of individual codes can be generated. For N decade counters, the maximum number of codes available is: $2^N x^{10}$. The output of OR* is fed to one input of a two-input exclusive OR gate (Ex*).

The optical or magnetic pulses in the lock transmitting sensor are picked up by the key receiving sensor, and are then reconstituted into digital pulses which feed an identical decade counter/decoder/diode-resistor OR gate arrangement to that in the lock. The output of the OR gate (EX**) in the key then feeds a key transmitter sensor (of the same or different kind to that used in the lock). There is no reason why the two information paths, lock-key and key-lock, need be of the same type, e.g. one could be optical while the other could be magnetic.

A receiving sensor in the lock picks up the optical or magnetic pulses transmitted by the key, and reconstitutes them into digital pulses. These then feed the second input of the two-input Exclusive-OR gate (EX*), if the two inputs of EX* are identical, the output remains at a logical '0' level and does not trigger the bistable B2, which would actuate an alarm and inhibit the lock from operating.

Note:— The output of EX* is AND-gated with CK3, which has a 1:3 mark-space ratio and is in step with CK2. This means that there is always the time of at least 1 CK1 pulses between the start of any digital level changes, in the main lock and key circuitry, and the time of allowing bistable B2 to look for any such changes. This precaution eradicates the possibility of tiny delays in timing, through the key as compared to the lock, causing false triggering of the alarm. Another bistable B4 is used to change state each time the lock operates, so as to engage or disengage a door bolt or alarm circuit, etc. But should the alarm be set off, bistable B2 (which sets off the alarm) will also set bistable B4 to engage the door bolt etc.

Appropriate conditions are set up when switching on the lock and key by using capacitor and resistor networks on the appropriate set or reset connections to the bistables and counters.

This invention has been described in general terms, and so no specific details of circuitry and associated sensors used have been given. The means of information interchange, which the lock and key use may also be contacts mechanically touching, or radio frequencies, or even microwave transmitter and receiver components, as well as optical or infra-red or magnetic, or ultra-violet radiation.

In a practically constructed version of this invention, only one decade counter/decoder was used to generate the code in the lock and the key (marked 'A' and 'B' in Figure 1 where two are shown).

The 'start' signal was obtained by physically pushing the key into a slot, in order to depress a push button; thus providing the 'start' signal for the lock as well as mechanically aligning the sensors used, which were light-emitting-diodes (LED's) for the transmitting sensors, and photo-transistors for the receiving sensors.

(Electronic circuitry may be added to both lock and key to remove the need for mechanical activation of the units).

Another locking system of the invention is an electronic security system consisting of two components — a lock unit and a key unit. This lock is a package of electronic circuitry which may be connected to an alarm system or a door bolt, or some similar means of allowing a particular action to take place, or not to take place, when controlled by the key.

The key is a second package of electronic circuitry, which when placed in such a position with respect to the lock unit that it controls the lock unit and then activated, will allow the lock to check the coding contained within the key. The lock will take one action if the key is coded correctly and a different action if the key is coded incorrectly.

The system is designed to have considerable advantages over currently available systems;

a) no mechanical or moving components;

b) extremely difficult to activate the system in error;

c) extremely high number of different codes available in both lock and key;

d) repid transmission of data between lock and key and visa versa;

e) impossible to extract correct code required to open lock from lock itself;

f) a great deal of time necessary to acquire the vital code from a key given required equipment;

g) ease of changing the combination in the units;

h) data transmission may be accomplished in many different ways;

i) two-way transmission of information;

j) reasonably immune to interference;

k) standby power supply may be used in the lock;

l) flat battery indication in the key;

m) availability of integration into existing security systems.

A brief description of the unit is as follows:

On activation of the key, a special sequence of pulses is sent from the key into the lock to activate the lock. A second coded stream of pulses is sent from the lock into the key. If the key considers this coded stream of pulses to be correct, it will then transmit a third coded stream of pulses back into the lock (this transmission will not take place if the second coded stream is incorrect). If the lock then decides that the third coded stream of pulses is correct it will then disable or enable an alarm and lock or unlock a bolt or take some similar action. If the third coded stream of pulses is incorrect or absent, the alarm will automatically be activated and the bolt locked or a similar action initiated.

CMOS logic was used in both lock and key to minimise power consumption.

On pressing the "on" button on the key, IC11c generates a nominal 20 m sec pulse burst of 2.5 KHz frequency which passes via T21, S8, T15, T14, IC10d into IC8. Electronic pulses are converted to optical pulses LED S8 and are reconverted to electronic pulses by T15. IC8 is a counter which counts the pulses and every ten pulses produces an output on pin 11. These pulses cause IC4aQ and IC4bQ to change from '0' to '1'. This change ensures IC6b is reset, allow IC10a to start oscillating (~1KHz) and allow IC3 to count. IC3 is a two bit Johnson counter with outputs A and B and by using D7 and D8 produces a waveform at a nominal 250Hz with a 3:1 mark space ratio. The positive edges of this trigger IC2, and thus after 37 pulses from IC10a i.e. on the 38th pulse, IC6a $\overline{Q}$ changes from '1' to '0'. On the positive rising edge of the 78th pulse from IC10a, IC6a $\overline{Q}$ changes from '0' to '1' changing IC4a Q from '1' to '0'. Thus on the positive rising edge of the 158th pulse from IC10a, IC4a Q changes from '0' to '1' changing IC4b Q from '1' to '0'. This stops pin 11 of IC10a high and resets IC3a and IC3b. Thus after a burst of start pulses, a burst of 157 complete pulses is produced from IC10a. These 157 pulses are also fed via T11 to S3.

The 4017 counter/decoder IC2 produces 4 pulses on pin 7 and 4 pulses on pin 10, these being at different times. By varying the number of diodes connected to IC2 and the cathodes of D9 and D6, different pulse trains or codes may be generated, (these diodes act as OR gates or OR together the selected outputs of IC2 see Figure 7). The pulse train at the cathode of D9 is called "code 2"; that at the cathode of D6 is called "code 1". The '0' decoded outputs of IC2 and IC16 are not used. Both codes are 72 pulses of IC10a in length.

These 157 pulses from IC10a are fed via S3 to IC12 via T16, T17, IC11a. Exactly the same process happens with IC12, IC16, IC17a, IC15a, IC14b as does with IC3, IC2, IC9d, IC6a, IC4a. Thus after 77 pulses from IC10a, IC14b Q changes from '0' to '1'. Code 1 is fed in via T13 and S5 to T18, T19, IC11b to IC13. Code 1 is also generated in the key by D15 and fed to IC13 also. Ic13 is wired to produce an exclusive or function, so if the code 1 generated in the key does not agree with the code 1 received in T18, the output of IC13 produces a logic '1'. By AND gating A & B, a 1:3 mark space waveform is produced with relation to the OR-gating of A and B as shown:

Only A AND gated with B is used to examine any coding, so there is always one pulse of IC10a between the changing edges of counters or bistables and the examination of their state. So if the code 1's do not agree, during A-B IC13 pin 11 produces a '1' which passes via IC17c to set IC14a whose $\overline{Q}$ output thus changes to '0'.

Code 2 in the key is generated by D16 and is fed to IC11d. Code 2 is generated twice sequentially in the key, but because IC14b inhibits IC17b and IC11d up to the 78th pulse, only the second generation of code 2 may be allowed to proceed via IC11d to T20 and S8 providing code 1's agree in the lock and key. Code 1 is generated twice sequentially in both lock and key and any disagreement at any time will inhibit IC11d even if code 2 is being transmitted to S8.

Code 2 generated in the key passes via T15, T14, IC10d to IC7. D9 generates code 2 twice immediately in sequence in the lock and code 2 from the key only arrives once, but the output of IC7 (exclusive OR) is AND-gated (IC9c) with IC4a $\overline{Q}$ which only allows an output during the second generation of code 2 in the lock. Again, A and B are AND-gated (IC9a) and used to check the similarity of the code 2's (IC9b). If the code 2's are also correct, on the 158th pulse of IC10a IC4b $\overline{Q}$ changes from a '0' to '1' resetting IC3, disabling IC10a and changing the state of IC5a, which is used to enable or disenable an alarm system.

The states of all the bistables of the start of the overall cycle may be determined by the connection to R1 (the reset line) of their S or R inputs.

If code 2's do not match, the error pulse(s) from IC9b will set IC5b, IC6b, IC5a thus automatically enabling the alarm which would be driven from IC5b Q or $\overline{Q}$. If the alarm has been triggered, the unit may be reset by a use of the

key. Before the key is applied, D12 cathode is '1', IC5b $\overline{Q}$ is '1': IC6b Q is '0'. On using the key IC6b $\overline{Q}$ changes from '0' to '1' simultaneously with IC4b $\overline{Q}$ changing from '1' to '0'. Any glitches will be ignored since the outputs of D10, D11, D12 feed via a time delay of 82 K ohms and 10nF to IC10b. Thus during the operating cycle D10 anode is '0'. Provided there are no incorrect pulses from the key, IC4b changingfrom '0' to '1' at the end of the cycle will allow D10 anode to change from '0' to '1' and after a short delay, IC10b output from '1' to '0', thus resetting the unit via T12.

IC10c resets the counter IC8 every 50mS, so a start pulse burst must have a frequency of at least 500 Hz; in fact 2.5 KHz is used. This makes the start circuitry immune to 50 or 100 Hz radiation from the mains driven lights. The start pulse burst is about 50 pulses to ensure more than one output pulse (for reliability) from pin 11 IC8.

Thus the first 77 pulses of IC10a must not occur before the last pulse from pin 11 IC8, otherwise the circuit will not work correctly. A frequency for IC10a of approximately 1KHz was chosen. (The 77 pulses must take longer than the start burst pulse length — say 50mS i.e. less than 1.6 KHz in this instance).

The start pulse burst does not produce an output from IC9c pin 3 as the $\overline{Q}$ output of IC4a is low (until after the first 77 pulses).

A burglar alarm sensor unit has been shown integrated with and controlled by the main unit. It consists of an ultrasonic doppler and trembler unit.

IC1 and S1 produce a field of acoustic ultrasonic waves. These are picked up by S2 and amplified by T8, T7. T1 is a phase sensitive detector whose output is amplified and fed through a low pass filter (T2, T3). T4 and T5 speed up any output pulses and feed these to a bistable T6, T9, When the lock is in the "off" state 'Y' is at '0', T9 is off and T10 is off irrespective of movement in the ultrasonic field or activation of the trembler. When the lock is in the "on" state switched by the main key the Y becomes '1' (fed from IC5a Q), and significant movement in the ultrasonic field will cause an output pulse (or several) to be passed via D3 to T6, switching off T6, switching on T9 and T10 and sending an error pulse at 'x' to IC5b and IC6b setting off the alarm.

Similarly, if when 'y' is at '1', the trembler connection is broken for only a fraction of a second T9 and T10 will be switched on, causing an error pulse to appear at 'x' setting off the alarm.

Note (1) a nominal 6V supply was used in the lock and a nominal 4V in the key.

Note (2) the coding shown was a special case of the full application (shown only for C1 in Figure 7).

Other Advantages of the Described Embodiment

(1) One unit may fit several locks — each with different coding.

(2) Several keys — 1 lock, priority/area coding, lock only looks at parts of the codes.

Claims

1. An electronic locking system comprising a lock and a key which are operable so that on inserting the key into the lock, the lock transmits to the key a lock code, the key receives the lock code, and transmits to the lock a key actuating code, and the lock samples the key actuating code and is actuated only if the key actuating code is correct.

2. A system as claimed in Claim 1, in which the lock code is a pulse train.

3. A system as claimed in Claim 2, in which the lock includes a diode resistor OR gate.

4. A system as claimed in Claim 3, in which the lock OR gate is fed from selected outputs of a BCD-decimal decoder coupled to a decade counter.

5. A system as claimed in Claim 4, in which the decade counter is fed by the gated output of a two-bit counter.

6. A system as claimed in Claim 5, in which the two-bit counter is fed by a master oscillator or clock actuated by inserting the key into the lock.

7. A system as claimed in any one of Claims 2 to 6, in which the key includes a key receiving sensor to reconstitute received lock pulses into digital pulses.

8. A system as claimed in Claim 7, in which the key also includes the decade counter, decoder and diode resistor OR gate as claimed in Claims 3 to 5 which are fed by said digital pulses.

9. A system as claimed in Claim 8, in which the key further includes a key transmitter sensor fed by said OR gate to produce said key actuating code.

10. A system as claimed in Claim 9, in which the lock includes a receiving sensor to receive the key actuating code and to reconstitute it into digital pulses.

11. A system as claimed in Claim 10, including a two-input exclusive OR gate in which one input is fed by said lock diode resistor OR gate, and the other input is fed by said lock receiving sensor.

12. An electronic locking system comprising a lock and a key which are operable so that the key transmits to the lock a starting code, the lock samples the key starting code and transmits to the key a lock code only if the key starting code is correct, the key samples the lock code, and transmits to the lock a key actuating code only if the lock code is correct, and the lock samples the key actuating code and is actuated only if the key actuating code is correct.

13. A system as claimed in Claim 12, in which at least one of the key starting code, lock code and key actuating code is a coded stream of pulses.

14. A system as claimed in Claim 13, in which the key starting code is a burst of pulses.

15. A system as claimed in any one of Claims 12 to 14, in which the lock includes diode resistor OR gates.

16. A system as claimed in Claim 15, in which the lock diode resistor OR gates are fed from selected outputs of a BCD/Decimal decorder coupled to a first decade counter.

17. A system as claimed in Claim 16, in which the first decade counter is fed by the gated output of a two-bit counter.

18. A system as claimed in Claim 17, in which the two-bit counter is fed by a master oscillator or clock actuated by an output of a second decade counter.

19. A system as claimed in Claim 18 in which the second decade counter is fed by a lock receiving sensor (and buffer circuitry), the sensor reconstituting received key pulses into digital signals.

20. A system as claimed in Claim 18 or Claim 19, in which the second decade counter is reset at regular intervals.

21. A system as claimed in any one of Claims 12 to 20, in which the key includes two (key) receiving sensors and buffer circuitry to reconstitute received lock pulses into digital pulses.

22. A system as claimed in Claim 21, in which the key also includes the first decade counter, decoder, and diode resistor OR gates as claimed in Claims 15 to 17 which are fed by said digital pulses.

23. A system as claimed in Claim 22 in which said lock code is also generated in the key by the said first decade counter, decoder and diode resistor OR gates of Claim 22.

24. A system as claimed in Claim 23, including a two input comparator to compare said lock code generated in the key with said lock code received by the key.

25. A system as claimed in Claim 24, in which said key actuating code is generated by said first decade counter, and decoder of Claim 22 using a different set of OR gates from Claim 16.

26. A system as claimed in Claim 12 to 25 in which said lock actuating code is received by the lock receiving sensor of Claim 19, and buffer circuitry to reconstitute received key pulses into digital pulses.

27. A system as claimed in Claim 26 in which said lock actuating code received by said lock receiving sensor is fed to one input of a comparator, whose other input is fed by said lock actuating code generated by said first decade counter decoder (and the different set of diode resistor OR gates) of Claim 25.

28. A system as claimed in Claim 27 in which said comparator circuit is fed from gated outputs of a two-bit counter.

29. An electronic locking system substantially as herein described and illustrated in the accompanying drawings.

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