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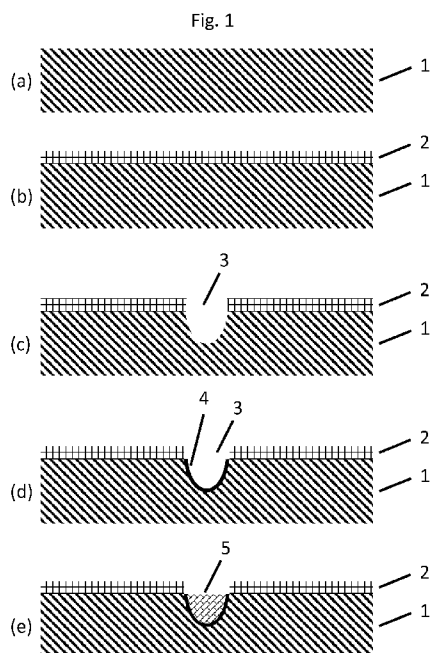
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(54) **Title:** METHOD FOR MANUFACTURING OF FINE LINE CIRCUITRY



(57) **Abstract:** The invention relates to a process for manufacturing of fine line circuitry, comprises: providing a dielectric substrate; coating a masking layer onto at least one side of said dielectric substrate, wherein the masking layer is a hydrophobic material having a contact angle against water of at least 90° determined by the static sessile drop method; forming openings in said dielectric substrate on the side bearing the masking layer; depositing a conductive metal seed layer selectively in said openings by electroless (autocatalytic) plating from a first plating bath composition; and filling said openings with at least one filling material selected from the group consisting of metals, metal alloys and optically transparent materials.

Method for manufacturing of fine line circuitry

5 **Field of the Invention**

The present invention relates to a method for manufacturing of fine line circuitry for printed circuit boards, package substrates (including wafer level packages), microchips, optical devices such as flat panel displays optoelectronic and photonic devices, and related electronic components.

10 **Background of the Invention**

Several methods for manufacturing fine line circuitry are known in the art. The term fine line circuitry is used for structures having a line width and inter line distance of 10 μm (10 μm line and space – L/S) or less. It is currently difficult to achieve such fine line circuitry on organic dielectrics in manufacturing processes, particularly in high yield and high volume manufacturing.

In the next few years conductor line dimensions will reduce from >10 μm L/S to initially 5/5 μm , followed by 3/3 μm and then 1/1 μm . For cost reasons silicon processing methodology, while capable, is unlikely to be used to produce the electronic components in question. It is, therefore a desire in the industry to maintain organic dielectric materials as suitable base material also for manufacture of such fine line circuitry. In case of organic dielectric materials, the cost levels are acceptable, but current techniques will not be able to produce L/S in the range of 5/5 μm or less. For this reason methodologies to enable fine features on organic or other low cost dielectric materials (e.g. glass) are needed.

25 Several attempts to obtain fine line circuitry have been described in the art.

A first method is referred to in the art as “semi-additive process” (SAP) and for example disclosed in US 6,278,185 B1. Herein, the copper circuitry is provided on top of a bare dielectric layer. One disadvantage of the SAP method is the weak adhesion between the copper circuitry and the bare dielectric layer.

5 Another method for manufacturing of fine line circuitry comprises the steps of a) forming recessed structures in a bare dielectric substrate by laser ablation, b) depositing a plating base onto the whole dielectric substrate including the recessed structures, c) electroplating copper onto the whole dielectric substrate including the recessed structures and d) removing the copper from all areas of
10 the dielectric substrate except of the recessed structures by e.g. chemical mechanical polishing (CMP). Such method is for example disclosed in WO 2005/076681 A1. Step d) can be problematic because copper plated dielectric substrates do not always have the required flatness, contrary to a copper plated silicon wafer which is well suited for CMP.

15 A method for manufacturing of fine line circuitry wherein openings on a semiconductor wafer are filled with copper by electroless (autocatalytic) plating is disclosed in US 5,891,513 A. The surface of the entire substrate comprising the openings is first activated with a noble metal catalyst and thereafter copper is deposited. The copper deposition is not selective and copper is deposited into
20 the openings to be filled and also onto other portions of the substrate. Accordingly, removal of excess copper after copper plating is required.

US 2009/0166320 A1 refers to a method comprising: forming a film on a surface of a substrate, the film designed to prevent the seeding of an electroless plating catalyst; laser ablating the surface of the substrate through the film to form
25 trenches; and seeding the surface of the substrate with an electroless plating catalyst.

US 2010/0126009 A1 refers to a method of enabling selective area plating on a substrate, the method comprising: forming a first electrically conductive layer on the substrate; covering the first electrically conductive layer with a solder resist layer; patterning the substrate in order to form a feature therein, the feature extending through the solder resist layer and the first electrically conductive layer; forming a second electrically conductive layer adjoining and electrically connected to the first electrically conductive layer; forming a third electrically conductive layer over the second electrically conductive layer; and removing the solder resist layer and the first electrically conductive layer.

Objective of the present Invention

It is, therefore, an objective of the present invention to provide a method for manufacturing of fine line circuitry on non-silicon materials, particularly organic resin materials, using the existing infrastructure in the printed circuit board and package substrate industry for manufacture of fine line circuitry.

Summary of the Invention

This objective is solved by a method for manufacturing of fine line circuitry comprising, in this order, the steps of

- (i) providing a dielectric substrate (1);
- (ii) coating a masking layer (2) onto at least one side of said dielectric substrate, wherein the masking layer is a hydrophobic material having a contact angle against water of at least 90° as determined by the static sessile drop method;
- (iii) forming openings (3) in said dielectric substrate on the at least one side bearing the masking layer;

(iv) depositing a conductive seed layer (4) selectively in said openings, preferably by electroless (autocatalytic) plating from a first plating bath composition; and

(v) filling said openings with at least one filling material (5) selected from the group consisting of metals, metal alloys and optically transparent materials, preferably having an optical loss of < 0.3 db/cm measured at 1.3 to 1.55 μm wavelength.

Preferably, this objective is solved by a method for manufacturing of fine line circuitry comprising the step

(vi) removing the masking layer from the dielectric substrate after step (v).

The method for manufacturing of fine line circuitry according to the present invention preferably further comprises an additional step (vi) wherein the masking layer is removed from said substrate prior to the addition of the next layer of circuitry or capping layer.

In a first particularly preferred method according to the present invention the at least one filling material (5) is selected from the group consisting of metals and metal alloys.

In a second particularly preferred method according to the present invention the at least one filling material (5) is selected from the group consisting of optically transparent materials.

In a third particularly preferred method according to the present invention the filling material (5) is selected from metals and metal alloys and selected from optically transparent materials. This means that some of said openings are filled with metals or metal alloys and some are filled with optically transparent materi-

als. In such a case the filling materials are metals (or metal alloys) and optically transparent materials.

When the filling material (5) as applied in step (v) is selected from metals and metal alloys it is preferably deposited by wet chemical plating methods and even more preferably by electroless (autocatalytic) plating.

Fine line circuitry within the meaning of this invention comprises trenches and vias.

The method for manufacturing of fine line circuitry according to the present invention provides sufficient adhesion between the circuitry and the dielectric substrate. Furthermore, when applying both metals or metal alloys and optically transparent materials as filling materials, the manufacture of hybrid circuitry comprising electrical and optical circuitry on the same dielectric substrate is feasible.

The predominant material for providing a masking layer in current technology is made from organic resin materials which either result in dry or liquid resist layers.

These layers typically have a minimum thickness of 10 – 50 μm . For the production of fine line circuitry, of e.g. $L/S < 5 \mu\text{m}$, the layer thickness of these photoimaging materials needs to be reduced to 5 μm or below. Reducing the thickness in this order of magnitude with the same material would result in significant yield loss because of film discontinuities. This issue is observed both during manufacture of the film at the material supplier and also in use at the PCB or IC substrate manufacturer. The knock on effect in either case will be a cost increase.

Hydrophobic material, which has a contact angle against water of at least 90° determined by the static sessile drop method, is typically deposited in situ by

the PCB or IC substrate manufacturer and preferably has a layer thickness of < 2.5 μm to be most effective. The thinner masking layer compared to conventional organic resin materials is possible because of the specific application method according to the present invention and the hydrophobic properties of said masking layer.

The majority of aqueous processable masks currently used in the art are pH sensitive in a particular range, e.g. stable at very low (acidic) but not at high (alkaline) pH values. This prevents their use in alkali based plating sequences. The pH sensitivity is typically less of an issue with a hydrophobic material as it is inherently more stable over a wide pH range and particularly at the alkali end of the pH scale. This is due to the nanostructure which is formed during its application and which limits the contact of aqueous solutions with its surface. According to the present invention such a hydrophobic material is used as material for the masking layer.

Current methods for manufacture of fine line circuitry rely on the adsorption of an aqueous based plating catalyst (e.g. palladium in either ionic or colloidal form) over the entire surface of a dielectric substrate. To ensure that there is no potential for shorts between conductors, residuals of this catalyst must be removed after the circuit formation step, using a stripping process. The finer the space between adjacent conductors, the more problematic this (palladium) removal becomes.

The hydrophobic material utilized in the method of the present invention, having a contact angle against water of at least 90° determined by the static sessile drop method, as masking layer prevents the adsorption of the aqueous based plating catalyst onto the surface of the dielectric substrate on all surface areas where said hydrophobic material remains after patterning. Consequently, there is no plating catalyst residue in the areas between the conductors, thus there is

no need to remove the catalyst, e.g. palladium, by problematic stripping processes.

When using standard materials for masking layers, film discontinuities (defects) frequently occur at lower layer thicknesses, e.g. thicknesses in the range of
5 5 μm or less. As a result, portions of the dielectric substrate remain unmasked and are prone to adsorb such plating catalysts, which can result in undesired circuit shorts when depositing a metal or metal alloy layer thereon in step (v) of the method according to the present invention.

The same problem occurs when electrically conductive polymers, inks, conduc-
10 tive carbon particles and other materials for surface activation are used which have to be partially removed prior to the metallisation step.

Brief Description of the Figures

Figure 1 shows a method for manufacturing of fine line circuitry according to an embodiment of the present invention.

15 Figure 2 shows contact angles for hydrophilic and hydrophobic liquids and measurement of the contact angle by the static sessile drop method.

Detailed Description of the Invention

The word "circuitry" according to the present invention comprises electrical and optical circuitry. Electrical circuitries are based on electrically conducting materials such as copper embedded in a dielectric material such as an epoxy resin.
20 Optical circuitries are based on an optically transparent material, preferably having an optical loss of $< 0.3 \text{ dB/cm}$ measured at 1.3 to 1.55 μm wavelength. Hybrid circuitries comprise electrical and optical circuitries as mentioned above on the same substrate.

The phrase "fine line" in respect to "circuitry" is defined herein as conductor lines or other geometrical features having a line width or characteristic geometrical width of 10 μm or less, preferably of 5 μm or less and even more preferably of 1 μm or less. Generally, the width between individual conductor lines is less
5 than 10 μm , preferably less than 5 μm and more preferably less than 1 μm .

According to the method of the present invention, a dielectric substrate is provided. Said dielectric substrate optionally comprises a metal layer such as a copper layer on one side of said dielectric substrate.

The dielectric substrate is selected from the group consisting of electrically non-
10 conductive glass materials and electrically non-conductive organic materials. It may also be a silicon wafer.

Suitable electrically non-conductive glass materials are silica based glasses such as silica glass, sodium and/or potassium silicate glasses, borosilicate glasses, and alkali-aluminosilicate glasses.

15 Suitable electrically non-conductive organic materials are selected from the group consisting of epoxy resin, polyimide, bismaleimide triazine resins, cyanate ester resins, polybenzocyclobutene resins, liquid crystal polymers, PMDA, ODA, DAPI, BTDA, BPDA, BPEDA, BPADA, DDBT, ODPA, DSDA and HQDA, fluorinated polyimides, polyimide siloxane, pre-imidized acetylene terminated
20 polyimides, poly-isoindolo-quinazolinedione, polythioetherimides, polyquinixalone, poly-phenyl-quinoxaline, imide-aryl ether phenylquinoxaline copolymers, polytetrafluoroethylene (PTFE), polybenzimidazole and polybenzoxazole.

Dielectric substrates based on said electrically non-conductive organic materials optionally comprise a reinforcement material such as glass particles, glass fi-
25 bers or meshes made of glass fibers.

Next, a masking layer is coated onto at least one side of the dielectric substrate. In case said dielectric substrate comprises a copper layer on one side of the substrate, said masking layer is coated onto the opposite side of the dielectric substrate.

- 5 The masking layer is a hydrophobic material having a contact angle against water of at least 90°, preferably of at least 120° and even more preferably of at least 140° as determined by the static sessile drop method which is an analytical method known in the art.

10 In the context of this invention contact angle measurements are used to characterise hydrophobicity of materials by determining the wettability of solid surfaces. Quantitatively, the contact angle is the interior angle formed by the solid surface and the tangent to the drop interface at the apparent intersection (three phase contact line) of all three interfaces (solid, liquid, vapor; see Fig. 2).

15 The static equilibrium contact angle of a liquid on a preferably smooth (e.g. roughness < 0.1 µm), homogeneous, rigid and isotropic solid surface is defined by Young's equation (1):

$$\gamma_{sv} = \gamma_{sl} + \gamma_{lv} \cdot \cos\theta \quad (1)$$

20 wherein γ_{sv} corresponds to the solid-vapor interfacial free energy, γ_{sl} to the solid-liquid interfacial free energy and γ_{lv} to the liquid-vapor interfacial tension (surface tension).

In general three different states can be differentiated. Liquids that totally wet the solid surface give contact angles of 0° (total wetting). In case of contact angles that are smaller than 90° the state of the surface is called hydrophilic. Whereas, 25 hydrophobic surfaces give contact angles greater than 90°, see Figure 2.

The solid surface should be planar and mostly free from scratches. All measurements should be performed on a plane surface in order to avoid asymmetric droplet formation. For that reason the underground has to be leveled out to a horizontal state using a liquid level (water level).

- 5 For the definition of the contact angle in the method according to the present invention water is used as the solvent. A suitable droplet volume is chosen to avoid gravitational forces. In this context the diameter of applied water droplets must not exceed the capillary lengths of water. A typical dosing volume ranges between 3 μ L and 10 μ L for water.
- 10 The droplet should not fall from a height but should gently touch the solid surface. The sample should not be charged electrically in order to avoid that the droplet is pulled down. Discharging can be realized using a suitable deionization tool. In case of not being able to gently deposit the droplet onto the solid surface, dosing can also be done while having contact to the surface. When meas-
- 15 uring large contact angles where the droplet is likely to stick to the needle, teflon coated tips might help.

The contact angle is tracked time-dependent using an optical video camera. A baseline is placed manually between the reflection level and the drop, the contour line is fitted and the contact angle is determined. If the contact angle

20 changes over time, measurement values are approximated according to a suitable mathematical model and the initial contact angle ($t = 0$ s) is determined. It is recommended to carry out at least five repeating measurements for each sample. Mean values and standard deviations are calculated. In case of strongly deviating contact angles the number of measurements should preferably be

25 raised to ten or fifteen.

Suitable masking layers can for example be selected from fluoroalkyl compounds and organofunctional silanes with at least one fluoro residue.

A hydrophobic material suitable as a masking layer for the method according to the present invention is disclosed in US 7,485,343 B1 which can be prepared by (i) preparing a precursor sol comprising a metal alkoxide, a solvent, a basic catalyst, a fluoroalkyl compound and water, (ii) depositing said precursor sol onto one side of the dielectric substrate as a film, (iii) heating said film and (iv) exposing said film to a hexamethyldisilazene vapour to form the masking layer.

Another hydrophobic material suitable as a masking layer for the method according to the present invention is disclosed in US 2014/0296409 A1. Such materials contain an acrylic binder and nanoparticles having a size of 8 nm to 100 nm and comprise covalently or non-covalently attached alkyl and/or fluoroalkyl groups on their outer surface. Suitable nanoparticles comprise for example silica, fumed silica, titanium dioxide or alumina.

Other hydrophobic materials suitable as a masking layer for the method according to the present invention comprise HydroFoe[®] and LotusShield[®] (available from Lotus Leaf Coatings), Hydrobead[®] T and P (available from Seashell Technology), Drywired[™] FP-101X (available from Drywired) and Ultra Ever Dry[®] SE (available from UltraTech International).

The masking layer can for example be coated onto the dielectric substrate in form of a dry film by lamination, by printing methods, dip coating, spin coating, and spray coating or ultrasonic spray and plasma deposition.

Preferably, the masking layer is coated onto the dielectric substrate by spin coating or spray coating.

The thickness of the masking layer preferably ranges from 0.01 to 10 μm , more preferably from 0.05 to 5 μm and most preferably from 0.1 to 2.5 μm .

One advantage of the masking layer made of the hydrophobic material having a contact angle against water of at least 90° determined by the static sessile drop

method is that the thickness of the masking layer can be reduced in comparison to the thickness of typical conventional resist materials/masking layers which have a contact angle against water of less than 90 °. Accordingly, the thickness of the masking layer in the method according to the present invention is preferably 0.01 to 10 µm, more preferably 0.05 to 5 µm and most preferably 0.1 to 2.5 µm. In contrast, conventional masking layers typically used in e.g. printed circuit board manufacture often require a thickness of more than 15 µm. Typical dry film resist materials have a layer thickness of e.g. 25 µm. A thinner masking layer provides less undesired shadowing effects during filling the openings with the at least one filling material. The thinner masking layer is possible because of the hydrophobic properties of said masking layer compared to conventional resist materials.

In step (iii) of the method according to the present invention, openings are formed in the dielectric substrate and the masking layer.

Openings are preferably formed by a method selected from the group consisting of laser ablation and spark erosion. Preferably, the openings are formed by laser ablation with e.g. focused laser beam radiation such as from excimer lasers or scanned mask imaging tools.

Said openings can be formed in one step, i.e. the dielectric material of the dielectric substrate and the masking layer above said portions of the dielectric substrate are removed in one step by e.g. laser ablation. This has the advantage of removing alignment issues common in the art.

Said openings can also be formed in two separate steps by. 1. removal of the respective portions of the masking layer and then 2. removal of the respective portions of the dielectric substrate.

Still another suitable method to form the desired openings comprises 1. pattern the masking layer coated in step (ii) to expose those portions of the dielectric

substrate where the openings need to be formed and then 2. remove those portions of the dielectric substrate by laser ablation which are not covered by the patterned masking layer.

5 The diameter or width of openings is preferably less than 25 μm , more preferably less than 15 μm and most preferably less than 1 μm .

The openings formed in the dielectric substrate may have the same size or have a different size. For example, one portion of openings may only extend to a portion of the dielectric substrate while another portion of openings extend through the whole dielectric substrate.

10 In another embodiment of the present invention, the masking layer is coated on both sides of the dielectric substrate in step (ii) and the openings formed in step (iii) extend from one side of the dielectric substrate to the other side of the dielectric substrate.

15 Geometrical shapes of openings comprise shallow or deep cylindrical openings, shallow or deep conical openings, and "u" shaped trenches, trapezoidal or square in cross section.

Next, a conductive seed layer is selectively deposited into the openings formed in step (iii) of the method according to the present invention. The conductive seed layer is deposited by electroless (autocatalytic) plating a metal or metal alloy from a first electroless (autocatalytic) plating bath onto the walls of the openings.
20

Preferably, the walls of the openings are activated by a noble metal prior to the deposition of the conductive seed layer. A suitable noble metal for activating the walls of the openings is for example palladium which can be used in form of ions and/or colloids. Such activation methods are known in the art and for ex-
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ample disclosed in Printed Circuits Handbook, C. F. Coombs Jr. (Ed.), 6th Edition, McGraw Hill, pages 28.9 and 30.2 to 30.3.

Alternatively, activation can be achieved by application of a catalytic seed layer by a metal-based catalytic ink. Such an ink can comprise nanoparticles, e.g.
5 described in patent application WO 2014/009927 A2. Such catalytic seed layers are e.g. formed by providing a mixture of fine metal particles and metal oxide particles, which form the basis for subsequent metal layer formation.

The application of such metal-based catalytic inks can be performed by inkjet printers.

10 Suitable metals as a conductive seed layer for the method according to the present invention are for example copper, nickel, palladium, ruthenium, rhodium, titanium, silver, iron, zinc, cobalt, molybdenum and alloys thereof. The elements copper and its alloys and nickel and its alloys are most preferred.

It is preferred that the conductive seed layer is deposited by electroless (auto-
15 catalytic) deposition methods, which are wet chemical, generally aqueous based processes. These methods are known to the person skilled in the art. Examples for depositing copper and nickel seed layers are exemplary provided below.

Suitable electrolytes (also referred to as plating bath compositions) for deposi-
20 tion of copper and copper alloys by electroless (autocatalytic) plating comprise a source of copper ions and optionally a source of second metal ions, pH modifiers, complexing agents such as EDTA, alkanol amines or tartrate salts, accelerators, stabilizer additives and reducing agents. In most cases formaldehyde is used as reducing agent, other common reducing agents are hypophosphite,
25 glyoxylic acid, dimethylamine borane and borohydride. Typical stabilizer additives for electroless copper plating electrolytes are compounds such as mercapto-
benzothiazole, thiourea, various other sulphur compounds, cyanide and/or

ferrocyanide and/or cobaltocyanide salts, polyethyleneglycol derivatives, heterocyclic nitrogen compounds, methyl butynol, and propionitrile. In addition, molecular oxygen is often used as a stabilizer additive by passing a steady stream of air through the copper electrolyte (ASM Handbook, Vol. 5: Surface Engineering, pp. 311–312). Such plating bath compositions are preferably alkaline.

A preferred plating bath composition for electroless (autocatalytic) plating of copper and copper alloys comprises a source of copper ions and optionally a source of second metal ions, a source of formaldehyde or glyoxylic acid as reducing agent, and at least one polyamino disuccinic acid, or at least one polyamino monosuccinic acid, or a mixture of at least one polyamino disuccinic acid and at least one polyamino monosuccinic acid, or tartrate or a mixture of N,N,N',N'-tetrakis-(2-hydroxypropyl)ethylenediamine and N'-(2-hydroxyethyl)-ethylenediamine-N,N,N'-triacetic acid, or a mixture of N,N,N',N'-tetrakis-(2-hydroxypropyl)ethylenediamine and ethylenediamine-tetra-acetic acid as complexing agent. Said complexing agents are particularly preferred in combination with glyoxylic acid as the reducing agent.

The plating bath composition for electroless (autocatalytic) deposition of copper and copper alloys is preferably held at a temperature in the range of 28 to 60 °C, more preferably 30 to 55 °C and most preferably 33 to 50 °C during step (iv). The dielectric substrate is preferably contacted with the plating bath composition for 0.5 to 20 min, more preferably for 1 to 15 min and most preferably for 2 to 10 min during step (iv). The plating time may also be outside said ranges in case a particularly thin or thick conductive seed layer is desired.

Another example for suitable electroless (autocatalytic) metal and metal alloy plating electrolytes are compositions for deposition of nickel and nickel alloys. Such electrolytes are usually based on hypophosphite compounds as reducing agent, complexing agents such as hydroxycarboxylic acids and further contain one or more of stabilizer additives which are selected from the group consisting

of compounds of main group VI elements (S, Se, Te), oxo-anions (AsO_2^- , IO_3^- , MoO_4^{2-}), heavy metal cations (Sn^{2+} , Pb^{2+} , Hg^+ , Sb^{3+}) and unsaturated organic acids (maleic acid, itaconic acid) (Electroless Plating: Fundamentals and Applications, Eds.: G. O. Mallory, J. B. Hajdu, American Electroplaters and Surface Finishers Society, Reprint Edition, pp. 34–36). Alternative reducing agents for electroless (autocatalytic) deposition of nickel and nickel alloys are for example borane compounds such as sodium borohydride and dimethylamino borane which results in Ni-B alloys.

The nickel ion may be provided by the use of any soluble salt such as nickel sulfate, nickel chloride, nickel acetate, nickel methyl sulfonate and mixtures thereof. The concentration of the nickel in solution may vary widely and is about 0.1 to 100 g/l, preferably about 2 to 50 g/l.

The preferred plating bath compositions for deposition of nickel and nickel alloys comprise hypophosphite ions as the reducing agent and are preferably acidic. Ni-P alloys are deposited from such plating bath compositions.

The plating bath composition for electroless (autocatalytic) deposition of nickel and nickel alloys is preferably held at a temperature in the range of 30 to 90 °C, more preferably 35 to 70 °C and most preferably 40 to 50 °C during step (iv). The dielectric substrate is preferably contacted with the plating bath for 0.5 to 20 min, more preferably for 1 to 15 min and most preferably for 1 to 10 min during step (iv). The plating time may also be outside said ranges in case a particularly thin or thick conductive seed layer is desired.

Electroless (autocatalytic) plating according to step (iv) in the method according to the present invention can be performed in horizontal, reel-to-reel, vertical and vertically conveyORIZED plating equipment.

Preferably, the conductive seed layer (step iv) is a layer of nickel or copper or alloys thereof. The respective metal layer produces a fine grained pore free structure.

5 The conductive seed layer obtained according to step (iv) is required as an optically non-transparent barrier in case the openings are filled with an optically transparent material instead of a metal or metal alloy layer as filling material.

In case where an optically transparent material is used to fill the openings the conductive seed layer is preferably first chemically polished to enhance reflectivity of said layer. Alternatively, the seed layer is coated with a layer of silver as
10 it is highly reflective or the seed layer is chemically polished and then coated (e.g. by wet chemical electroless or immersion plating) with a layer of silver.

In step (v) of the method for manufacturing of fine line circuitry according to the present invention, the openings comprising the conductive seed layer are filled with a filling material selected from the group consisting of metals, metal alloys
15 and optically transparent materials, preferably having an optical loss of $< 0.3 \text{ db/cm}$ at 1.3 to $1.55 \mu\text{m}$ wavelength. The optically transparent materials are preferably resin based materials which possess the right physical properties to fill the openings.

Preferably, the conductive seed layer is deposited from a first electroless (autocatalytic) plating bath composition and the metal or metal alloy as filling material
20 in step (v) from a second electroless (autocatalytic) plating bath composition which is different from said first electroless (autocatalytic) plating bath composition.

The main advantage of deposition of the metal or metal alloy as filling material
25 by electroless (autocatalytic) plating in step (v) in comparison to electroplating is that no excess metal or metal alloy needs to be removed from the dielectric substrate after said plating operation.

The word "filling" in respect to openings is defined herein as completely filling said openings with a filling material selected from the group consisting of metals, metal alloys and optically transparent materials, preferably having an optical loss of < 0.3 db/cm at 1.3 to 1.55 μm wavelength as determined by optical spectroscopy. In case of metals and metal alloys as filling material the word "filling" also includes conformally filled openings.

The same or different electroless (autocatalytic) plating bath compositions applied in step (iv) can also be applied in step (v) of the method according to the present invention. Preferably, the metal or metal alloy for filling in step (v) is copper or a copper alloy. Alternatively, nickel or nickel alloys can be used for filling in step (v).

Filling of the openings with a metal or metal alloy in step (v) as filling material results in the formation of an electrical circuitry.

In one preferred embodiment of the present invention, an optically transparent material, preferably having an optical loss of < 0.3 db/cm at 1.3 to 1.55 μm wavelength, is used as filling material in step (v) of the method according to the present invention for filling the openings comprising the conductive seed layer. This optically transparent material preferably is a resin based optically transparent material.

The optical loss of an optically transparent material at 1.3 to 1.55 μm wavelength in db/cm is measured by a method known in the art. For the measurement, the substrate bearing the optically transparent material is irradiated with light from a suitable source from one side. Suitable light sources are e.g. a laser or LED with emitting light in the wavelength region of between 1.3 to 1.55 μm . The light transmission capability of the material is measured. For this, on the opposite side of the optically transparent material the received optical power is determined.

The optically transparent material preferably is a resin based optically transparent material and is selected from the group consisting of polyimides, polyolefins, polycarbonates, polyacrylates, polymethylmethacrylates, polycyanurates, polysiloxanes, benzocyclobutanes, epoxy resins and fluorinated derivatives of the
5 aforementioned. Such materials are also known as “optically clear resins” and for example commercially available from Dow Corning, NTT, Dow and DuPont.

Other suitable resin based optically transparent materials as filling material are disclosed in US 2008/0286580 A1 (cross-linkable homo- and copolymers having an olefin backbone with a pendant group comprising fluorinated aromatic
10 and aliphatic moieties), US 2002/0160297 A1 (homo- and copolymers of perfluoroisopropanol-styrenes, co-monomers being fluorinated and non-fluorinated aliphatic substituted styrenes), WO 03/099907 A1 (arylene ether organic polymers and oligomers having olefinic end-groups), WO 03/054042 A1 (copolymers of pentafluorostyrene with highly fluorinated aliphatic acrylates and glycidyl methacrylate),
15 US 6,627,383 (acrylic derivative of hexafluorobisphenol compounds) and US 2002/0164538 A1 (copolymers of styrene monomers substituted with a fluorine containing moiety and a fluorinated or non-fluorinated acrylic monomer).

The aforementioned resin based optically transparent materials or suitable precursors thereof can for example be used for filling the openings by dissolving
20 said materials in a suitable solvent or by preparing a slurry of said materials in a suitable solvent which is then used for filling the openings followed by curing said materials in the openings.

Suitable filling methods for said resin based optically transparent materials or suitable precursors thereof comprise spin-coating, dip coating, ink jet printing
25 and syringe deposition.

Said resin based optically transparent materials can be polymerized and/or cured in the openings for example by convection drying, heat treatment and exposition to IR and/or UV radiation.

5 The word "curing" also comprises "cross-linking" of portions of said resin based optically transparent materials.

Filling the openings with an optically transparent material in step (v) as filling material leads to an optical circuitry comprising optical waveguides also known as optical waveguide circuits. The conductive seed layer optically separates the optical waveguides from the dielectric substrate because photons cannot pass
10 through said conductive seed layer.

A second beneficial effect of the conductive seed layer is to serve as a barrier layer for moisture within the dielectric substrate. Accordingly, the optically transparent material (in particular the resin based optically transparent material) is protected in those regions from undesired moisture which alters the optical
15 properties of said materials.

Filling one portion of a plurality of openings with a metal or metal alloy and filling another portion of the plurality of openings in the same dielectric substrate with an optically transparent material in step (v) leads to a hybrid circuitry. In such a case, openings filled with an optically transparent material benefit from the deposited conductive seed layer (for the benefits see the text above).
20

All three types of the aforementioned fine line circuitries can be manufactured by the method according to the present invention.

Figure 1 shows an embodiment of the present invention, wherein manufacturing of fine line circuitry comprises: providing a dielectric substrate (1), Fig. 1(a);
25 coating a masking layer (2) onto at least one side of said dielectric substrate, Fig. 1(b), wherein the masking layer is a hydrophobic material having a contact

angle against water of at least 90° determined by the static sessile drop method; forming openings (3), Fig. 1(c) in said dielectric substrate on the side bearing the masking layer; depositing a conductive seed layer, preferably a copper seed layer (4), Fig. 1(d) selectively in said openings performing electroless (autocatalytic) plating from a first plating bath composition; and filling said openings with at least one filling material (5), Fig. 1(e) selected from the group consisting of metals, metal alloys and optically transparent materials having an optical loss of < 0.3 db/cm at 1.3 to 1.55 μm wavelength.

In a further embodiment of the present invention, the masking layer is removed from the dielectric substrate after step (v) in a step (vi). This means that the masking layer is still coated onto the substrate while step (v) is carried out. As a result, the masking layer is not dissolved and/or delaminated during steps (iii) to (v), in particular during steps (iv) and (v). This in particular means that the masking layer shows a comparatively high stability in aqueous compositions exhibiting a strong acidic or strong basic pH value. In particular, the masking layer utilized in step (ii) of the method of the present invention shows high stability in an aqueous composition exhibiting a strong basic pH, such as in a typical plating bath composition for electroless (autocatalytic) deposition of copper and copper alloys.

Maintaining the masking layer while step (v) is carried out prevents or at least reduces random seeding and/or lateral growth, preferably both.

The masking layer is preferably removed by mechanical abrasion and/or stripping in a solution containing amines and/or alcohols depending on the particular type of masking layer.

CLAIMS

1. A method for manufacturing of fine line circuitry comprising, in this order, the steps of
 - (i) providing a dielectric substrate (1);
 - 5 (ii) coating a masking layer (2) onto at least one side of said dielectric substrate, wherein the masking layer is a hydrophobic material having a contact angle against water of at least 90° as determined by the static sessile drop method;
 - (iii) forming openings (3) in said dielectric substrate on the at least one
10 side bearing the masking layer,
 - (iv) depositing a conductive seed layer (4) selectively in said openings, and
 - (v) filling said openings with at least one filling material (5) selected from
15 the group consisting of metals, metal alloys and optically transparent materials.
2. The method for manufacturing of fine line circuitry according to claim 1 comprising the step
 - (vi) removing the masking layer from the dielectric substrate after step
(v).
- 20 3. The method for manufacturing of fine line circuitry according to claim 1 or 2, wherein the masking layer is coated on both sides of the dielectric substrate in step (ii) and the openings formed in step (iii) extend from one side of the dielectric substrate to the other side of the dielectric substrate.

4. The method for manufacturing of fine line circuitry according to claim 1 or 2, wherein the masking layer is coated on one side of the dielectric substrate in step (ii) only and wherein the openings formed in step (iii) do not extend through the entire dielectric substrate.
- 5 5. The method for manufacturing of fine line circuitry according to any of the foregoing claims, wherein depositing the conductive seed layer (4) in step (iv) is by electroless (autocatalytic) plating from a first plating bath composition.
6. The method for manufacturing of fine line circuitry according to any of the
10 foregoing claims, wherein the masking layer is a hydrophobic material having a contact angle against water of at least 120° as determined by the static sessile drop method, preferably of at least 140° as determined by the static sessile drop method.
7. The method for manufacturing fine line circuitry according to any of the
15 foregoing claims, wherein the thickness of the masking layer ranges from 0.01 to 10 μm , preferably the thickness of the masking layer ranges from 0.05 to 5 μm .
8. The method for manufacturing of fine line circuitry according to any of the
20 foregoing claims, wherein the masking layer is selected from fluoroalkyl compounds and organofunctional silanes with at least one fluoro residue.
9. The method for manufacturing of fine line circuitry according to any of the foregoing claims, wherein the openings are formed by a method selected from the group consisting of laser ablation and spark erosion.
10. The method for manufacturing of fine line circuitry according to any of the
25 foregoing claims, wherein the optically transparent materials have an optical loss of $< 0.3 \text{ db/cm}$ at 1.3 to 1.55 μm wavelength.

11. The method for manufacturing of fine line circuitry according to any of the foregoing claims, wherein the optically transparent materials are selected from the group consisting of polyimides, polyolefins, polycarbonates, polyacrylates, polymethylmethacrylates, polycyanurates, polysiloxanes, benzocyclobutanes, epoxy resins and fluorinated derivatives of the aforementioned.
12. The method for manufacturing of fine line circuitry according to any of the foregoing claims, wherein the openings are activated with a noble metal or a metal-based catalytic ink between steps (iii) and (iv).
13. The method for manufacturing of fine line circuitry according to any of the foregoing claims, wherein the conductive seed layer is selected from the group consisting of copper, nickel, palladium, ruthenium, rhodium, titanium, silver, iron, zinc, cobalt, molybdenum and alloys thereof.
14. The method for manufacturing of fine line circuitry according to any of the foregoing claims, wherein the metals and metal alloys used in step (v) are selected from the group consisting of copper, nickel, palladium, ruthenium, rhodium, titanium, silver, iron, zinc, cobalt, molybdenum and alloys thereof.
15. The method for manufacturing of fine line circuitry according to any of the foregoing claims further comprising step (vi) wherein the masking layer is removed from said substrate prior to the addition of the next layer of circuitry or capping layer.

1/2

Fig. 1

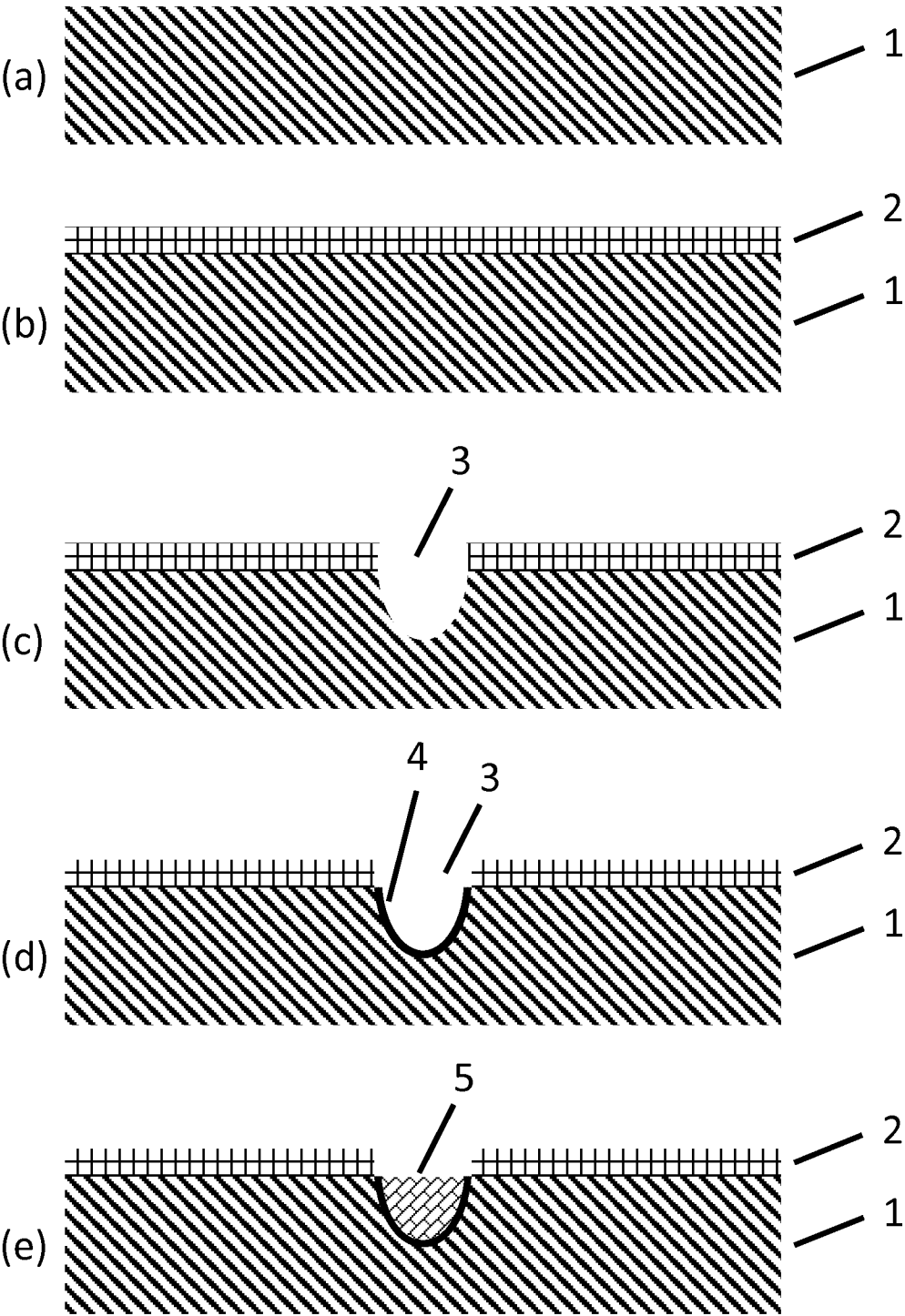
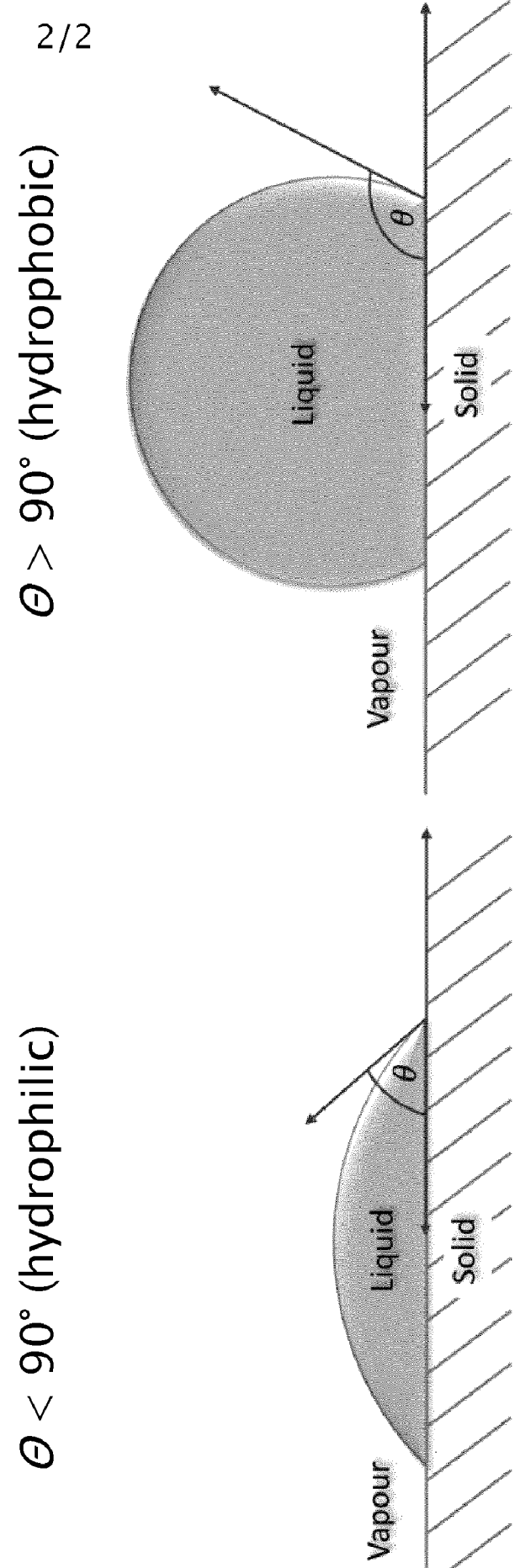


Fig. 2



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/060761

A. CLASSIFICATION OF SUBJECT MATTER

INV. H05K3/00 H05K3/10 H05K3/18
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/126009 A1 (LI YONGGANG [US] ET AL) 27 May 2010 (2010-05-27) paragraph [0009] - paragraph [0029]; figures 1-8	1-15
A	----- US 2009/166320 A1 (JOMAA HOUSSAM [US] ET AL) 2 July 2009 (2009-07-02) paragraph [0014] - paragraph [0022]; figures 1-8	1-15
A	----- US 7 485 343 B1 (BRANSON ERIC D [US] ET AL) 3 February 2009 (2009-02-03) cited in the application the whole document -----	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search

21 July 2016

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2016/060761

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