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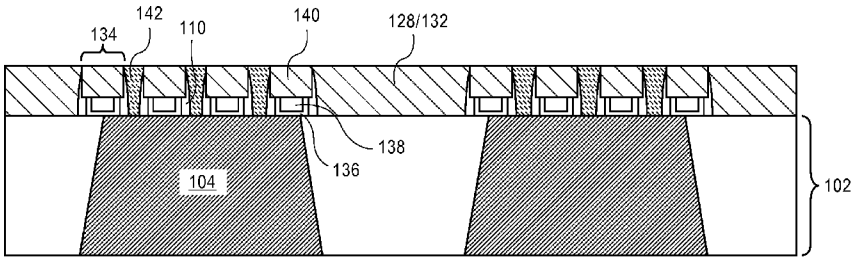


FIG. 2

(57) Abstract: Gate aligned contacts and methods of forming gate aligned contacts are described. For example, a method of fabricating a semiconductor structure includes forming a plurality of gate structures above an active region formed above a substrate. The gate structures each include a gate dielectric layer, a gate electrode, and sidewall spacers. A plurality of contact plugs is formed, each contact plug formed directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures. A plurality of contacts is formed, each contact formed directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures. The plurality of contacts and the plurality of gate structures are formed subsequent to forming the plurality of contact plugs.

Gate Aligned Contact and Method to Fabricate Same

TECHNICAL FIELD

[0001] Embodiments of the invention are in the field of semiconductor devices and processing and, in particular, gate aligned contacts and methods of forming gate aligned contacts.

BACKGROUND

[0002] For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

[0003] In the manufacture of integrated circuit devices, multi-gate transistors, such as tri-gate transistors, have become more prevalent as device dimensions continue to scale down. In conventional processes, tri-gate transistors are generally fabricated on either bulk silicon substrates or silicon-on-insulator substrates. In some instances, bulk silicon substrates are preferred due to their lower cost and because they enable a less complicated tri-gate fabrication process. In other instances, silicon-on-insulator substrates are preferred because of the improved short-channel behavior of tri-gate transistors.

[0004] Scaling multi-gate transistors has not been without consequence, however. As the dimensions of these fundamental building blocks of microelectronic circuitry are reduced and as the sheer number of fundamental building blocks fabricated in a given region is increased, the constraints on the lithographic processes used to pattern these building blocks have become overwhelming. In particular, there may be a trade-off between the smallest

dimension of a feature patterned in a semiconductor stack (the critical dimension) and the spacing between such features.

SUMMARY

[0005] Embodiments of the present invention include gate aligned contacts and methods of forming gate aligned contacts.

[0006] In an embodiment, a semiconductor structure includes a plurality of gate structures disposed above a top surface of, and along sidewalls of, a three-dimensional active region disposed above a substrate. The gate structures each include a gate dielectric layer, a gate electrode, and sidewall spacers. A plurality of contacts is included, each contact disposed directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures. A plurality of contact plugs is also included, each contact plug disposed directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures.

[0007] In another embodiment, a method of fabricating a semiconductor structure includes forming a plurality of gate structures above an active region formed above a substrate. The gate structures each include a gate dielectric layer, a gate electrode, and sidewall spacers. A plurality of contact plugs is formed, each contact plug formed directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures. A plurality of contacts is formed, each contact formed directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures. The plurality of contacts and the plurality of gate structures are formed subsequent to forming the plurality of contact plugs.

[0008] In another embodiment, a method of fabricating a semiconductor structure includes forming a gate line grating above a substrate. The gate line grating includes a plurality of dummy gate lines. A masking stack is formed above and between the dummy gate lines of the gate line grating. A patterned hardmask layer is formed from the masking stack above and between only a first portion of the dummy gate lines of the gate line grating, exposing a second portion of the dummy gate lines. A dielectric layer is formed above the patterned hardmask layer and above and between the second portion of the dummy gate lines. The dielectric layer is planarized to form a patterned dielectric layer above and between the second

portion of the dummy gate lines, and to re-expose the patterned hardmask layer. The patterned hardmask layer is removed from the first portion of the dummy gate lines of the gate line grating, re-exposing the first portion of the dummy gate lines. An interlayer dielectric layer is formed above the patterned dielectric layer, and above and between the first portion of the dummy gate lines. The interlayer dielectric layer and the patterned dielectric layer are planarized to, respectively, form a first permanent interlayer dielectric portion between but not above the first portion of the dummy gate lines, and form a sacrificial dielectric portion between but not above the second portion of the dummy gate lines. One or more of the dummy gate lines of the first or second portions, or both, of the dummy gate lines is patterned to provide trench regions among a plurality of dummy gates and among remaining regions of the first permanent interlayer dielectric portion and the sacrificial dielectric portion. The trench regions are filled with a second permanent interlayer dielectric portion. The plurality of dummy gates is replaced with permanent gate structures. The remaining region of the sacrificial dielectric portion is removed to provide contact openings. Contacts are then formed in the contact openings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figures 1A-1K illustrate cross-sectional views representing various operations in a method of fabricating a semiconductor structure having gate aligned contacts, in accordance with an embodiment of the present invention, with:

[0010] Figure 1A illustrating a gate line grating formed above a substrate, the gate line grating including a plurality of dummy gate lines;

[0011] Figure IB illustrating a masking stack formed above and between the dummy gate lines of the gate line grating of Figure 1A;

[0012] Figure 1C illustrating a patterned hardmask layer formed from the masking stack of Figure IB, the patterned hardmask layer formed above and between only a first portion of the dummy gate lines of the gate line grating, exposing a second portion of the dummy gate lines;

[0013] Figure ID illustrating a dielectric layer formed above the patterned hardmask layer of Figure 1C and above and between the second portion of the dummy gate lines;

[0014] Figure 1E illustrating the dielectric layer of Figure 1D planarized to form a patterned dielectric layer above and between the second portion of the dummy gate lines, and to re-expose the patterned hardmask layer;

[0015] Figure 1F illustrating the patterned hardmask layer of Figure 1E removed from the first portion of the dummy gate lines of the gate line grating, re-exposing the first portion of the dummy gate lines;

[0016] Figure 1G illustrating an interlayer dielectric layer formed above the patterned dielectric layer, and formed above and between the first portion of the dummy gate lines;

[0017] Figure 1H illustrating the interlayer dielectric layer and the patterned dielectric layer planarized to, respectively, form a first permanent interlayer dielectric portion between but not above the first portion of the dummy gate lines, and form a sacrificial dielectric portion between but not above the second portion of the dummy gate lines;

[0018] Figure 1I illustrating one or more of the dummy gate lines of the first or second portions, or both, of the dummy gate lines of Figure 1H patterned to provide trench regions among a plurality of dummy gates and among remaining regions of the first permanent interlayer dielectric portion and the sacrificial dielectric portion, the trench regions filled with a second permanent interlayer dielectric portion;

[0019] Figure 1J illustrating the plurality of dummy gates of Figure 1I replaced with permanent gate structures; and

[0020] Figure 1K illustrating the remaining region of the sacrificial dielectric portion removed to provide contact openings.

[0021] Figure 2 illustrates a cross-sectional view of a semiconductor structure having gate aligned contacts, in accordance with an embodiment of the present invention.

[0022] Figure 3 illustrates a plan view of a semiconductor structure having gate aligned contacts, in accordance with an embodiment of the present invention.

[0023] Figure 4 illustrates a plan view of another semiconductor structure having gate aligned contacts, in accordance with another embodiment of the present invention.

[0024] Figure 5 illustrates a computing device in accordance with one implementation of the invention.

DETAILED DESCRIPTION

[0025] Gate aligned contacts and methods of forming gate aligned contacts are described. In the following description, numerous specific details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0026] One or more embodiments of the present invention are directed to a gate aligned contact process. Such a process may be implemented to form contact structures for semiconductor structure fabrication, e.g., for integrated circuit fabrication. In an embodiment, a contact pattern is formed as aligned to an existing gate pattern. By contrast, conventional approaches typically involve an additional lithography process with tight registration of a lithographic contact pattern to an existing gate pattern in combination with selective contact etches. For example, a conventional process may include patterning of a poly (gate) grid with separately patterning of contacts and contact plugs.

[0027] In accordance with one or more embodiments described herein, a method of contact formation involves formation of a contact pattern which is perfectly aligned to an existing gate pattern while eliminating the use of a lithographic step with exceedingly tight registration budget. In one such embodiment, this approach enables the use of intrinsically highly selective wet etching (e.g., versus conventionally implemented dry or plasma etching) to generate contact openings. In an embodiment, a contact pattern is formed by utilizing an existing gate pattern in combination with a contact plug lithography operation. In one such embodiment, the approach enables elimination of the need for an otherwise

critical lithography operation to generate a contact pattern, as used in conventional approaches. In an embodiment, a trench contact grid is not separately patterned, but is rather formed between poly (gate) lines. For example, in one such embodiment, a trench contact grid is formed subsequent to gate grating patterning but prior to gate grating cuts.

[0028] Figures 1A-1K illustrate cross-sectional views representing various operations in a method of fabricating a semiconductor structure having gate aligned contacts, in accordance with an embodiment of the present invention. Figure 2 illustrates a cross-sectional view of a semiconductor structure having gate aligned contacts, in accordance with an embodiment of the present invention.

[0029] Referring first to Figure 2, a semiconductor structure includes a plurality of gate structures 134 disposed above an active region 102 of a substrate. For example, the active region may include a diffusion region 104, as depicted in Figure 2. The gate structures 134 each include a gate dielectric layer 136, a gate electrode 138, and sidewall spacers 110. A dielectric cap 140 may also be included, as described in greater detail below. A plurality of contacts 142 is included, each contact disposed directly between the sidewall spacers 110 of two adjacent gate structures of the plurality of gate structures 134. A plurality of contact plugs 128/132 is also included, each contact plug disposed directly between the sidewall spacers 110 of two adjacent gate structures of the plurality of gate structures. Possible material options for gate structures 134, active region 102, diffusion region 104, gate dielectric layer 136, gate electrode 138, sidewall spacers 110, dielectric cap 140, contacts 142, and contact plugs 128/132 are provided below. Accordingly, in an embodiment, there is no intervening material layer or residue of such disposed between the sidewalls spacers 110 of gate structures 134 and contacts 142.

[0030] Referring to Figure 1A, an initiating point in a method for fabricating a semiconductor structure, such as the structure described in association with Figure 2, may begin with the fabrication of a gate line grating 106. The gate line grating 106 may include dummy gate 106 with spacers 110. The gate line grating 106 may be formed above an active region 102 and, in some places, above a diffusion region 104 of the active region 102. Thus, in an embodiment, source and drain regions (e.g., region 104) have been fabricated at this stage. A final gate pattern, however,

has not been formed yet although the gate grating pattern has been formed. The gate line grating 106 may be composed of nitride pillars or some other sacrificial material, which may be referred to as gate dummy material, as described in greater detail below.

[0031] In an embodiment, the active region 102 is composed of a single crystal of a material which may include, but is not limited to, silicon, germanium, silicon-germanium or a III-V compound semiconductor material. Diffusion regions 104 are, in one embodiment, heavily doped regions of active region 102. In one embodiment, active region 102 is composed of a group IV material and one or more portions 104 are doped with boron, arsenic, phosphorus, indium or a combination thereof. In another embodiment, active region 102 is composed of a group III-V material and one or more portions 104 are doped with carbon, silicon, germanium, oxygen, sulfur, selenium or tellurium. In an embodiment, at least a portion of active region 102 is strained. Active regions 102 may be, in an embodiment, a part of, or entirely, a three-dimensional structure, such as a patterned semiconductor body. Alternatively, in another embodiment, active region 102 is globally planar.

[0032] Active region 102 may be included as a portion of a broader substrate. The substrate may be composed of a material suitable for semiconductor device fabrication. In an embodiment, the substrate is a bulk substrate. For example, in one embodiment, the substrate is a bulk substrate composed of a single crystal of a material which may include, but is not limited to, silicon, germanium, silicon-germanium or a III-V compound semiconductor material. Alternatively, the substrate includes an upper epitaxial layer and a lower bulk portion, either of which may be composed of a single crystal of a material which may include, but is not limited to, silicon, germanium, silicon-germanium or a III-V compound semiconductor material. An intervening insulator layer composed of a material which may include, but is not limited to, silicon dioxide, silicon nitride or silicon oxy-nitride may be disposed between the upper epitaxial layer and the lower bulk portion.

[0033] The gate line grating 106 may be formed from dummy gates 108. The dummy gates 108 are, in an embodiment, composed of a material suitable for removal at the replacement gate operation, as discussed below. In one embodiment,

dummy gates 108 are composed of polycrystalline silicon, amorphous silicon, silicon dioxide, silicon nitride, or a combination thereof. In another embodiment, a protective capping layer (not shown), such as a silicon dioxide or silicon nitride layer, is formed above dummy gates 108. In an embodiment, an underlying dummy gate dielectric layer (also not shown) is included. In an embodiment, dummy gates 108 further include sidewall spacers 110, which may be composed of a material suitable to ultimately electrically isolate a permanent gate structure from adjacent conductive contacts. For example, in one embodiment, the spacers 110 are composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0034] Referring to Figure IB, a masking stack 112 is formed above and between the dummy gates 108 of the gate line grating 106. The masking stack 112 includes a hardmask layer 114, and anti-reflective coating (ARC) layer 116, and a patterned photo-resist layer 118. In accordance with an embodiment of the present invention, the photo-resist layer 118 of the masking stack 112 is patterned to ultimately facilitate formation of interruptions in a subsequently formed contact pattern. The interruptions may be referred to as "contact plugs."

[0035] In an embodiment, the hardmask layer 114 is composed of a material suitable to act as a subsequent sacrificial layer. For example, in one embodiment, as described in greater detail below, the hardmask layer 114 is ultimately patterned to leave portions remaining which are subsequently removed selective to other features. In a specific such embodiment, hardmask layer 114 is composed substantially of carbon, e.g., as a layer of cross-linked organic polymer. In one embodiment, the hardmask layer 114 is composed of an organic polymer material such as a bottom anti-reflective coating (BARC) layer. In an embodiment, the hardmask layer 114 is formed by a chemical vapor deposition (CVD) process.

[0036] In an embodiment, ARC layer 116 is suitable to suppress reflective interference during lithographic patterning of the photo-resist layer 118. In one such embodiment, the ARC layer 116 is composed of a spin-on-glass material. The patterned photo-resist layer 118 may be composed of a material suitable for use in a lithographic process. In one embodiment, the patterned photo-resist layer 118 is formed by first masking a blanket layer of photo-resist material and then exposing it

to a light source. The patterned photo-resist layer 118 may then be formed by developing the blanket photo-resist layer. In an embodiment, the portions of the photo-resist layer exposed to the light source are removed upon developing the photo-resist layer. Thus, patterned photo-resist layer 118 is composed of a positive photo-resist material. In a specific embodiment, the patterned photo-resist layer 118 is composed of a positive photo-resist material such as, but not limited to, a 248nm resist, a 193nm resist, a 157nm resist, an extreme ultra violet (EUV) resist, an e-beam imprint layer, or a phenolic resin matrix with a diazonaphthoquinone sensitizer. In another embodiment, the portions of the photo-resist layer exposed to the light source are retained upon developing the photo-resist layer. Thus, patterned photo-resist layer 118 is composed of a negative photo-resist material. In a specific embodiment, the patterned photo-resist layer 118 is composed of a negative photo-resist material such as, but not limited to, consisting of poly-cis-isoprene or poly-vinyl-cinnamate.

[0037] Referring to Figure IC, the pattern of the photo-resist layer 118 is transferred to hardmask layer 114 by an etch process to provide a patterned hardmask layer 120 above and between some of the dummy gates 108 of the gate line grating 106. The photo-resist layer 118 is removed. However, a patterned portion of ARC layer 116 may remain, as depicted in Figure IC. In accordance with an embodiment of the present invention, the pattern of the photo-resist layer 118 is transferred to hardmask layer 114 to expose the dummy gates 108 overlying the diffusion regions 104, as is also depicted in Figure IC. In one such embodiment, the pattern of the photo-resist layer 118 is transferred to hardmask layer 114 by using a plasma etch process.

[0038] Referring to Figure ID, any remaining portions of ARC layer 116 are removed and a dielectric layer 122 is formed above the patterned hardmask layer 120 and above and between the exposed dummy gates 108 of the gate line grating 106. In an embodiment, the dielectric layer 122 is composed of a material suitable to act as a subsequent sacrificial layer. For example, in one embodiment, as described in greater detail below, the dielectric layer 122 is ultimately removed selective to other exposed features. In a specific embodiment, the dielectric layer is composed of silicon dioxide.

[0039] Referring to Figure IE, the dielectric layer 122 is planarized to form patterned dielectric layer 124 and to re-expose the patterned hardmask layer 120. In an embodiment, the dielectric layer 122 is planarized by a chemical mechanical planarization (CMP) process operation. In one such embodiment, the CMP process operation involves polishing the dielectric layer 122 on a polishing pad using a slurry. In another embodiment, a dry etch process is used.

[0040] Referring to Figure IF, the patterned hardmask layer 120 is removed with selectivity to the patterned dielectric layer 124, and with selectivity to any underlying dummy gates 108 of the gate line grating 106. In an embodiment, the patterned hardmask layer 120 is composed substantially, or entirely, or carbon and is removed with selectivity to a patterned dielectric layer 124 composed of silicon dioxide. In an embodiment, the patterned hardmask layer 120 is composed substantially, or entirely, or carbon and is removed with an ash process. In one embodiment, the patterned hardmask layer 120 is composed of carbon-containing species and is removed in a dry ash operation utilizing oxygen (0_2) gas or a combination of nitrogen (N_2) gas and hydrogen (H_2) gas.

[0041] Referring to Figure 1G, an interlayer dielectric layer 126 is formed above the patterned dielectric layer 124 and above and between the exposed dummy gates 108 of the gate line grating 106. In accordance with an embodiment of the present invention, the interlayer dielectric layer 126 provides a first portion of a permanent interlayer dielectric layer, as described below. In one embodiment, the interlayer dielectric layer 126 is composed of a silicon carbide material. In a specific such embodiment, the silicon carbide material is formed using a chemical vapor deposition (CVD) process. In another embodiment, the interlayer dielectric layer 126 is composed of a material such as, but not limited to, silicon dioxide, silicon nitride, or silicon oxynitride.

[0042] Referring to Figure 1H, the interlayer dielectric layer 126 and the patterned dielectric layer 124 are planarized to expose the top portions of all dummy gates 108 of the gate line grating 106. In accordance with an embodiment of the present invention, the planarizing provides a first permanent interlayer dielectric portion 128 and a sacrificial dielectric portion 130. In an embodiment, the interlayer

dielectric layer 126 and the patterned dielectric layer 124 are planarized by a CMP process operation, as described above in association with Figure 1E.

[0043] At this stage, the dummy gates 108, including the spacers 110, of the gate line grating 106 may be patterned orthogonal to the grating structure. As an example, portions of the gate line grating 106 that are not over a diffusion area, e.g., over an isolation region, may be removed. In another example, the patterning yields discrete dummy gate structures. Referring to Figure 11, in one such embodiment, the portions of the dummy gates 108 (and corresponding spacer 110 portions) not overlying diffusion regions 104 are removed, e.g., by a lithography and etch process.

[0044] Referring again to Figure 11, the regions where portions of the gate line grating 106 are removed may then be filled by a second permanent interlayer dielectric portion 132. The second permanent interlayer dielectric portion 132 may be formed in a manner similar to, and from the same or like material as, the first permanent interlayer dielectric portion 128, e.g., by deposition and planarization. It is to be understood that the view in Figure 11 may be of a cross-section in a location different (e.g., into or out of the page) than the cross-section illustrated in Figure 1H. Thus, at this point, a permanent interlayer dielectric layer may be defined by the combination of the first permanent interlayer dielectric portion 128 formed in first regions (not shown in Figure 11) and the second permanent interlayer dielectric portion 132 formed in second regions. In one such embodiment, both the first permanent interlayer dielectric portion 128 and the second permanent interlayer dielectric portion 132 are composed of silicon carbide.

[0045] At this stage, the exposed remaining dummy gates 108 may be replaced in a replacement gate process scheme. In such a scheme, dummy gate material such as polysilicon or silicon nitride pillar material, may be removed and replaced with permanent gate electrode material. In one such embodiment, a permanent gate dielectric layer is also formed in this process, as opposed to being carried through from earlier processing.

[0046] In an embodiment, dummy gates 108 are removed by a dry etch or wet etch process. In one embodiment, dummy gates 108 are composed of polycrystalline silicon or amorphous silicon and are removed with a dry etch process comprising SF_6. In another embodiment, dummy gates 108 are composed of

polycrystalline silicon or amorphous silicon and are removed with a wet etch process comprising aqueous NH_4OH or tetramethylammonium hydroxide. In one embodiment, dummy gates 108 are composed of silicon nitride and are removed with a wet etch comprising aqueous phosphoric acid.

[0047] Referring to Figure 1J, permanent gate structures 134 are formed to include a permanent gate dielectric layer 136 and a permanent gate electrode layer or stack 138. Additionally, in an embodiment, a top portion of the permanent gate structures 134 are removed, e.g., by an etch process, and replaced with a dielectric cap layer 140. In an embodiment, the dielectric cap layer 140 is composed of the same material as both the first permanent interlayer dielectric portion 128 and the second permanent interlayer dielectric portion 132 are composed of silicon carbide. In one such embodiment, all of the dielectric cap layer 140, the first permanent interlayer dielectric portion 128, and the second permanent interlayer dielectric portion 132 are composed of silicon carbide.

[0048] In an embodiment, the permanent gate dielectric layer 136 is composed of a high-K material. For example, in one embodiment, the permanent gate dielectric layer 136 is composed of a material such as, but not limited to, hafnium oxide, hafnium oxy-nitride, hafnium silicate, lanthanum oxide, zirconium oxide, zirconium silicate, tantalum oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, lead zinc niobate, or a combination thereof. Furthermore, a portion of the permanent gate dielectric layer 136 may include a layer of native oxide formed from the top few layers of the diffusion region 104. In an embodiment, the permanent gate dielectric layer 136 is composed of a top high-k portion and a lower portion composed of an oxide of a semiconductor material. In one embodiment, the permanent gate dielectric layer 136 is composed of a top portion of hafnium oxide and a bottom portion of silicon dioxide or silicon oxy-nitride.

[0049] In an embodiment, the permanent gate electrode layer or stack 138 is composed of a metal gate. In one embodiment, the permanent gate electrode layer or stack 138 is composed of a metal layer such as, but not limited to, metal nitrides, metal carbides, metal silicides, metal aluminides, hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel or conductive

metal oxides. In a specific embodiment, the permanent gate electrode layer or stack 138 is composed of a non-workfunction-setting fill material formed above a metal workfunction- setting layer. In an embodiment, the permanent gate electrode layer or stack 138 also includes sidewall spacers 110 which may be composed of an insulative dielectric material, as described above.

[0050] Referring to Figure IK, the sacrificial dielectric portion 130 is removed selective to the dielectric cap layer 140, the first permanent interlayer dielectric portion 128, the second permanent interlayer dielectric portion 132, the spacers 110, and the exposed portions of the diffusion regions 104. In an embodiment, the sacrificial dielectric portion 130 is removed with a dry etch or wet etch process, e.g., an aqueous hydrofluoric acid (HF) wet etch process. In accordance with an embodiment of the present invention, the sacrificial dielectric portion 130 acts as a sacrificial placeholder for subsequent contact formation.

[0051] Referring again to Figure 2, contacts 142 are formed the sacrificial dielectric portion 130 once resided. Thus, the contacts 142 are formed between the permanent gate structures 134. In an embodiment, the contacts 142 are formed by deposition and planarization, e.g., by CMP, of a conductive material. Contacts 142 may be composed of a conductive material. In an embodiment, contacts 142 are composed of a metal species. The metal species may be a pure metal, such as nickel or cobalt, or may be an alloy such as a metal-metal alloy or a metal-semiconductor alloy (e.g., such as a silicide material).

[0052] Figure 3 illustrates a plan view showing certain features of the semiconductor structure of Figure 2, in accordance with an embodiment of the present invention. Referring to Figure 3, a semiconductor structure includes a plurality of gate structures 134 disposed above an active region 102, such as a diffusion region 104, of a substrate. A plurality of contacts 142 is included, each contact disposed directly between two adjacent gate structures of the plurality of gate structures 134, e.g., directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures 134.

[0053] Accordingly, in an embodiment, a method of fabricating a semiconductor structure includes forming a gate line grating above a substrate. The gate line grating includes a plurality of dummy gate lines. A masking stack is

formed above and between the dummy gate lines of the gate line grating. A patterned hardmask layer is formed from the masking stack above and between only a first portion of the dummy gate lines of the gate line grating, exposing a second portion of the dummy gate lines. A dielectric layer is formed above the patterned hardmask layer and above and between the second portion of the dummy gate lines. The dielectric layer is planarized to form a patterned dielectric layer above and between the second portion of the dummy gate lines, and to re-expose the patterned hardmask layer. The patterned hardmask layer is removed from the first portion of the dummy gate lines of the gate line grating, re-exposing the first portion of the dummy gate lines. An interlayer dielectric layer is formed above the patterned dielectric layer, and above and between the first portion of the dummy gate lines. The interlayer dielectric layer and the patterned dielectric layer are planarized to, respectively, form a first permanent interlayer dielectric portion between but not above the first portion of the dummy gate lines, and form a sacrificial dielectric portion between but not above the second portion of the dummy gate lines. One or more of the dummy gate lines of the first or second portions, or both, of the dummy gate lines is patterned to provide trench regions among a plurality of dummy gates and among remaining regions of the first permanent interlayer dielectric portion and the sacrificial dielectric portion. The trench regions are filled with a second permanent interlayer dielectric portion. The plurality of dummy gates is replaced with permanent gate structures. The remaining region of the sacrificial dielectric portion is removed to provide contact openings. Contacts are then formed in the contact openings.

[0054] In one such embodiment, forming the patterned hardmask layer includes forming a cross-linked organic polymer layer, forming the dielectric layer includes forming a layer of silicon dioxide, forming the interlayer dielectric layer includes forming a layer of silicon carbide, and filling the trench regions with a second permanent interlayer dielectric portion includes forming and planarizing a second layer of silicon carbide. In a specific such embodiment, replacing the plurality of dummy gates with permanent gate structures includes forming a permanent gate dielectric layer, a permanent gate layer, and a silicon carbide cap layer. In another such embodiment, forming the gate line grating above the substrate

includes forming the dummy gate lines above a top surface of, and along sidewalls of, a three-dimensional active region.

[0055] In an embodiment, one or more approaches described herein contemplate effectively a dummy and replacement gate process in combination with a dummy and replacement contact process. In one such embodiment, the replacement contact process is performed after the replacement gate process to allow high temperature anneal of at least a portion of the permanent gate stack. For example, in a specific such embodiment, an anneal of at least a portion of the permanent gate structures, e.g., after a gate dielectric layer is formed, is performed at a temperature greater than approximately 600 degrees Celsius. The anneal is performed prior to formation of the permanent contacts.

[0056] In an embodiment, dummy contacts are formed prior to the formation of contact plugs. That is, the dummy contacts may be formed prior to cutting dummy gate structures in a gate grating. Such an approach may provide flexibility in ultimate layout. In one such embodiment, a contact structure is formed in contact with two or more diffusion regions. For example, Figure 4 illustrates a plan view of another semiconductor structure having gate aligned contacts, in accordance with another embodiment of the present invention.

[0057] Referring to Figure 4, a semiconductor structure includes a plurality of gate structures 134 disposed above an active region 102, such as a diffusion region 104, of a substrate. A plurality of contacts 142 is included, each contact disposed directly between two adjacent gate structures of the plurality of gate structures 134, e.g., directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures 134. One of the contacts 144 is formed in contact with two diffusion regions. The formation of the contact 144 is , in a specific embodiment, facilitated by the previous presence of dummy gate grating lines that are not cut until at least a dummy contact placeholder for contact 144 is formed.

[0058] It is to be understood that not all aspects of the processes described above need be practiced to fall within the spirit and scope of embodiments of the present invention. For example, in one embodiment, dummy gates need not ever be formed. The gate stacks described above may actually be permanent gate stacks as

initially formed. In one such embodiment, so long as plug formation is followed by gate cut operations, benefits and advantages will be realized.

[0059] The processes described herein may be used to fabricate one or a plurality of semiconductor devices. The semiconductor devices may be transistors or like devices. For example, in an embodiment, the semiconductor devices are a metal-oxide semiconductor (MOS) transistors for logic or memory, or are bipolar transistors. Also, in an embodiment, the semiconductor devices have a three-dimensional architecture, such as a trigate device, an independently accessed double gate device, or a FIN-FET.

[0001] Figure 5 illustrates a computing device 500 in accordance with one implementation of the invention. The computing device 500 houses a board 502. The board 502 may include a number of components, including but not limited to a processor 504 and at least one communication chip 506. The processor 504 is physically and electrically coupled to the board 502. In some implementations the at least one communication chip 506 is also physically and electrically coupled to the board 502. In further implementations, the communication chip 506 is part of the processor 504.

[0002] Depending on its applications, computing device 500 may include other components that may or may not be physically and electrically coupled to the board 502. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0003] The communication chip 506 enables wireless communications for the transfer of data to and from the computing device 500. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term

does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 506 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 500 may include a plurality of communication chips 506. For instance, a first communication chip 506 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 506 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0004] The processor 504 of the computing device 500 includes an integrated circuit die packaged within the processor 504. In some implementations of the invention, the integrated circuit die of the processor includes one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0005] The communication chip 506 also includes an integrated circuit die packaged within the communication chip 506. In accordance with another implementation of the invention, the integrated circuit die of the communication chip includes one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention.

[0006] In further implementations, another component housed within the computing device 500 may contain an integrated circuit die that includes one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention.

[0007] In various implementations, the computing device 500 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a

server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 500 may be any other electronic device that processes data.

[0008] Thus, gate aligned contacts and methods of forming gate aligned contacts have been disclosed. In an embodiment, a method of fabricating a semiconductor structure includes forming a plurality of gate structures above an active region formed above a substrate. The gate structures each include a gate dielectric layer, a gate electrode, and sidewall spacers. A plurality of contact plugs is formed, each contact plug formed directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures. A plurality of contacts is formed, each contact formed directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures. The plurality of contacts and the plurality of gate structures are formed subsequent to forming the plurality of contact plugs. In one embodiment, the plurality of gate structures is formed by replacing a plurality of dummy gates prior to forming the plurality of contacts. In one embodiment, forming the plurality of contacts includes forming a contact structure in contact with two or more diffusion regions of the active region.

CLAIMS

What is claimed is:

1. A semiconductor structure, comprising:

a plurality of gate structures disposed above a top surface of, and along sidewalls of, a three-dimensional active region disposed above a substrate, the gate structures each comprising a gate dielectric layer, a gate electrode, and sidewall spacers;

a plurality of contacts, each contact disposed directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures; and

a plurality of contact plugs, each contact plug disposed directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures.

2. The semiconductor structure of claim 1, wherein the plurality of contacts comprises a conductive material, and the plurality of contact plugs comprises silicon carbide.

3. The semiconductor structure of claim 2, wherein the gate structures each comprise a high-K gate dielectric, a metal gate, and a silicon carbide cap.

4. The semiconductor structure of claim 1, wherein one of the contacts is in contact with two or more diffusion regions of the three-dimensional active region.

5. A method of fabricating a semiconductor structure, the method comprising:

forming a plurality of gate structures above an active region formed above a substrate, the gate structures each comprising a gate dielectric layer, a gate electrode, and sidewall spacers;

forming a plurality of contact plugs, each contact plug formed directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures; and

forming a plurality of contacts, each contact formed directly between the sidewall spacers of two adjacent gate structures of the plurality of gate structures, wherein the plurality of contacts and the plurality of gate structures are formed subsequent to forming the plurality of contact plugs.

6. The method of claim 5, wherein forming the plurality of gate structures above the active region comprises forming the plurality of gate structures above a top surface of, and along sidewalls of, a three-dimensional active region formed above the substrate.

7. The method of claim 5, wherein the plurality of gate structures is formed by replacing a plurality of dummy gates prior to forming the plurality of contacts.

8. The method of claim 7, further comprising:

performing an anneal of at least a portion of each of the plurality of gate structures at a temperature greater than approximately 600 degrees Celsius.

9. The method of claim 8, wherein forming the plurality of contact plugs comprises forming silicon carbide contact plugs.

10. The method of claim 5, wherein forming the plurality of contacts comprises forming a contact structure in contact with two or more diffusion regions of the active region.

11. A method of fabricating a semiconductor structure, the method comprising:

forming a gate line grating above a substrate, the gate line grating comprising a plurality of dummy gate lines;

forming a masking stack above and between the dummy gate lines of the gate line grating;

forming, from the masking stack, a patterned hardmask layer above and between only a first portion of the dummy gate lines of the gate line grating, exposing a second portion of the dummy gate lines;

forming a dielectric layer above the patterned hardmask layer and above and between the second portion of the dummy gate lines;

planarizing the dielectric layer to form a patterned dielectric layer above and between the second portion of the dummy gate lines, and to re-expose the patterned hardmask layer;

removing the patterned hardmask layer from the first portion of the dummy gate lines of the gate line grating, re-exposing the first portion of the dummy gate lines;

forming an interlayer dielectric layer above the patterned dielectric layer, and above and between the first portion of the dummy gate lines;

planarizing the interlayer dielectric layer and the patterned dielectric layer to, respectively, form a first permanent interlayer dielectric portion between but not above the first portion of the dummy gate lines, and form a sacrificial dielectric portion between but not above the second portion of the dummy gate lines;

patterning one or more of the dummy gate lines of the first or second portions, or both, of the dummy gate lines to provide trench regions among a plurality of dummy gates and among remaining regions of the first permanent interlayer dielectric portion and the sacrificial dielectric portion;

filling the trench regions with a second permanent interlayer dielectric portion;

replacing the plurality of dummy gates with permanent gate structures;

removing the remaining region of the sacrificial dielectric portion to provide contact openings; and

forming contacts in the contact openings.

12. The method of claim 11, wherein forming the gate line grating above the substrate further comprises forming the dummy gate lines having sidewall spacers.

13. The method of claim 11, wherein forming the masking stack comprises forming a patterned photo-resist layer above an anti-reflective coating layer, which is formed above a hardmask layer.

14. The method of claim 13, wherein forming the patterned hardmask layer above and between the first portion of the dummy gate lines comprises forming a cross-linked organic polymer layer.

15. The method of claim 11, wherein forming the dielectric layer above the patterned hardmask layer and above and between the second portion of the dummy gate lines comprises forming a layer of silicon dioxide.

16. The method of claim 11, wherein planarizing the dielectric layer to form the patterned dielectric layer comprises using a chemical mechanical planarization process.

17. The method of claim 11, wherein removing the patterned hardmask layer comprises using a dry ash process based on oxygen (0_2) gas or a combination of nitrogen (N_2) gas and hydrogen (H_2) gas.

18. The method of claim 11, wherein forming the interlayer dielectric layer comprises forming a layer of silicon carbide.

19. The method of claim 11, wherein planarizing the interlayer dielectric layer and the patterned dielectric layer comprises using a chemical mechanical planarization process.

20. The method of claim 11, wherein patterning the dummy gate lines to provide the trench regions comprises removing one or more portions of the dummy gate lines which are disposed over an isolation region.

21. The method of claim 11, wherein filling the trench regions with a second permanent interlayer dielectric portion comprises forming and planarizing a layer of silicon carbide.

22. The method of claim 11, wherein replacing the plurality of dummy gates with permanent gate structures comprises forming a permanent gate dielectric layer, a permanent gate layer, and a dielectric cap layer.

23. The method of claim 11, wherein removing the remaining region of the sacrificial dielectric portion comprises using an aqueous hydrofluoric acid (HF) process or a dry etch process.

24. The method of claim 11, wherein forming the contacts in the contact openings comprises depositing and planarizing a conductive material layer.

25. The method of claim 11, wherein forming the patterned hardmask layer comprises forming a cross-linked organic polymer layer, forming the dielectric layer comprises forming a layer of silicon dioxide, forming the interlayer dielectric layer comprises forming a layer of silicon carbide, and filling the trench regions with a second permanent interlayer dielectric portion comprises forming and planarizing a second layer of silicon carbide.

26. The method of claim 25, wherein replacing the plurality of dummy gates with permanent gate structures comprises forming a permanent gate dielectric layer, a permanent gate layer, and a silicon carbide cap layer.

27. The method of claim 11, wherein forming the gate line grating above the substrate comprises forming the dummy gate lines above a top surface of, and along sidewalls of, a three-dimensional active region.

28. The method of claim 11, wherein replacing the plurality of dummy gates with permanent gate structures is performed prior to forming the contacts in the contact openings.

29. The method of claim 28, further comprising:

performing an anneal of at least a portion of the permanent gate structures at a temperature greater than approximately 600 degrees Celsius.

30. The method of claim 11, wherein forming contacts in the contact openings comprises forming a contact structure in contact with two or more diffusion regions.

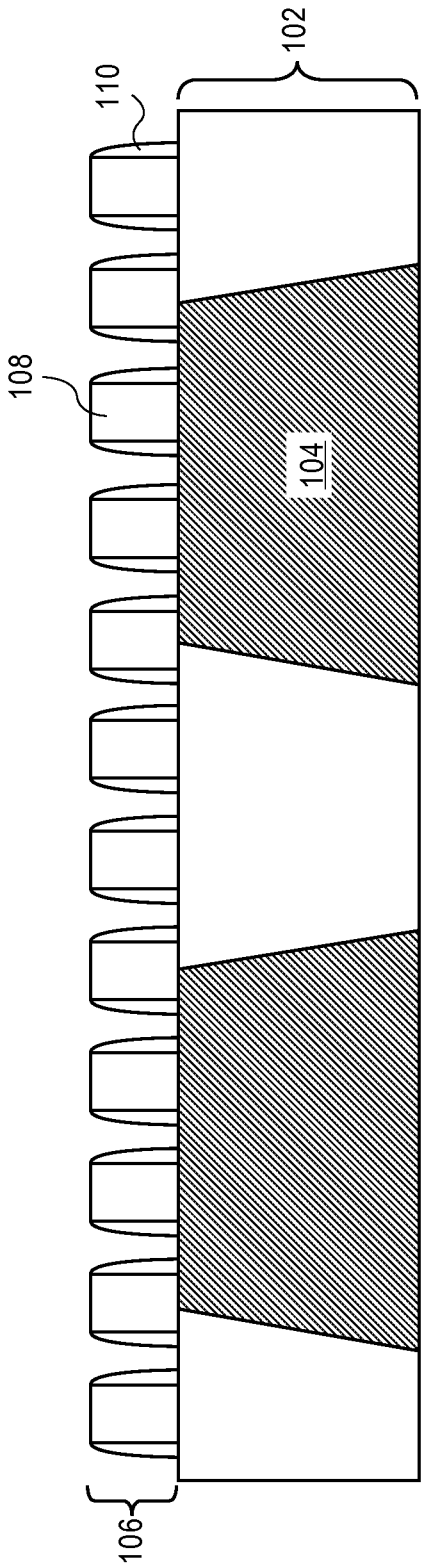


FIG. 1A

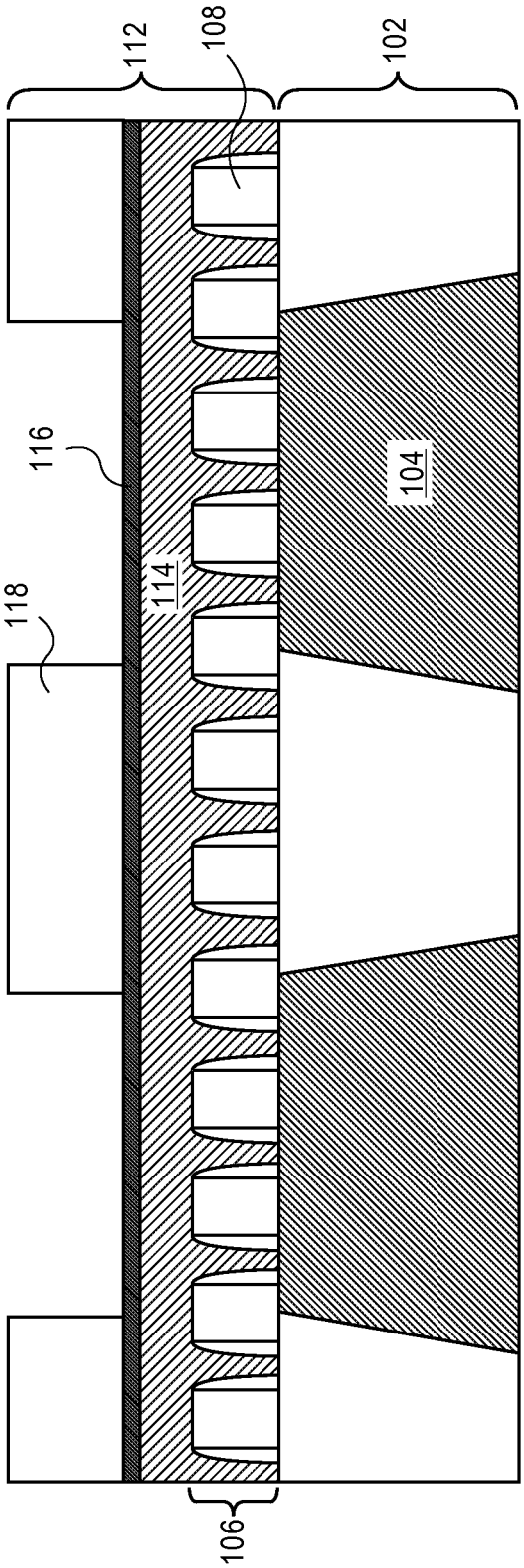


FIG. 1B

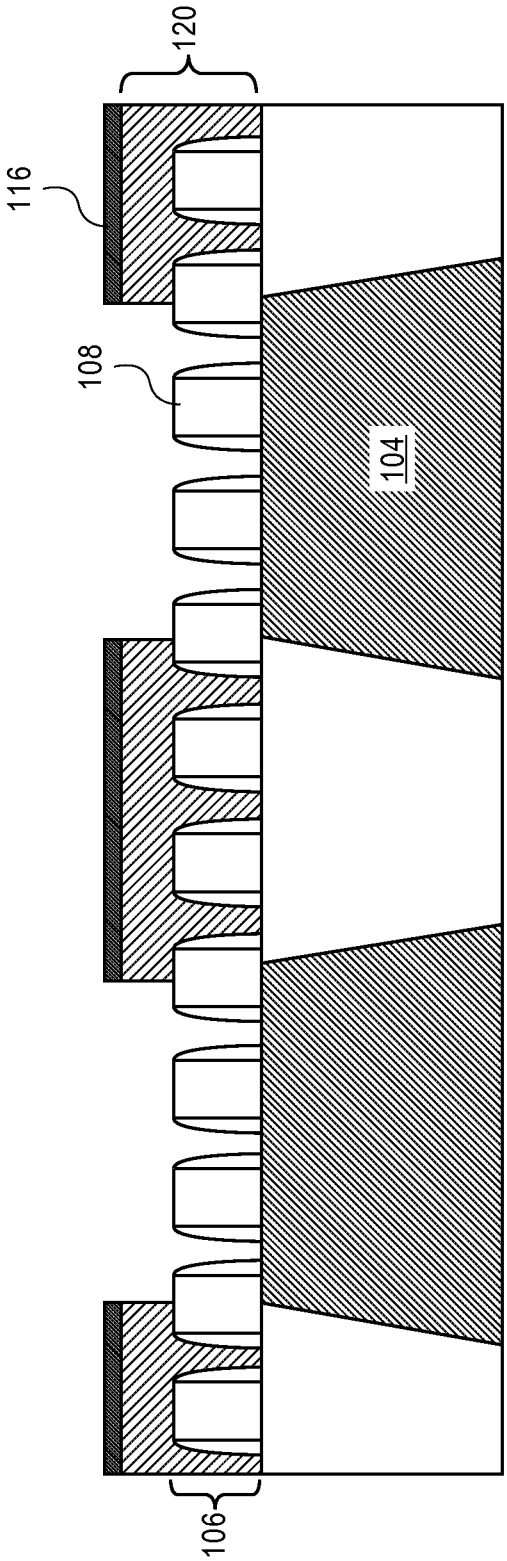


FIG. 1C

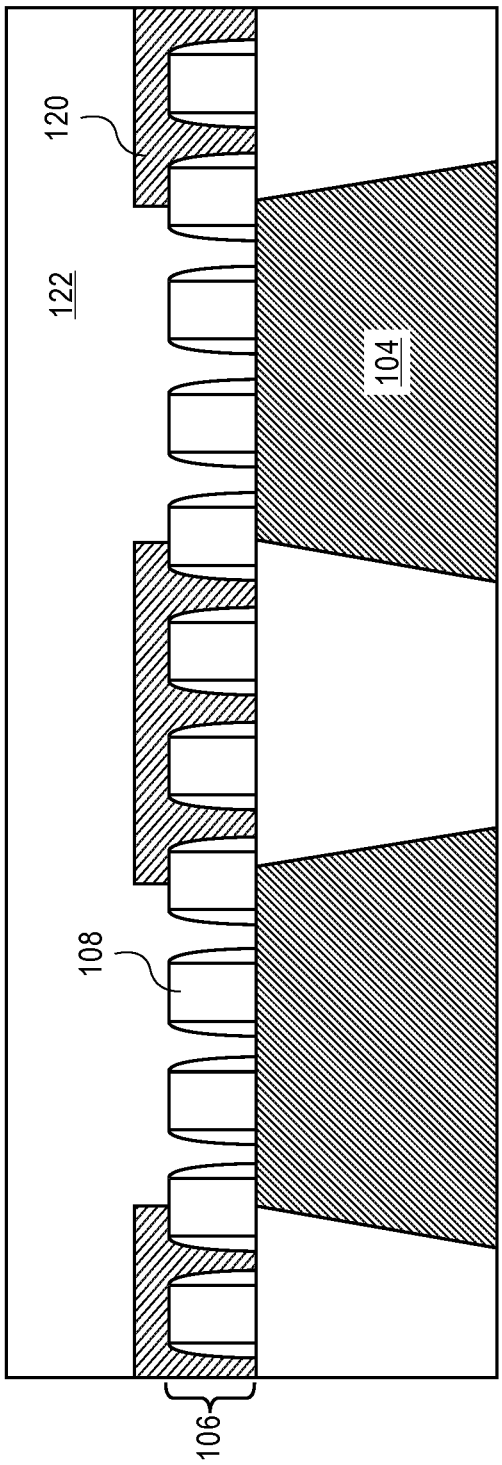


FIG. 1D

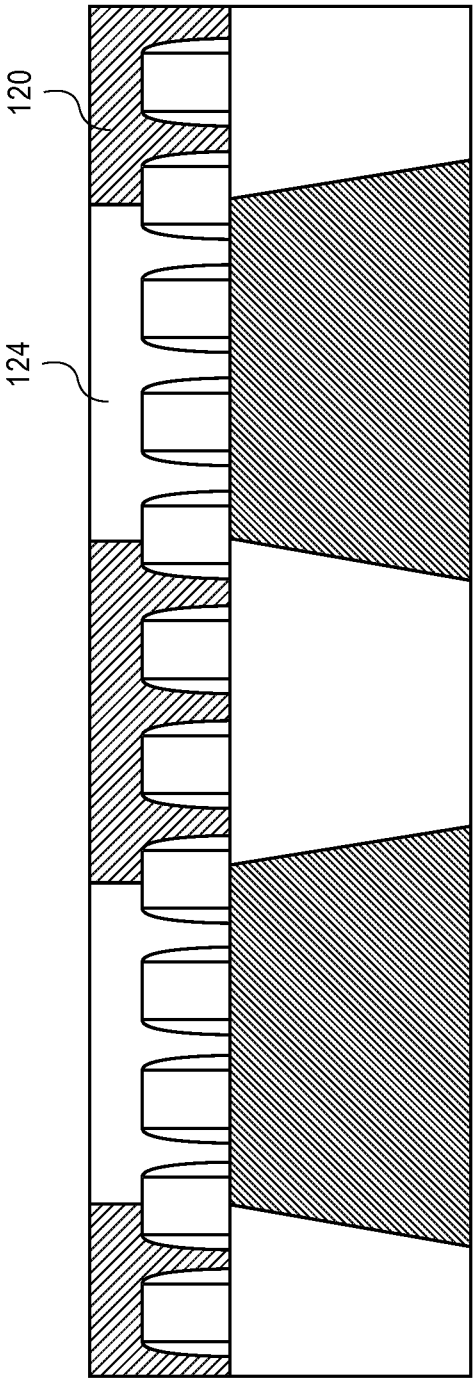


FIG. 1E

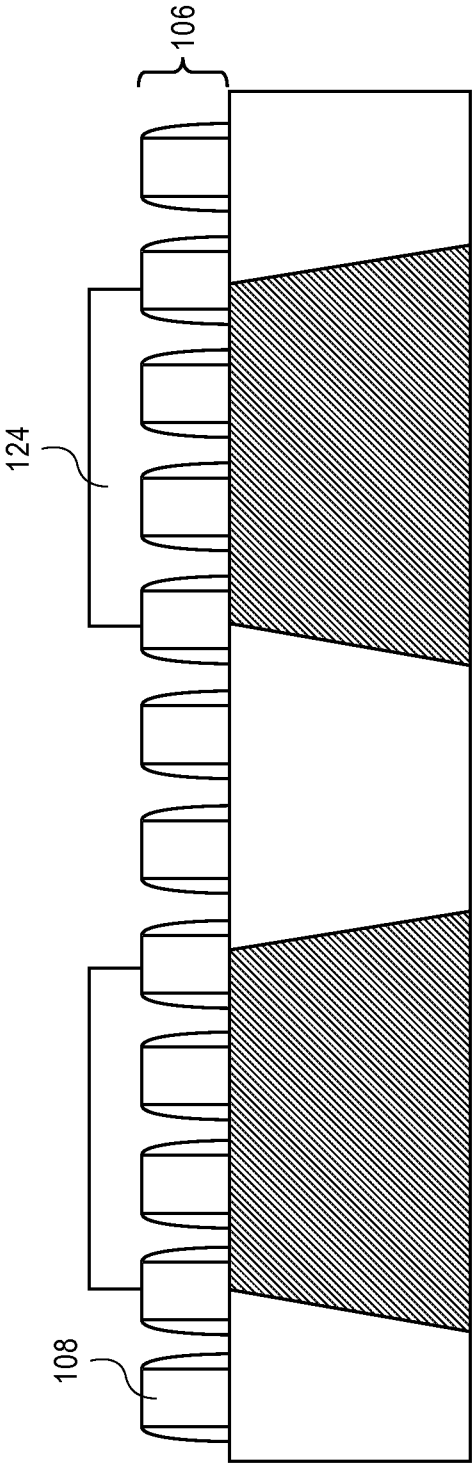


FIG. 1F

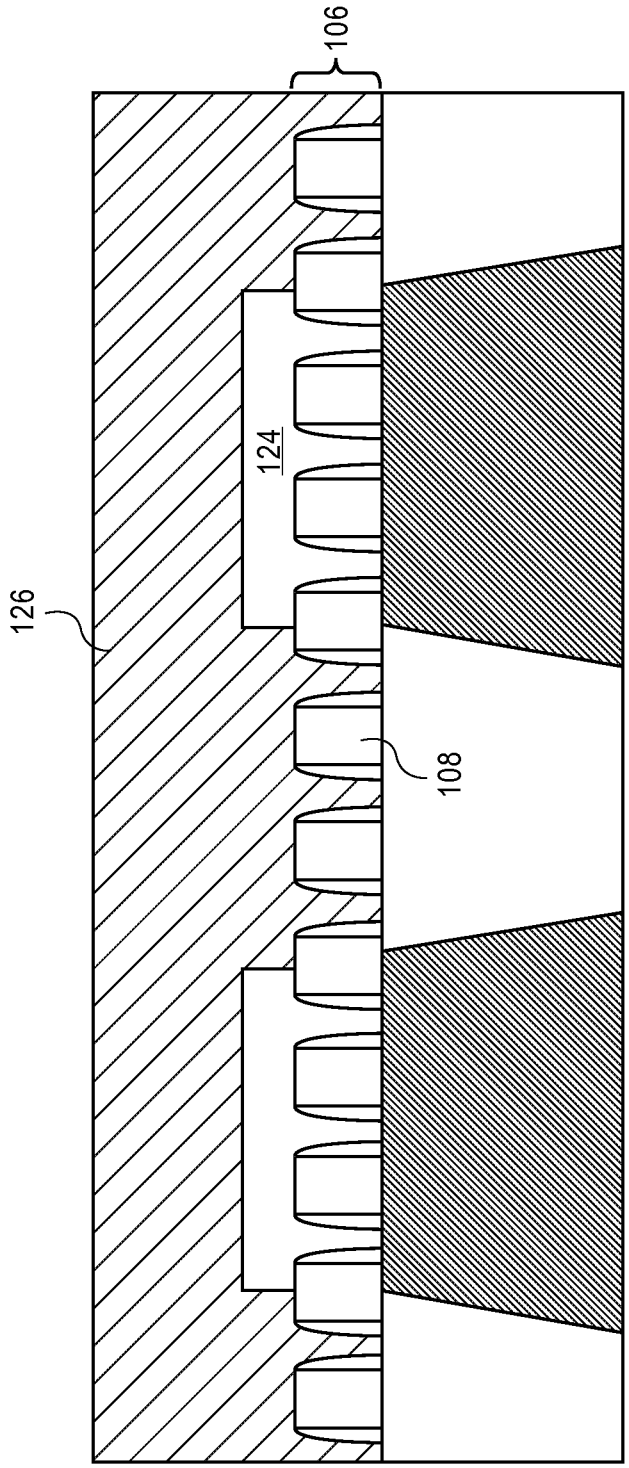


FIG. 1G

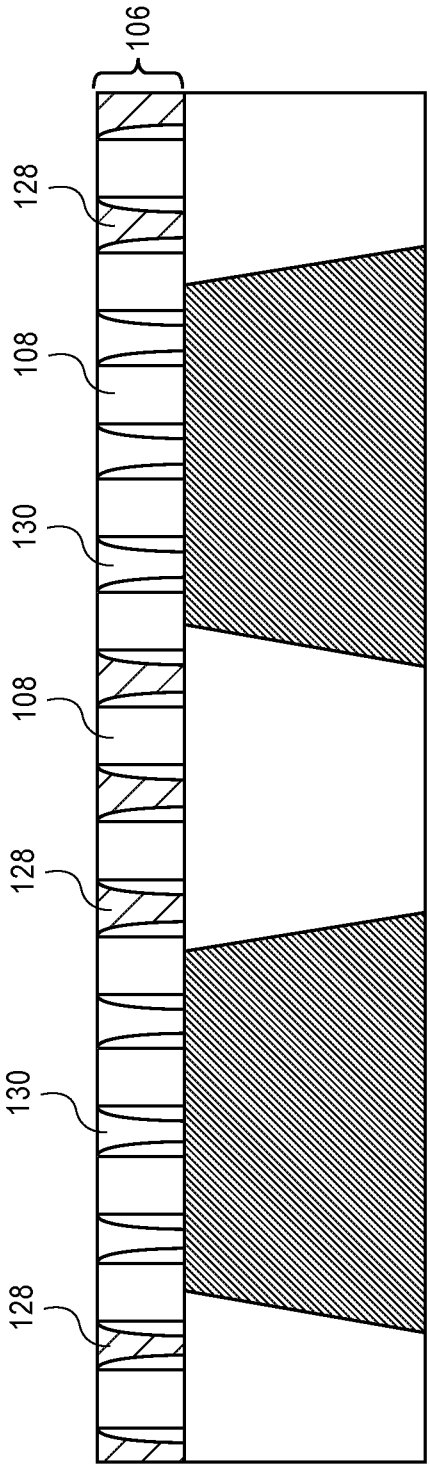


FIG. 1H

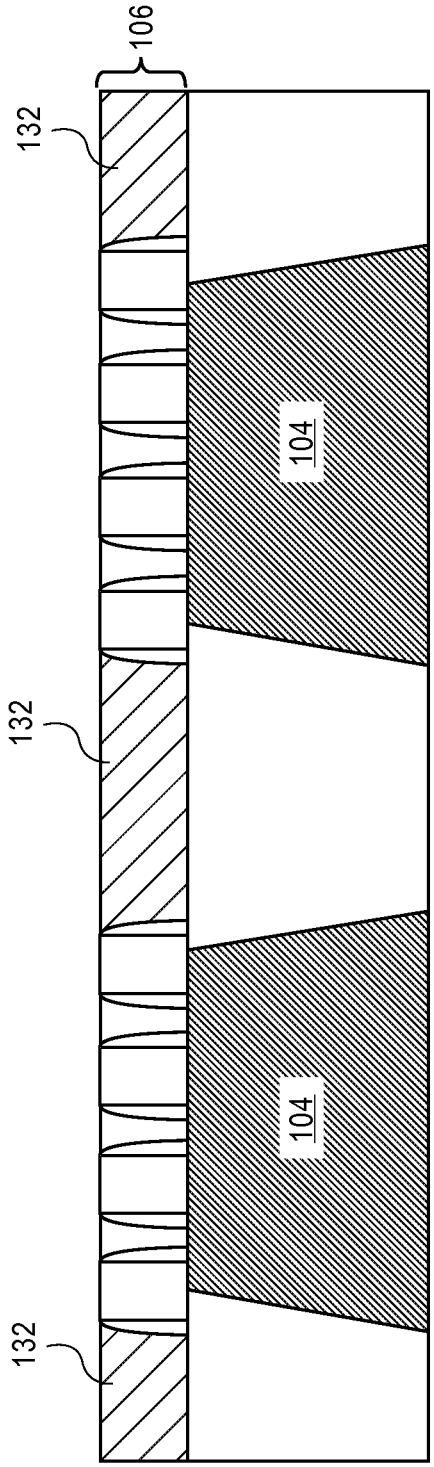


FIG. 1I

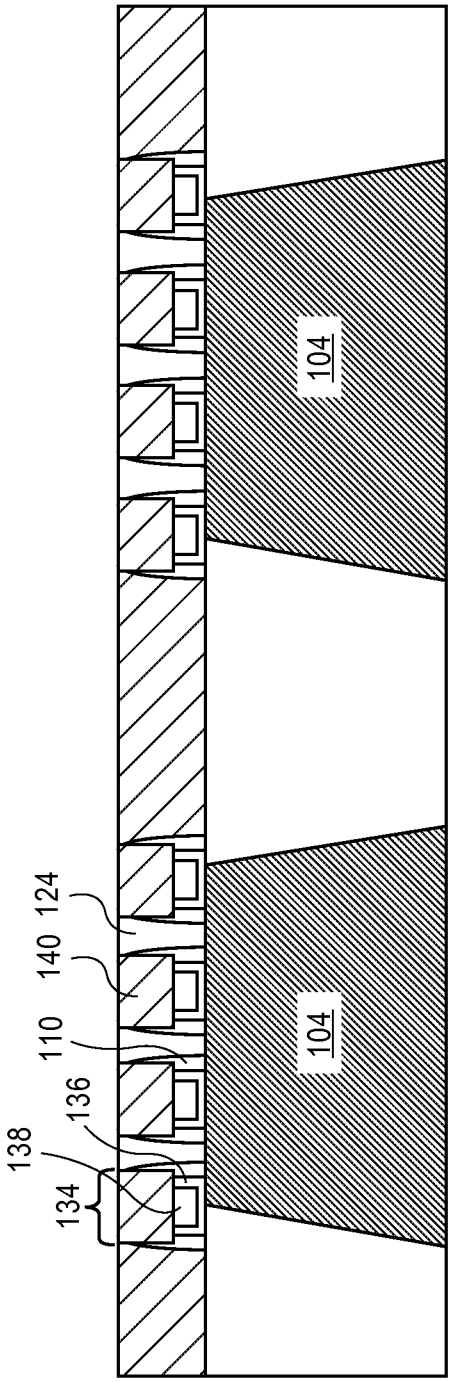


FIG. 1J

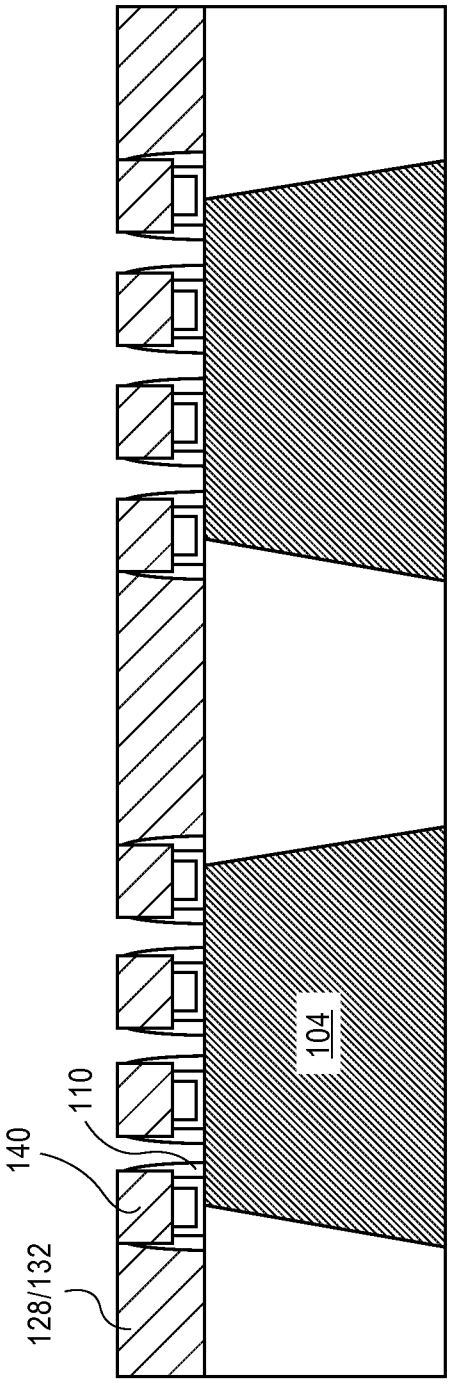


FIG. 1K

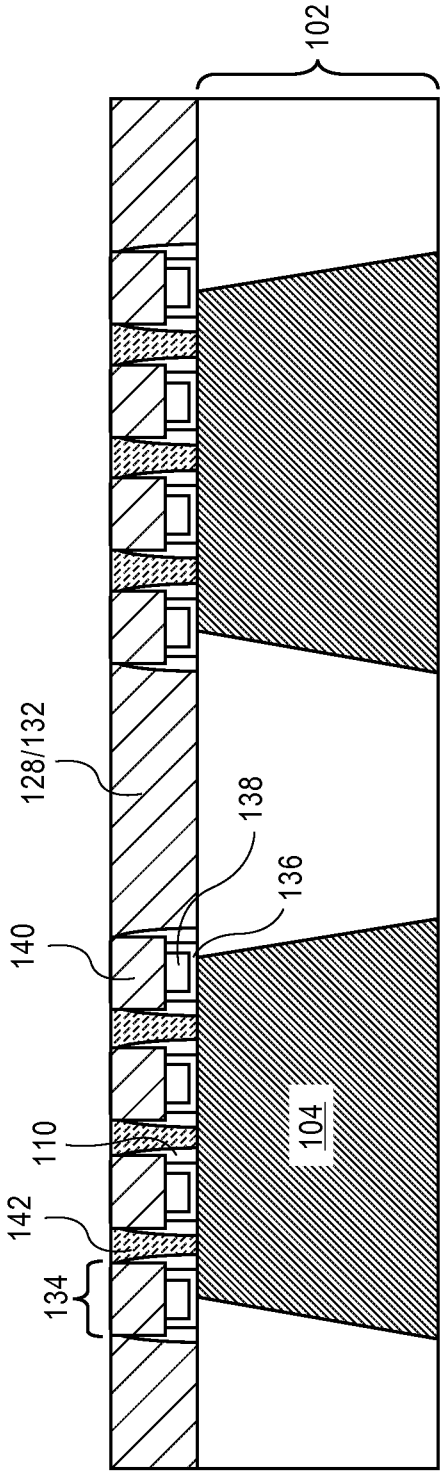


FIG. 2

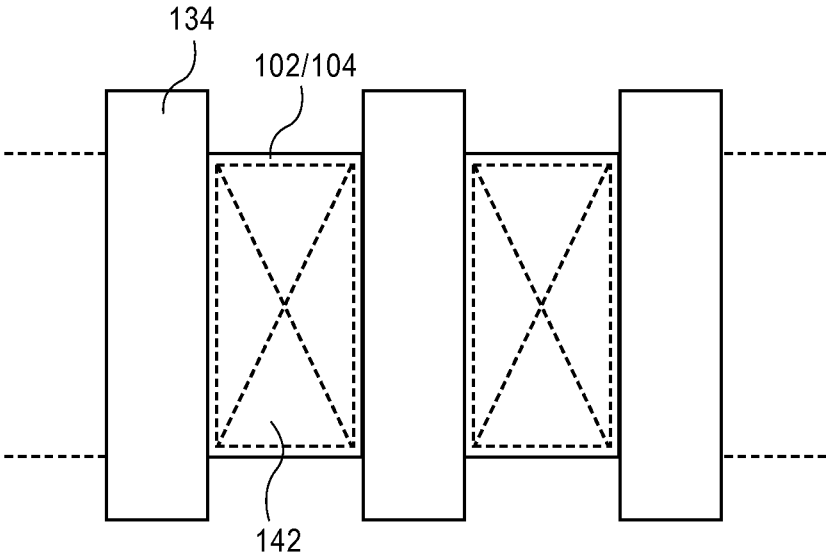


FIG. 3

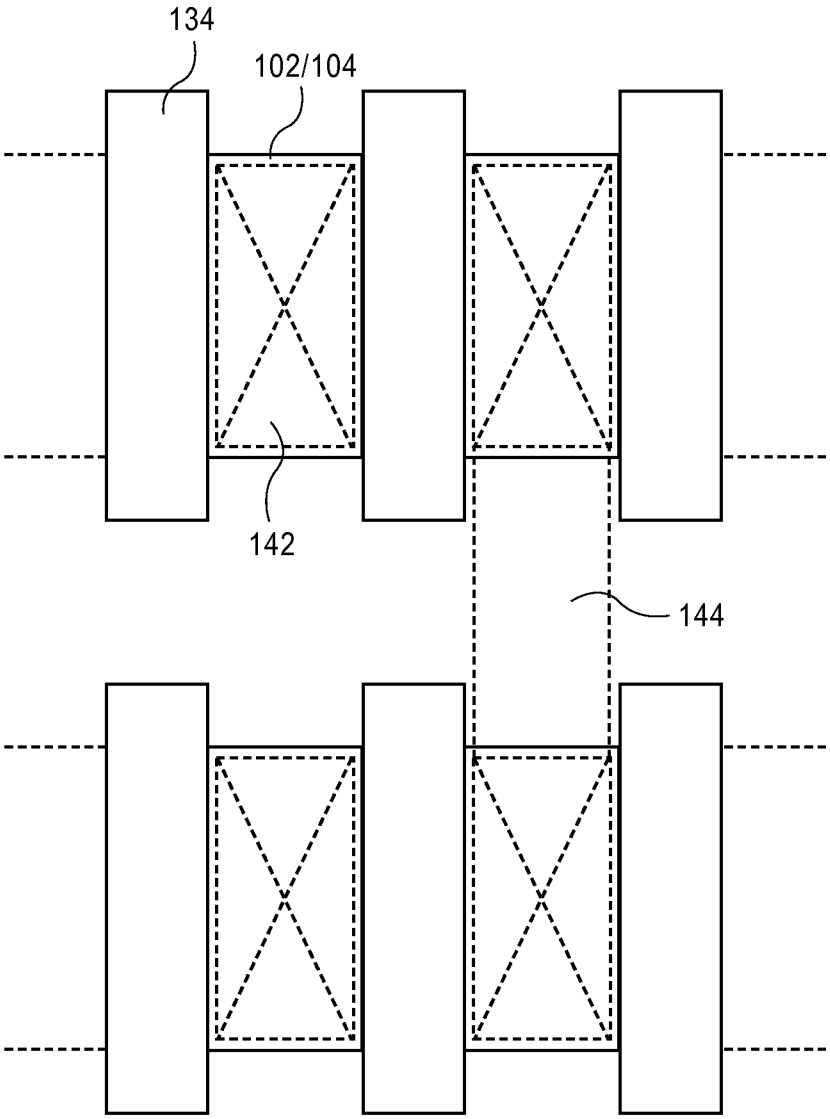


FIG. 4

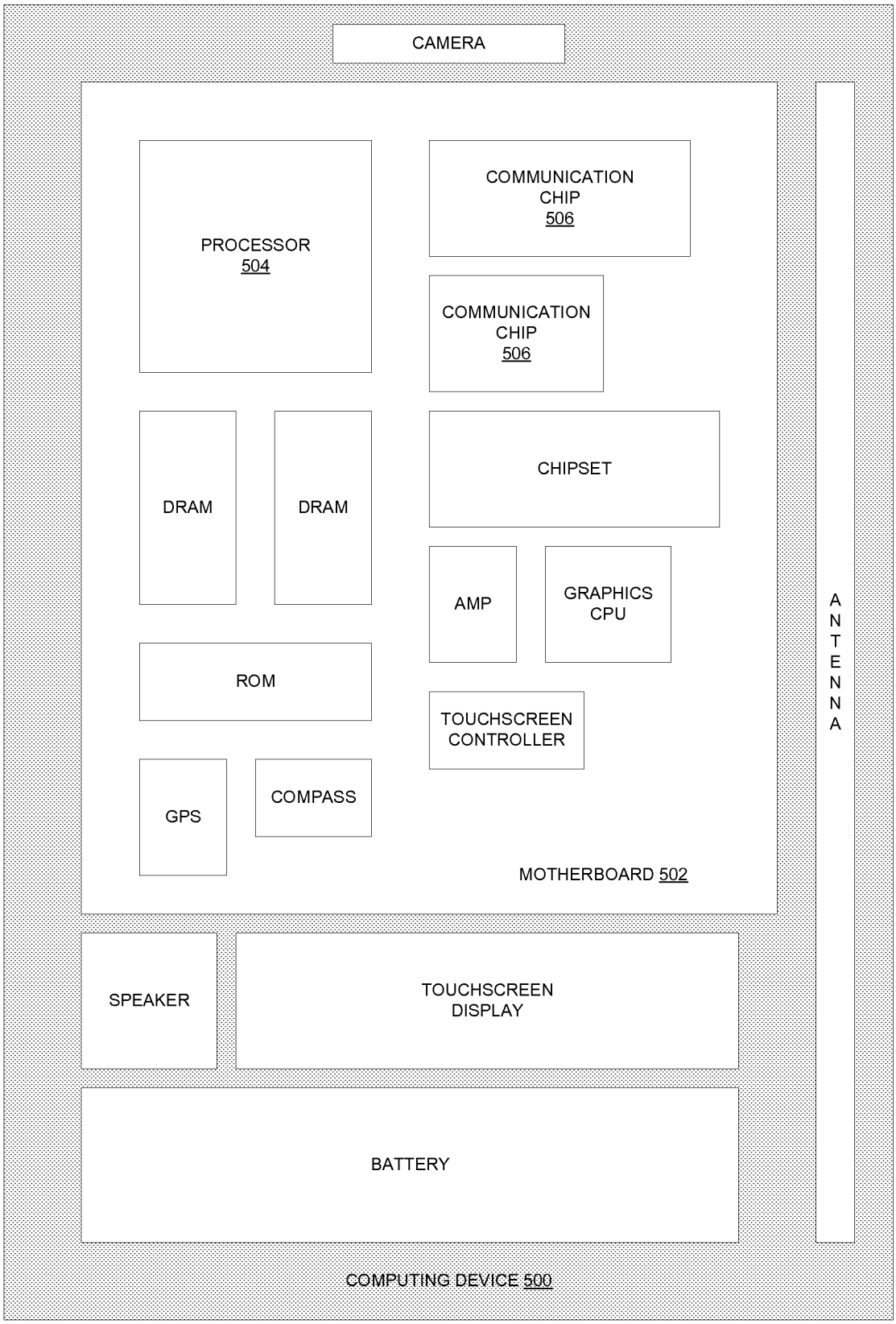

CAMERA
PROCESSOR
504
COMMUNICATION
CHIP
506
COMMUNICATION
CHIP
506
DRAM
DRAM
CHIPSET
AMP
GRAPHICS
CPU
ROM
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD 502
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE 500

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/066989

A. CLASSIFICATION OF SUBJECT MATTER

HOIL 21/28(2006.01)i, HOIL 21/3205(2006.01)1, HOIL 29/78(2006.01)1, HOIL 21/336(2006.01)1

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

HOIL 21/28; HOIL 27/1 15; HOIL 31/1 13; HOIL 21/4763; HOIL 21/8242; HOIL 21/8247; HOIL 21/3205

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: gate aligned contacts, plurality gate, spacer, contact plug, and mask

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005-0167758 Al (TAE-HYUK AHN et al.) 04 August 2005 See the abstract, figures 1-8, paragraphs [0034] -[0051] and claims 10-16.	1-30
A	KR 10-2011-0069305 A (DONGBU HITEK CO., LTD.) 23 June 2011 See the abstract, figures 1-2, pages 3-4 and claims 1-12.	1-30
A	US 2002-0055222 Al (MYEONG-CHEOL KIM et al.) 09 May 2002 See the abstract, figures 1-10, paragraphs [0026]-[0026] and claims 1-10.	1-30
A	US 2001-0055867 Al (KYU-HYUN LEE) 27 December 2001 See the abstract, figures 1-4, paragraphs [0029] -[0040] and claims 1-7.	1-30

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 AUGUST 2012 (16.08.2012)	**17 AUGUST 2012 (17.08.2012)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-70 1, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

Kim, Sang-Taek

Telephone No. 82-42-481-8623

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2011/066989

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