United States Patent [19]

Tomisawa et al.

[11] **3,890,602**

[45] **June 17, 1975**

[54] **WAVEFORM PRODUCING DEVICE**

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[73] Assignee: **Nippon Gakki Seizo Kabushiki Kaisha,** Shizuoka, Japan

[22] Filed: **Oct. 23, 1973**

[21] Appl. No.: **408,430**

[30] **Foreign Application Priority Data**

Oct. 25, 1972 Japan 47-106945
Oct. 25, 1972 Japan 47-106946
Oct. 25, 1972 Japan 47-106947
Oct. 25, 1972 Japan 47-106948

[52] **U.S. Cl.** ..... **340/173 R;** 338/22 SD
[51] **Int. Cl.** **G11c 11/40**
[58] **Field of Search** .... 340/173 R, 173 SP, 173 DR; 338/17, 22 SD

[56] **References Cited**

UNITED STATES PATENTS

3,721,964 3/1973 Barrett ..... 340/173 R
3,735,367 5/1973 Bennett ..... 340/173 R

Primary Examiner—Terrell W. Fears
Attorney, Agent, or Firm—Holman & Stern

[57] **ABSTRACT**

A single resistor bar having a plurality of connection points is formed by a diffused layer on a semiconduuctor substrate. A predetermined voltage is applied across the resistance layer so that the respective connection points exhibit different potentials. A decoder designates, via a reading switch circuit and successively at a predetermined time rate and order, which of the potentials to read out. Thus sequentially readout voltages constitute a waveform of a particular tone color or an envelope of a particular shape. The decoder and the reading switch circuit may be formed by MOS transistors, and the circuits thus formed may be combined together with the resistance layer in an integrated structure on the semiconductor substrate.

8 Claims, 29 Drawing Figures

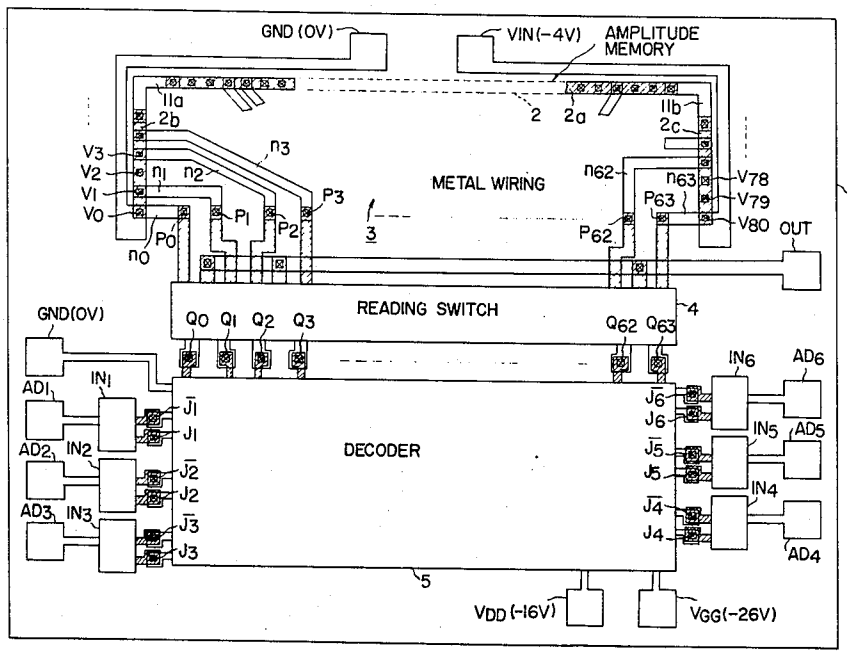


FIG. 1

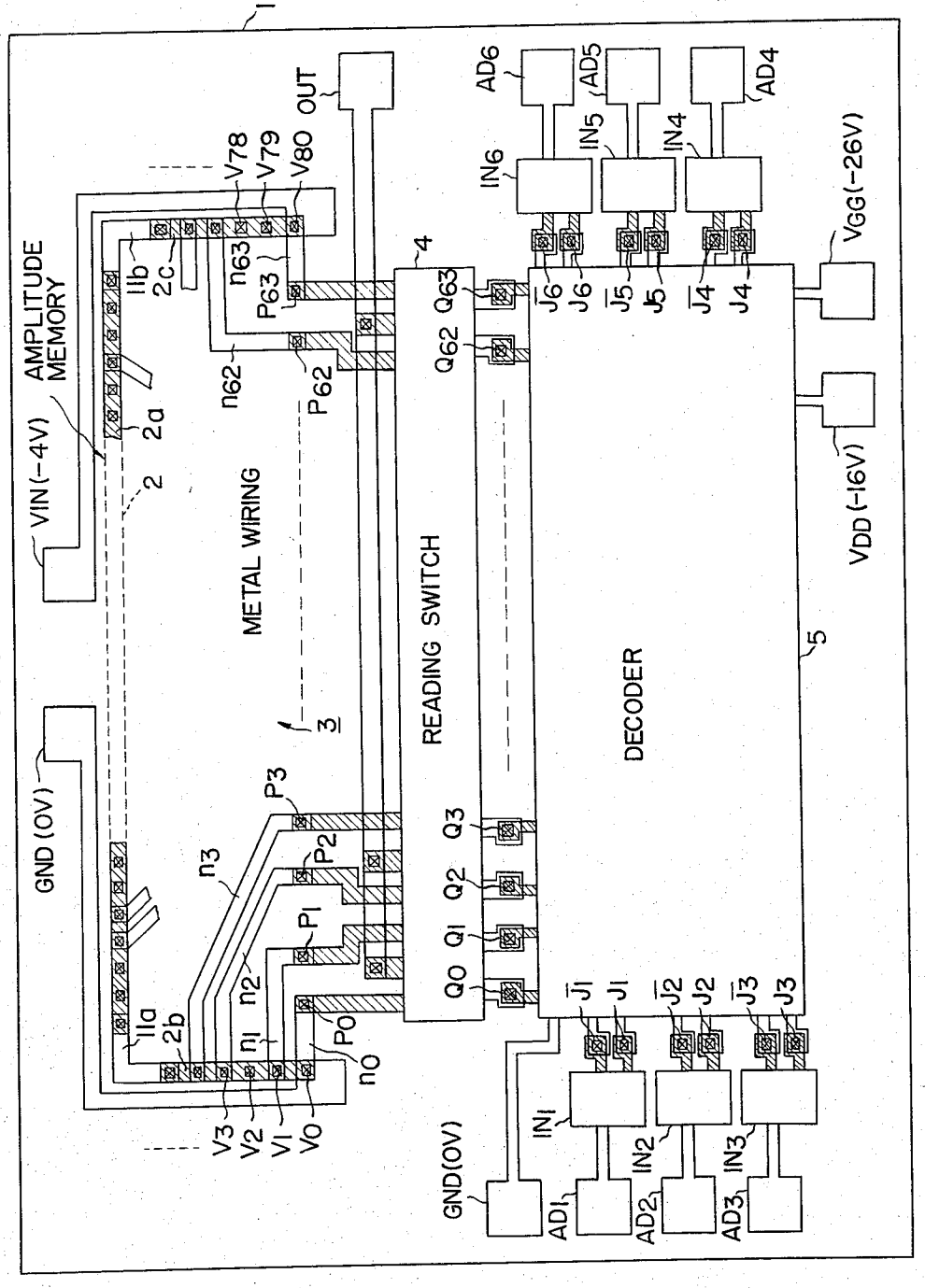

1
AMPLITUDE MEMORY
VIN(-4V)
2
2a
2b
2c
11a
11b
METAL WIRING
3
READING SWITCH
4
DECODER
5
GND (OV)
OUT
V78
V79
V80
V3
V2
V1
V0
n63
P63
n62
P62
n3
P3
n2
P2
n1
P1
n0
P0
Q63
Q62
Q3
Q2
Q1
Q0
AD6
AD5
AD4
IN6
IN5
IN4
J6
J5
J4
VGG(-26V)
VDD(-16V)
J1
J2
J3
IN1
IN2
IN3
AD1
AD2
AD3
GND(OV)

FIG. 2

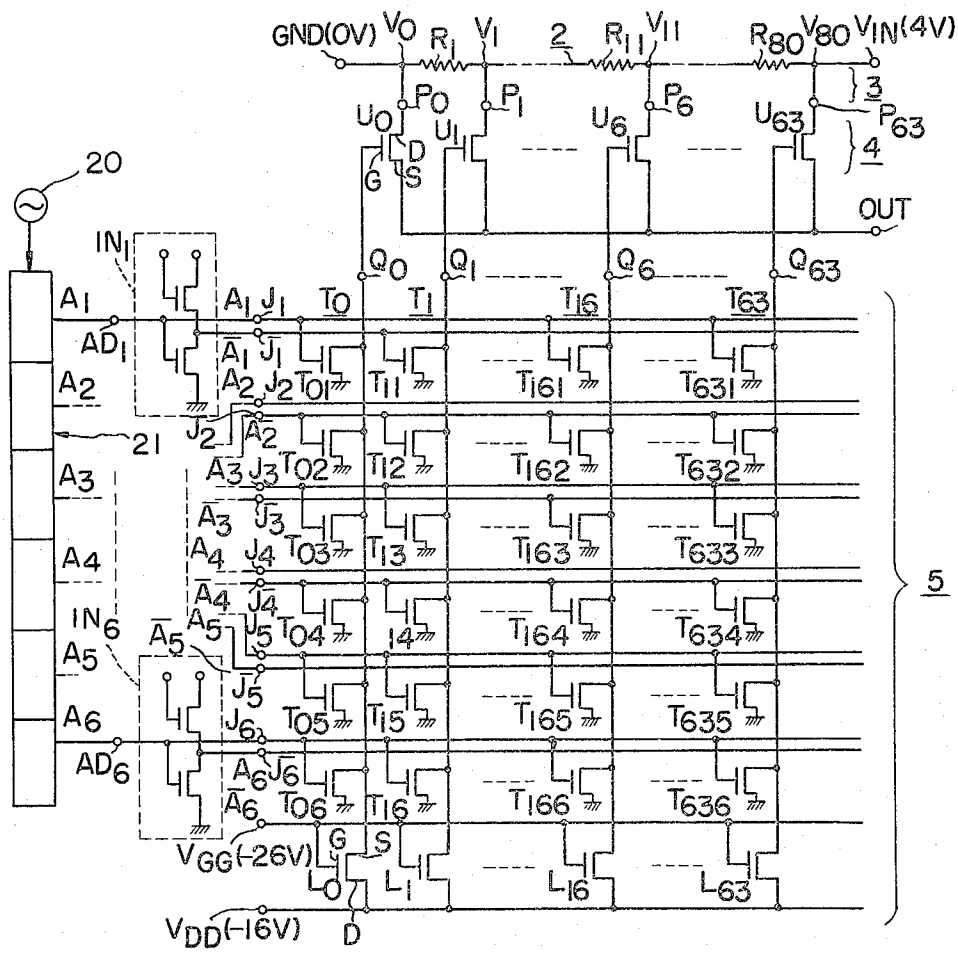

GND(0V)
V_O
R_1
V_1
2
R_{11}
V_{11}
R_{80}
V_{80}
V_{IN}(4V)
3
4
U_O
U_1
U_6
U_{63}
P_O
P_1
P_6
P_{63}
G
D
S
OUT
20
21
IN_1
IN_6
Q_O
Q_1
Q_6
Q_{63}
A_1
AD_1
A_2
A_3
A_4
A_5
A_6
AD_6
$\bar{A}_1$ J_1 T_O T_1 T_{16} T_{63}
$\bar{A}_2$ J_2 T_{01} T_{11} T_{161} T_{631}
$\bar{A}_3$ J_3 T_{02} T_{12} T_{162} T_{632}
$\bar{A}_4$ J_4 T_{03} T_{13} T_{163} T_{633}
$\bar{A}_5$ J_5 T_{04} T_{14} T_{164} T_{634}
$\bar{A}_6$ J_6 T_{05} T_{15} T_{165} T_{635}
T_{06} T_{16} T_{166} T_{636}
V_{GG}(-26V)
V_{DD}(-16V)
L_O L_1 L_{16} L_{63}
5

FIG. 3

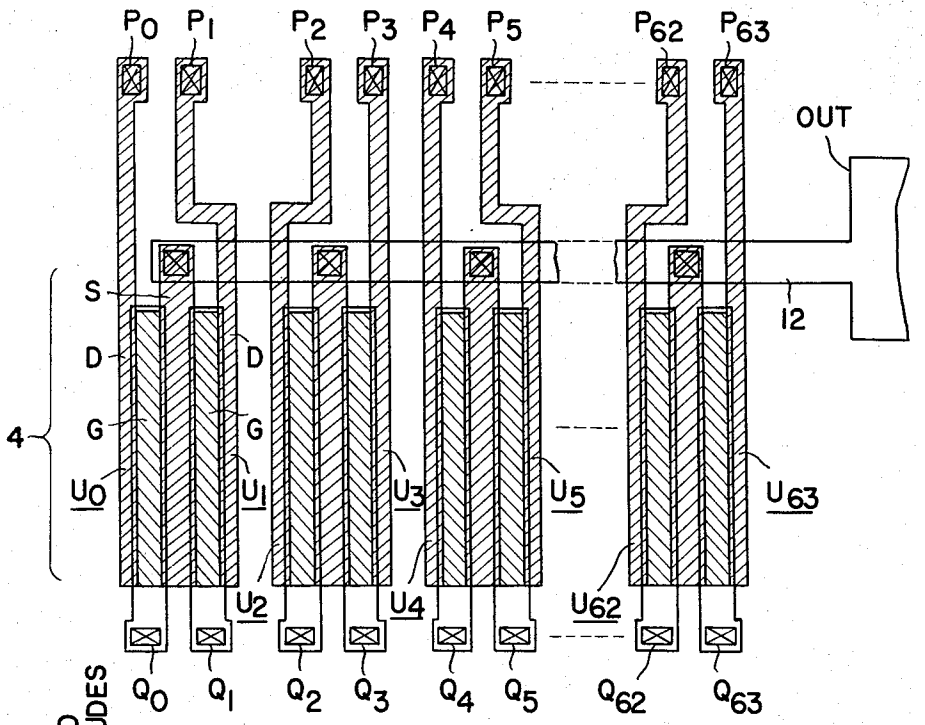

P0 P1 P2 P3 P4 P5 P62 P63
OUT
S
D
G
4
U0 U1 U2 U3 U4 U5 U62 U63
12
Q0 Q1 Q2 Q3 Q4 Q5 Q62 Q63

FIG. 4

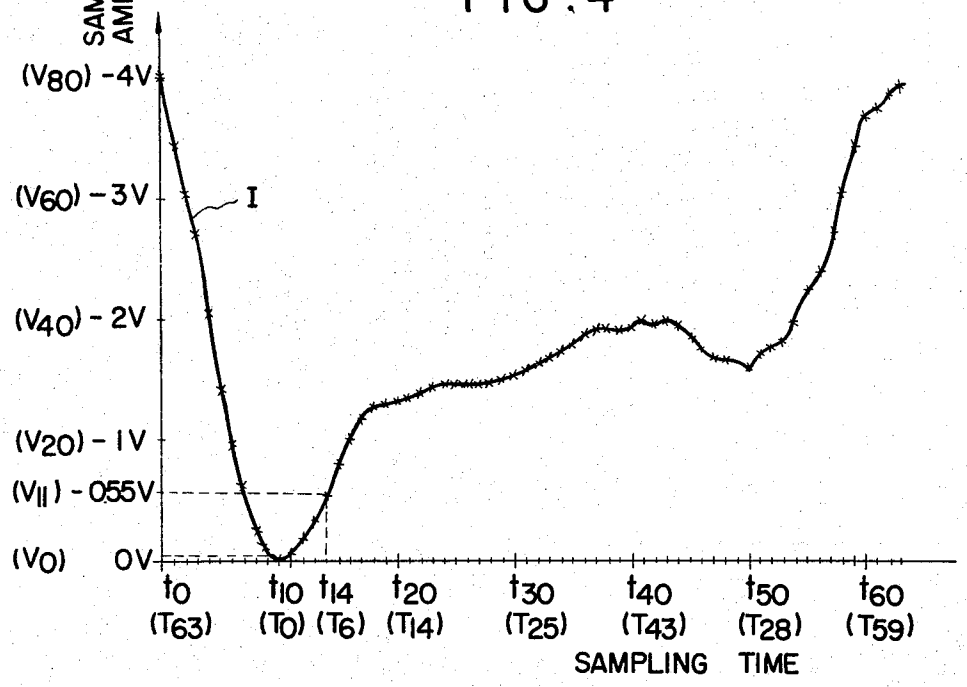

SAMPLED AMPLITUDES
(V80) -4V
(V60) -3V
(V40) -2V
(V20) -1V
(V11) -055V
(V0) 0V
I
t0 (T63)
t10 (T0)
t14 (T6)
t20 (T14)
t30 (T25)
t40 (T43)
t50 (T28)
t60 (T59)
SAMPLING TIME

FIG. 5

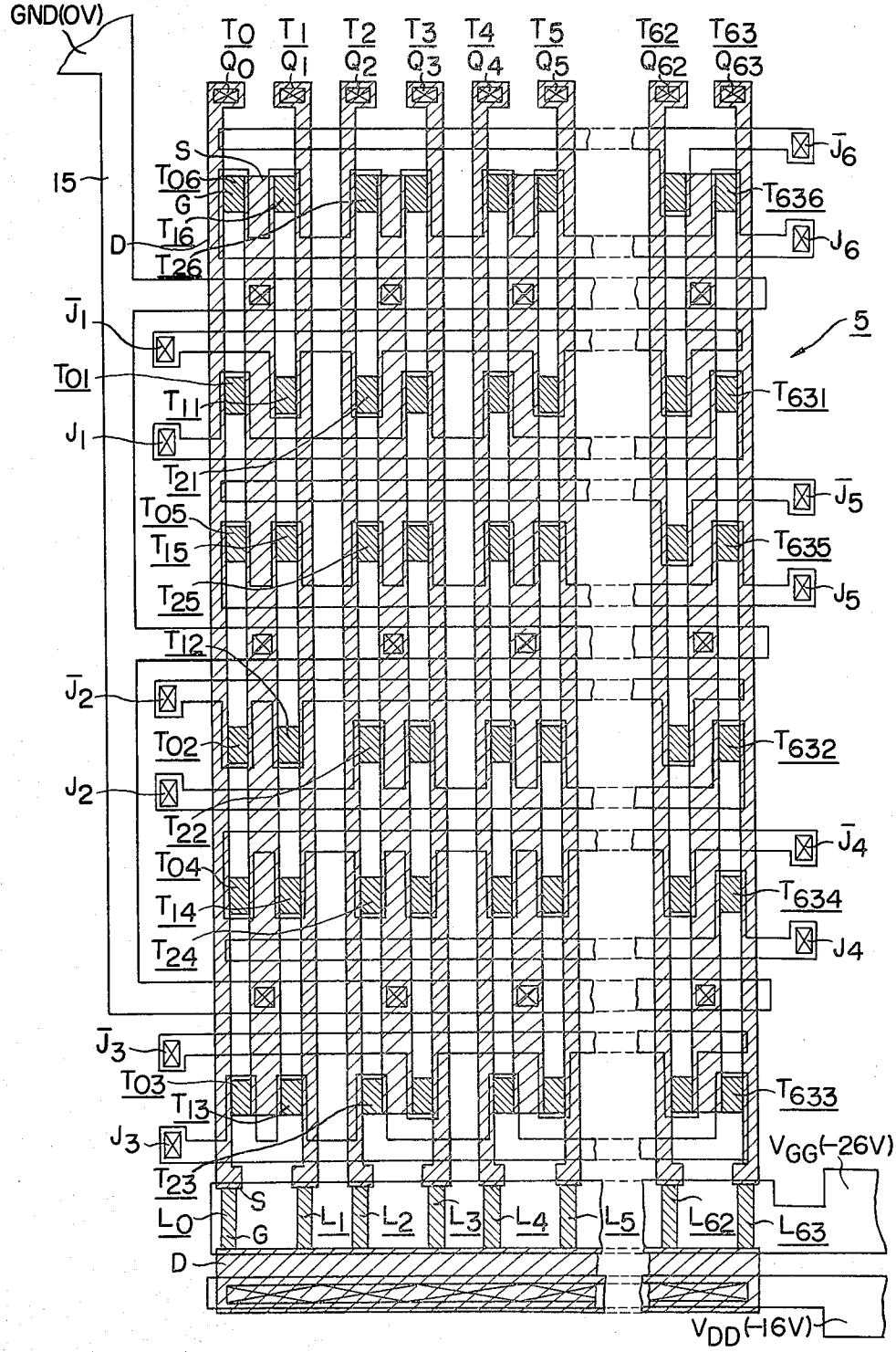

GND(0V)
T0 Q0
T1 Q1
T2 Q2
T3 Q3
T4 Q4
T5 Q5
T62 Q62
T63 Q63
15
S
T06
G
T16
D
T26
J1
T01
T11
J1
T21
T05
T15
T25
T12
J2
T02
J2
T22
T04
T14
T24
J3
T03
T13
J3
T23
S
L0
G
D
L1
L2
L3
L4
L5
L62
L63
J6
T636
J6
5
T631
J5
T635
J5
T632
J4
T634
J4
T633
VGG(-26V)
VDD(-16V)

FIG. 6(A)

TRANSISTOR GROUB	BIT NO 1	2	3	4	5	6
T0	J1	$\overline{J2}$	J3	$\overline{J4}$	J5	J6
T1	$\overline{J1}$	$\overline{J2}$	J3	$\overline{J4}$	J5	J6
T2	$\overline{J1}$	J2	J3	$\overline{J4}$	J5	J6
T3	$\overline{J1}$	J2	$\overline{J3}$	$\overline{J4}$	J5	J6
T4	J1	J2	J3	$\overline{J4}$	J5	J6
T5	$\overline{J1}$	J2	$\overline{J3}$	$\overline{J4}$	J5	J6
T6	J1	$\overline{J2}$	$\overline{J3}$	$\overline{J4}$	J5	J6
T7	$\overline{J1}$	$\overline{J2}$	$\overline{J3}$	J4	J5	J6
T8	$\overline{J1}$	$\overline{J2}$	$\overline{J3}$	$\overline{J4}$	J5	J6
T9	J1	$\overline{J2}$	$\overline{J3}$	J4	J5	J6
T10	J1	J2	J3	J4	$\overline{J5}$	J6
T11	$\overline{J1}$	J2	J3	J4	$\overline{J5}$	J6
T12	J1	$\overline{J2}$	J3	J4	$\overline{J5}$	J6
T13	$\overline{J1}$	$\overline{J2}$	J3	J4	$\overline{J5}$	J6
T14	J1	J2	$\overline{J3}$	J4	$\overline{J5}$	J6
T15	$\overline{J1}$	J2	$\overline{J3}$	J4	$\overline{J5}$	J6
T16	J1	$\overline{J2}$	$\overline{J3}$	J4	$\overline{J5}$	J6
T17	$\overline{J1}$	J2	$\overline{J3}$	J4	J5	J6
T18	$\overline{J1}$	$\overline{J2}$	$\overline{J3}$	J4	$\overline{J5}$	J6
T19	J1	J2	J3	$\overline{J4}$	$\overline{J5}$	J6
T20	$\overline{J1}$	J2	J3	$\overline{J4}$	$\overline{J5}$	$\overline{J6}$

FIG. 6(B)

TRANSISTOR GROUB	BIT NO 1	2	3	4	5	6
T21	J1	$\overline{J2}$	J3	$\overline{J4}$	$\overline{J5}$	J6
T22	$\overline{J1}$	$\overline{J2}$	J3	$\overline{J4}$	$\overline{J5}$	J6
T23	J1	J2	$\overline{J3}$	$\overline{J4}$	$\overline{J5}$	J6
T24	$\overline{J1}$	J2	$\overline{J3}$	$\overline{J4}$	$\overline{J5}$	J6
T25	J1	$\overline{J2}$	$\overline{J3}$	$\overline{J4}$	$\overline{J5}$	J6
T26	$\overline{J1}$	$\overline{J2}$	$\overline{J3}$	$\overline{J4}$	$\overline{J5}$	J6
T27	J1	J2	J3	J4	J5	$\overline{J6}$
T28	J1	$\overline{J2}$	J3	J4	$\overline{J5}$	$\overline{J6}$
T29	$\overline{J1}$	J2	J3	J4	J5	$\overline{J6}$
T30	$\overline{J1}$	$\overline{J2}$	$\overline{J3}$	$\overline{J4}$	J5	$\overline{J6}$
T31	J1	J2	J3	J4	$\overline{J5}$	$\overline{J6}$
T32	$\overline{J1}$	J2	J3	J4	$\overline{J5}$	$\overline{J6}$
T33	J1	$\overline{J2}$	J3	J4	J5	$\overline{J6}$
T34	$\overline{J1}$	$\overline{J2}$	J3	J4	$\overline{J5}$	$\overline{J6}$
T35	J1	$\overline{J2}$	$\overline{J3}$	$\overline{J4}$	J5	$\overline{J6}$
T36	J1	J2	$\overline{J3}$	J4	$\overline{J5}$	$\overline{J6}$
T37	$\overline{J1}$	$\overline{J2}$	J3	J4	J5	$\overline{J6}$
T38	$\overline{J1}$	J2	$\overline{J3}$	J4	$\overline{J5}$	$\overline{J6}$
T39	J1	J2	$\overline{J3}$	J4	J5	$\overline{J6}$
T40	$\overline{J1}$	J2	$\overline{J3}$	$\overline{J4}$	J5	$\overline{J6}$
T41	$\overline{J1}$	J2	$\overline{J3}$	J4	J5	$\overline{J6}$

FIG. 6(C)

TRANSISTOR GROUP	BIT NO 1	2	3	4	5	6
T42	$\overline{J1}$	$\overline{J2}$	$\overline{J3}$	J4	J5	$\overline{J6}$
T43	J1	J2	J3	$\overline{J4}$	J5	$\overline{J6}$
T44	J1	$\overline{J2}$	$\overline{J3}$	J4	J5	$\overline{J6}$
T45	J1	$\overline{J2}$	J3	$\overline{J4}$	J5	$\overline{J6}$
T46	J1	J2	$\overline{J3}$	$\overline{J4}$	J5	$\overline{J6}$
T47	J1	$\overline{J2}$	$\overline{J3}$	J4	$\overline{J5}$	$\overline{J6}$
T48	$\overline{J1}$	J2	J3	$\overline{J4}$	J5	$\overline{J6}$
T49	$\overline{J1}$	$\overline{J2}$	J3	$\overline{J4}$	J5	$\overline{J6}$
T50	J1	J2	$\overline{J3}$	J4	J5	J6
T51	$\overline{J1}$	$\overline{J2}$	$\overline{J3}$	J4	$\overline{J5}$	$\overline{J6}$
T52	J1	J2	J3	$\overline{J4}$	$\overline{J5}$	$\overline{J6}$
T53	$\overline{J1}$	$\overline{J2}$	J3	J4	J5	J6
T54	$\overline{J1}$	J2	J3	$\overline{J4}$	$\overline{J5}$	$\overline{J6}$
T55	J1	$\overline{J2}$	J3	J4	J5	J6
T56	J1	$\overline{J2}$	J3	$\overline{J4}$	$\overline{J5}$	$\overline{J6}$
T57	$\overline{J1}$	J2	J3	J4	J5	J6
T58	$\overline{J1}$	$\overline{J2}$	J3	$\overline{J4}$	$\overline{J5}$	$\overline{J6}$
T59	J1	J2	$\overline{J3}$	$\overline{J4}$	$\overline{J5}$	$\overline{J6}$
T60	$\overline{J1}$	J2	$\overline{J3}$	$\overline{J4}$	$\overline{J5}$	$\overline{J6}$
T61	J1	$\overline{J2}$	$\overline{J3}$	$\overline{J4}$	$\overline{J5}$	$\overline{J6}$
T62	$\overline{J1}$	$\overline{J2}$	$\overline{J3}$	$\overline{J4}$	$\overline{J5}$	$\overline{J6}$
T63	J1	J2	J3	J4	J5	J6

FIG. 7(A)

TIME INSTANT	A1	A2	A3	A4	A5	A6
t_0	0	0	0	0	0	0
t_1	1	0	0	0	0	0
t_2	0	1	0	0	0	0
t_3	1	1	0	0	0	0
t_4	0	0	1	0	0	0
t_5	1	0	1	0	0	0
t_6	0	1	1	0	0	0
t_7	1	1	1	0	0	0
t_8	0	0	0	1	0	0
t_9	1	0	0	1	0	0
t_{10}	0	1	0	1	0	0
t_{11}	1	1	0	1	0	0
t_{12}	0	0	1	1	0	0
t_{13}	1	0	1	1	0	0
t_{14}	0	1	1	1	0	0
t_{15}	1	1	1	1	0	0
t_{16}	0	0	0	0	1	0
t_{17}	1	0	0	0	1	0
t_{18}	0	1	0	0	1	0
t_{19}	1	1	0	0	1	0
t_{20}	0	0	1	0	1	0

FIG. 7(B)

TIME INSTANT	A1	A2	A3	A4	A5	A6
t21	1	0	1	0	1	0
t22	0	1	1	0	1	0
t23	1	1	1	0	1	0
t24	0	0	0	1	1	0
t25	1	0	0	1	1	0
t26	0	1	0	1	1	0
t27	1	1	0	1	1	0
t28	0	0	1	1	1	0
t29	1	0	1	1	1	0
t30	0	1	1	1	1	0
t31	1	1	1	1	1	0
t32	0	0	0	0	0	1
t33	1	0	0	0	0	1
t34	0	1	0	0	0	1
t35	1	1	0	0	0	1
t36	0	0	1	0	0	1
t37	1	0	1	0	0	1
t38	0	1	1	0	0	1
t39	1	1	1	0	0	1
t40	0	0	0	1	0	1
t41	1	0	0	1	0	1

FIG. 7(C)

TIME INSTANT	A1	A2	A3	A4	A5	A6
t42	0	1	0	1	0	1
t43	1	1	0	1	0	1
t44	0	0	1	1	0	1
t45	1	0	1	1	0	1
t46	0	1	1	1	0	1
t47	1	1	1	1	0	1
t48	0	0	0	0	1	1
t49	1	0	0	0	1	1
t50	0	1	0	0	1	1
t51	1	1	0	0	1	1
t52	0	0	1	0	1	1
t53	1	0	1	0	1	1
t54	0	1	1	0	1	1
t55	1	1	1	0	1	1
t56	0	0	0	1	1	1
t57	1	0	0	1	1	1
t58	0	1	0	1	1	1
t59	1	1	0	1	1	1
t60	0	0	1	1	1	1
t61	1	0	1	1	1	1
t62	0	1	1	1	1	1
t63	1	1	1	1	1	1

FIG. 8(A)

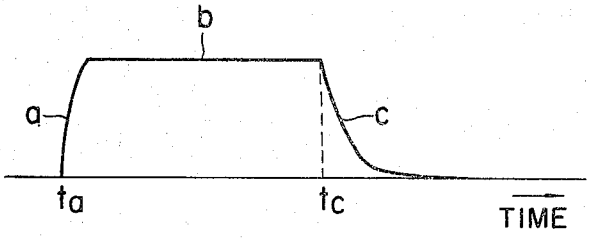


FIG. 8(B)

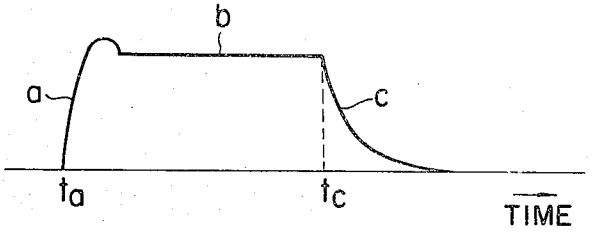


FIG. 8(C)

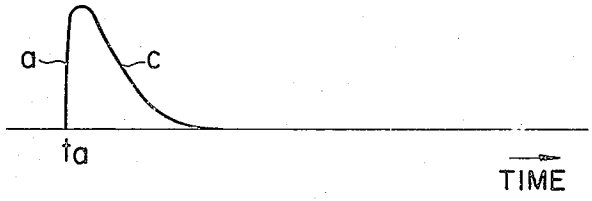


FIG. 12

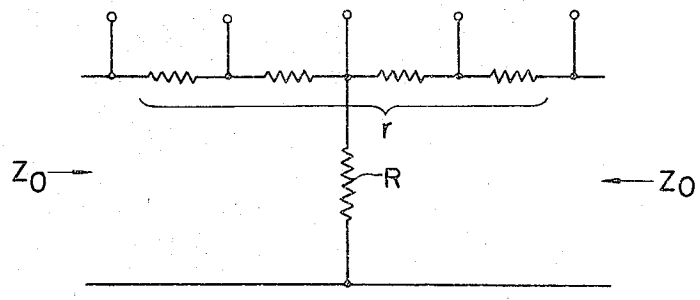
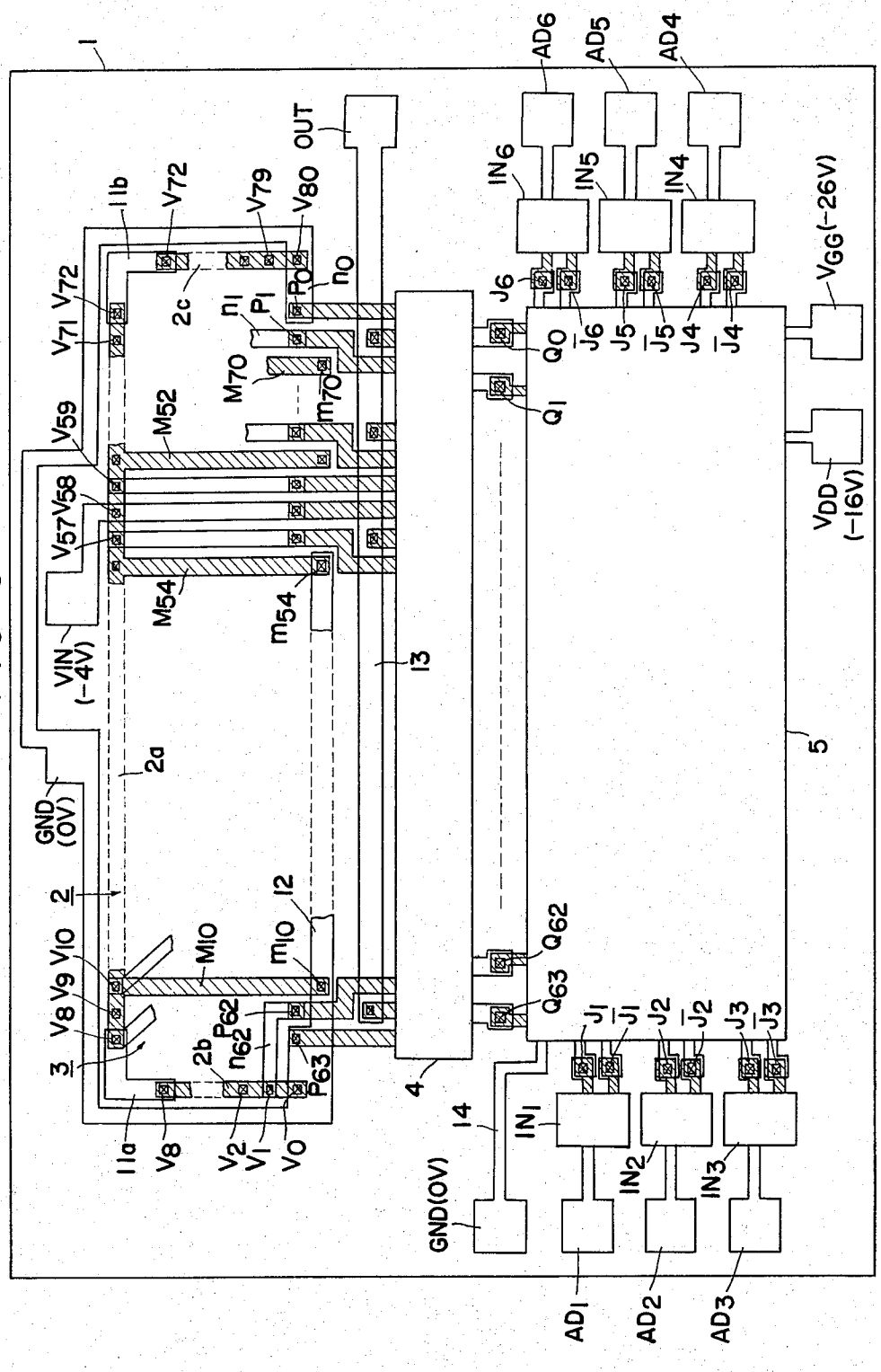


FIG. 9


1
AD6
AD5
AD4
OUT
IN6
IN5
IN4
VGG(-26V)
11b
V72
V79
V80
J6
J5
J4
2c
n1
P1
P0
n0
Q0
Q1
V71
V72
M70
m70
M52
V59
V57
V58
VDD (-16V)
M54
m54
VIN (-4V)
13
5
2a
GND (0V)
2
12
M10
m10
Q62
Q63
V10
V9
V8
J1
J2
J3
3
P62
n62
2b
P63
4
14
IN1
IN2
IN3
GND(0V)
11a
V8
V2
V1
V0
AD1
AD2
AD3

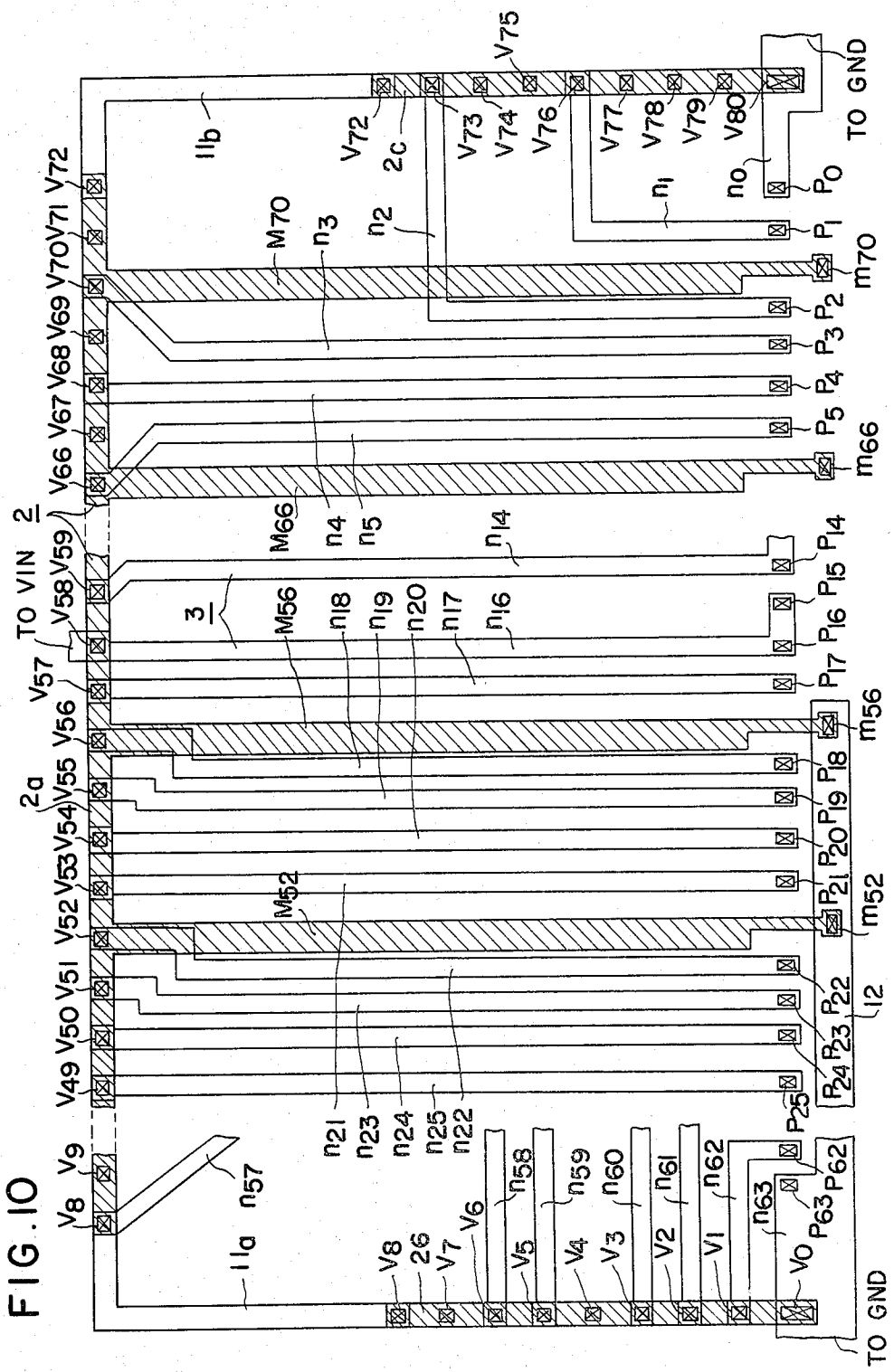

TO VIN
TO GND
TO GND
2
2a
3
11a
11b
12
2c
26
M70
M66
M56
M52
m70
m66
m56
m52
n1
n2
n3
n4
n5
n14
n16
n17
n18
n19
n20
n21
n22
n23
n24
n25
n57
n58
n59
n60
n61
n62
n63
V0
V1
V2
V3
V4
V5
V6
V7
V8
V9
V49
V50
V51
V52
V53
V54
V55
V56
V57
V58
V59
V66
V67
V68
V69
V70
V71
V72
V73
V74
V75
V76
V77
V78
V79
V80
P0
P1
P2
P3
P4
P5
P14
P15
P16
P17
P18
P19
P20
P21
P22
P23
P24
P25
P62
P63

FIG. 10

FIG. 11

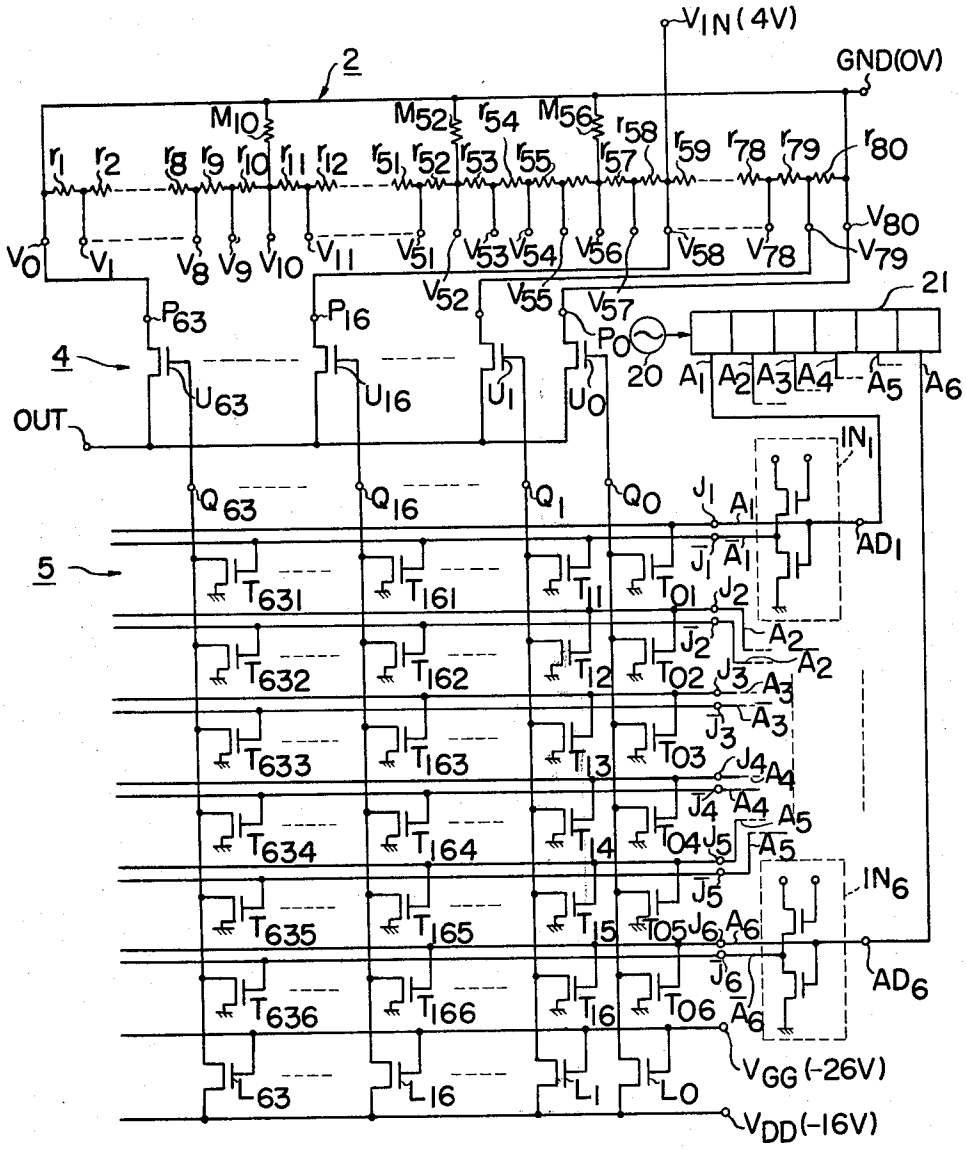
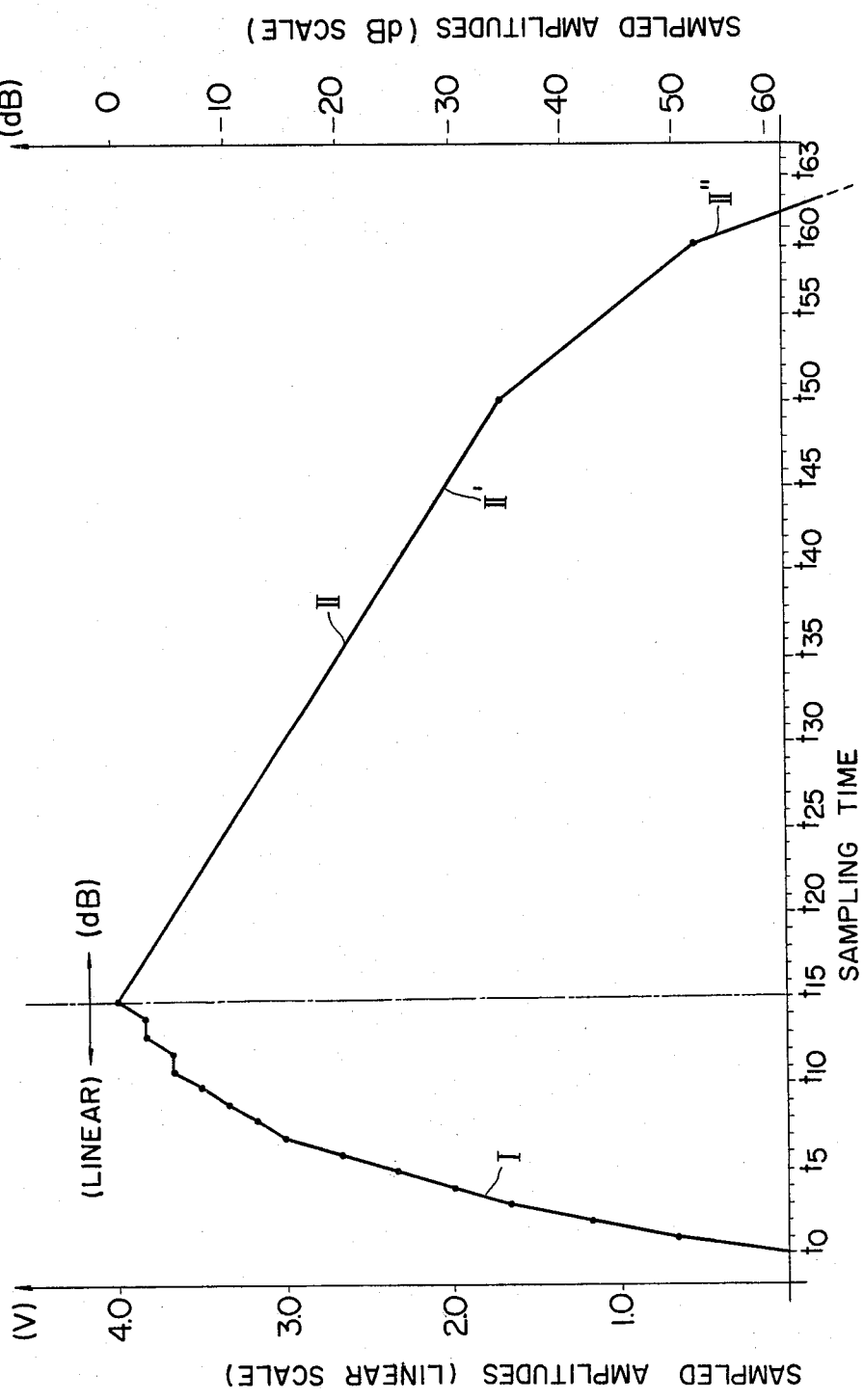

VIN(4V)
GND(0V)
2
M10
M52
r54
M56
r58
r1 r2 r8 r9 r10 r11 r12 r51 r52 r53 r55 r57 r59 r78 r79 r80
V0 V1 V8 V9 V10 V11 V51 V52 V53 V54 V55 V56 V57 V58 V78 V79 V80
P63 P16 P0
4
U63 U16 U1 U0
OUT
20
21
A1 A2 A3 A4 A5 A6
IN1 IN6
AD1 AD6
Q63 Q16 Q1 Q0
J1 A1
5
T631 T161 T11 T01
J2 A2
T632 T162 T12 T02
J3 A3
T633 T163 T13 T03
J4 A4
T634 T164 T14 T04
J5 A5
T635 T165 T15 T05
J6 A6
T636 T166 T16 T06
L63 L16 L1 L0
VGG(-26V)
VDD(-16V)

FIG. 13


SAMPLED AMPLITUDES (dB SCALE)
(dB)
0
-10
-20
-30
-40
-50
-60
II"
II'
II
I
(dB)
(LINEAR)
(V)
4.0
3.0
2.0
1.0
SAMPLED AMPLITUDES (LINEAR SCALE)
t0
t5
t10
t15
t20
t25
t30
t35
t40
t45
t50
t55
t60
t63
SAMPLING TIME

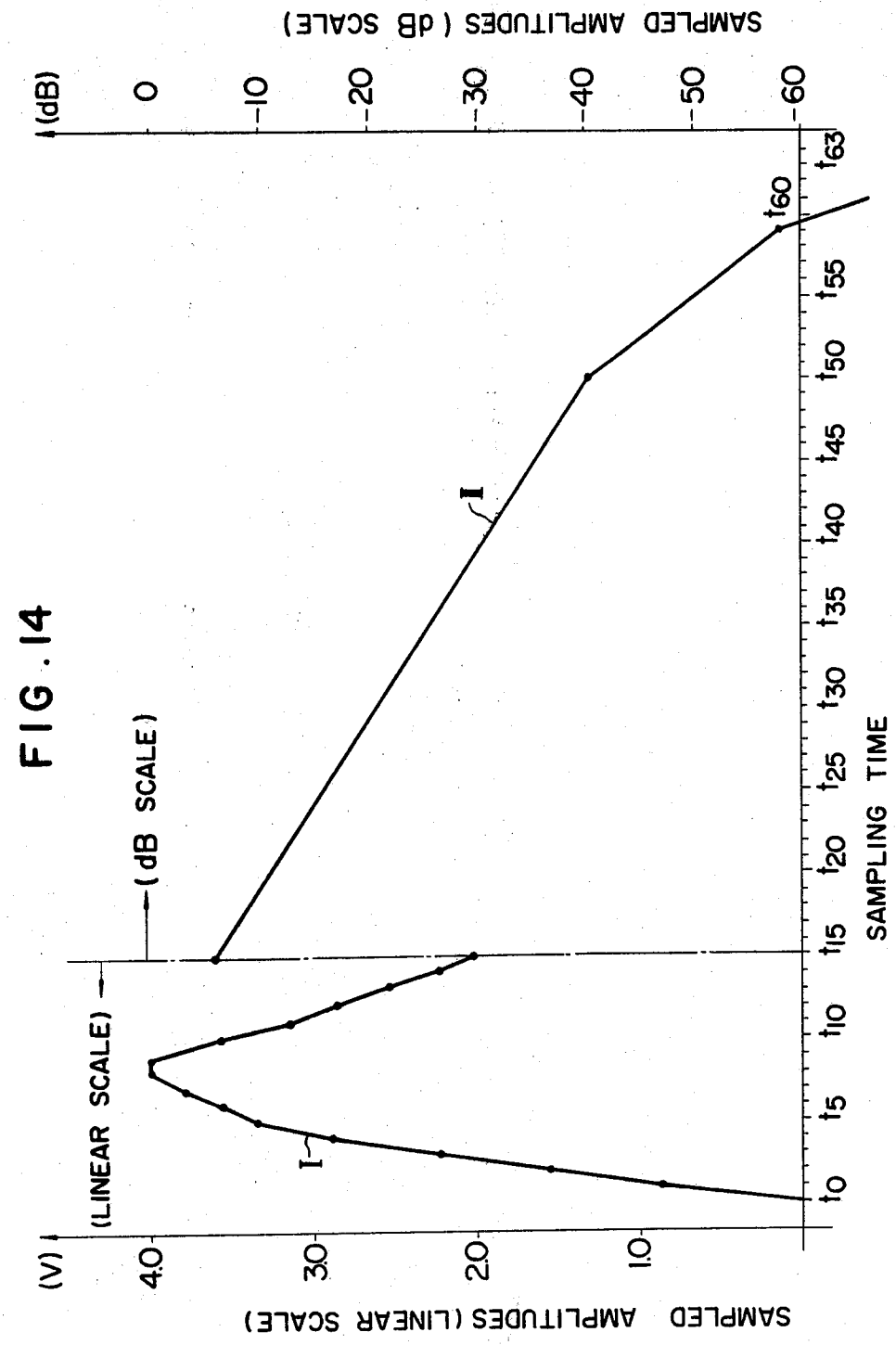

SAMPLED AMPLITUDES (dB SCALE)
(dB)
0
-10
-20
-30
-40
-50
-60
I
(dB SCALE)
(LINEAR SCALE)
I
(V)
4.0
3.0
2.0
1.0
SAMPLED AMPLITUDES (LINEAR SCALE)
t0 t5 t10 t15 t20 t25 t30 t35 t40 t45 t50 t55 t60 t63
SAMPLING TIME

FIG. 14

FIG. 15

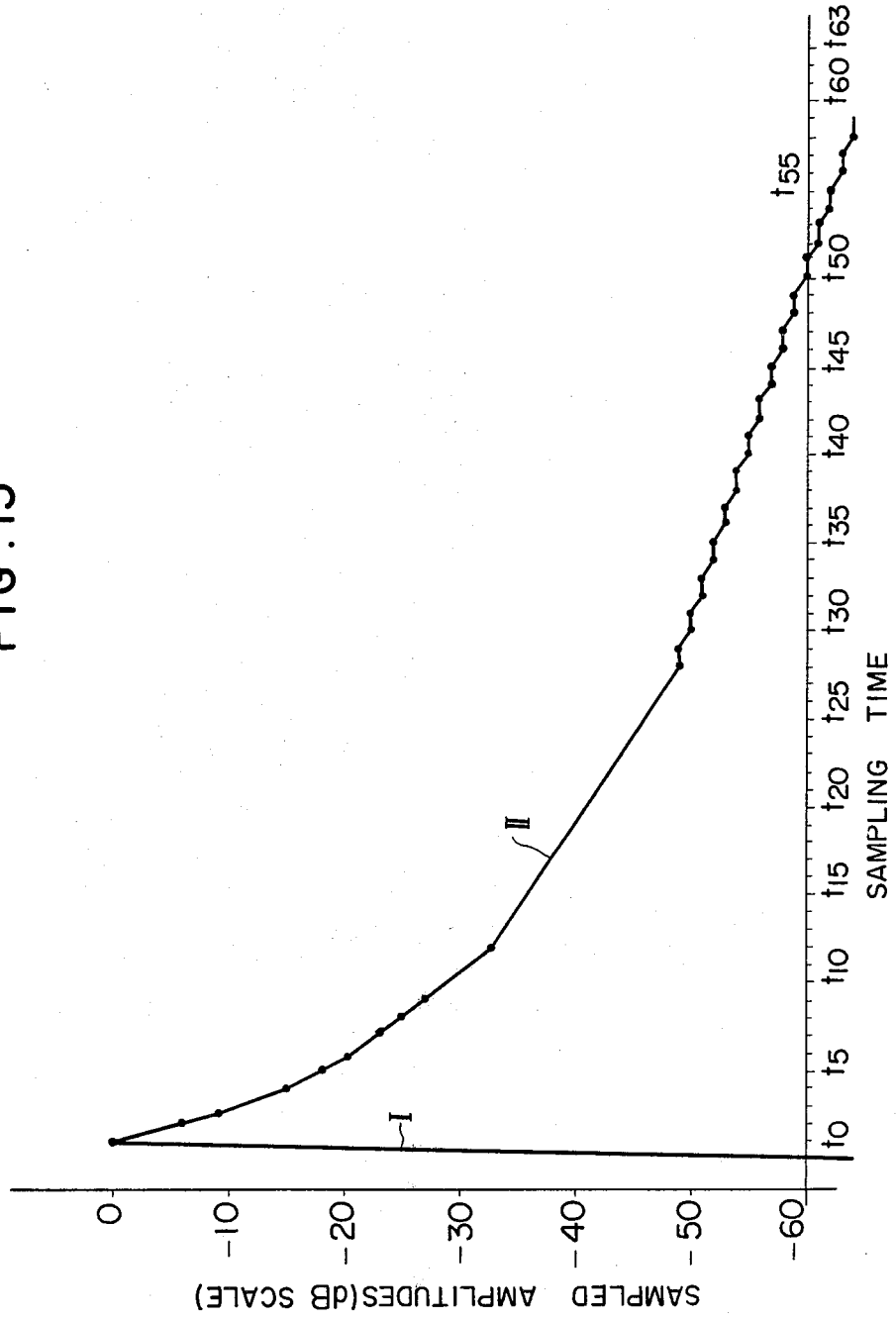

SAMPLED AMPLITUDES(dB SCALE)
0
-10
-20
-30
-40
-50
-60
I
II
t0 t5 t10 t15 t20 t25 t30 t35 t40 t45 t50 t55 t60 t63
SAMPLING TIME

FIG. 16

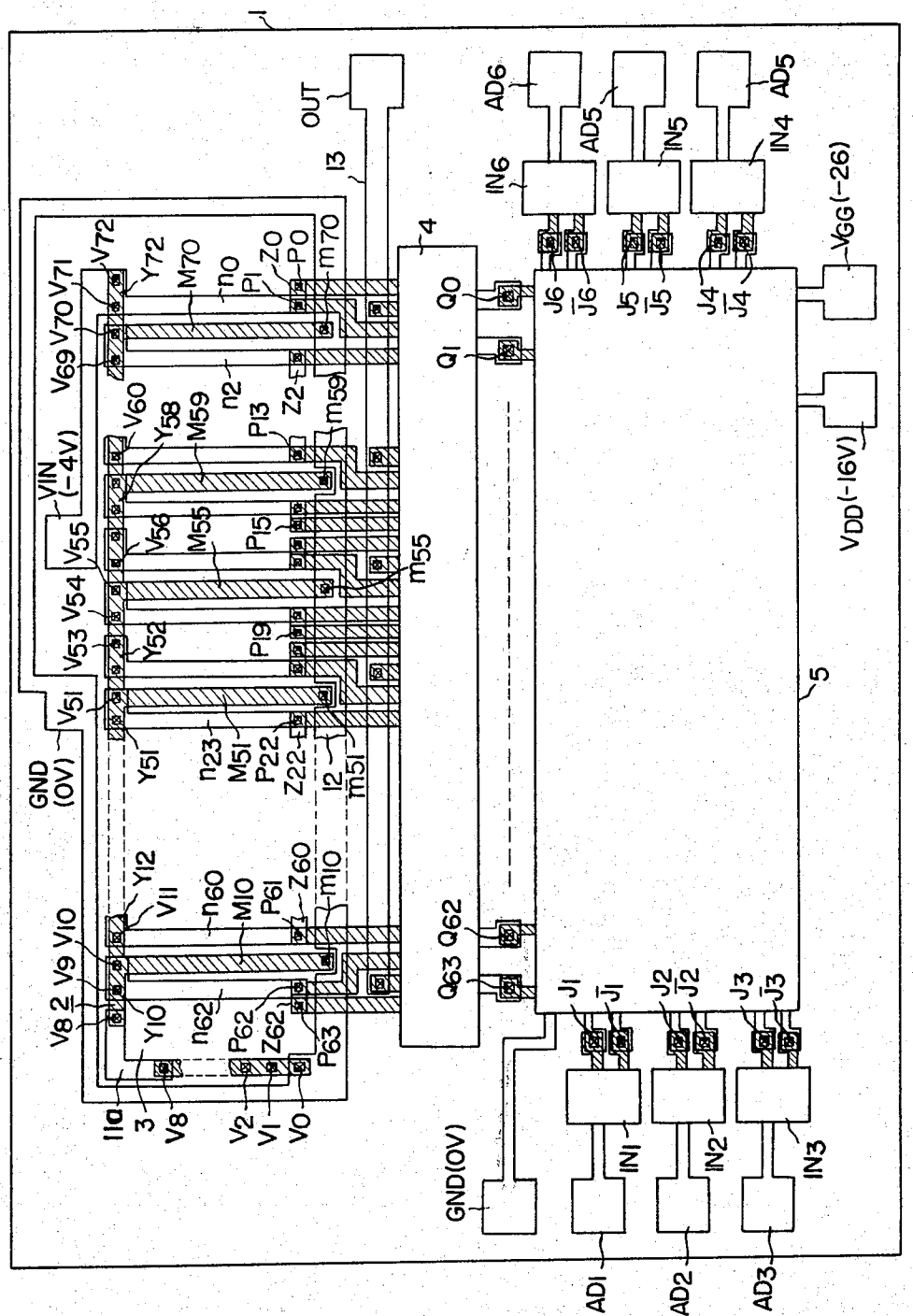

1
OUT
13
4
5
AD6
AD5
AD4
IN6
IN5
IN4
VGG(-26)
VDD(-16V)
VIN (-4V)
GND (0V)
GND(0V)
AD1
AD2
AD3
IN1
IN2
IN3
Q0
Q1
Q62
Q63
J6
J5
J4
J1
J2
J3
V72
V71
V70
V69
V60
V58
V56
V55
V54
V53
V52
V51
V12
V11
V10
V9
V8
V2
V1
V0
Y72
Y58
Y52
Y51
Y12
Y10
M70
M59
M55
M51
M10
n0
n2
n23
n60
n62
P0
P1
P13
P15
P19
P22
P61
P62
P63
Z0
Z2
Z22
Z60
Z62
m70
m59
m55
m51
m10
12
11a
3
V8
V2
V1
V0

FIG. 17

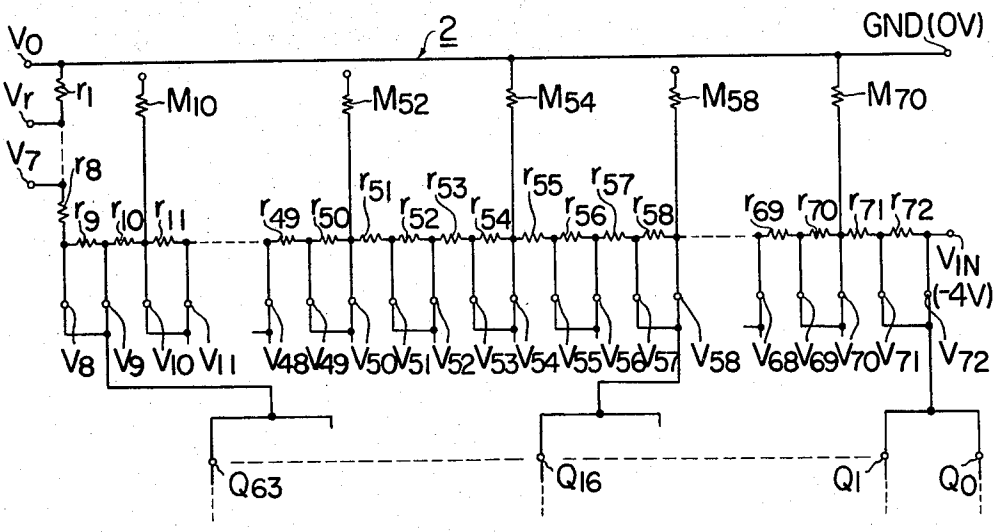

V0
2
GND(0V)
Vr
r1
M10
M52
M54
M58
M70
V7
r8
r9 r10 r11
r49 r50 r51 r52 r53 r54 r55 r56 r57 r58
r69 r70 r71 r72
VIN
(-4V)
V8 V9 V10 V11 V48 V49 V50 V51 V52 V53 V54 V55 V56 V57 V58 V68 V69 V70 V71 V72
Q63
Q16
Q1
Q0

FIG. 18

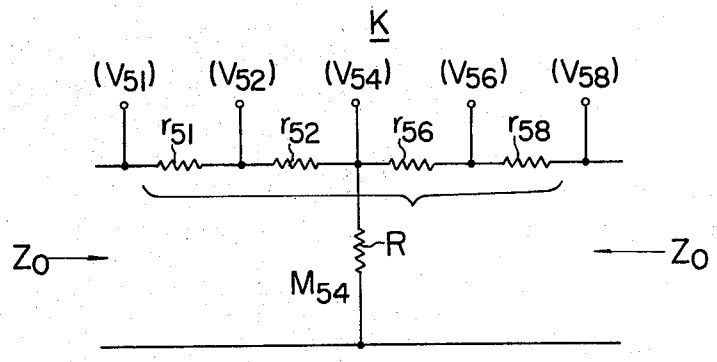
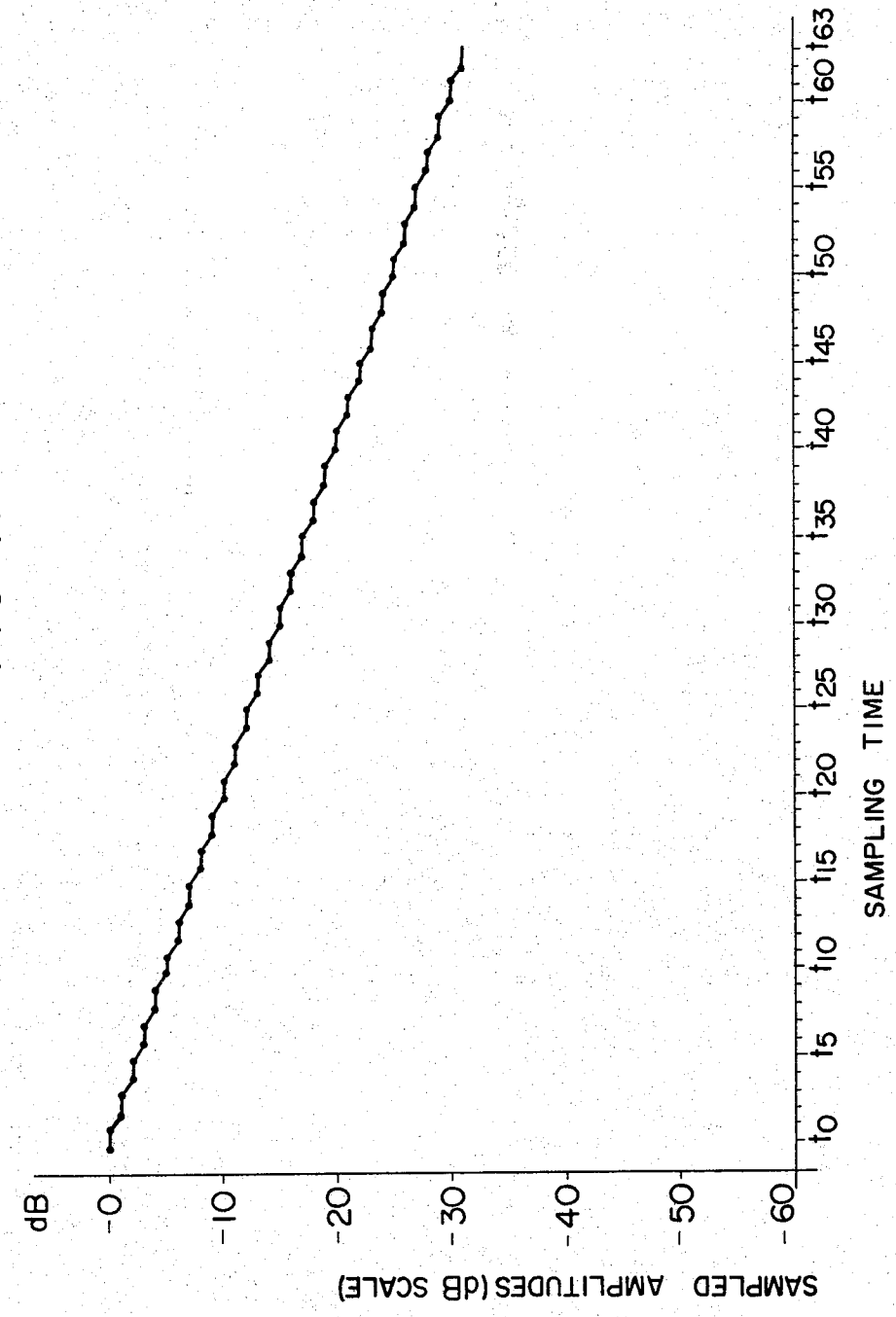

K
(V51) (V52) (V54) (V56) (V58)
r51 r52 r56 r58
R
M54
Z0
Z0

FIG. 19


dB
-0
-10
-20
-30
-40
-50
-60
SAMPLED AMPLITUDES (dB SCALE)
t0
t5
t10
t15
t20
t25
t30
t35
t40
t45
t50
t55
t60
t63
SAMPLING TIME

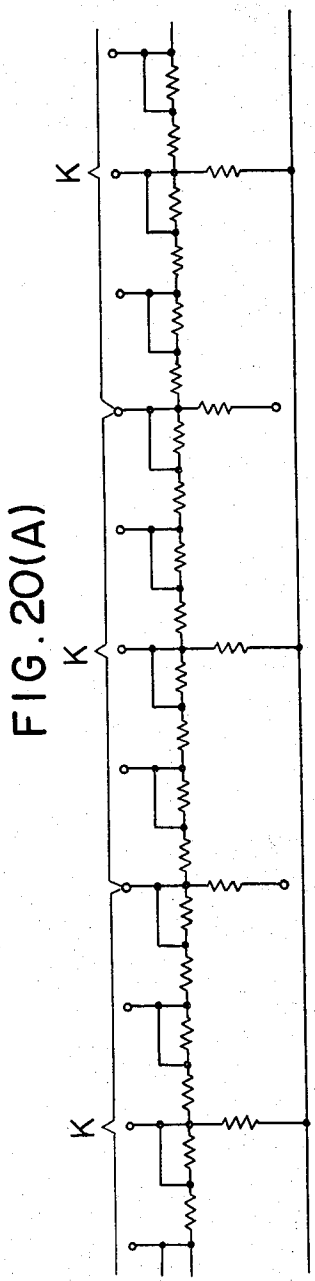


FIG. 20(A)

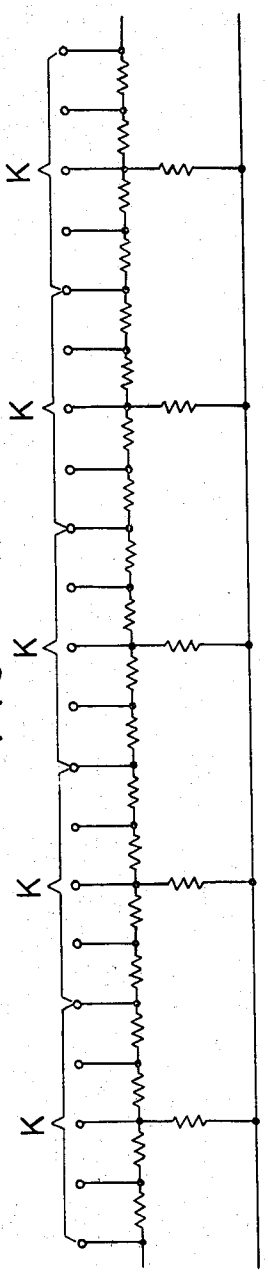


FIG. 20(B)

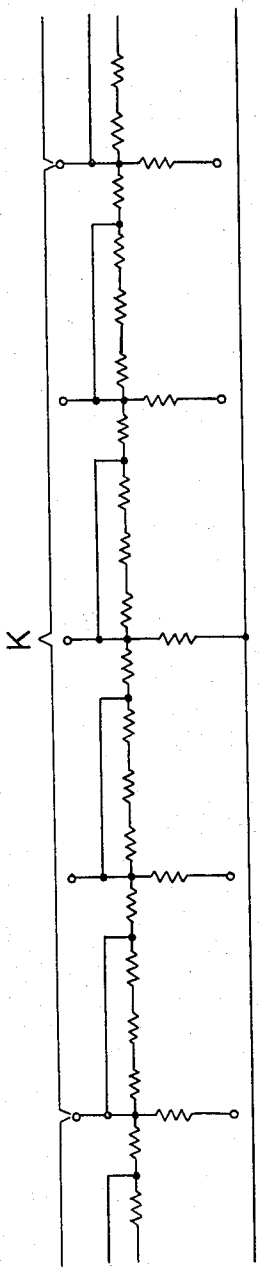
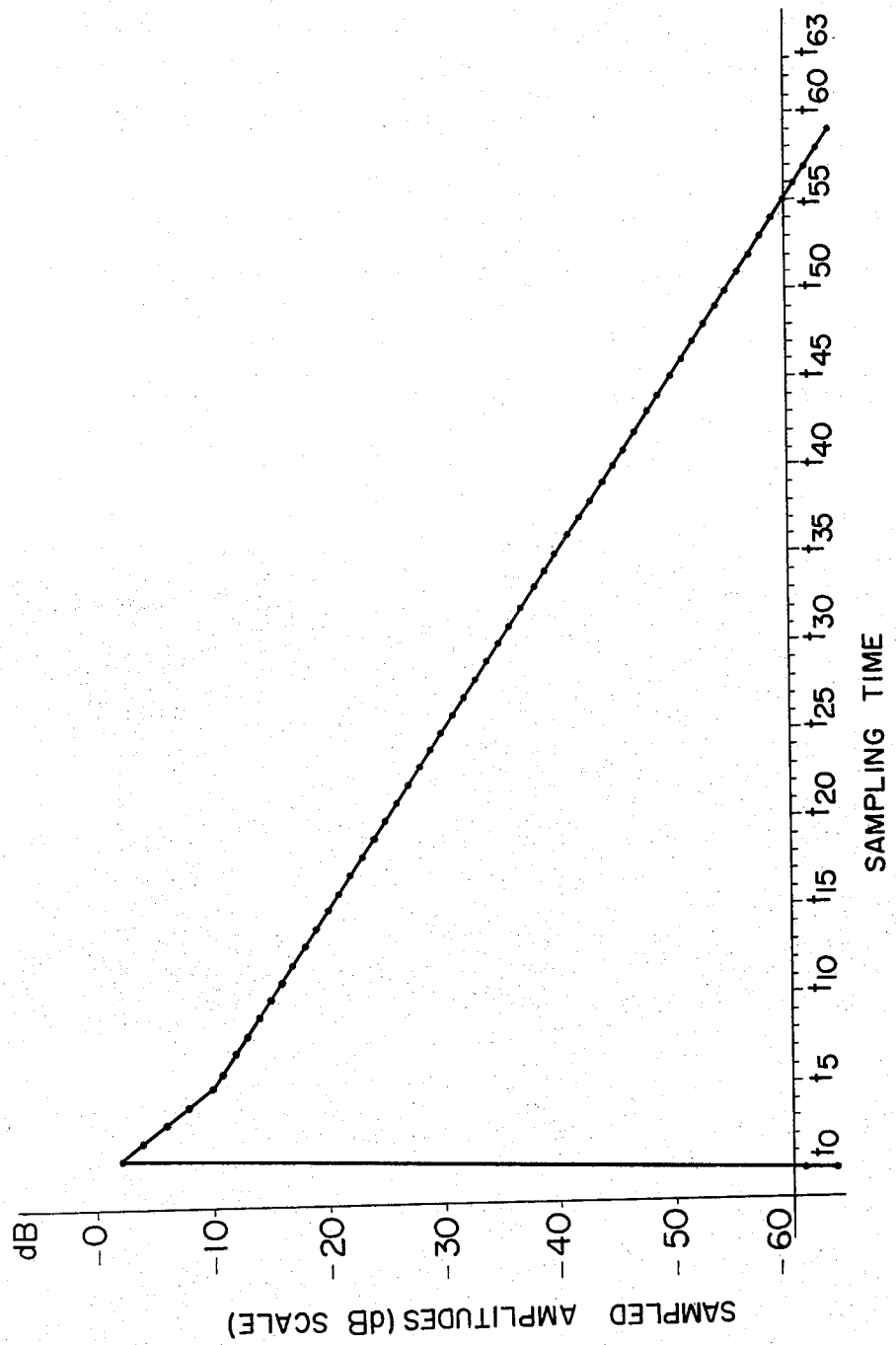


FIG. 20(C)

FIG. 21


SAMPLED AMPLITUDES (dB SCALE)
dB
-0
-10
-20
-30
-40
-50
-60
t0 t5 t10 t15 t20 t25 t30 t35 t40 t45 t50 t55 t60 t63
SAMPLING TIME

WAVEFORM PRODUCING DEVICE

BACKGROUND OF THE INVENTION

This invention relates to a device for producing a waveform having a particular tone-color or an envelope of a particular shape for electronic musical instruments.

A device for producing a waveform constituted by analog sampled values at successive time points in which resistance elements having resistances decisive of the amplitude values to be produced are provided and electrical circuits for these elements are sequentially formed by means of mechanical contacts, is known in the art.

However, such a conventional device needs as many resistance elements as the number of amplitude values (i.e. sampling time points) for forming an analog waveform to be produced, that is, it needs a number of resistance elements, and the size of the device is therefore inevitably large. Furthermore, the more ideal analog waveform we try to produce, the more amplitude values it requires, that is, much more resistance elements are necessary for the production of the ideal analog waveform. However, the actual size of the device is naturally limited to a certain extent, and accordingly the number of resistance elements employed therein is also limited to a certain number. Consequently, analog waveforms produced from the conventional device are of a non-continuous (stepwise) waveform.

In general, resistance elements vary widely in their resistance, and precision resistance elements less in resistance fluctuation are high in price.

The resistances of resistance elements available in the market are standardized. Therefore, when resistance elements having resistances other than standard resistances are required for the production of a desired analog value, it is necessary to special order them, which will result in the increase of the price of the waveform producing device.

Furthermore, since the conventional device reads information by means of mechanical contacts, it suffers from various difficulties such as a relatively short service life and a slow reading speed.

On the other hand, for the purpose of producing an analog waveform in response to digital information, a digital-to-analog converter is employed. However, in the digital-analog converter proposed heretofore, the number of bits is limited to a certain value, and therefore analog waveforms produced are not always satisfactory in waveform continuity.

Furthermore, a waveform producing device employing integrated circuits has been proposed. In this conventional waveform producing device, a plurality of diffused resistance layers each having a certain width are formed on a semiconductor substrate, resistance values corresponding to amplitude values at respective sampling time points of an analog waveform to be produced are set on the diffused resistance layers, respectively, and by sequentially scanning these resistance layers from one outermost layer to the other outermost layer terminal voltages of the resistance layers are sequentially read out, whereby a desired analog waveform having variation of amplitudes corresponding to variation of the terminal voltages thus read is produced.

In this conventional waveform producing device, since a number of parallel diffused resistance layers are

formed on the semiconductor substrate as described above, it follows that a relatively large space is necessary for the device and a relatively large amount of electric power is consumed therein. These difficulties become significant as the number of the diffused resistance layers is increased for the purpose of improving the continuity of the analog waveform to be produced.

SUMMARY OF THE INVENTION

Accordingly, a primary object of this invention is to provide a waveform producing device having a low manufacturing cost which is free from the above-described difficulties accompanying conventional waveform producing devices and is capable of producing analog waveforms having satisfactory waveform continuity.

Another object of the invention is to provide a waveform producing device which is suitable for the production of a tone-color waveform or an envelope waveform having a rising and decaying characteristic necessary for electronic musical instruments.

A further object of the invention is to provide a waveform producing device which can readily produce a wave-form having variation of amplitudes similar to variation of logarithmical functions.

A still further object of the invention is to provide a reliable waveform producing device which can be made to be small in size with the aid of a technique on MOS integrated circuits.

The foregoing objects and other objects of this invention have been achieved by the provision of a waveform producing device which comprises, per unit, one diffused layer resistor formed on a semi-conductor substrate and having a plurality of connection points, means for applying a predetermined voltage across the resistance layer to respectively provide different potentials at the connection points, and a reading circuit for reading the potentials at the connection points in a predetermined order, thereby to produce a desired waveform having variation of amplitude corresponding to variation of the potentials thus selected.

It is preferable that the reading circuit comprises a switching circuit having a plurality of MOS transistors connected to the connection points and an addressing circuit with MOS transistors for driving the switching circuit so that the MOS transistors in the switching circuit are turned on in a predetermined order, the reading circuit being combined together with the resistance layer in an integrated structure on the semicondutor.

Furthermore, T-type attenuation circuits may be connected by connecting additional resistors to the resistance layer.

The manner in which the above described objects are achieved by this invention will become more apparent from the following detailed description and the appended claims when read in conjunction with the accompanying drawings, in which like parts are designated by like reference numerals or characters.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. 1 is a plan view illustrating a first example of a waveform producing device according to this invention;

FIG. 2 is an equivalent circuit diagram of the waveform producing device shown in FIG. 1;

FIG. 3 is an enlarged detail of a waveform output section in the waveform producing device shown in FIG. 1;

FIG. 4 is a graphical representation indicating a waveform generated;

FIG. 5 is an enlarged view showing a decoder section in the device shown in FIG. 1;

FIGS. 6*a*, 6*b* and 6*c* provide tables indicating the relationships between transistor groups and address input connection points in the decoder section shown in FIG. 5;

FIGS. 7*a*, 7*b* and 7*c* provide code tables for address inputs;

FIGS. 8(A), 8(B) and 8(C) are graphical representation indicating envelope waveforms employed in electronic musical instruments;

FIG. 9 is a plan view illustrating a second example of the waveform producing device according to the invention;

FIG. 10 is an enlarged view showing an amplitude generating section and a metal wiring section in the waveform producing device shown in FIG. 9;

FIG. 11 is an equivalent circuit diagram of the waveform producing device shown in FIG. 9;

FIG. 12 is an equivalent circuit diagram of a resistance attenuator unit in the amplitude generating section shown in FIGS. 9 and 11;

FIG. 13 is a graphical representation indicating the envelope waveform of a sustain tone;

FIGS. 14 and 15 are also graphical representations respectively indicating the envelope waveforms of an attack-sustain tone and a percussive tone;

FIG. 16 is a plan view illustrating a third example of the waveform producing device according to this invention;

FIG. 17 is an equivalent circuit diagram of the waveform producing device shown in FIG. 16;

FIG. 18 is also an equivalent circuit of a resistance attenuator unit in an amplitude generating section of the waveform producing device shown in FIGS. 16 and 17;

FIG. 19 is a graphical representation indicating an output waveform from the device shown in FIG. 16;

FIGS. 20(A), 20(B) and 20(C) are circuit diagrams of various attenuation circuits, and

FIG. 21 is a graphical representation indicating the envelope waveform of a percussive tone.

DETAILED DESCRIPTION OF THE INVENTION

With reference to FIG. 1 there is shown a first example of a waveform producing device for electronic musical instruments according to this invention, which comprises an N-type semiconductor substrate 1 and amplitude memory section 2 formed in the upper half portion of the substrate 1. The amplitude memory section 2 comprises a P-type diffused resistance layer 2*a* extended horizontally, and P-type diffused resistance layers 2*b* and 2*c* which are respectively extended vertically on the left and right sides of the layer 2*a*, in combination forming a single resistor zone. Below the amplitude memory section 2, or in the middle portion of the substrate 1, there is provided a waveform reading switch section 4 extended horizontally in parallel with the section 2. Between the amplitude memory section 2 and the waveform reading switch section 4, there is a metal wiring section 3 to electrically connect these two sections 2 and 4. Furthermore, below the waveform reading switch section 4, or in the lower half portion of the substrate 1, there is a decoder section 5 for driving the waveform reading switch section 4.

In FIG. 1, a pattern ▨ represents a P-type diffused layer, ▧ a gate electrode of a P-channel MOS transistor □ a layer formed by vaccum-evaporation of a metal such as aluminum, and ⊠ a connection point for connecting the metal vacuum-evaporated layer to the P-type diffused layer. In addition, an insulation film (not shown) is formed on the surface of the semiconductor substrate 1.

The diffused resistance layers 2*a*, 2*b* and 2*c* of the amplitude memory section 2 are in the form of a belt or stripe having the same width, for the left end of the layer 2*a* and the upper end of the layer 2*b* is connected by a metal connecting layer 11*a* while the right end of the layer 2*a* and the upper end of the layer 2*c* is connected by another metal connecting layer 11*b*. Thus, the layers 2*a*, 2*b* and 2*c* form one resistor assembly comprising resistors R_1 through R_{80}, when expressed circuit diagram representation as is shown in FIG. 2. This resistor assembly has the same resistance per unit length. In the resistance layers 2a, 2b and 2c thus organized, there are provided, for instance, 81 connection points V_0, V_1, V_2 through V_{80} at equal intervals. The connection points V_0 and V_{80} provided on both ends of the resistor assembly 2 are respectively connected to terminals GND (OV) and Vin (−4V) of a power source. Thus, voltages proportional to the ratios of resistances from the connection point V_0 to the other connection points V_1 through V_{80} to the whole resistance from the point V_0 to the point V_{80} are provided at the connection points, the differences between these voltages being the same, namely, (4V/80 = 0.05V). The voltages thus provided at the connection points V_0 through V_{80} are utilized as amplitude voltages of a waveform to be generated, as will be described later.

The reading switch section 4, as shown in FIG. 3, comprises, for instance, 64 MOS type output switching transistors U_0 and U_1 through U_{63} ,horizontally disposed in the order described. In this reading switch section 4, adjacent two transistors have a common P-type diffused layer serving as a source S and extended vertically. The adjacent transistors are disposed back-to-back through two P-type diffused layers, or drains D, provided on the both sides of the source and two metal vacuum-evaporated layers, or gates G, formed between the source S and the drains D thereby to economize space.

One-ends of the drains D of the transistors U_0 and U_1 through U_{63} are extended upward. On the one-ends thus extended of the drains D there are provided connection points P_0 and P_1 through P_{63}. One-ends of the sources S are also extended upward and are connected to a waveform output terminal OUT. Furthermore, one-ends of the gate G of the transistors U_0 and U_1 through U_{63} are extended downward and connected to driving input connection points Q_0 and Q_1 through Q_{63}.

Referring back to FIG. 1, the metal wiring section 3 will be described. The metal wiring section 3 comprises metal wiring connection layers n_0 and n_1 through n_{63} which are adapted to connect the connection points P_0 and P_1 through P_{63} to connection points selected, in accordance with a waveform to be produced, out of the connection points V_0 and V_1 through V_{80} in the amplitude generating section 2. In this connection, it should

be noted that these layers n_0 through n_{63} are not crossed with each other.

Consider, for instance, one period of a tone waveform of a trumpet voice as an example of the waveforms to be produced. In this case, a curve I such as shown in FIG. **4** is memorized by time-sequentially plotting the amplitude voltages of the waveform to be generated. More specifically, if voltages 0.00V and − 0.05V through − 4.00V respectively provided at the connection points V_0 and V_1 through V_{80} are read on the vertical axis expressing amplitude voltages while sampling time instants t_0 and t_1 through t_{63} are read on the horizontal axis expressing read time instants, then for instance the voltage 0.00V at the connection point V_0, the voltage −0.05V at the connection point V_1, the voltage −0.55V at the connection point V_{11} and the voltage −4.00V at the connection point V_{80} are read at the time instants t_{10}, t_{11}, t_{14} and t_0, respectively, whereby an analog waveform signal similar to the tone waveform of the trumpet voice can be obtained.

According to this invention, since potentials at the connection points V_0 and V_1 through V_{80} on the diffused resistance layers are selected in a particular order so that variation of these potentials represent variation of the amplitudes of a waveform to be generated, it is not necessary to have the connection layers n_0 and n_1 through crossed with each other.

The decoder section **5** operates to address output transistors corresponding to amplitude voltages to be read at the read time instants t_0, t_1 through t_{63} in FIG. **4.** In the first example, the decoder section **5** is of a 6-binary-input and 64-individual-output type (binary to individual converter) which comprises 64 transistor groups each group comprising six MOS transistors which represents a six-bit address as is shown in FIG. **5.** The transistors in each transistor group are provided with a common P-type diffused layer, or common source S, disposed vertically and a common P-type layer, or a common drain, disposed in parallel to the source S, and are arranged vertically. The upper ends of the drains D are connected to the driving input connection points Q_0 and Q_1 through Q_{63} of the reading switch section **4** described above, while the source S are connected through a metal connecting layer to a terminal GND (OV) of a power source. In this case also, adjacent transistors in adjacent transistor groups are disposed back-to-back in the same manner as in the case of the reading switch sectional **4.** Thus, the transistor groups T_0 (T_{01} – T_{06}) and T_1 (T_{11} – T_{16}) through T_{63} (T_{631} – T_{636}) are arranged in the order described from the left to the right.

The diffused layers forming the drains D of the transistors in the transistor groups are extended downward, and the lower ends of these layers and a P-type diffused layer extended horizontally form load resistance transistors L_0 through L_{63}. The drains D and the gates G of the load resistance transistors are connected to terminals V_{DD} (−16V) and V_{GG}(−26V) of the power source and a negative voltage (approximately − 16V) is supplied to the drains D of the transistor groups.

Six-bit address inputs A_1 through A_6 to the decoder section **5,** as is apparent from FIG. **2,** are applied to address input terminals AD_1 through AD_6 from an address signal generator constituted by a clock pulse generator **20** and a binary counter **21.** These binary coded address inputs A_1 through A_6 are applied, together with address inversion inputs $\overline{A_1}$ through $\overline{A_6}$ which are obtained by inverting the address inputs A_1 through A_6 in address inverters IN_1 through IN_6, to address input connection points J_1 and $\overline{J_1}$ through J_6 and $\overline{J_6}$ provided on metal connection layers which are connected to the gates G of transistors provided for the first bit through the sixth bit in the decoder section **5.**

In the case where a tone waveform shown in FIG. **4** is produced the gates G of the transistors for the first bit through the sixth bit in the transistor groups T_0 through T_{63} of the decoder section **5** are connected to address input connection points predetermined out of the address input connecting points J_1 or $\overline{J_1}$ through J_6 or $\overline{J_6}$ as is indicated in FIGS. **6**(*a*), **6**(*b*) and **6**(*c*) as a result of which the transistor groups T_0 through T_{63} in the decoder section **5** and accordingly their driving output terminals Q_0 through Q_{63} are disposed in the order described from the left to the right so as to be connected to the gate terminals Q_0 through Q_{63} of the transistors in FIG. **3.**

When address inputs A_1 through A_6 having codes as shown in FIGS. **7**(*a*), **7**(*b*) and **7**(*c*) are applied to the address input terminals AD_1 through AD_6 in the decoder section **5** sequentially at the time instants t_0 through t_{63}, an input of logic "0" is applied to the gates of transistors T_{631} through T_{636} in the transistor group T_{63}, as a result of which a negative voltage (−16V) obtained by the transistor $L_{63}$is applied to the connection point Q_{63} at the time instant t_0 thereby allowing the output transistor U_{63} to turn on, or to become conductive. Through this transistor U_{63}, a voltage (−4.00V) at the connection point V_{80} in the amplitude memory section **2** is introduced to the output terminal OUT.

Thereafter, an input of logic 0 is applied to the gates of the transistors T_{581} through T_{586} in the transistor group T_{58} in the decoder section **5** at the time instant t_1 and a negative voltage is applied to the connecting point Q_{58}, as a result of which a voltage (−3.4V) at the connection point V_{69} in the amplitude memory section **2** is introduced to the output terminal OUT.

Similarly as in the cases described, the output transistors corresponding to the sampled amplitudes to be read are sequentially addressed by the address inputs applied to the decoder section **5** and the voltages at the connection points, in the amplitude memory section **2** which are connected to the transistors are sequentially introduced to the output terminal OUT. For instance, at the time instance t_{14} the output transistor U_6 is addressed whereby a voltage (−0.55V) at the connecting point V_{11} is introduced to the output terminal OUT, and at the time instant t_{63} the output transistor U_{62} is addressed whereby a voltage (−3.95V) at the connecting point V_{79} is introduced to the output terminal OUT.

As is apparent from the above description, according to this invention, only by determining the sequence for addressing a plurality of switching transistors connected to the connection points on the diffused resistance layers, desired analog waveforms can be produced. Furthermore, since the diffused resistance layer formed into one unit with the connection points provided at equal voltage intervals is employed as the amplitude memory section, it follows that the space occupied by the amplitude memory section in the semiconductor substrate can be reduced. Accordingly, the size of the semiconductor substrate in this invention can be made much smaller than that of the conventional waveform producing device in which a plurality of diffused resistance layers are employed.

Furthermore, it should be noted that in this invention the production of waveforms can be carried out by the provision of only one diffused layer resistor in the waveform memory section **2**, and therefore power consumption in the waveform producing device of the invention is also much less than that in the conventional one.

In addition, in this invention since the output voltages from the amplitude memory section **2** are produced on the basis of the resistance ratios with respect to the whole resistance value of the diffused resistance layers formed into one unit, even if a process of diffusion were varied in a mass production of the waveform producing devices according to this invention, the variation would not appear as fluctuation in the output voltages of the amplitude memory section **2**. Accordingly, the waveform producing device according to the invention can carry out reproduction of waveforms with high accuracy. On the other hand, in the conventional waveform generating device described above, a waveform is stored as resistance values of the diffused resistance layers, the fluctuation in the process of diffusion will result in fluctuation in the regeneration of the waveforms. In contrast, such a result is not caused in the device of this invention.

Furthermore, according to this invention, production of other different waveforms can be achieved by changing the binary coded input signals and controlling, or turning on, the switching transistors with a different addressing sequence, and no other change is necessary. However, for the same purpose a wiring pattern of the connection layers n_0 through n_{63} which adapted to connect the connection points V_0 through V_{80} to the connection points P_0 through P_{63} may be changed.

Furthermore, in the device according to this invention, since the connection layers of the metal wiring section **3** are not crossed with each other, the manufacturing of the device is much simpler.

Incidentally, in the case where a section for generating envelope waveforms for electronic musical instruments is practised in the form of a semiconductor integrated circuit, there are some difficulties as follows. That is, in general, there are three types of envelope waveforms: the first one, as is shown in FIG. **8**(A), is a waveform consisting of a waveform portion *a* which abruptly rises at the time instant t_a (hereinafter referred to as "an attack waveform portion of *a*"), a waveform portion *b* (hereinafter referred to as "a sustain waveform portion *b*") which maintains a substantially certain amplitude, a waveform portion *c* (hereinafter referred to as "a decay waveform portion *c*") which starts logarithmically decaying at the time instant t_c, a tone having the first envelope waveform being a so-called sustain tone; the second envelope waveform is one in which the trailing edge of its attack waveform portion *a* falls once as is shown in FIG. **8**(*b*), a tone having the second envelope waveform being a so-called attack-sustain tone; and the third envelope waveform is one which abruptly rises and immediately after this rise falls, that is, it has no sustain waveform portion *b*, as is shown in FIG. **8**(*c*), a tone having the third envelope waveform being a so-called percussive tone.

In this connection, there has been a demand for an envelope waveform producing device which can produce such a waveform logarithmically decaying as the decay waveform portion *c* and such a waveform abruptly rising as the attack waveform portion *a*. Furthermore, there has been a demand for an envelope waveform producing device which is small in size, low in power consumption and simple in manufacture.

In order to satisfy these demands, there is shown a second example of the wavefrom generating device, according to this invention, with reference to FIG. **9** which comprises an N-type semiconductor substrate **1**, an envelope generating section **2**, a metal wiring section **3**, a reading switch section **4** and a decoder section **5**, these sections being disposed one after another from the upper portion of the substrate **1** to the lower portion.

As is shown in FIG. **10**, the amplitude generating section **2** comprises a belt-shaped section of a P-type diffused resistance layer **2***a* extended horizontally, and P-type diffused resistance layers **2***b* and **2***c* extended vertically on the both sides of the layer **2***a*. The P-type diffused resistance layers **2***b* and **2***c* are connected through metal connection layers **11***a* and **11***b* to the left end and right end of the P-type diffused resistance layer **2***a*, respectively, to form a series of diffused resistance layers. That is, one resistor comprising resistors r_1 through r_{80} and having an equal resistance per unit length is formed as is shown in FIG. **11** illustrating an equivalent circuit of the second device. On the resistance layers **2***a*, **2***b* and **2***c* thus formed into one unit, there are provided **81** connection points V_0 and V_1 through V_{80} at equal intervals.

Furthermore, there are provided P-type diffused resistance layers extended downward like legs of the resistance layer **2***a* (hereinafter referred to as "resistance layer legs" when applicable) from some of the connection points which are located at predetermined intervals on the resistance layer **2***a*, and the lower ends of these resistance layer legs are provided with connection points, respectively. More specifically, in FIG. **10**, 16 resistance layer legs M_{10}, M_{14} - - - M_{66} and M_{70} are extended from the connection points V_{10}, V_{14} - - - - V_{66} and V_{70} which are located at every fourth connection point of the connection points V_9 through V_{70} on the resistance layer **2***a*.

A predetermined connection point (V_{58} in the second device shown in FIG. **10**) on the resistance layer **2***a* is connected a terminal Vin (−4V) of a power source, while the connection points V_0 and V_{80} located at the end portions of the resistance layers **2***b* and **2***c* are connected to a ground terminal GND (OV) of the power source. Connection points m_{56} - - - m_{10} are provided respectively on the lower ends of the resistance layer legs M_{56} - - - M_{10} which are disposed on the left side of the connection position V_{58}. The connection points m_{56} - - - m_{10} thus provided are connected to a common connection layer **12** extended horizontally. This connection layer **12** is connected to the connection point V_0 on the resistance layer **2***b*.

Thus, at the connection points on the resistance layers **2***a* and **2***c* on the right side of the connection point V_{58} voltages corresponding to the resistance ratios of the resistances from the points V_{80} to these connection points to the whole resistance from the point V_{58} to the point V_{80} can be obtained. The differences between the voltages thus obtained are the same, namely, (4V/24 = 0.166V), that is the voltages thus obtained are in a linear relationship. Therefore, they can be employed for the production of an attack waveform.

For each of the resistance layer legs M_{56} - - - M_{10} of the resistance layer **2***a* on the left side of the connection point V_{58}, a T-type resistance attenuator unit is formed. These attenuator units forms a ladder-type network as is shown in FIG. **11.**

In this unit, it is assumed that, as is shown in FIG. **12,** resistance of the resistance layer leg is indicated by R, the whole resistance between two connection points which are the second connection points from the connection point of the resistance layer leg R is indicated by *r*, a damping coefficient *n* is 4dB ($n = 4$dB), and the following equation (1) is attained:

$$\frac{R}{r} = \frac{k}{(k-1)^2} = 4.6327 \quad (1)$$

where $k = 10^{\frac{n}{20}} = 10^{0.2} = 1.5849$

Then, at the connection points, voltages differing by substantially 1 dB in attenuation from one another can be obtained.

An image impedance Z_o of this unit can be obtained by the following equation (2):

$$Z_o = \frac{2k}{k^2 - 1} r = 2.096\, r \quad (2)$$

In this second device, the resistance layer **2**b forms the terminal resistance of the attenuator. In the above equations, preferable values of the factors are as follows: n=4dB; $r = 780\Omega$; $R = 3610\Omega$; $Z_o = 1634\Omega$; and $k = 1.5849$.

The voltages thus obtained at the connection points V_{58} through V_8 on the resistance layer **2***a* are in a logarithmical relationship and can be utilized for the production of a decay waveform. In addition, in this second device, voltages which differ by a certain voltage from one another are obtained at the connection points on the resistance layer **2***b* forming the terminal resistance and may therefore be utilized for the production of the ending portion of a decay envelope waveform.

Similarly as in FIG. **3,** the waveform output section **4** is constituted by, for instance, 64 MOS output switching transistors and operates in the same manner.

The metal wiring sections **3** comprises metal wiring connection layers n_0 and n_1 through n_{63} for connecting the connection points, P_0 and P_1 through P_{63} to connection points, predetermined according to an output waveform, out of the connection points V_{80} through V_0, respectively in the order described. In this connection, it should be noted that these metal wiring connection layers are arranged in such a manner that they are not crossed with each other, and some of them are formed over the resistance layer legs M_{56} - - - M_{10} through insulating films. This arrangement of the connection layers contribute to economization in size of the semiconductor substrate.

Incidentally, in FIG. **13,** the attack envelope portion *a* of the sustain tone in FIG. **8**(A) is indicated by a curve I with a vertical axis of a linear scale, while the decay envelope is indicated by a curved II with a vertical axis of a dB scale. Furthermore, the connection points P_0, P_1 through P_{14}, P_{16} and P_{17} through P_{63} are assigned to the sampling time instants t_0 and t_1 through t_{63} on the horizontal axis of FIG. **13,** respectively, while the voltages at the connection points V_{80}, V_{76} through V_{59}, V_{58}, and V_{57} through V_0 are taken as amplitude voltages on the vertical axes in FIG. **13.**

The decoder section **5** operates to respectively address the output transistors corresponding to the sampled voltages to be read at the time instants t_0 and t_1 through t_{63}. The decoder section **5** in the second device of this invention is of a 6-binary-input and 64-individual-output type which comprises 64 transistor groups each consisting of six MOS transistors representing a 6-bit address as was described with reference to FIG. **5,** and the decoder section operates in the same manner as was described before.

In the decoder section **5** thus organized, when the address inputs A_1 through A_6 having the codes as indicated in FIGS. **7**(*a*), **7**(*b*) and **7**(*c*) are sequentially applied to the address input terminals AD_1 through AD_6 at the time instants t_0 through t_{63}, an input of logic 0 is applied to the gates of the transistors T_{01} through T_{06} in the decoder section **5** at the time instant t_0, as a result of which a negative voltage (−16V) obtained by the transistor L_0 is applied to the connection point Q_0 to turn on, or to make conductive the transistor U_0. Through the transistor U_0 thus made conductive a voltage (OV) at the connection point V_{80} in the amplitude memory section **2** is introduced to the output terminal OUT. Similarly as in the case described above, voltages at the connection points connected to the connection layers n_1 through n_{63} in the amplitude memory section **2** are sequentially introduced to the output terminal OUT.

Thus, the attack waveform portion I (in FIG. **13**) corresponding to the variation of potentials at the connection points V_{80} through V_{58} is obtained during the period of from the time instant t_0 to the time instant t_{15}. Furthermore, the decay waveform portion II′ logarithmically decaying in correspondence to the variation of potentials at the connection points V_{56} through V_8 and the decay waveform portion II″ are obtained during the period of from the time instant t_{15} to the time instant t_{63}.

Accordingly, if after the attack waveform has been read, the sustain waveform is obtained with the aid of a constant voltage source separately provided and succeedingly the decay waveform portion is obtained, then such an envelope waveform as indicated in FIG. **8**(A) can be obtained.

As is apparent from the above descriptions, according to this invention, the metal wiring section **3** is formed, on the basis of the amplitude voltages forming an envelope waveform to be produced, between the reading switch section **4** and the amplitude memory section **2,** and a desired waveform output can be obtained by controlling the operation of the output switching transistors, or turning on the output switching transistors, in a predetermined sequence by combining the belt-shaped section of the diffused resistance layer and the diffused resistance legs extended from the belt-shaped section leads to the production of a logarithmically decaying curve effective as a decay envelope.

The above descriptions are for the production of the sustain tone shown in FIG. **8**(A).

The attack-sustain tone as shown in FIG. **8**(B) can be obtained by producing an attack envelope curve I and a decay envelope curve II as shown in FIG. **14** instead of those shown in FIG. **13,** while the percussive tone as

shown in FIG. 8(C) can be obtained by producing only a decay envelope curve II as shown in FIG. **15.** The envelope form shown in FIG. **15** has no attack portion, and it can therefore obtained by connecting the common connection layer **12** of the amplitude memory layer **2** to all of the diffused resistance legs and by connecting the terminal Vin of the power source to the connection point V_{72}. Thus, various envelope shapes can be obtained by changing the wiring pattern in the wiring section **3** or by changing the addressing sequence of the output transistors U_0 through U_{63}.

With reference to FIG. **16,** there is shown a third example of the waveform producing device according to this invention, which comprises an N-type semiconductor substrate **1,** an amplitude memory section **2,** a metal wiring section **3,** a reading switch section **4** and a decoder section **5,** to produce a logarithmically decaying envelope.

The amplitude memory section **2** comprises a belt-shaped section of a P-type diffused resistance layer **2***a* extended horizontally, and a P-type diffused resistance layer **2***b* extended vertically at the left side of the diffused resistance layer **2***a*. The left end of the diffused resistance layer **2***a* is connected through a metal connection layer **11***a* to the upper end of the diffused resistance layer **2***b*. There is, these layers **2***a* and **2***b* are formed into one unit, or one resistor consisting of resistors r_1 through r_{72} and having an equal resistance per unit length. Furthermore, for instance 73 connection points V_0, V_1 and V_2 through V_{72} are provided at equal intervals on the resistance layers **2***a* and **2***b* formed into one unit.

P-type diffused resistance layers like legs of the resistance layer **2***a* (hereinafter to as "resistance layer legs" when applicable) are extend downward from some of the connection points which are located at predetermined intervals on the resistance layer **2**a. More specifically, in FIG. **16,** 16 resistance layer legs M_{10}, M_{14} - - - - M_{66}, and M_{70} are extended downward from the connection points V_{10}, V_{14} - - - V_{66} and V_{70} which are located at every fourth connection point of the connection points V_{10} through V_{70}.

The lower ends with connection points m_{70} - - - m_{10} of the resistance layer legs M_{70} - - - M_{10} are extended to a common connection layer **12** which is extended horizontally below the amplitude memory section **2,** but, out of the connection points m_{70} - - - m_{10}, connection points determined according to a waveform to be generated are connected to the common connection layer **12.** More specifically, in FIG. **16,** every other connection point of the connection points m_{70} - - - m_{10}, namely, the connection points m_{70}, m_{62}, m_{54} - - - m_{14} are connected to the common connection layer **12.**

Furthermore, adjacent connection points V_{72} and V_{71}, V_{70} and V_{69}, V_{68} and V_{67}, - - - V_{10} and V_9 on the resistance layer **2***a* are short-circuited by connection layers Y_{72}, Y_{70}, Y_{68} - - - Y_{10}, respectively.

The connection points V_{72} and V_0 on the ends of the resistance layers **2***a* and **2***b* are connected to terminals Vin (−4V) and GND (OV) of a power source, respectively, and the common connection layer **12** is connected to the terminal GND. Thus, the resistance layer **2***a*, the resistance layer legs M_{70}, M_{62}, M_{54} - - - M_{14} and the common connecton layer **12** form a ladder type network, whereby a T-type resistance attenuation unit K is formed for each of the resistance layers M_{70}, M_{62}, M_{54} - - - M_{14}. In this unit K, if it is assumed that, as is shown in FIG **18,** resistance of a resistance layer leg (for instance M_{54}) is represented by R, the whole resistance between two connection points (V_{50} and V_{58}) which are the second connection points from the connection point (V_{54}) of the resistance layer leg is represented by *r*, and a damping coefficient *n* is 4dB, then the relation between resistances R and r can be represented by equation (1) previously described, and at the connection points (V_{58}, V_{56}, V_{54}, V_{52} and V_{50}) located at every other connection point voltages differing by substantially 1 dB in attenuation from one another can be obtained. An image impedance Z_o of this unit K can be obtained from equation (2) previously described. In this example, the resistance layer **2***b* is the terminal resistance of the attenuator. In the above equations (1) and (2), preferable values of the factors are as follows: $n = 4\text{dB}$; $r = 780\ \Omega R = 3610\ \Omega$; $Z_o = 1634\ \Omega$; and $k = 1.5849$.

Thus, the voltages obtained at the connection point V_{72}, V_{70}, V_{68} - - - V_{10} located at every other connection point are in a logarithmic relation.

The reading switch section **4** is constituted by, for instance, 64 MOS output transistors and operates similarly as in FIG. **3.**

The metal wiring section **3** comprises metal wiring connection layers for connecting the connecton points P_0 and P_1 through P_{63} of the transistors in the reading switch section **4** to connection points, predetermined according to a waveform to be generated, out of the connection points V_{72} through V_8 on the resistance layer **2***a*, respectively in the order described. In this third example of this invention, as is shown in FIG. **16,** adjacent two connection points P_0 and P_1, P_2 and P_3, P_4 and P_5 - - - P_{62} and P_{63} are short-circuited by connection layers Z_0, Z_2, Z_4 - - - Z_{62}, respectively. Furthermore, the connection points P_0 and P_1, P_2 and P_3, - - - P_{62} and P_{63} are connected through connection layers n_0, n_2 - - - n_{62} to the connection points V_{72} and V_{71}, V_{70} and V_{69}, - - - V_{10} and V_9, respectively. Thus, connection layers n_0 through n_{62} are laid over the resistance layer legs M_{70} through M_{10}, but are not crossed with each other.

The decoder section **5** is to respectively address the output transistors corresponding to the voltages to read at the time instants t_0 and t_1 through t_{63}. The decoder section **5** in the third example of this invention is also of a 6-binary-input and 64-individual-output type which comprises **64** transistor groups each consisting of six MOS transistors provided for a six-bit address as was described previously with reference to FIG. **5** and the decoder section **5** thus organized operates in the same manner as described previously.

In the decoder section **5** thus organized, when the address inputs A_1 through A_6 are sequentially applied to the address input terminals AD_1 through AD_6 at the time instants t_0 through t_{63}, an input of logic 0 is applied to the gates of the transistors T_{01} through T_{06} in the transistor group T_0 of the decoder section **5** at the time instant t_0, as a result of which a negative voltage (−16V) obtained by the transistor L_0 is applied to the connection point Q_0 to turn on, or to make conductive, the transistor U_0. Through the transistor U_0 thus made to be conductive, a voltage (−4.00V) at the connection points V_{72} and V_{71} in the amplitude memory section **2** is introduced to the output terminal OUT. Similarly as in the operation described above, voltages at the connection points connects to the connection layers n_2

through n_{62} in the amplitude memory section **2** are sequentially introduced to the output terminal OUT.

Thus, an output voltage of a decay waveform decaying at a substantially certain inclination from 0 dB to −30dB on a logarithmical scale is produced as indicated in FIG. **19.**

Incidentally, it is assumed that in FIG. **16** the shorting connection layers Y_{72}, Y_{70} - - - Y_{10} and Z_0, Z_2 - - - - Z_{62} are omitted, the connection points P_0, and P_1 through P_{63} are connected to the connection points V_{72}, and V_{71} through V_8 through metal wiring connection layers, respectively, and all of the connection points m_{70}, m_{66} - - - m_{10} on the resistance layer legs are connected to the common connection layer **12.** As a result, the resistance attenuator unit K shown in FIG. **18** is formed for each of the resistance layers M_{70}, M_{66} - - - M_{10} as is shown in FIG. **20**(B). As is apparent from the comparison of the circuit shown in FIG. **20**(B) with that shown in FIG. **20**(A) which is an equivalent circuit of the attenuation network in the third device of this invention shown in FIG. **16,** an attenuation quantity by the circuit in FIG. **20**(B) is twice as much as that by the circuit in FIG. **20**(A), during the period of the time instant t_0 to the time instant t_{63}. Accordingly, a decay envelope shape obtained at the output terminal OUT decays from 0 dB to −60dB at an inclination twice as much as that of a curve shown in FIG. **19.**

On the other hand, if in FIG. **16** the connection points V_{72} through V_8 are divided into connection point groups each consisting of adjacent four connection points and in each of the connection point groups its first connection point is connected to its fourth connection point, and furthermore connection points located at every fourth connection point out of the connection points m_{70} - - - m_{10} on the resistance layer legs M_{70} - - - M_{10} are connected to the common connection layer **12,** then the resistance attenuation unit K shown in FIG. **18** is formed for every four resistance layer legs as is shown in FIG. **20**(C). Accordingly, for the period of from the time instant t_0 to the time instant t_{63} an attenuation quantity by the circuit shown in FIG. **20**(C) is half that by the circuit shown in FIG. **20**(A) which is the equivalent circuit of the attenuator units for the device shown in FIG. **16.** Accordingly, a decay envelope shape obtained at the output terminal OUT decays from 0 dB to −15dB at an inclination which is half that of the curve shown in FIG. **19.**

As is apparent from the descriptions on the third device of this invention described above, a logarithmically decaying waveform can be produced as desired by selectively shorting the connection points on the diffused resistance layer **2**a in the amplitude generating section **2** and by selectively connecting the resistance layer legs to the common connection layer **12.**

While there has been described in connection with the example where an envelope decaying at a substantially, certain inclination is produced as is shown in FIG. **9,** such an example can be effectively practised in a touch-responsive decay envelope producing device in electronic musical instruments.

In this example, if the amplitude memory section is rearranged so that an attenuation quantity per unit reading time interval is changed at a predetermined reading time instant, a device for producing a logarithmically decaying waveform which consists of decay curves having different inclinations can be provided. Such a device can be applied to a device for producing an envelope shape of a percussive tone in electronic musical instruments. Furthermore, this invention can be effectively applied to a device for producing a logarithmical waveform.

It can be easily understood that the waveform producing devices described as the second and the third example of this invention can also provide advantages such as those provided by the device described as the first example.

In the above descriptions, the output transistors U_0 through U_{63} in the decoder section **5** are addressed in the order described, but the order of addressing the output transistors may be changed as required. Furthermore, the pattern of the metal wiring section is not limitative to the example described above, that is, it may be changed in such a manner that some of the connection layers are crossed with each other.

Moreover, the above description, the MOS integrated circuit comprising MOS transistors has been disclosed, but these MOS transistors may be replaced by bipolar type transistors. In addition, a P-type semiconductor substrate can be employed as the semiconductor substrate **1.**

While there has been described in connection with the application of this invention to the waveform producing device in electronic musical instruments, the application of this invention is not limited thereto, that is, this invention can be applied not only to a device for producing a particular waveform and an envelope shape in electronic musical instruments but also devices for producing other waveforms.

Furthermore, in the above descriptions, the amplitude memory section **2** has a pattern like a character "U" by connecting three diffused resistance layers **2***a*, **2***b* and **2***c* into one unit; however, this pattern and the number of the diffused resistance layers may be changed suitably as required. For instance, the amplitude generating section **2** may be formed by one belt-shaped resistance layer **2***a* only without the resistance layer **2***b* and **2***c*.

We claim:

1. A waveform producing device which comprises,

a. a resistor zone of a diffused layer formed on a semiconductor substrate and having a plurality of connection points,

b. means for applying a predetermined voltage across the resistor zone so that different potentials appear at the respective connection points, and

c. a reading circuit for reading the different potentials at the connection points in a predetermined order, so that a waveform having variation of amplitudes corresponding to variation of the potentials at the connection points thus read is produced.

2. A waveform producing device as claimed in claim **1** in which said reading circuit comprises

a. a read-out switching circuit having a plurality of switching transistors with input terminals connected to said connection points and with a common output terminal, and

b. an addressing circuit for turning on the switching transistors in a predetermined order according to binary-coded signals to drive the switching circuit so as to produce said waveform at the common output terminal.

3. A waveform producing device as claimed in claim **2** in which said switching transistors are MOS transistors, said addressing circuit includes a decoder formed

by a plurality of MOS transistors, said switching circuit and the decoder together with said diffused resistance layer being combined in an integrated structure on said semiconductor substrate.

4. A waveform producing device as claimed in claim **1** in which said voltage is applied through at least one resistor to the connection points on said diffused resistance layer.

5. A waveform producing device as claimed in claim **4** in which said resistor is a diffused resistance layer formed on said semiconductor substrate.

6. A waveform producing device as claimed in claim **4** in which a connection point connected with said resistor is shorted by another connection point.

7. A waveform producing device as claimed in claim **4** in which connection points to which said resistor is not connected are connected to each other.

8. A waveform producing device as claimed in claim **1** in which said voltage is applied to said diffused resistance layer through a resistor for every predetermined number of connection points and a multiple T-type attenuation circuit is formed.

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