(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
02 November 2017 (02.11.2017)

(10) International Publication Number
WO 2017/189367 A1

(51) International Patent Classification:
H01L 21/48 (2006.01) *H05K 1/18* (2006.01)
H01L 23/52 (2006.01) *H05K 3/30* (2006.01)
H01P 5/04 (2006.01) *H05K 3/40* (2006.01)

(21) International Application Number: PCT/US2017/028964

(22) International Filing Date: 21 April 2017 (21.04.2017)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/329,301 29 April 2016 (29.04.2016) US

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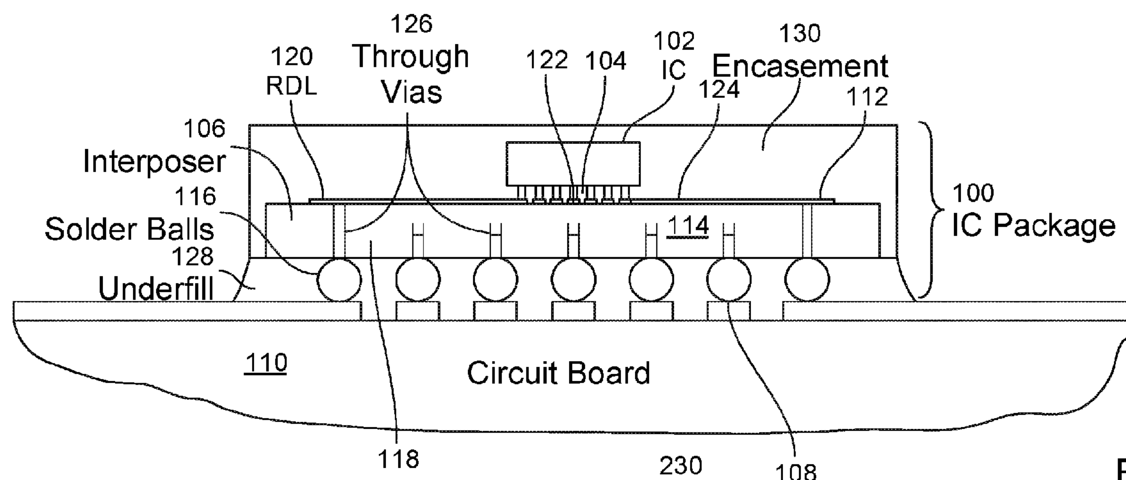
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:
— *with international search report (Art. 21(3))*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) **Title:** CONNECTING ELECTRONIC COMPONENTS TO SUBSTRATES



(57) **Abstract:** An apparatus includes a first substrate including one or more electrical connection features; and an assembly including: a second substrate; conductive features formed on the second substrate, one or more of which are electrically connected to corresponding electrical connection features of the first substrate; and an electronic component between the second substrate and the first substrate and electrically connected to one or more of the conductive features.

CONNECTING ELECTRONIC COMPONENTS TO SUBSTRATES

Claim of Priority

[001] This application claims priority to U.S. Patent Application Serial No. 62/329,301,
5 filed on April 29, 2016, the entire contents of which are incorporated here by reference.

Background

[002] Discrete components including integrated circuits are packaged for use in various applications. Packaging a discrete component includes electrically connecting the discrete component to a substrate, such as a printed circuit board.

10 ## Summary

[003] In an aspect, an apparatus includes a first substrate including one or more electrical connection features; and an assembly including a second substrate; conductive features in contact with the second substrate, one or more of which are electrically connected to corresponding electrical connection features of the first substrate; and an
15 electronic component between the second substrate and the first substrate and electrically connected to one or more of the conductive features. A separation between the first substrate and the second substrate is 500 μm or less.

[004] Embodiments can include one or more of the following features.

[005] The assembly includes multiple electronic components between the second
20 substrate and the first substrate. The electronic component includes a discrete component. The electronic component includes one or more of a sensor, a MEMS device, an LED, a power source, a chemical sensing element, and a biological sensing element. The electronic component is formed on the second substrate. The electronic component is embedded into a body of the second substrate. The apparatus includes a second electronic
25 component embedded within a body of the second substrate. The electronic component is positioned at a first surface of the second substrate, and in which the assembly includes a second electronic component positioned at a second surface of the second substrate, the second surface opposite the first surface. The first substrate includes a circuit board.

[006] The second substrate includes an interposer. The electronic component includes an integrated circuit.

[007] The one or more conductive features are formed on a surface of the second substrate. A surface of the first substrate faces the surface of the second substrate on which the conductive features are formed and the electronic component is at least partially within a gap between the two surfaces. The surface of the second substrate on which the one or more conductive features are formed faces the first substrate. The gap between the two surfaces is filled with an encapsulant.

[008] At least portions of the one or more conductive features are embedded within a body of the interposer.

[009] The electronic component includes one or more bond pads, at least one of the bond pads electrically connected to a corresponding one of the conductive features of the second substrate. Each bond pad includes a corresponding bump, and in which the at least one of the bond pads is electrically connected to the corresponding one of the conductive features through the bump. The one or more bond pads are formed on a surface of the electronic component. A surface of the electronic component on which the one or more bond pads are formed faces the second substrate. A pitch of the bond pads of the electronic component is different than a pitch of the electrical connection features of the first substrate.

[010] The electronic component is electrically connected to one or more of the conductive features by an interconnection system. The interconnection system includes a conductive adhesive.

[011] Each conductive feature includes a first conductive structure oriented in parallel to a surface of the second substrate and a second conductive structure oriented perpendicular to a surface of the second substrate. The assembly includes an encapsulant layer between the second substrate and the first substrate, and in which the second conductive structures are formed through a thickness of the encapsulant layer. The second conductive structures protrude beyond a bottom surface of the encapsulant layer. The first conductive structures are formed of a different material than the second conductive structures. The first conductive structures include a redistribution structure.

[012] One or more of the conductive features of the second substrate each includes a contact pad connected to a corresponding conductive line. The contact pads are positioned around the edges of the electronic component. The contact pads are arranged

in an array. The contact pads are positioned on one side of the electronic component. One or more of the contact pads is each connected to a corresponding electrode, and in which one or more of the electrodes is each electrically connected to a corresponding one of the electrical connection features of the first substrate. The electrodes include one or more of solder balls, pillars, studs, bumps, pads, and conductive particles. The electronic component has a thickness no greater than the combination of a thickness of the electrodes and a thickness of the electrical connection features of the first substrate.

[013] The apparatus includes an underfill material disposed between the first substrate and the second substrate. The underfill material includes a non-conductive polymer.

[014] The electronic component is encapsulated in an encapsulant. At least a portion of the conductive features is encapsulated in the encapsulant.

[015] The separation between the first substrate and the second substrate is 200 μm or less, 100 μm or less, or 50 μm or less. The first substrate is 100 μm or less, 50 μm or less, 25 μm or less, or 10 μm or less from a surface of the electronic component facing the first substrate. The first substrate is in physical contact with the surface of the electronic component facing the first substrate.

[016] The first substrate includes a flexible substrate. The first substrate includes a printed flexible circuit board. The second substrate includes a material that is flexible. The second substrate is stretchable. The one or more conductive features include meandering conductive features. The second substrate includes an elastomeric material. The electronic component includes a material that is flexible. The electronic component has a thickness of less than about 50 μm. The electrical connection features of the first substrate include printed conductors. The apparatus includes an adhesive disposed between the flexible substrate and the assembly. The adhesive includes a conductive adhesive. The adhesive forms a seal around the electronic component. The adhesive includes an anisotropic conductive adhesive. The anisotropic conductive adhesive provides an electrical connection between the conductive features formed on the second substrate and the corresponding electrical connection features of the first substrate.

[017] The assembly includes second conductive features formed through a thickness of the second substrate, each second conductive feature electrically connected to one of the conductive features. The apparatus includes a second electronic component electrically connected to one or more of the second conductive features, the assembly arranged such that the second substrate is disposed between the electronic component and the second

electronic component. The apparatus includes a second assembly disposed on the second substrate, the second assembly including a third substrate; third conductive features in contact with the third substrate, one or more of which are electrically connected to corresponding second conductive features of the second substrate; and a second electronic component between the third substrate and the second substrate and electrically connected to one or more of the third conductive features.

[018] The apparatus includes a third substrate disposed on the assembly such that the assembly is between the first substrate and the third substrate, the third substrate including one or more second electrical connection features electrically connected to one or more of the electrical connection features of the first substrate. The apparatus includes an adhesive layer between the first substrate and the third substrate, wherein the assembly is at least partially encapsulated in the adhesive layer. The apparatus includes a second electronic component disposed on the third substrate and electrically connected to one or more of the second electrical connection features. The second electrical connection features are formed through a thickness of the third substrate and in which one or more of the electrical connection features of the first substrate are formed through a thickness of the first substrate. A first surface of the first substrate faces the third substrate, and including a second electronic component disposed on a second surface of the first substrate, the second electronic component electrically connected to one or more of the second electrical connection features.

[019] In an aspect, an assembly includes an electronic component having a first surface at which a pattern of electrical connection features are exposed, a substrate having a substrate surface at which a pattern of electrical connection features are exposed, and an interposer including conductors that connect at least some of the electrical connection features of the electronic component with at least some of the electrical connection features of the substrate, with the electronic component in a space between the interposer and the substrate and the first surface of the electronic component not facing the substrate surface. A second surface of the electronic component is 100 μm or less from the surface of the substrate.

[020] Embodiments can include one or more of the following features.

[021] The electronic component includes an integrated circuit. The conductors are exposed on a surface of the interposer, and in which the surface of the interposer faces the substrate surface. The conductors are electrically connected with the electrical connection features of the electronic component through an interconnection system. Each

conductor includes a first conductive feature in physical and electrical contact with the interconnection system and a second conductive feature connecting the first conductive feature to an electrical connection feature of the substrate.

[022] One or more of the conductors of the interposer is each connected to a corresponding electrode that electrically connects the conductor to a corresponding electrical connection feature of the substrate. The electrodes include one or more of solder balls, pillars, studs, bumps, pads, and conductive particles. The electronic component has a thickness that is no greater than the combination of a thickness of the electrodes and a thickness of the electrical connection features of the substrate.

[023] The substrate includes a material that is flexible. The substrate includes an elastomeric material. The substrate is stretchable. The conductors of the interposer include meandering conductors.

[024] The second surface of the electronic component is 50 μm or less, 25 μm or less, or 10 μm or less from the surface of the substrate. The second surface of the electronic component is in physical contact with the surface of the substrate. A separation between the substrate and the interposer is 500 μm or less, 200 μm or less, 100 μm or less, or 50 μm or less.

[025] In an aspect, a method includes electrically connecting an electronic component to one or more conductive features formed on a second substrate; disposing the second substrate on a surface of a first substrate, including positioning the electronic component between the first substrate and the second substrate, in which a separation between the second substrate and the surface of the first substrate is 500 μm or less; and electrically connecting one or more of the conductive features of the second substrate each to a corresponding electrical connection feature of the first substrate.

[026] Embodiments can include one or more of the following features.

[027] Electrically connecting the electronic component includes electrically connecting one or more bond pads of the electronic component each to a corresponding one of the conductive features. Positioning the electronic component between the first substrate and the second substrate includes positioning the electronic component such that a surface including the bond pads faces away from the second substrate.

[028] Electrically connecting the one or more conductive features each to a corresponding electrical connection feature includes applying a stimulus to an adhesive

disposed between the first substrate and the second substrate. Applying the stimulus includes applying heat or light. The adhesive includes a conductive adhesive.

[029] The method includes bonding the first substrate to the second substrate. The method includes curing an adhesive disposed between the first substrate and the second substrate.

[030] The first substrate includes a printed circuit board. The first substrate includes a printed flexible circuit board. The second substrate includes an interposer. The electronic component has a thickness that is no greater than the combination of a thickness of the electrodes and a thickness of the electrical contacts of the first substrate.

[031] In an aspect, a method includes disposing one or more electronic components on a first surface of an interposer substrate, in which one or more sets of conductive features are formed on the first surface of the interposer substrate and extend away from the interposer substrate, in which each conductive feature extends to a height of 500 µm or less from the first surface of the interposer substrate, and in which the height of the conductive features is greater than or equal to a height of the electronic components; electrically connecting each electronic component to a corresponding set of conductive features; and separating the interposer substrate into multiple packages, each package including a portion of the interposer substrate, one or more of the electronic components, and the corresponding set of conductive features.

[032] Embodiments can include one or more of the following features.

[033] Each conductive feature extends to a height of 200 µm or less, 100 µm or less, or 50 µm or less from the first surface of the interposer substrate. The conductive features are not formed through a thickness of the interposer substrate.

[034] Separating the interposer substrate into multiple packages includes dicing the interposer substrate. The method includes attaching the interposer substrate to a support substrate. Dicing the interposer substrate into multiple packages includes dicing the support substrate such that each package includes a portion of the support substrate. The method includes attaching the interposer substrate to the support substrate with a temporary bonding material.

[035] The method includes connecting one of the packages to a device substrate such that at least one of the electronic components of the package is disposed between the interposer substrate and the device substrate. Connecting the package to the device

substrate includes electrically connecting the conductive features of the package to respective electrical connection features of the device substrate. Connecting the package to the device substrate includes orienting the package such that the electronic component is between the interposer substrate and the device substrate.

5 **[036]** The method includes forming molded layer on the surface of the interposer substrate, the molded layer including an encapsulant at least partially covering the electronic components and sets of conductive features. The method includes thinning the molded layer to expose ends of the conductive features. The electronic components include ultra-thin electronic components.

10 **[037]** In an aspect, a method includes forming one or more interconnection structures on an interposer substrate, including connecting a first end of each of one or more interconnection structures to corresponding conductive features on a surface of an interposer substrate, in which an electronic component disposed on the surface of the interposer substrate is electrically connected to one or more of the conductive features,
15 and in which a second surface of the electronic component and a second end of each of the interconnection structures are less than 500 µm from the surface of the interposer substrate; disposing the interposer substrate on a device substrate, including positioning the electronic component between the interposer substrate and the device substrate; and electrically connecting the second end of each of one or more of the interconnection
20 structures to a corresponding electrical connection feature of the device substrate.

[038] In an aspect, an apparatus includes a substrate; conductive features formed on a surface of the substrate, each conductive feature having a first end and a second end on the first side of the substrate, in which at least a portion each conductive feature extends away from the substrate, in which each conductive feature extends to a height of 500 µm
25 or less from the surface of the substrate; an electronic component disposed on the surface of the substrate, one or more connection elements on a first surface of the electronic component each electrically connected to the first end of a corresponding one of the conductive features, in which a second surface of the electronic component is 500 µm or less from the surface of the substrate, and in which the height of the conductive features
30 is greater than or equal to the separation between the second surface of the electronic component and the surface of the substrate; and a second end of one or more of the conductive features arranged to each be in electrical contact with a corresponding electrical contact of a circuit board.

[039] Embodiments can include one or more of the following features.

[040] The second surface of the electronic component is 200 μm or less, 100 μm or less, or 50 μm or less from the surface of the substrate. A separation between the surface of the substrate and the circuit board is 500 μm or less, 200 μm or less, 100 μm or less, or 50 μm or less. The second surface of the electronic component is 100 μm or less, 50 μm or less, 25 μm or less, or 10 μm or less from the circuit board. The second surface of the electronic component is in physical contact with the circuit board.

[041] The conductive features are not formed through a thickness of the substrate. The apparatus includes multiple electronic components disposed on the surface of the first side of the substrate. The first ends of the conductive features are electrically connected to the corresponding connection elements of the electronic component through an interconnection system. When the conductive features are in electrical contact with the electrical contacts of the circuit board, the circuit board and the electronic component are both disposed on a same side of the substrate.

[042] The second end of one or more of the conductive features is each in physical contact with a corresponding electrode disposed on the surface of the substrate. The electrodes include one or more of solder balls, pillars, studs, bumps, pads, and conductive particles. The second end of each conductive feature includes a contact pad formed on the surface of the substrate. The second ends of one or more of the conductive features are arranged in an array. The second ends of one or more of the conductive features are positioned around the edges of the electronic component. A pitch of the connection elements of the electronic component is different than a pitch of the electrical contacts of the circuit board.

[043] The apparatus includes a support substrate attached to the substrate such that the substrate is disposed between the electronic component and the support substrate. The support substrate is releasably attached to the substrate. The support substrate is attached to the substrate with a temporary bonding material. The temporary bonding material has an adhesion that changes responsive to application of a stimulus. The substrate includes a material that is flexible. The substrate is stretchable. The electronic component includes a material that is flexible. The apparatus includes an adhesive disposed on the surface of the substrate.

[044] In an aspect, an assembly includes an interposer substrate, multiple sets of conductive features being formed on a surface of the interposer substrate, in which at least a portion of each conductive feature extends away from the interposer substrate, and in which each conductive feature extends to a height of 500 μm or less from the surface

of the interposer substrate; and multiple electronic components disposed on the surface of the interposer substrate, each electronic component corresponding to one of the multiple sets of conductive features formed on the surface of the interposer substrate, in which, for each electronic component, one or more connection elements on a first surface of the
5 electronic component are each electrically connected to an end of a corresponding one of the conductive features of the corresponding set, in which a second surface of the electronic component is 500 μm or less from the surface of the interposer substrate, and in which the height of the conductive features is greater than or equal to the separation between the second surface of the electronic component and the surface of the interposer
10 substrate.

[045] Embodiments can include one or more of the following features.

[046] The assembly includes a support substrate, wherein the interposer substrate is disposed between the support substrate and the multiple electronic components.

[047] In an aspect, an apparatus includes a first substrate including one or more
15 electrical connection features; and an assembly including a second substrate; conductive features formed on the second substrate, one or more of which are electrically connected to corresponding electrical connection features of the first substrate; and an electronic component positioned at a surface of the second substrate and electrically connected to one or more of the conductive features, the surface of the second substrate facing the first
20 substrate, in which a separation between the surface of the second substrate and the first substrate is 500 μm or less.

[048] In an aspect, an apparatus includes a first substrate, a first electrical connection feature formed on a surface of the first substrate; and a molded layer including an electronic component and a conductive element encapsulated within a molding material,
25 a second electrical connection feature formed on a surface of the electronic component, the second electrical connection feature of the electronic component being electrically connected to the first electrical connection feature of the first substrate through the conductive element; the surface of the electronic component facing away from the surface of the first substrate.

30 **[049]** Embodiments can include one or more of the following features.

[050] The apparatus includes a second substrate attached to the molded layer such that the molded layer is positioned between the first substrate and the second substrate. At least a portion of the conductive element is in physical contact with the surface of the

second substrate. The conductive element includes a first conductive feature and a second conductive feature, the first conductive feature formed along a surface of the second substrate, and the second conductive feature formed through a thickness of the molded layer. The second substrate is releasably attached to the molded layer. The second substrate is attached to the molded layer with a temporary bonding material. The temporary bonding material has an adhesion that changes responsive to application of a stimulus. The second substrate is removable from the molded layer by one or more of wet etching, dry etching, and mechanical removal. The method includes a third substrate attached to the second substrate such that the molded layer and second substrate are positioned between the first substrate and the third substrate. The third substrate is releasably attached to the second substrate. The third substrate is attached to the second substrate with a temporary bonding material. The apparatus includes a second conductive element formed through a thickness of the second substrate and electrically connected to the portion of the conductive element. The apparatus includes a second electronic component electrically connected to the second conductive element, in which the second substrate is disposed between the molded layer and the second electronic component. The apparatus includes a second molded layer disposed such that the molded layer is between the second molded layer and the first substrate, the second molded layer including a second electronic component and a third conductive element encapsulated within a molding material, a third electrical connection feature of the second electronic component formed on a surface of the second electronic component, the third electronic feature of the electronic component being electrically connected to the second conductive element of the second substrate through the third conductive element. The surface of the second electronic component faces away from the first molded layer.

[051] The apparatus includes a second substrate disposed such that the molded layer is between the first substrate and the second substrate, the second substrate including one or more third electrical connection features electrically connected to one or more of the first electrical connection features of the first substrate. The apparatus includes a second electronic component disposed on the second substrate and electrically connected to one or more of the third electrical connection features. The third electrical connection features are formed through a thickness of the second substrate and in which one or more of the first electrical connection features of the first substrate are formed through a thickness of the first substrate. The surface of the first substrate faces the second substrate, and including a second electronic component disposed on a second surface of the first

substrate, the second electronic component electrically connected to one or more of the third electrical connection features.

[052] The second electrical connection feature of the electronic component is connected to the conductive element through an interconnection system.

[053] The conductive element includes a first conductive element and a second conductive element. The first conductive element is oriented parallel to the molded layer and the second conductive element is oriented perpendicular to the molded layer. A first end of the first conductive feature is in physical contact with an interconnection system that is in contact with the second electrical connection feature of the electronic component, and a second end of the first conductive feature is in physical contact with a first end of the second conductive feature. A second end of the second conductive feature includes an interconnection structure. The interconnection structure includes one or more of solder cap, solder ball, pillar, stud, bump, pad, conductive particle. The interconnection structure includes a conductive adhesive. The interconnection structure is in physical contact with the first electrical connection feature of the first substrate. The second end of the second conductive feature is flush with a bottom surface of the molded layer. The second conductive feature is formed through a thickness of the molded layer. The first conductive feature is exposed on a top surface of the molded layer, the top surface facing away from the first substrate. A top surface of the first conductive feature is coplanar with the top surface of the molded layer. The apparatus includes a second electronic component disposed on the top surface of the molded layer, in which an electrical connection feature of the second electronic component is electrically connected to the exposed first conductive feature.

[054] The electronic component includes an ultra-thin electronic component. The apparatus includes an underfill in a gap between the molded layer and the first substrate. The apparatus includes an assembly including a second electronic component, the assembly disposed on the molded layer such that the molded layer is positioned between the assembly and the first substrate. The molded layer includes multiple conductive elements, and in which the second electronic component is electrically connected to the first substrate through a conductive element. The molded layer includes multiple electronic components encapsulated within the molding material. The multiple electronic components are disposed between the conductive element and the first substrate.

[055] In an aspect, an apparatus includes a first substrate; a molded layer disposed on the first substrate such that a first surface of the molded layer is in contact with the first

substrate, the molded layer including an electronic component encapsulated within a molding material, the electronic component having electrical connection features, the electronic connection features facing the first substrate; and conductive elements, each conductive element electrically connected to a corresponding electrical connection
5 feature of the electrical component; in which first ends of the conductive elements are exposed at a second surface of the molded layer and arranged in an arrangement corresponding to an arrangement of electrical contacts of a circuit board.

[056] Embodiments can include one or more of the following features.

[057] The electronic component includes an ultra-thin electronic component. The
10 apparatus includes a second substrate attached to the first substrate such that the first substrate is positioned between the molded layer and the second substrate. The second substrate is releasably attached to the first substrate. The second substrate is attached to the first substrate with a temporary bonding material. The first substrate is releasably attached to the molded layer. The first substrate is removable from the molded layer by
15 one or more of wet etching, dry etching, and mechanical removal. The first substrate is attached to the molded layer with a temporary bonding material.

[058] The apparatus includes an interconnection structure in physical and electrical contact with each of the first ends of the conductive elements. The interconnection structure includes one or more of solder cap, solder ball, pillar, stud, bump, pad, and
20 conductive particle. The interconnection structure includes a conductive adhesive.

[059] Second ends of the conductive elements are in physical and electrical contact with an anisotropic conductive adhesive that is in electrical contact with the electrical connection features of the electronic component. Each conductive element includes a first portion formed on a surface of the first substrate and a second portion formed through a
25 thickness of the molded layer. The apparatus includes an interconnection structure disposed at the first end of each conductive element. The apparatus includes a second conductive element formed through a thickness of the first substrate and electrically connected to at least one of the conductive elements of the molded layer. The apparatus includes a second electronic component electrically connected to the second conductive
30 element, in which the first substrate is disposed between the molded layer and the second electronic component.

[060] In an aspect, an apparatus includes a molded layer including: an electronic component encapsulated within a molding material, the electronic component having

electrical connection features, the electronic connection features facing a first surface of the molded layer; and conductive elements, each conductive element electrically connected to a corresponding electrical connection feature of the electrical component; in which first ends of the conductive elements are exposed at a second surface of the molded layer and arranged in an arrangement corresponding to an arrangement of electrical contacts of a circuit board.

[061] Embodiments can include one or more of the following features.

[062] A portion of each conductive element is exposed at the first surface of the molded layer. The apparatus includes a second electronic component disposed on the first surface of the molded layer. The second electronic component is electrically connected to one or more of the exposed portions of the conductive elements. The second electronic component includes one or more of a passive component, a battery, and a sensor. The apparatus includes an interconnection structure in physical and electrical contact with each of the first ends of the conductive elements. The interconnection structure includes one or more of solder cap, solder ball, pillar, stud, bump, pad, and conductive particle. The interconnection structure includes a conductive adhesive. Second ends of the conductive elements are in physical and electrical contact with an anisotropic conductive adhesive that is in electrical contact with the electrical connection features of the electronic component. The apparatus includes a second molded layer disposed facing the first surface of the molded layer, the second molded layer including: a second electronic component encapsulated within a molding material, the second electronic component having second electrical connection features, the second electrical connection features facing a first surface of the second molded layer; and second conductive elements, a second end of each second conductive element electrically connected to a corresponding second electrical connection feature of the electrical component, in which first ends of the second conductive elements are exposed at a second surface of the second molded layer and arranged in an arrangement corresponding to an arrangement of the exposed portions of the conductive elements.

[063] In an aspect, an apparatus includes a molded layer including multiple electronic components encapsulated within a molding material, each electronic component having electrical connection features facing a first surface of the molded layer; and multiple sets of conductive elements, each set corresponding to one of the electronic components, each conductive element of a set electrically connected to a corresponding electrical

connection feature of the corresponding electronic component; in which first ends of the conductive elements are exposed at a second surface of the molded layer.

[064] Embodiments can include one or more of the following features.

[065] The apparatus includes a substrate, in which the molded layer is disposed on the substrate such that the first surface of the molded layer is in contact with the substrate. The apparatus includes a support substrate, in which the substrate is disposed on the support substrate such that the substrate is between the support substrate and the molded layer.

[066] The apparatus includes multiple interconnection structures, each interconnection structure in physical and electrical contact with the first ends of a corresponding set of conductive elements. Each interconnection structure includes one or more of solder cap, solder ball, pillar, stud, bump, pad, conductive particle.

[067] The apparatus includes a second electronic component disposed on the first surface of the molded layer. The second electronic component is in electrical contact with at least one of the conductive elements of one of the sets of conductive elements. The apparatus includes multiple second electronic components disposed on the first surface of the molded layer, each second electronic component in electrical contact with at least one of the conductive elements of a corresponding set of conductive elements. The second electronic component includes one or more of a passive component, a battery, and a sensor.

[068] In an aspect, a method includes attaching an interposer substrate to a support substrate, in which multiple sets of conductive features are formed on a surface of the interposer substrate; electrically connecting each of multiple electronic components to a corresponding set of conductive features; forming a molded layer on the surface of the interposer substrate, the molded layer including an encapsulant covering the electronic components and sets of conductive features; thinning the molded layer to expose ends of the conductive features, in which thinning the molded layer includes thinning the electronic components; and separating the thinned molded layer into multiple packages, each package including at least one of the electronic components, and the corresponding set of conductive features.

[069] Embodiments can include one or more of the following features.

[070] Thinning the electronic components includes forming ultra-thin electronic components. The method includes forming an interconnection structure at the exposed end of each of one or more of the conductive features. The interconnection structure includes one or more of a solder cap, a solder ball, a pillar, a stud, a bump, a pad, and a conductive particle. The method includes attaching the interposer substrate to the support substrate with a temporary bonding material.

[071] The method includes connecting one of the packages to a device substrate. Connecting the package to the device substrate includes electrically connecting the conductive features of the package to respective electrical connection features of the device substrate. The method includes removing the support substrate from the interposer substrate of the connected package.

[072] Separating the thinned molded layer into multiple packages includes dicing the interposer substrate and the support substrate such that each package includes a portion of the interposer substrate and a portion of the support substrate. The method includes connecting one of the packages to a device substrate and removing the portion of the support substrate from the portion of the interposer substrate of the connected package. Connecting the package to the device substrate includes orienting the package such that the electronic component is between the portion of the interposer substrate and the device substrate. The method includes assembling a second molded layer onto the portion of the interposer substrate, the second molded layer including a second electronic component encapsulated within a molding material. Assembling the second molded layer includes electrically connecting the second electronic component to a conductive feature formed through a thickness of the portion of the interposer substrate.

[073] The method includes removing the support substrate from the interposer substrate after thinning the molded layer. Separating the thinned molded layer into multiple packages includes dicing the interposer substrate such that each package includes a portion of the interposer substrate. The method includes connecting one of the packages to a device substrate such that the electronic component is between the portion of the interposer substrate and the device substrate. The method includes assembling a second molded layer onto the portion of the interposer substrate, the second molded layer including a second electronic component encapsulated within a molding material. The method includes assembling the second molded layer includes electrically connecting the second electronic component to a conductive feature formed through a thickness of the interposer substrate.

[074] The method includes removing the support substrate from the interposer substrate after forming the molded layer. The method includes removing the interposer substrate from the molded layer. The method includes removing the interposer substrate by one or more of wet etching, dry etching, and mechanical removal. The method includes attaching the molded layer to a second support substrate. Thinning the molded layer includes thinning the molded layer attached to the second support substrate. Separating the thinned molded layer into multiple packages includes dicing the second support substrate such that each package includes a portion of the second support substrate. The method includes connecting one of the packages to a device substrate such that the electronic component is between the portion of the second support substrate and the device substrate. The method includes removing the portion of the second support substrate from the connected package. When the portion of the second support substrate is removed, one or more electrical connection features of the electronic component are exposed on a surface of the electronic component facing away from the device substrate. The method includes assembling one or more second electronic components onto a surface of the electronic component facing away from the device substrate. The method includes assembling a second molded layer onto the molded layer, the second molded layer including a second electronic component encapsulated within a molding material. Assembling the second molded layer includes electrically connecting the second electronic component to one or more of the conductive features in the molded layer. The method includes removing the second support substrate from the thinned molded layer. When second support substrate is removed, the ends of the conductive features are exposed on a first surface of the molded layer and one or more electrical connection features of the electronic component are exposed on a second surface of the molded layer. The method includes assembling one or more second electronic components onto the second surface of the molded layer. The method includes assembling a second molded layer onto the molded layer, the second molded layer including a second electronic component encapsulated within a molding material. The method includes assembling the second molded layer includes electrically connecting the second electronic component to one or more of the conductive features in the molded layer. Assembling the second electronic component includes electrically connecting the second electronic component to at least one of the electrical connection features exposed on the second surface of the molded layer. The method includes connecting one of the packages to a device substrate such that the first surface of the molded layer of the package faces the device substrate.

[075] We use the term discrete component broadly to include, for example, any unit that is to become part of a product or electronic device, for example, electronic, electromechanical, or optoelectronic components, modules, or systems, for example, any semiconductor material having a circuit formed on a portion of the semiconducting material.

[076] Other aspects, features, implementations and advantages will become apparent from the following description and from the claims.

Brief Description of Drawings

[077] Fig. 1 is a diagram of an integrated circuit package.

[078] Figs. 2A and 2B are side view and top view diagrams, respectively, of an integrated circuit package.

[079] Fig. 3 is a flow chart.

[080] Figs. 4A-4C are diagrams of integrated circuit packages.

[081] Figs. 5-8 are diagrams of fabrication and assembly of integrated circuit packages.

[082] Figs. 9A and 9B are side view and top view diagrams, respectively, of an integrated circuit package.

[083] Figs. 10 and 11 are diagrams of integrated circuit packages.

[084] Fig. 12 is a diagram of an integrated circuit package.

[085] Fig. 13 is a flow chart.

[086] Figs. 14-17 are diagrams of integrated circuit packages.

[087] Fig. 18 is a diagram of an interposer assembly.

[088] Figs. 19A-19C are diagrams of three-dimensional integrated circuit packages.

[089] Figs. 20-24 are diagrams of fabrication and assembly of integrated circuit packages.

[090] Figs. 25 and 26 are diagrams of assembly of an integrated circuit package.

Detailed Description

[091] We describe here an approach to connecting electronic components to substrates, such as printed circuit boards. Although this description sometimes refers to printed circuit boards, it is to be understood that other substrates can also be used. One or more electronic components are electrically connected to or formed on an interposer, and the interposer is electrically connected to the printed circuit board such that the one or more electronic components are positioned between the interposer and the printed circuit board. This arrangement enables an arrangement of electrical contacts of the one or more electronic components (e.g., a dense array of high resolution electrical contacts) to be connected with a different arrangement of electrical contacts on the printed circuit board (e.g., a less dense array of lower resolution electrical contacts). In this arrangement, all circuitry can be formed on the same side of the interposer, allowing the length of the signal lines to be reduced, which in turn reduces parasitic capacitance and resistance and improves device performance. In addition, because all circuitry is formed on the same side of the interposer, the package can be created without through vias formed through the body of the interposer, which can contribute to more straightforward manufacturing and a more reliable package.

[092] In some examples, the electronic component can be a discrete component that is fabricated separately and independently from the interposer, disposed on a surface of the interposer, and electrically connected to the interposer. Examples of discrete components can include a semiconductor die that includes one or more integrated circuits, passive components such as resistors, capacitors, inductors, sensors, microelectromechanical (MEMS) devices, light emitting diodes (LEDs), power sources, chemical or biological sensing elements, or other examples, or a combination of any two or more of them.

[093] In some examples, the electronic component can be formed on the surface of the interposer. In some cases, conductive features on the surface of the interposer can be configured into a certain geometry to form the electronic component (e.g., a planar capacitor, a filter, or another type of electronic component). In some cases, the electronic component can be formed on the surface of the interposer by an additive method such as direct write or screen printing (e.g., to form a printed transistor or another type of printed electronic component).

[094] In some examples, the electronic component can be embedded into a body of the interposer during fabrication of the interposer such that the electronic component forms an integral part of the interposer.

[095] Referring to Fig. 1, in a known mounting technique, an integrated circuit (IC) package 100 including an electronic component 102 is mounted on a printed circuit board 110. The electronic component 102 is mounted in a face-down orientation, meaning that bond pads 104 on the electronic component 102 face towards the printed circuit board 110. An interposer 106 disposed between the electronic component 102 and the printed circuit board 110 serves to electrically connect bond pads 104 on the electronic component 102 to electrical connection features, such as contact pads 108, on the printed circuit board.

[096] The pitch and line/space resolution of the bond pads 104 on the electronic component 102 can reflect the pitch and line/space resolution of the circuitry in the electronic component 102. By pitch, we mean the distance between an identical point in two adjacent features in a pattern of repeating features, such as bond pads. Pitch can be viewed as the sum of the width of a feature (e.g., a bond pad) and the width of the space on one side of the feature (e.g., a space filled by a material, such as an insulator) that separates that feature from an adjacent feature. By line/space resolution, we mean the size and spacing of the smallest features on the printed circuit boards, such as the conductor lines. The size of the smallest features can be approximately equal to the smallest line spacing. Features having a large line width and large line spacing are referred to as having a coarse line/space resolution; features having a small line width and small line spacing are referred to as having a fine line/space resolution. Sometimes, the pitch of the bond pads 104 on the electronic component 102 does not match the pitch of the contact pads 108 on the printed circuit board 110 to which the electronic component 102 is to be connected. For instance, some integrated circuits may reach a pitch of 10 microns, but printed circuit boards may not have contact pads 108 with the same pitch. For instance, the contact pads 108 on printed circuit boards are often larger and less closely spaced than the bond pads 104 on electronic components.

[097] The interposer 106 enables the electronic component 102 to be electrically connected to the printed circuit board 110 even if there is a mismatch between the pitch of the bond pads 104 on the electronic component 102 and the contact pads 108 on the printed circuit board 110. In the example of Fig. 1, the electronic component 102 is disposed on a top surface 112 of the interposer 106, and the interposer 106 is disposed on

a top surface of the printed circuit board 110. By top surface, we mean the surface of the interposer 106 that faces away from the printed circuit board 110. Circuitry (e.g., conductors) formed through a body 114 of the interposer enables the electronic component 102 to be electrically connected to interface electrodes 116 formed on a bottom surface 118 of the interposer 106, which can contact the contact pads 108 on the printed circuit board 110. By bottom surface, we mean the surface of the interposer 106 that faces the printed circuit board 110.

[098] A redistribution layer (RDL) 120 is disposed on the top surface 112 of the interposer 106 or forms an inner layer of a multilayer interposer. The redistribution layer 120 is formed of a conductive material such as aluminum, copper, gold, silver, or another conductive material, or a combination of any two or more of them. The redistribution layer 120 includes multiple, fine resolution conductive features, such as conductive lines 122. Each conductive line 122 is positioned such that one end of the conductive line aligns with a corresponding one of the bond pads 104 on the electronic component and the other end forms an RDL contact pad 124. The pitch of the RDL contact pads 124 can be greater than the pitch of the bond pads 104 of the electronic component 102. For example, the width of the bond pads 104 can be between about 10 μm and about 1,000 μm and the pitch of the bond pads 104 can be between about 20 μm and about 2,000 μm.

[099] Each RDL contact pad 124 is electrically connected to a conductive vertical interconnect structure 126 (sometimes referred to as a through via 126) formed through the thickness of the body 114 of the interposer 106. We use the term "through via" broadly to include, for example, any vertical interconnect that is used to electrically connect a component on the top surface of a substrate to a component on the bottom surface of a substrate. Each through via 126 connects one of the RDL contact pads 124 formed on the top surface 112 of the interposer 106 to a corresponding one of the interface electrodes 116 formed on the bottom surface 118 of the interposer. The interface electrodes 116 can be, for instance, solder balls, pillars, studs, bumps, pads, conductive particles, or other electrode structures. Each interface electrode 116 contacts a corresponding contact pad 108 on the printed circuit board 110. As a result, an electrical connection is established from each of the bond pads 104 on the electronic component 102, through the thickness of the interposer 106, and to a corresponding contact pad 108 on the printed circuit board 110.

[0100] The IC package 100 can be secured to the printed circuit board 110 by an underfill layer 128, such as a non-conductive polymer, e.g., a thermosetting polymer such

as an epoxy. The underfill layer 128 can help to resolve thermal mechanical issues arising from the coefficient of thermal expansion (CTE) mismatch between the silicon die or interposer and the printed circuit board to which the IC package is attached. The electronic component 102 and interposer 106 can be encased or encapsulated in a
5 protective case 130, such as a plastic or ceramic case, that can provide mechanical or environmental protection to the electronic component 102 and the circuitry of the interposer 106.

[0101] Referring to Figs. 2A (side view) and 2B (top view), in an IC package 200, an electronic component 202 is mounted on a printed circuit board 210. An inverted
10 interposer 206 electrically connects conductive features, such as bond pads 204, on the electronic component 202 to electrical connection features, such as contact pads 208, on the printed circuit board 210, thus creating an electrical connection between the electronic component 202 and the printed circuit board 210. In the example of Figs. 2A and 2B, the electronic component 202 is shown as a discrete component. In some
15 examples, the electronic component 202 can be formed on the surface of the inverted interposer 206 or embedded within a body 214 of the inverted interposer 206. In some examples, the inverted interposer 206 can create an electrical connection between multiple electronic components 202 and the printed circuit board 210.

[0102] The inverted interposer 206 can be formed of silicon, glass, an organic material,
20 or another material compatible with integrated circuit interconnection and packaging technologies. Example organic materials for the inverted interposer 206 can include polymers such as polyimide (PI), polytetraflouroethylene (PTFE), polyethylene (PET), composite materials such as glass-reinforced epoxy laminate sheets commonly used in printed circuit board fabrication, or a combination of any two or more of them. In the
25 inverted interposer 206, the same surface of the interposer (e.g., a bottom surface 218 of the interposer 206) faces both the electronic component 202 and the printed circuit board 210. In this arrangement, the electronic component is positioned in a gap 215 between the inverted interposer 206 and the printed circuit board 210. The presence of the inverted interposer 206 enables the electronic component 202 to be electrically connected to the
30 printed circuit board 210 even if there is a mismatch between the dimensions of the bond pads 204 on the electronic component 202 and the contact pads 208 on the printed circuit board 210.

[0103] A redistribution layer 220 is disposed on the bottom surface 218 of the inverted interposer 206, which is the same surface that faces both the electronic component 202

and the printed circuit board 210. The redistribution layer 220 includes multiple, fine resolution conductive features, such as conductive lines 222, each of which connects one of the bond pads 204 on the electronic component 202 to a corresponding RDL contact pad 224. In some examples, the bond pads 204 can include bumps and the conductive lines 222 connect the bumps of the bond pads 204 to the corresponding RDL contact pads 224. In order for the bond pads 204 or the bumps of the bond pads 204 on the electronic component 202 to contact the redistribution layer 220, the electronic component 202 is disposed in a face-up orientation such that the bond pads 204 on the electronic component 202 face away from the printed circuit board 220.

[0104] In some examples, the RDL contact pads 224 can be located toward the periphery of the interposer 206, resulting in a fan-out design of the conductive lines 222. In this arrangement, the contact pads 224 are positioned around the edges of the electronic component 202 such that the electronic component is inside of a shape defined by the contact pads 224. In some examples, the RDL contact pads can be formed into other arrangements, such as arranged in an array. The redistribution layer thus acts as a signal routing structure that routes signals from the bond pads 204 of the electronic component 202 to other locations. In some examples, the RDL contact pads 224 can be formed into an arrangement that aligns with the arrangement of the contact pads 208 on the printed circuit board 210.

[0105] Each RDL contact pad 224 can be in direct, physical and electrical contact with a corresponding interface electrode 216, such as a solder ball, pillar, stud, bump, pad, or other electrode structure. Each interface electrode 216 contacts a corresponding contact pad 208 on the printed circuit board 210. As a result, an electrical connection is established from a bond pad 204 on the electronic component 202 to a corresponding contact pad 208 on the printed circuit board 210.

[0106] In the IC package 200 of Fig. 2, the electrical connection between the electronic component 202 and the printed circuit board 210 is achieved without the use of through vias through a body 214 of the inverted interposer 206. Rather, the electrical connection is implemented through circuitry that is all formed on the same surface (e.g., the bottom surface 218) of the inverted interposer 206. The absence of through vias allows the IC package 200 to be fabricated using a more straightforward fabrication process, e.g., without the use of lithography and etching process steps used to form through vias through the body 214 of the interposer, thus reducing manufacturing costs. In addition,

the formation of all of the circuitry on the same surface of the inverted interposer 206, without the presence of through vias, can result in a more reliable IC package 200.

[0107] The formation of all of the circuitry on the same surface of the inverted interposer 206 also reduces the length of the signal lines between the bond pads on the electronic component 202 and the corresponding contact pads 208 on the printed circuit board 210. As a result, the parasitic capacitance and resistance along the signal lines is reduced, and hence the performance of the IC package 200 can be enhanced.

[0108] The IC package 200 can be secured to the printed circuit board 210 by an underfill layer 228, such as a non-conductive epoxy. In some examples, the inverted interposer 206 can be encased or encapsulated in a protective case 230, such as a plastic or ceramic case, that can provide mechanical or environmental protection. However, because the electronic component 202 and the circuitry of the inverted interposer 206 are already protected by their position adjacent the bottom surface 218 of the inverted interposer 206, such a protective case can be optional. The absence of a protective case can allow the IC package 200 to be fabricated with fewer process steps and less material, and thus fabrication can be more efficient and less expensive.

[0109] In some examples, the IC package 200 using the inverted interposer 206 can be assembled if the height of the electronic component 202 satisfies a criterion, such as that the height of the electronic component 202 plus the bond pads 204 and any desired clearance between the electronic component 202 and the printed circuit board 210 is equal to or smaller than the separation between the bottom surface 218 of the inverted interposer 206 and the printed circuit board 210 (known as the standoff height). For instance, the electronic component 202 can have a thickness that is no greater than the combination of a thickness of the electrodes 216 and a thickness of the contact pads 208 of the printed circuit board 210 less than the height of the bond pads 204. In a specific example, if the expected standoff height after bonding the inverted interposer 206 to the printed circuit board 210 is 50 μm, then the IC package 200 can be compatible with electronic components that are less than about 50 μm thick, less than about 40 μm thick, less than about 30 μm thick, less than about 25 μm thick, less than about 20 μm thick, less than about 10 μm thick, or less than about 5 μm thick.

[0110] In some examples, the overall height of the IC package 200 can be less in the configuration shown in Fig. 2 than if components of the same thickness were assembled according to the IC package 100. In the IC package 200, the electronic component 202 is disposed within a space between the bottom surface 218 of the inverted interposer 206

and the printed circuit board 210 that would have existed even without the presence of the electronic component 202. In contrast, in the IC package 100, the electronic component 102 is disposed on the top surface 112 of the interposer 106, increasing the height of the IC package 100 by an amount equal to at least the thickness of the electronic component 102. The low profile of the IC package 200 thus enables the IC package 200 to be used in applications for which thinner components are appropriate.

[0111] In the example of Fig. 2, the circuitry of the inverted interposer 206, such as the redistribution layer 220 and the interface electrodes 216, is formed on the bottom surface 218 of the inverted interposer 206. For instance, the redistribution layer 220 can be formed by deposition techniques such as plating, etching, thin film processing techniques, thick film processing techniques, direct write, or other techniques compatible with forming patterned conductors on a substrate.

[0112] In some examples, some or all of the circuitry of the inverted interposer 206, such as the redistribution layer 220, can be embedded within the body 214 of the inverted interposer 206. For instance, embedding some or all of the circuitry within the body 214 of the inverted interposer 206 can be useful if a complete electric circuit is formed on the bottom surface of the interposer, thus not allowing sufficient space on the surface of the interposer to create a network of conductors without conductor lines crossing. In an example, a portion of the redistribution layer 220 is buried in the body 214 of the interposer and accessed through blind vias. In some examples, a buried redistribution layer can be used if the pads 204 are arranged in an array pattern in order to allow access to the inner pads.

[0113] In some examples, additional electronic components can be disposed or formed on the bottom surface 218, on a top surface 212 of the inverted interposer 206, or both, or can be embedded within the body 214 of the inverted interposer 206.

[0114] In some examples, multiple electronic components 202 can be electrically connected to the printed circuit board 210 via electrical connections through a single inverted interposer 206. For instance, multiple electronic components 202 can be positioned between the inverted interposer 206 and the printed circuit board 210. In some cases, one or more electronic components 202 can be positioned between the inverted interposer 206 and the printed circuit board 210 and one or more electronic components can be mounted on the top surface 212 of the inverted interposer 206. In some cases, one or more electronic components can be embedded within the body 214 of the inverted interposer 206. By embedded, we mean formed within the material of the body 214.

[0115] Referring to Fig. 3, in an example approach to assembling an IC package with an inverted interposer, such as the IC package 200, the bond pads on an electronic component are each electrically connected to a corresponding conductive line on a bottom surface of an inverted interposer (600). For instance, the connection can be made using, soldering, adhesive bonding, thermocompression bonding, ultrasonic or thermosonic bonding, diffusion bonding, or other techniques, or a combination of any two or more of them. Each conductive line terminates in a contact pad that is in electrical contact with a corresponding interface electrode disposed on the bottom surface of the inverted interposer. In some examples, the contact pad of a conductive line can be in direct, physical contact with the corresponding interface electrode of the inverted interposer. In some examples, the contact pad can be in electrical contact with the interface electrode via an intermediate conductor, such as conductive adhesive.

[0116] The interface electrodes are each electrically connected to a corresponding contact pad on a printed circuit board (602), thus establishing a connection between the electronic component and the printed circuit board. For instance, the connection can be made using soldering, adhesive bonding, thermocompression bonding, ultrasonic or thermosonic bonding, diffusion bonding or other techniques, or a combination of any two or more of them. The IC package is secured to the printed circuit board, for instance, using an underfill layer, such as a non-conductive epoxy (604).

[0117] Referring to Fig. 4A, in an IC package 250, an electronic component 252 is mounted on a printed circuit board 260. An inverted interposer substrate 256 electrically connects conductive features on the electronic component 252, such as bond pads or bumps on the bond pads, to electrical connection features on the printed circuit board 260. The IC package is oriented such that the bottom surface of the inverted interposer substrate 256 faces both the electronic component 252 and the printed circuit board 260.

[0118] In the IC package 250, the bond pads on the electronic component 252 are in electrical contact with an interconnection system 258. The interconnection system 258 can be an adhesive, such as an anisotropic conductive adhesive, an isotropic conductive adhesive, a conductive adhesive. The interconnection system 258 can be an interconnection formed by soldering, adhesive bonding, ultrasonic or thermosonic bonding, thermocompression bonding, diffusion bonding, or other techniques, or a combination of any two or more of them.

[0119] The interconnection system 258 is in turn in electrical contact with a redistribution structure 262. By redistribution structure, we mean a network of

conductors, such as metal conductors, that redistributes the bond pads on the electronic component and that conducts electrical signals from the electronic component to the printed circuit board. A redistribution structure can be a three-dimensional structure that has conductors oriented in multiple directions, such as conductors oriented substantially parallel to the surface of the interposer substrate 256 and conductors oriented substantially perpendicular to the surface of the interposer substrate 256. The conductors in the redistribution structure 262 that are oriented substantially perpendicular to the surface of the interposer substrate 256 are oriented away from, rather than through, the interposer substrate 256.

[0120] The redistribution structure 262 can include multiple conductive features. Each of the conductive features of the redistribution structure 262 is in electrical contact with a corresponding conductive features of an electrode structure 264. The end 266 of each of the conductive features of the electrode structure 264 is configured to be in electrical contact with a corresponding electrical connection feature on the printed circuit board 260, such as a conductive pad or an electrode structure such as a solder ball, pillar, stud, bump, or other electrode structure. As a result, an electrical connection is established between a bond pad on the electronic component 252 and a corresponding electrical connection feature on the printed circuit board 260. In some examples, the end 266 of one of the conductive features of the electrode structure 264 can be in direct, physical contact with the corresponding electrical connection feature on the printed circuit board 260. For instance, the connection can be made by ultrasonic or thermosonic bonding, thermocompression bonding, diffusion bonding, or other techniques, or a combination of any two or more of them. In some examples, the end 266 of one of the conductive features of the electrode structure 264 can be in electrical contact with the corresponding electrical connection feature via an intermedia conductor, e.g., through a conductor formed by soldering, adhesive bonding, wire bonding, or other techniques, or a combination of any two or more of them.

[0121] In some examples, the conductive features of the redistribution structure 262 are oriented to be substantially parallel to the bottom surface of the inverted interposer substrate 256 and the conductive features of the electrode structure 264 are oriented to be substantially perpendicular to the bottom surface of the inverted interposer substrate 256. The conductive features of the electrode structure 264 can be formed into an arrangement that aligns with the arrangement of the electrical connection features on the printed circuit board 260.

[0122] In some examples, an encapsulant 268 at least partially surrounds the electronic component 252, the redistribution structure 262, and the electrode structure 264. The encapsulant can be, e.g., a non-conductive polymer, such as liquid or film polymers, e.g., epoxies, silicones, polyimides, or other polymers. In some examples, the ends 266 of the conductive features of the electrode structure 264 can extend beyond a bottom surface of the encapsulant to provide a contact point with the printed circuit board 260. In some examples, the ends 266 of the conductive features of the electrode structure 264 can be flush with the bottom surface of the encapsulant. In some examples, no encapsulant is present.

[0123] In some examples, the redistribution structure 262 and the electrode structure 264 are formed of the same material, such as aluminum, copper, silver, gold, tin, alloys based on these metals, or another conductive material (e.g., as shown in Fig. 4C). For instance, the redistribution structure 262 and the electrode structure 264 can be a single, integral conductive feature, such as a conductive frame, e.g., a lead frame. In some examples, the redistribution structure 262 is formed of a different material than the electrode structure 264. For instance, the redistribution structure can be a redistribution layer that includes multiple, fine resolution conductive features, such as conductive lines (e.g., such as in the redistribution layer 220 of Fig. 2A), and the electrode structure can include solder balls, pillars, studs, bumps, pads or other electrode structures (e.g., such as the interface electrodes 216 of Fig. 2A).

[0124] In some examples, the IC package 252 has a height that equal to or less than the height of the electrode structure 264. In some examples, the sum of the heights of the IC package 252 and the interconnection system 258 is equal or less than the sum of the heights of the redistribution structure 262 and the electrode structure 264.

[0125] Referring to Fig. 4B, in some examples, the IC package 250 can be assembled if the height of the electronic component 252 satisfies a criterion, such as that the height of the electronic component 252 plus the redistribution structure 262 and any desired clearance between the electronic component 252 and the printed circuit board 260 is equal to or smaller than the standoff height between the bottom surface of the interposer256 and the printed circuit board 260.

[0126] Referring to Fig 4C, in some examples, an interposer structure 250′ for mounting an electronic component 252′ onto a printed circuit board (not shown) does not include a substrate on a top surface of the interposer structure 250′. In this configuration, the top surface of the redistribution structure 262′ is exposed and coplanar with the top surface of

the encapsulant 268′. This exposure can provide opportunities to assemble additional components on top of the interposer structure 250′, thus increasing electronics packaging density. This exposure can allow for the inclusion of additional components, such as passive electronic components (e.g., resistors, capacitors, filters, or other passive
5 components), batteries, sensors, micro-electromechanical systems, or connectors, or other components. This exposure can provide an exposed area for components with which a user can interface, such as displays, optoelectronic components, touch sensors, switches, fingerprint detectors, or other components.

[0127] In the example of Fig. 4C, the redistribution structure 262′ and the electrode
10 structure 264′ are formed of the same material and form a single, integral structure, such as a conductive frame, e.g., a lead frame. In some examples, the redistribution structure 262′ and the electrode structure, 264′ can be formed of different materials.

[0128] The IC packages 250, 250′ can be rigid structures or flexible structures, such as structures that incorporate flexible electronic components.

15 **[0129]** In some examples, the IC package 252′ has a height that is equal to or less than the height of the electrode structure 264′. In some examples, the sum of heights of the IC package 252′ and the interconnection system 258′ is equal to or less than the sum of the heights of the redistribution structure 262′ and the electrode structure 264′.

[0130] Referring to Fig. 5, in an example approach to fabricating and assembling an IC
20 package, such as the IC package 250 of Fig. 4A, an interposer substrate 450 including multiple interposers 452 is provided (481). Each interposer 452 includes a redistribution structure 454 and an electrode structure 456, such as raised bond pads. In the example shown, the redistribution structure 454 and the electrode structure 456 are formed of the same material; in some examples, the redistribution structure and the electrode structure
25 456 can be formed of different materials, such as to form a conductive frame.

[0131] In some examples, the redistribution structure 454 and the electrode structure 456 can be fabricated directly on the interposer substrate 450. In some examples, the redistribution structure 454 and the electrode structure 456 can be fabricated separately and attached to the interposer substrate 450. In some examples, the redistribution
30 structure 454 can be fabricated directly on the interposer substrate 450 and the electrode structure 456 can be fabricated separately and then attached to the interposer substrate 450. The redistribution structure 454 and the electrode structure 456 can be fabricated using the same process or using different processes.

[0132] Multiple ultra-thin electronic components 458, such as bumped dies, are also provided. By ultra-thin, we mean having a maximum thickness of 50 μm or less, 40 μm or less, 30 μm or less, 25 μm or less, 20 μm or less, 10 μm or less, or 5 μm or less. The ultra-thin electronic components 458 can be thinned and diced, e.g., as described in PCT
5 Application No. PCT/US2017/013216, the contents of which are incorporated here by reference in their entirety. By bumped, we mean that small conductive bumps are formed on the contact pads of the electronic components.

[0133] Each electronic component 458 is assembled into a corresponding interposer 452 using a die assembly method (483), such as contact assembly methods (e.g., pick-and-
10 place methods) or non-contact assembly methods (e.g., thermomechanical selective laser assisted die transfer (tmSLADT)). tmSLADT is described further in PCT Application No. WO2012/142177, WO2016/022528, PCT/US2017/013216, the contents of all of which are incorporated here by reference in their entirety. The bumps on the electronic component 458 are electrically connected to a corresponding conductive feature of the
15 redistribution structure 454 of the interposer 452. Each conductive feature of the redistribution structure 454 is electrically connected to a corresponding conductive feature (e.g., raised bond pad) of the electrode structure 456.

[0134] In some examples, the bond pads on the electronic component 458 are in direct, physical contact with the corresponding conductive features of the redistribution structure
20 454. For instance, the connection can be made using ultrasonic or thermosonic bonding, thermocompression bonding, diffusion bonding, or other techniques, or a combination of any two or more of them. In some examples, the bond pads on the electronic component 458 are in electrical contact with the conductive features of the redistribution structure 454 via an intermediate conductor, such as an intermediate conductor formed by
25 soldering, adhesive bonding, wire bonding, or other techniques, or a combination of any two or more of them.

[0135] The assembly of electronic components on interposers is diced into packages 463 (485), e.g., using methods such as blade dicing, laser dicing, plasma dicing, wet etching, or other dicing techniques, or a combination of any two or more of them. Each package
30 including a single interposer 452 with its corresponding electronic component 458. For instance, the stack can be placed on a dicing tape 467 for the dicing.

[0136] An individual package 463 is bonded to a device substrate 466, such as a printed circuit board (487), using any of a variety of interconnection methods. For instance, the package 464 can be transferred onto the device substrate 466 using a pick-and-place

approach. The conductive features (e.g., raised bond pads) of the electrode structure 456 of the interposer are connected to corresponding conductive features on the device substrate 466 using soldering, adhesive bonding, ultrasonic or thermosonic bonding, thermocompression bonding, diffusion bonding, or other techniques, or a combination of any two or more of them. This bonding establishes an electrical connection from a bond pad on the electronic component 458, through the raised electrode structure 456, and to the conductive feature on the device substrate 466.

[0137] Referring to Fig. 6, in an example approach to assembling an IC package, such as the IC package 250, an interposer substrate 450 including multiple interposers 452 is provided (480). Each interposer 452 includes a redistribution structure 454 and an electrode structure 456, such as raised bond pads. Multiple ultra-thin electronic components 458, such as bumped dies, are also provided.

[0138] The interposer substrate 450 is attached to a support substrate 460 with a temporary bonding material 462 (482). The temporary bonding material 462 provides adhesion between the support substrate 460 and the interposer substrate 450 that can be released upon application of a stimulus, such as ultraviolet (UV) light, heat, a normal or shear mechanical force, or another stimulus, or a combination of any two or more of them. Examples of temporary bonding materials that release upon exposure to heat include, e.g., the Valtron® Heat Release Epoxy System by Valtech or the Logitech's OCON-196 Thin Film Bonding Wax. Examples of temporary bonding materials that release upon exposure to UV light include, e.g., polymers with photofunctional groups that change their chemical structure when exposed to UV light. Other examples of temporary bonding materials are provided in PCT Application No. PCT/US2017/013216, the contents of which are incorporated here by reference in their entirety.

[0139] Each electronic component 458 is assembled into a corresponding interposer 452 using a die assembly method, such as contact assembly methods (e.g., pick-and-place methods) or non-contact assembly methods (e.g., tmSLADT). The bond pads on the electronic component 458 are electrically connected to a corresponding conductive feature of the redistribution structure of the interposer 452, and each conductive feature of the redistribution structure 454 is electrically connected to a corresponding conductive feature (e.g., raised bond pad) of the electrode structure 456. In some examples, the bond pads on the electronic component 458 can be in direct, physical contact with the corresponding conductive feature of the redistribution structure 454. In some examples, the bond pads can be in electrical contact with the corresponding conductive features of

the redistribution structure 454 via an intermediate conductor, such as conductive adhesive.

[0140] The stack formed of the support substrate 460 with the interposers 452 and electronic components 458 assembled thereon is diced into packages 464 (484), each package including a portion of the support substrate 460 underlying a single interposer 452 with its corresponding electronic component 458. For instance, the stack can be placed on a dicing tape 467 for the dicing.

[0141] An individual package 464 is bonded to a device substrate 466, such as a printed circuit board (486). The conductive features (e.g., raised bond pads) of the electrode structure 456 of the interposer are connected to corresponding conductive features on the device substrate 466 to establish an electrical connection from a bond pad on the electronic component 458, through the electrode structure 456, and to the conductive feature on the device substrate 466.

[0142] The support substrate 460 is removed (488). For instance, a stimulus, such as heat, UV light, normal or shear force, or another type of stimulus, can be applied to cause release of the temporary bonding material. The temporary bonding material is also removed, leaving the interposer 452 with connected electronic component 458 assembled on the device substrate. In some examples, an underfill, such as a non-conductive polymer, e.g., an epoxy resin, can be added to fill in the space between the interposer 452 and the device substrate 466.

[0143] Fig. 7 shows an example approach to assembling an IC package, such as the IC package 250, having a thick layer of encapsulation. An interposer substrate 550 including multiple interposers 552 is provided (580). Each interposer 552 includes a redistribution structure 554 and an electrode structure 556, such as raised bond pads. Multiple ultra-thin electronic components 558, such as bumped dies, are also provided.

[0144] The interposer substrate 550 is attached to a support substrate 560 with a temporary bonding material 562 and each electronic component 558 is assembled into a corresponding interposer 552 (582). A layer of an encapsulant 564 is provided to cover the interposers 552 and electronic components 558 (584). The encapsulant 564 can be a curable liquid, a film that is laminated onto the interposer substrate 550, or a powder that is melted to form the encapsulant layer. After deposition, the encapsulant thickness is reduced, e.g., by dry or wet etching or another method, to expose the bond pads 556 of the interposers 552 (586).

[0145] Assembly of the encapsulated interposer assemblies proceeds according to steps 484-488, described above in conjunction with Fig. 6.

[0146] Fig. 8 shows an example approach to assembling an IC package, such as the IC package 250, having a thin layer of encapsulation. An interposer substrate 650 including multiple interposers 652 is provided (680). Each interposer 652 includes a redistribution structure 654 and an electrode structure 656, such as raised bond pads. Multiple ultra-thin electronic components 658, such as bumped dies, are also provided.

[0147] Each electronic component 658 is assembled into a corresponding interposer 652 (682). A layer of a curable liquid encapsulant 664 is provided to cover the interposers 652 to a desired thickness (684), such as a thickness that is less than the height of the raised bond pads 656 of the interposers 652. The encapsulant is cured and assembly of the encapsulated interposer assemblies proceeds according to steps 485-487, described above in conjunction with Fig. 5.

[0148] Referring to Figs. 9A (side view) and 9B (top view), in a flexible hybrid electronics (FHE) package 300, a flexible, solid-state electronic component 302 is mounted in a face-up orientation on a flexible circuit board 310. The flexible electronic component 302 can have a thickness of less than about 50 μm, less than about 40 μm, less than about 30 μm, less than about 25 μm, less than about 20 μm, less than about 10 μm, or less than about 5 μm. By flexible, we mean able to bend without breaking and compromising its functionality.

[0149] A flexible, inverted interposer 306 (sometimes referred to as a flexible interposer) electrically connects conductive features, such as bond pads 304, on the flexible electronic component 302 to electrical connection features 308 on the flexible circuit board 310, thus creating an electrical connection between the flexible electronic component 302 and the flexible circuit board 310. The electrical connection features can be conductors formed by printing, etching, plating, deposition, or another substrate processing technology, or a combination of any two or more of them. In the example of Figs. 9A and 9B, the flexible electronic component 302 is shown as a discrete component. In some examples, the flexible electronic component 302 can be formed on the surface of the flexible interposer 306 or embedded within a body 314 of the flexible interposer 306. In some examples, the flexible interposer 306 can create an electrical connection between multiple flexible electronic components 302 and the flexible circuit board 310. The flexible interposer 306 can be formed of a flexible material, such as a polymer, e.g., polyimide (PI), polytetrafluoroethylene (PTFE), polyethylene (PET), or

another type of polymer. In the flexible interposer 306, the same surface of the interposer (e.g., a bottom surface 318 of the interposer 306) faces both the flexible electronic component 302 and the flexible circuit board 310, thus achieving electrical connection between the flexible electronic component 302 and the flexible circuit board 310 without circuitry through a body 314 of the flexible interposer 306. In this arrangement, the flexible electronic component 302 is positioned between the flexible interposer 306 and the flexible circuit board 310.

[0150] A redistribution layer 320 is disposed on the bottom surface 318 of the flexible interposer 306. The redistribution layer 320 includes multiple, fine resolution conductive features, such as conductive lines 322, each of which connects one of the bond pads 304 on the flexible electronic component 302 to a corresponding RDL contact pad 324. In the example of Figs. 9A and 9B, the RDL contact pads 324 are located toward the periphery of the flexible interposer 306, resulting in a fan-out design of the conductive lines 322. In this arrangement, the contact pads 324 are positioned around the edges of the electronic component 302 such that the electronic component is inside of a shape defined by the contact pads 324. In some examples, the RDL contact pads 324 can be formed into other arrangements. For instance, referring to Fig. 10, in an example, the RDL contact pads 324 can be formed into an area array pattern (sometimes also known as a land grid array). In some examples, the RDL contact pads 324 can be formed into an arrangement that aligns with the arrangement of the printed conductors 308 on the flexible circuit board 310.

[0151] Each RDL contact pad 324 can be in electrical contact with a corresponding conductor 308 on the flexible circuit board 310. For instance, the flexible interposer 306 can be bonded to the flexible circuit board 310 using a flexible interconnection technology, such as adhesive bonding with a conductive adhesive 330, such as an anisotropic conductive adhesive (ACA), an isotropic conductive adhesive, or a conductive adhesive. As a result, an electrical connection is established from a bond pad 304 on the flexible electronic component 302 to a corresponding - conductor 308 on the flexible circuit board 310. The adhesive 330 can also serve to form a seal, such as an airtight or watertight seal, around the electronic component 302.

[0152] When the flexible interposer 306 is bonded to the flexible circuit board 310 using adhesive 330, the spacing between the bottom surface 318 of the flexible interposer 306 and the flexible circuit board 310 is determined based in part on the size of conductive particles 332 in the adhesive 330 and the thickness of the conductors 308. For instance, to achieve a spacing of about 50 μm with printed conductors 308 having a thickness of

about 10-20 μm, adhesive 330 with conductive particles 332 having a diameter of about 30-40 μm can be used.

[0153] In some examples, adhesive 330 is applied to the flexible circuit board 310 in areas where electrical contact between an RDL contact pad 324 and a printed conductor 308 is to occur (e.g., as shown in Fig. 9A). A stimulus, such as heat, light, pressure, or a combination of any two or more of them, can be applied to selected areas (e.g., in areas where electrical contact between an RDL contact pad 324 and a printed conductor 308 is to occur), in order to achieve adhesive bonding and electrical connection only in those areas. For instance, a thermode having an appropriate shape can be used to apply a heat and pressure to certain areas, or an ultraviolet light source can be used to illuminate certain areas with ultraviolet light.

[0154] The FHE package 300, when bonded to the flexible circuit board 310, forms a structure that includes flexible components (the flexible circuit board 310, the flexible interposer 306, and the flexible electronic component 302). The entire assembly is flexible and, in some cases, stretchable (discussed below), and thus compatible with applications for which flexible electronics are appropriate. The flexibility and (in some cases) stretchability enable the assembly to be reliable and resistant to stress. The placement of the electronic component 302 and circuitry between the flexible interposer 306 and the flexible circuit board 310 can further contribute to enhanced reliability of the assembly, e.g., because the electronic component 302 and circuitry are protected from mechanical impact, environmental stimuli or contaminants, or other factors than can be damaging to the sensitive components of the structures.

[0155] Although Figs. 9A and 9B are described with respect to a flexible package, the structure of Figs. 9A and 9B can also be used for a rigid, ultra-thin package.

[0156] In general, the line/space resolution of printed conductor technologies is at least about 10 μm, at least about 20 μm, at least about 30 μm, at least about 40 μm, at least about 50 μm, at least about 60 μm, at least about 70 μm, at least about 80 μm, at least about 90 μm, or at least about 100 μm. Improving the resolution and precision of printed conductors can be challenging and expensive, and thus can be counter to the idea of printed electronics as an inexpensive, high-throughput technology. By using a flexible, inverted interposer to connect an electronic component having a fine pitch (e.g., having sub-100 μm pitch) to a printed circuit board having much coarser line/space resolution, the challenges of improving the resolution of the printed circuit board can be avoided.

Integration of fine pitch electronic components can thus be achieved in an inexpensive and efficient manner.

[0157] An inverted interposer can be attached to the circuit board using standard methods and tooling, thus making the approaches described here compatible with existing
5 processes and technologies.

[0158] The approaches described here can be used to carry out a high assembly rate process to assemble the interposer and electronic component separately from the assembly of the interposer and the printed circuit board. This separation can enable high throughput at relatively low cost, and enables out-of-spec assemblies of interposer and
10 electronic component to be screened out before integration into high cost circuit board assemblies. Furthermore, this separation can make flexible integrated circuits accessible to manufacturers that lack integrated circuit packaging, handling, or test expertise. In addition, this stepwise approach enables faulty components to be easily reworked by replacing one interposer assembly with another.

15 **[0159]** The fan-out interposer design, such as shown in Figs. 2 and 9, enables the assembly of thin electronic components (e.g., less than 50 μm thick) of various sizes to be simplified. For instance, the same size interposer can be used with electronic components of various sizes, reducing the need for a large number of bonding tools.

[0160] In some examples, such as when the size of the flexible interposer 306 is large
20 and the bend radius small, the flexible interposer 302 can be stretchable. In some examples, the use of a stretchable interposer can depend on the interposer size, bend radius, elastic properties of the adhesive, the thickness or material of the flexible circuit board, or other factors, or a combination of any two or more of them. By stretchable, we mean a material that can increase in dimension (e.g., increase in length, width, or height)
25 without damage and compromise to its functionality. Stretchable interposers can be made of materials such as elastomers, e.g., polydimethylsiloxane (PDMS), silicone rubbers, polyurethane, or other elastomers, or a combination of any two or more of them. Stretchable interposers can be made of materials that have an elongation at break ranging from about 10% to about 500%. When the flexible circuit board 310 is bent, the flexible
30 interposer 306 is subjected to tension forces in addition to the bending forces. The magnitude of these tension forces is proportional to the size of the interposer, for a given thickness of the flexible circuit board 310 and a given bend radius. As a result, a shear stress can develop in the adhesive 330. If the flexible interposer 306 is unable to stretch to accommodate the tension forces, the shear stress may exceed the shear strength of the

adhesive material 330, thus causing adhesive failure on the interface between the flexible interposer 306 and the adhesive 330, or in the interface between the flexible circuit board 310 and the adhesive 330, or both, or cohesive failure within the adhesive 330, all resulting in electrical discontinuity between the RDL contact pad 324 and the corresponding conductor 308 on the flexible circuit board 310.

[0161] Referring to Fig. 11, an example of a stretchable, flexible interposer 506 includes a redistribution layer 520 having meandering conductive lines 522, each of which terminates at a corresponding RDL contact pad 524. By a meandering line, we mean a line that is not straight and that has multiple changes in direction. The meandering configuration of the conductive lines 522 enables the conductive lines 522 to sustain a certain amount of stretching without comprising their mechanical and electrical integrity. Thus, even when the stretchable, flexible interposer 506 stretches responsive to a bending of a flexible circuit board to which it is attached, the conductive lines can remain intact.

[0162] Referring to Fig. 12, in a flexible hybrid electronics package 350, a flexible, solid-state electronic component 352 is mounted in a face-up orientation on a flexible circuit board 360. A flexible, inverted interposer 356 (sometimes referred to as a flexible interposer) electrically connects bond pads (not shown) on the flexible electronic component 352 to conductors 358 on the flexible circuit board 360. An adhesive 380 connects the flexible interposer 356 to the flexible circuit board 360.

[0163] A redistribution layer (not shown) is disposed on the bottom surface of the flexible interposer 356. The redistribution layer includes multiple, fine resolution lines 372, each of which connects one of the bond pads on the flexible electronic component 352 to a corresponding RDL contact pad 374. Each RDL contact pad 374 can be in electrical contact with a corresponding one of the conductors 358 on the flexible circuit board 360, thus establishing an electrical connection between the flexible electronic component 352 and the flexible circuit board 360.

[0164] In the example of Fig. 12, the RDL contact pads 374 are all located towards the same side of the flexible interposer 356. As a result, the other side of the flexible interposer can be free to bend. This design can be useful, e.g., to attach flexible interposers having a relatively small number of RDL contact pads 374 to flexible circuit boards. In this design, the bending and tensile stresses are confined to the region of the adhesive 380, which is much smaller than the size of the entire flexible interposer 356.

[0165] Referring to Fig. 13, in an example approach to assembling an FHE package with an inverted interposer, the bond pads on a flexible electronic component are each electrically connected to a corresponding conductive line on a bottom surface of a flexible, inverted interposer (700). Each conductive line terminates in a contact pad.

5 [0166] A complete or partial layer of an adhesive material is disposed on the surface of a flexible circuit board (702). The conductive adhesive may be isotropic conductive adhesive (ICA), anisotropic conductive paste (ACP), anisotropic conductive film (ACF), or another type of conductive adhesive. ICA and ACP are dispensed onto the substrate by methods such as stencil and screen printing, stamping, syringe and jet deposition, or other 10 methods. ACF is precut and adhesively bonded to the substrate. The inverted interposer, including the electrically connected electronic component, is brought into contact with the layer of adhesive material on the flexible circuit board (704) such that the bottom surface of the inverted interposer faces the flexible circuit board. The adhesive material is cured (706), e.g., by application of a stimulus such as light, heat, pressure, or a 15 combination of any two or more of them, such that an electrical connection is established between each contact pad on the bottom surface of the flexible interposer and a corresponding conductor on the flexible circuit board.

[0167] Referring to Fig. 14, in an IC package 750, an ultra-thin electronic component 752 is mounted on a printed circuit board 760. A layer 758, mounted on an interposer 20 substrate 754, includes the ultra-thin electronic component 752 embedded in a molding compound 757, such as a non-conductive polymer, e.g., liquid, sheet, or powdered thermoplastic or thermosetting molding compounds such as an epoxy resin heavily filled with SiO_2. The layer 758 can be thin enough to be flexible when standing on its own. First and second conductive elements 768, 770 embedded in the molding compound 758 25 provide for an electrical connection to be formed between the electronic component 752 and the printed circuit board 760. For instance, the first conductive elements 768 can be a redistribution structure such as the redistribution structure 262 of Fig. 4, and the second conductive elements 770 can be an electrode structure such as the electrode structure 264 of Fig. 4.

30 [0168] An interconnection system 766 is in direct physical and electrical contact with conductive features, such as bond pads or bumps, on the electronic component 752. The interconnection system 766 is also in direct physical and electrical contact with the first conductive features 768 that include multiple, fine resolution conductive features, such as conductive lines. The interconnection system 766 can be an adhesive, such as an

anisotropic conductive adhesive, an isotropic conductive adhesive, a conductive adhesive. The interconnection system 766 can be an interconnection formed by soldering, adhesive bonding, ultrasonic or thermosonic bonding, thermocompression bonding, diffusion bonding, or other techniques, or a combination of any two or more of them.

[0169] Each conductive element 768 is positioned such that a first end of the conductive line is positioned to be in electrical contact with a corresponding conductive feature on the electronic component 752 via the interconnection system 766. A second end of each conductive element 768 is in electrical contact with a corresponding one of the second conductive elements 770. In some examples, the second end of each conductive element can be in direct, physical contact with the corresponding second conductive element. In some examples, the second end of each conductive element can be in electrical contact with the corresponding second conductive element via an intermediate conductor, such as conductive adhesive.

[0170] The second conductive elements 770 are vertical electrode structures formed through the thickness of the molding compound 757. The end of each second conductive element 770 is coplanar with a bottom surface of the molding compound 757, and is connected to an interconnection structure 772, such as a solder cap, solder ball, pillar, stud, bump, pad, conductive particle, or other interconnection structure. When assembled onto the printed circuit board 760, each interconnection structure 772 contacts a corresponding contact pad on the printed circuit board 760. As a result, an electrical connection is established from a conductive feature on the electronic component, through the first and second conductive elements, and to a corresponding contact pad on the printed circuit board 760.

[0171] In some examples, the first and second conductive elements 768, 770 are formed of the same material. For instance, each pair of first and second conductive elements 768, 770 can be a single, integral conductive element, such as a redistribution structure. In some examples, the first conductive elements 768 are formed of a different material than the second conductive elements 770.

[0172] The bottom surface of the molding compound 757 can be finished with a high degree of flatness and smoothness. This allows for an additional redistribution structure to be formed on the bottom surface of the molding compound 757, thus enabling a denser distribution of interconnection structures 772 to be achieved over the entire bottom surface of 757. For instance, interconnection structures 772 can be formed on the bottom surface of the electronic component 752, e.g., as illustrated in Fig. 17 below.

[0173] Referring to Fig. 15, in some examples of an IC package 780, the layer 758 including the electronic component 752 embedded therein is provided without the overlying substrate (754 in Fig. 14). In this configuration, the top surface of the first conductive elements 768 is exposed and coplanar with the top surface of the molding compound 757. This exposure can provide opportunities to assemble additional components on top of the layer 758, thus increasing electronics packaging density. This exposure can allow for the inclusion of thicker components that otherwise would be difficult to fit into the IC package 780, such as passive components, batteries, sensors, or connectors, or other thick components. This exposure can provide an exposed area for compounds with which a user can interface, such as displays, touch sensors, switches, fingerprint detectors, or other components.

[0174] The IC packages 750, 780 can be rigid structures or flexible structures, such as structures that incorporate flexible electronic components.

[0175] Referring to Fig. 16, with the conductive elements 768 exposed, the backside of the IC package 780 can serve as a substrate for assembly of other electronic components. For instance, a three-dimensional assembly 769 can include an electronic circuit containing one or more components mounted on a secondary device substrate 771 that electrically connected to the exposed conductive elements 768 of a first IC package 780, and together mounted onto a device substrate 773.

[0176] Referring to Fig. 17, in some examples, the IC package 750, 780 is provided with a pad redistribution structure 774 to which the interconnection structure 772 is connected.

[0177] Referring to Fig. 18, in some examples, second conductive structures 776 can be formed through the thickness of an interposer substrate 778. The second conductive structures 776 electrically connect the pad redistribution structure 754 on a top surface 775 of the interposer with a network of conductors 777 on a bottom surface 779 of the interposer substrate 778, enabling assembly of additional components or circuits on the bottom surface 779.

[0178] Referring to Figs. 19A-19C, three-dimensional (3-D) IC packages can be assembled by stacking multiple packages each including an electronic component, such as the packages described above. Referring specifically to Fig. 19A, two or more packages without the overlying substrate, such as the IC package 780 or 250’, can be stacked to form a 3-D package 930. Referring to Fig. 19B, two or more packages including a substrate, such as the IC package 750 with interposer 752, can also be stacked

to form a 3-D package 932. Referring to Fig. 19C, to assemble the 3-D packages 930, 932, the arrangement of bond pads on a device substrate 920 (e.g., a printed circuit board) and in each of the individual IC packages can be such that there is unobstructed access from each of the interposers down to the device substrate. For instance, the bond pads can be staggered such that bond pads 934 in a first IC package 936 are directly above a subset of the bond pads 938 on the device substrate 920 but not directly above bond pads 940 in a second IC package 942. Similarly, the bond pads 940 in the second IC package 942 can be positioned to be above a different subset of the bond pads 938 on the device substrate 920.

[0179] Referring to Fig. 20, in an example approach to assembling the IC package 750, an interposer substrate 850 including multiple interposers 852 is provided (880). Multiple electronic components 858, such as bumped dies, are also provided.

[0180] Each interposer 852 includes a redistribution structure 854, such as a conductive frame, and an electrode structure 856. In the example shown, the redistribution structure 854 and the raised bond pads are formed of different materials; in some examples, the redistribution structure 854 and the electrode structure 856 can be formed of the same material. The redistribution structure 854 and the electrode structure 856 can be fabricated directly on the interposer substrate 850 or can be fabricated separately and attached to the interposer substrate 850.

[0181] The interposer substrate 850 is attached to a support substrate 860 with a temporary bonding material 862 (882). Each electronic component 858 is assembled into a corresponding interposer 852 using a die assembly method. A molding process (884), such as compression molding or transfer molding, is used to encapsulate the interposers 852 with assembled electronic components 858 within a molding compound 864, resulting in a molded assembly 866 disposed on the support substrate 860. The molded assembly 866 is thinned (886) to thin the electronic component 858 and to expose the electrode structure 856 at the top surface of the molded assembly 866. For instance, the molded assembly 866 can be thinned using one or more of backgrinding, dry or wet etching or chemical mechanical polishing, or other approaches to component thinning. An interconnection structure 868, such as a solder cap, solder ball, pillar, stud, bump, pad, conductive particle, or other interconnection structure, is assembled (888) onto the exposed electrode structure 856.

[0182] The thinned molded assembly 866 is diced into molded packages (890), each package 870 including a portion of the support substrate 850 underlying a single

interposer 852 with its corresponding electronic component. For instance, the molded assembly 866 can be placed on a dicing tape 872 for the dicing.

[0183] An individual molded package 870 is bonded to a device substrate 874, such as a printed circuit board (892), using any of a variety of interconnection methods. For instance, the molded package 870 can be transferred onto the device substrate 874 using a pick-and-place approach. The interconnection structures 868 connected to the electrode structure 856 of the interposer are connected to corresponding conductive features on the device substrate 874 using soldering, adhesive bonding, ultrasonic or thermosonic bonding, thermocompression bonding, diffusion bonding, or other techniques, or a combination of any two or more of them. This bonding establishes an electrical connection from a bump on the electronic component 858, through the electrode structure 856, and to the conductive feature on the device substrate 874.

[0184] The support substrate 860 is removed (894), for instance, by applying a stimulus to cause release of the temporary bonding material. The temporary bonding material is also removed, leaving the interposer 852 with connected electronic component 858 assembled on the device substrate. In some examples, the support substrate 860 is attached by a permanent adhesive material and the support substrate 860 is removed by wet or dry etching or by a mechanical means, such as polishing.

[0185] Fig. 21 shows an example approach to making an IC package without the overlying substrate, such as the IC package 780. The interposer substrate 850 is attached to the support substrate 860 and the electronic components 858 are assembled into the corresponding interposers as described above (880, 882). A molding process (884) is used to encapsulate the interposers 852 with assembled electronic components 858 within the molding compound 864 to form the molded assembly 866.

[0186] The molded assembly 866 is thinned (886) and the support substrate 860 is released from the thinned molded assembly 866 (180), for instance, by applying a stimulus to cause release of the temporary bonding material. In some examples, the support substrate 860 is not attached by a temporary bonding material and the support substrate 860 is removed by wet or dry etching or by a mechanical means.

[0187] Interconnection structures 868 are assembled onto the exposed bond pads 856. The support substrate 860 can be released or removed before or after thinning of the molded layer. The support substrate 860 can be released or removed before or after the interconnection structures 868 are assembled. The thinned molded assembly is diced into

molded packages 873 (182) and the molded packages are transferred individually to the device substrate 874 (184).

[0188] Referring to Fig. 22, in an example approach to making an IC package without the overlying substrate, such as the IC package 780, the interposer substrate 850 is attached to the support substrate 860 and the electronic components 858 are assembled into the corresponding interposers as described above (880, 882). A molding process (884) is used to encapsulate the interposers 852 with assembled electronic components 858 within the molding compound 864 to form the molded assembly 866. The support substrate 860 is released or removed from the molded assembly 866 (270) and the interposer substrate 850 is removed, e.g., by dry or wet etching or by mechanical polishing or abrasion, leaving the redistribution structure 854 exposed at the bottom surface of the molded layer.

[0189] The molded layer is attached to a second support substrate 876 via a second temporary bonding material and the molded layer is thinned (272) to expose the bond pads 856 at the top surface. Interconnection structures 868 are assembled (274) onto the exposed bond pads 856.

[0190] In some examples, the second support substrate 876 can be attached after thinning of the molded layer. In some examples, the second support substrate 876 can be attached after the interconnection structures 868 are assembled.

[0191] The thinned molded layer on the second support substrate 876 is diced into molded packages 878 (276) and the molded packages 878 are transferred individually to and assembled on the device substrate 874 (278). The second support substrate 876 is removed (280) by applying a stimulus to the second temporary bonding material, causing the redistribution structure 854to be exposed on the top surface of the IC package, thus allowing for the assembly of other electronic components. In some examples, the second support substrate 876 is not attached by a temporary bonding material and is removed by wet or dry etching or by a mechanical means.

[0192] Referring to Fig. 23, in an example approach to making an IC package without the overlying substrate, such as the IC package 780, the interposer substrate 850 is attached to the support substrate 860 and the electronic components 858 are assembled into the corresponding interposers (880). A molding process (884) is used to encapsulate the interposers 852 with assembled electronic components 858 within the molding compound 864 to form the molded assembly 866. The support substrate 860 is released from the

molded assembly 866 (886) and the interposer substrate 850 is removed. The molded assembly 866 is attached to a second support substrate 869 via a second temporary bonding material and the molded layer is thinned (888) to expose the bond pads 856 at the top surface. The second support substrate 869 is removed (889), leaving the redistribution structure 854 exposed at the bottom surface of the molded assembly 866. Interconnection structures 868 are assembled onto the exposed bond pads 856. The thinned molded assembly is diced (891) into molded packages 873 and the molded packages are transferred (893) individually to the device substrate 874.

[0193] Referring to Fig. 24, in an example approach to making an IC package using ultra-thin bumped electronic components, the interposer substrate 850 is attached to the support substrate 860 and the ultra-thin electronic components are assembled into the corresponding interposers using a die assembly method, such as contact assembly methods (e.g., pick-and-place methods) or non-contact assembly methods (e.g., tmSLADT). The assembly can be transferred onto a device substrate and interconnected to the device substrate using the processes shown in any of Figs. 20-23.

[0194] Referring to Fig. 25, an IC package 900 including an ultra-thin electronic component can be embedded into a multilayer device substrate 902. The IC package 900 can be assembled according to any of the approaches described above. A first circuit board 904 includes vias 906 through the circuit board 904 and conductors 908 formed on the top and bottom surfaces of the circuit board 904.

[0195] The IC package 900 is assembled onto the first circuit board 904 such that electrical connection features of the ultra-thin electronic component are electrically connected to the conductors 908 of the first circuit board 904, e.g., by way of conductive features in the IC package 900.

[0196] A second circuit board 910 with an adhesive layer 912 formed thereon is attached to the first circuit board, e.g., by lamination. The adhesive layer can be a liquid, semisolid, or solid material attached or dispensed onto the second circuit board 910 prior to assembly or added separately as a standalone film during assembly. The adhesive layer 912 encompasses the package 900, filling the space between the first and second circuit boards 904, 910. The adhesive layer 912 is sufficiently thick to accommodate the IC package 900.

[0197] In some examples, the second circuit board 910 can include conductors 914 formed on a top surface of the second circuit board 910. To enable the conductors 914 to

be electrically connected to the first circuit board 904, vias 916 can be formed through the second circuit board 910 and the first circuit board 904. Additional electronic components 918 can be assembled onto the second circuit board 910 and electrically connected to the first circuit board 904 by way of the conductors 914 and vias 916.
5 Additional circuit boards can be added to the multilayer device substrate 902, and additional IC packages can be assembled on one or more of the circuit boards of the 3-D device substrate 902, using a similar approach.

[0198] The multilayer device substrate 902 does not require a cavity to be formed in the circuit boards (e.g., the second circuit board 910) to accommodate the thickness of the
10 electronic components. As a result, the multilayer device substrate 902 has a thinner profile and can have a lower production cost than other multilayer substrates with embedded IC packages.

[0199] In some examples, the IC packages described here can be very thin. For instance, referring to Fig. 26, a representative IC package 50 is shown. The IC package 50 can be
15 any of the IC packages described here, such as the IC packages 250, 750. In the representative IC package 50, the thickness of an electronic component 52 and an interconnection system 54 together ($t1+t2$) can be less than the thickness of an interconnection structure 56 and an electrode 58 ($t4+t5$). In some examples, the thicknesses $t1+t2$ and $t4+t5$ can both be about 500 μm or less, such as about 200 μm or
20 less, about 100 μm or less, or about 50 μm or less. For instance, the interconnection system 54 can be, e.g., the interconnection system 258 of the IC package 250 or the interconnection system 766 of the IC package 750. The interconnection structure 56 can be, e.g., the second conductive element 770 of the IC package 750 and the electrode 58 can be, e.g., the interconnection structure 772 of the IC package 750. The interconnection
25 structure 56 and electrode 58 together can correspond to the electrode structure 264 of the IC package 250.

[0200] The thickness of the electronic component 52 and the interconnection system 54 ($t1+t2$) can be less than the thickness $t4$ of the interconnection structure 56. The thicknesses $t1+t2$ and $t4$ can both be about 200 μm or less, such as about 100 μm or less,
30 or about 50 μm or less.

[0201] The separation $t7$ between an interposer substrate 60 and a device substrate 62 in the IC package 50 can be about 500 μm or less, such as about 200 μm or less, about 100 μm or less, or about 50 μm or less. In some cases, the bottom surface of the electronic component 52 can be in close proximity to the device substrate 62. For instance, the

separation *t8* between a bottom surface of the electronic component 52 and the device substrate 62 can be about 100 µm or less, such as about 50 µm or less, about 25 µm or less, or about 10 µm or less. In some examples, the bottom surface of the electronic component 52 can be in physical contact with the device substrate 62 (e.g., *t8* can be
5 zero).

[0202] The thickness of the IC package 50 can be about 500 µm or less, such as about 200 µm or less, about 100 µm or less, or about 50 µm or less.

[0203] Other implementations are also within the scope of the following claims.

10

What is claimed is:

1. An apparatus comprising:

a first substrate including one or more electrical connection features; and

5 an assembly including:

a second substrate;

conductive features in contact with the second substrate, one or more of which are electrically connected to corresponding electrical connection features of the first substrate; and

10 an electronic component between the second substrate and the first substrate and electrically connected to one or more of the conductive features,

in which a separation between the first substrate and the second substrate is 500 µm or less.

15 2. The apparatus of claim 1, in which the assembly includes multiple electronic components between the second substrate and the first substrate.

3. The apparatus of claim 1, in which the electronic component comprises a discrete component.

4. The apparatus of claim 1, in which the electronic component comprises one or more of
20 a sensor, a MEMS device, an LED, a power source, a chemical sensing element, and a biological sensing element.

5. The apparatus of claim 1, in which the electronic component is formed on the second substrate.

6. The apparatus of claim 1, in which the electronic component is embedded into a body
25 of the second substrate.

7. The apparatus of claim 1, comprising a second electronic component embedded within a body of the second substrate.

8. The apparatus of claim 1, in which the electronic component is positioned at a first surface of the second substrate, and in which the assembly comprises a second electronic
5 component positioned at a second surface of the second substrate, the second surface opposite the first surface.

9. The apparatus of claim 1, in which the first substrate comprises a circuit board.

10. The apparatus of claim 1, in which the second substrate comprises an interposer.

11. The apparatus of claim 1, in which the electronic component comprises an integrated
10 circuit.

12. The apparatus of claim 1, in which the one or more conductive features are formed on a surface of the second substrate.

13. The apparatus of claim 12 in which a surface of the first substrate faces the surface of the second substrate on which the conductive features are formed and the electronic
15 component is at least partially within a gap between the two surfaces.

14. The apparatus of claim 12, in which the surface of the second substrate on which the one or more conductive features are formed faces the first substrate.

15. The apparatus of claim 12, in which the gap between the two surfaces is filled with an encapsulant.

20 16. The apparatus of claim 1, in which at least portions of the one or more conductive features are embedded within a body of the interposer.

17. The apparatus of claim 1, in which the electronic component comprises one or more bond pads, at least one of the bond pads electrically connected to a corresponding one of the conductive features of the second substrate.

18. The apparatus of claim 17, in which each bond pad includes a corresponding bump,
5 and in which the at least one of the bond pads is electrically connected to the corresponding one of the conductive features through the bump.

19. The apparatus of claim 17, in which the one or more bond pads are formed on a surface of the electronic component.

20. The apparatus of claim 19, in which a surface of the electronic component on which
10 the one or more bond pads are formed faces the second substrate.

21. The apparatus of claim 17, in which a pitch of the bond pads of the electronic component is different than a pitch of the electrical connection features of the first substrate.

22. The apparatus of claim 1, in which the electronic component is electrically connected
15 to one or more of the conductive features by an interconnection system.

23. The apparatus of claim 22, in which the interconnection system comprises a conductive adhesive.

24. The apparatus of claim 1, in which each conductive feature includes a first conductive structure oriented in parallel to a surface of the second substrate and a second
20 conductive structure oriented perpendicular to a surface of the second substrate.

25. The apparatus of claim 24, in which the assembly includes an encapsulant layer between the second substrate and the first substrate, and in which the second conductive structures are formed through a thickness of the encapsulant layer.

26. The apparatus of claim 25, in which the second conductive structures protrude beyond a bottom surface of the encapsulant layer.

27. The apparatus of claim 24, in which the first conductive structures are formed of a different material than the second conductive structures.

5 28. The apparatus of claim 27, in which the first conductive structures comprise a redistribution structure.

29. The apparatus of claim 1, in which one or more of the conductive features of the second substrate each comprises a contact pad connected to a corresponding conductive line.

10 30. The apparatus of claim 29, in which the contact pads are positioned around the edges of the electronic component.

31. The apparatus of claim 29, in which the contact pads are arranged in an array.

32. The apparatus of claim 29, in which the contact pads are positioned on one side of the electronic component.

15 33. The apparatus of claim 29, in which one or more of the contact pads is each connected to a corresponding electrode, and in which one or more of the electrodes is each electrically connected to a corresponding one of the electrical connection features of the first substrate.

34. The apparatus of claim 33, in which the electrodes comprise one or more of solder
20 balls, pillars, studs, bumps, pads, and conductive particles.

35. The apparatus of claim 33, in which the electronic component has a thickness no greater than the combination of a thickness of the electrodes and a thickness of the electrical connection features of the first substrate.

36. The apparatus of claim 1, comprising an underfill material disposed between the first substrate and the second substrate.

37. The apparatus of claim 36, in which the underfill material comprises a non-conductive polymer.

5 38. The apparatus of claim 1, in which the electronic component is encapsulated in an encapsulant.

39. The apparatus of claim 38, in which at least a portion of the conductive features is encapsulated in the encapsulant.

40. The apparatus of claim 1, in which the separation between the first substrate and the
10 second substrate is 200 μm or less.

41. The apparatus of claim 40, in which the separation between the first substrate and the second substrate is 100 μm or less.

42. The apparatus of claim 41, in which the separation between the first substrate and the second substrate is 50 μm or less.

15 43. The apparatus of claim 1, in which the first substrate is 100 μm or less from a surface of the electronic component facing the first substrate.

44. The apparatus of claim 43, in which the first substrate is 50 μm or less from the surface of the electronic component facing the first substrate.

45. The apparatus of claim 44, in which the first substrate is 25 μm or less from the
20 surface of the electronic component facing the first substrate.

46. The apparatus of claim 45, in which the first substrate is 10 μm or less from the surface of the electronic component facing the first substrate.

47. The apparatus of claim 46, in which the first substrate is in physical contact with the surface of the electronic component facing the first substrate.

48. The apparatus of claim 1, in which the first substrate comprises a flexible substrate.

49. The apparatus of claim 48, in which the first substrate comprises a printed flexible
5 circuit board.

50. The apparatus of claim 48, in which the second substrate comprises a material that is flexible.

51. The apparatus of claim 50, in which the second substrate is stretchable.

52. The apparatus of claim 51, in which the one or more conductive features comprise
10 meandering conductive features.

53. The apparatus of claim 50, in which the second substrate comprises an elastomeric material.

54. The apparatus of claim 48, in which the electronic component comprises a material that is flexible.

15 55. The apparatus of claim 48, in which the electronic component has a thickness of less than about 50 μm.

56. The apparatus of claim 48, in which the electrical connection features of the first substrate include printed conductors.

57. The apparatus of claim 48, comprising an adhesive disposed between the flexible
20 substrate and the assembly.

58. The apparatus of claim 57, in which the adhesive comprises a conductive adhesive.

59. The apparatus of claim 57, in which the adhesive forms a seal around the electronic component.

60. The apparatus of claim 57, in which the adhesive comprises an anisotropic conductive adhesive.

5 61. The apparatus of claim 60, in which the anisotropic conductive adhesive provides an electrical connection between the conductive features formed on the second substrate and the corresponding electrical connection features of the first substrate.

62. The apparatus of claim 1, in which the assembly includes second conductive features formed through a thickness of the second substrate, each second conductive
10 feature electrically connected to one of the conductive features.

63. The apparatus of claim 62, comprising a second electronic component electrically connected to one or more of the second conductive features, the assembly arranged such that the second substrate is disposed between the electronic component and the second electronic component.

15 64. The apparatus of claim 62, comprising a second assembly disposed on the second substrate, the second assembly comprising:

a third substrate;

third conductive features in contact with the third substrate, one or more of which are electrically connected to corresponding second conductive features of
20 the second substrate; and

a second electronic component between the third substrate and the second substrate and electrically connected to one or more of the third conductive features.

65. The apparatus of claim 1, comprising a third substrate disposed on the assembly
25 such that the assembly is between the first substrate and the third substrate, the third substrate comprising one or more second electrical connection features electrically connected to one or more of the electrical connection features of the first substrate.

66. The apparatus of claim 65, comprising an adhesive layer between the first substrate and the third substrate, wherein the assembly is at least partially encapsulated in the adhesive layer.

67. The apparatus of claim 65, comprising a second electronic component disposed on the third substrate and electrically connected to one or more of the second electrical connection features.

68. The apparatus of claim 65, in which the second electrical connection features are formed through a thickness of the third substrate and in which one or more of the electrical connection features of the first substrate are formed through a thickness of the first substrate.

69. The apparatus of claim 68, in which a first surface of the first substrate faces the third substrate, and comprising a second electronic component disposed on a second surface of the first substrate, the second electronic component electrically connected to one or more of the second electrical connection features.

70. An assembly comprising:

an electronic component having a first surface at which a pattern of electrical connection features are exposed,

a substrate having a substrate surface at which a pattern of electrical connection features are exposed, and

an interposer comprising conductors that connect at least some of the electrical connection features of the electronic component with at least some of the electrical connection features of the substrate, with the electronic component in a space between the interposer and the substrate and the first surface of the electronic component not facing the substrate surface,

in which a second surface of the electronic component is 100 μm or less from the surface of the substrate.

71. The assembly of claim 70, in which the electronic component comprises an integrated circuit.

72. The assembly of claim 70, in which the conductors are exposed on a surface of the interposer, and in which the surface of the interposer faces the substrate surface.

73. The assembly of claim 70, in which the conductors are electrically connected with the electrical connection features of the electronic component through an interconnection
5 system.

74. The assembly of claim 73, in which each conductor comprises a first conductive feature in physical and electrical contact with the interconnection system and a second conductive feature connecting the first conductive feature to an electrical connection feature of the substrate.

10 75. The assembly of claim 70, in which one or more of the conductors of the interposer is each connected to a corresponding electrode that electrically connects the conductor to a corresponding electrical connection feature of the substrate.

76. The assembly of claim 75, in which the electrodes comprise one or more of solder balls, pillars, studs, bumps, pads, and conductive particles.

15 77. The assembly of claim 75, in which the electronic component has a thickness that is no greater than the combination of a thickness of the electrodes and a thickness of the electrical connection features of the substrate.

78. The assembly of claim 70, in which the substrate comprises a material that is flexible.

20 79. The assembly of claim 78, in which the substrate comprises an elastomeric material.

80. The assembly of claim 70, in which the substrate is stretchable.

81. The assembly of claim 80, in which the conductors of the interposer comprise meandering conductors.

82. The assembly of claim 70, in which the second surface of the electronic component is 50 μm or less from the surface of the substrate.

83. The assembly of claim 82, in which the second surface of the electronic component is 25 μm or less from the surface of the substrate.

5 84. The assembly of claim 83, in which the second surface of the electronic component is 10 μm or less from the surface of the substrate.

85. The assembly of claim 84, in which the second surface of the electronic component is in physical contact with the surface of the substrate.

86. The assembly of claim 70, in which a separation between the substrate and the
10 interposer is 500 μm or less.

87. The assembly of claim 86, in which the separation between the substrate and the interposer is 200 μm or less.

88. The assembly of claim 87, in which the separation between the substrate and the interposer is 100 μm or less.

15 89. The assembly of claim 88, in which the separation between the substrate and the interposer is 50 μm or less.

90. A method comprising:

electrically connecting an electronic component to one or more conductive features formed on a second substrate;

20 disposing the second substrate on a surface of a first substrate, including positioning the electronic component between the first substrate and the second substrate, in which a separation between the second substrate and the surface of the first substrate is 500 μm or less; and

electrically connecting one or more of the conductive features of the second substrate each to a corresponding electrical connection feature of the first substrate.

91. The method of claim 90, in which electrically connecting the electronic component
5 comprises electrically connecting one or more bond pads of the electronic component each to a corresponding one of the conductive features.

92. The method of claim 91, in which positioning the electronic component between the first substrate and the second substrate comprises positioning the electronic component such that a surface including the bond pads faces away from the second substrate.

10 93. The method of claim 90, in which electrically connecting the one or more conductive features each to a corresponding electrical connection feature comprises applying a stimulus to an adhesive disposed between the first substrate and the second substrate.

94. The method of claim 93, in which applying the stimulus comprises applying heat.

95. The method of claim 93, in which applying the stimulus comprises applying light.

15 96. The method of claim 93, in which the adhesive comprises a conductive adhesive.

97. The method of claim 90, comprising bonding the first substrate to the second substrate.

98. The method of claim 97, comprising curing an adhesive disposed between the first substrate and the second substrate.

20 99. The method of claim 90, in which the first substrate comprises a printed circuit board.

100. The method of claim 90, in which the first substrate comprises a printed flexible circuit board.

101. The method of claim 90, in which the second substrate comprises an interposer.

102. The assembly of claim 90, in which the electronic component has a thickness that is
5 no greater than the combination of a thickness of the electrodes and a thickness of the electrical contacts of the first substrate.

103. A method comprising:

disposing one or more electronic components on a first surface of an interposer substrate, in which one or more sets of conductive features are formed on
10 the first surface of the interposer substrate and extend away from the interposer substrate, in which each conductive feature extends to a height of 500 µm or less from the first surface of the interposer substrate, and in which the height of the conductive features is greater than or equal to a height of the electronic components;

15 electrically connecting each electronic component to a corresponding set of conductive features; and

separating the interposer substrate into multiple packages, each package including a portion of the interposer substrate, one or more of the electronic components, and the corresponding set of conductive features.

20 104. The method of claim 103, in which each conductive feature extends to a height of 200 µm or less from the first surface of the interposer substrate.

105. The method of claim 104, in which each conductive feature extends to a height of 100 µm or less from the first surface of the interposer substrate.

106. The method of claim 105, in which each conductive feature extends to a height of
25 50 µm or less from the first surface of the interposer substrate.

107. The method of claim 103, in which the conductive features are not formed through a thickness of the interposer substrate.

108. The method of claim 103, in which separating the interposer substrate into multiple packages comprises dicing the interposer substrate.

5 109. The method of claim 103, comprising attaching the interposer substrate to a support substrate.

110. The method of claim 109, in which dicing the interposer substrate into multiple packages comprises dicing the support substrate such that each package includes a portion of the support substrate.

10 111. The method of claim 109, comprising attaching the interposer substrate to the support substrate with a temporary bonding material.

112. The method of claim 103, comprising connecting one of the packages to a device substrate such that at least one of the electronic components of the package is disposed between the interposer substrate and the device substrate.

15 113. The method of claim 112, in which connecting the package to the device substrate comprises electrically connecting the conductive features of the package to respective electrical connection features of the device substrate.

114. The method of claim 112, in which connecting the package to the device substrate comprises orienting the package such that the electronic component is between the
20 interposer substrate and the device substrate.

115. The method of claim 103, comprising forming molded layer on the surface of the interposer substrate, the molded layer comprising an encapsulant at least partially covering the electronic components and sets of conductive features.

116. The method of claim 115, comprising thinning the molded layer to expose ends of the conductive features.

117. The method of claim 103, in which the electronic components comprise ultra-thin electronic components.

5 118. A method comprising:

forming one or more interconnection structures on an interposer substrate, including connecting a first end of each of one or more interconnection structures to corresponding conductive features on a surface of an interposer substrate,

10 in which an electronic component disposed on the surface of the interposer substrate is electrically connected to one or more of the conductive features, and

in which a second surface of the electronic component and a second end of each of the interconnection structures are less than 500 μm from
15 the surface of the interposer substrate;

disposing the interposer substrate on a device substrate, including positioning the electronic component between the interposer substrate and the device substrate; and

electrically connecting the second end of each of one or more of the
20 interconnection structures to a corresponding electrical connection feature of the device substrate.

119. An apparatus comprising:

a substrate;

conductive features formed on a surface of the substrate, each conductive feature
25 having a first end and a second end on the first side of the substrate, in which at least a portion each conductive feature extends away from the substrate, in which each conductive feature extends to a height of 500 μm or less from the surface of the substrate;

an electronic component disposed on the surface of the substrate, one or more connection elements on a first surface of the electronic component each electrically connected to the first end of a corresponding one of the conductive features, in which a second surface of the electronic component is 500 μm or less from the surface of the substrate, and in which the height of the conductive features is greater than or equal to the separation between the second surface of the electronic component and the surface of the substrate; and

a second end of one or more of the conductive features arranged to each be in electrical contact with a corresponding electrical contact of a circuit board.

120. The method of claim 119, in which the second surface of the electronic component is 200 μm or less from the surface of the substrate.

121. The method of claim 120, in which the second surface of the electronic component is 100 μm or less from the surface of the substrate.

122. The method of claim 121, in which the second surface of the electronic component is 50 μm or less from the surface of the substrate.

123. The method of claim 119, in which a separation between the surface of the substrate and the circuit board is 500 μm or less.

124. The method of claim 123, in which the separation between the surface of the substrate and the circuit board is 200 μm or less.

125. The method of claim 124, in which the separation between the surface of the substrate and the circuit board is 100 μm or less.

126. The method of claim 125, in which the separation between the surface of the substrate and the circuit board is 50 μm or less.

127. The method of claim 119, in which the second surface of the electronic component is 100 μm or less from the circuit board.

128. The method of claim 127, in which the second surface of the electronic component is 50 μm or less from the circuit board.

5 129. The method of claim 128, in which the second surface of the electronic component is 25 μm or less from the circuit board.

130. The method of claim 129, in which the second surface of the electronic component is 10 μm or less from the circuit board.

131. The method of claim 130, in which the second surface of the electronic
10 component is in physical contact with the circuit board.

132. The apparatus of claim 119, in which the conductive features are not formed through a thickness of the substrate.

133. The apparatus of claim 119, comprising multiple electronic components disposed on the surface of the first side of the substrate.

15 134. The apparatus of claim 119, which the first ends of the conductive features are electrically connected to the corresponding connection elements of the electronic component through an interconnection system.

135. The apparatus of claim 119, in which when the conductive features are in electrical contact with the electrical contacts of the circuit board, the circuit board and the
20 electronic component are both disposed on a same side of the substrate.

136. The apparatus of claim 119, in which the second end of one or more of the conductive features is each in physical contact with a corresponding electrode disposed on the surface of the substrate.

137. The apparatus of claim 136, in which the electrodes comprise one or more of solder balls, pillars, studs, bumps, pads, and conductive particles.

138. The apparatus of claim 119, in which the second end of each conductive feature comprises a contact pad formed on the surface of the substrate.

5 139. The apparatus of claim 119, in which the second ends of one or more of the conductive features are arranged in an array.

140. The apparatus of claim 119, in which the second ends of one or more of the conductive features are positioned around the edges of the electronic component.

141. The apparatus of claim 119, in which a pitch of the connection elements of the
10 electronic component is different than a pitch of the electrical contacts of the circuit board.

142. The apparatus of claim 119, comprising a support substrate attached to the substrate such that the substrate is disposed between the electronic component and the support substrate.

15 143. The apparatus of claim 142, in which the support substrate is releasably attached to the substrate.

144. The apparatus of claim 143, in which the support substrate is attached to the substrate with a temporary bonding material.

145. The apparatus of claim 144, in which the temporary bonding material has an
20 adhesion that changes responsive to application of a stimulus.

146. The apparatus of claim 119, in which the substrate comprises a material that is flexible.

147. The apparatus of claim 146, in which the substrate is stretchable.

148. The apparatus of claim 119, in which the electronic component comprises a material that is flexible.

149. The apparatus of claim 119, comprising an adhesive disposed on the surface of
5 the substrate.

150. An assembly comprising:

an interposer substrate, multiple sets of conductive features being formed on a surface of the interposer substrate, in which at least a portion of each conductive feature extends away from the interposer substrate, and in
10 which each conductive feature extends to a height of 500 μm or less from the surface of the interposer substrate; and

multiple electronic components disposed on the surface of the interposer substrate, each electronic component corresponding to one of the multiple sets of conductive features formed on the surface of the interposer
15 substrate, in which, for each electronic component, one or more connection elements on a first surface of the electronic component are each electrically connected to an end of a corresponding one of the conductive features of the corresponding set, in which a second surface of the electronic component is 500 μm or less from the surface of the
20 interposer substrate, and in which the height of the conductive features is greater than or equal to the separation between the second surface of the electronic component and the surface of the interposer substrate.

151. The assembly of claim 150, comprising a support substrate, wherein the interposer substrate is disposed between the support substrate and the multiple electronic
25 components.

152. An apparatus comprising:

a first substrate including one or more electrical connection features; and

an assembly including:

a second substrate;

conductive features formed on the second substrate, one or more of which are electrically connected to corresponding electrical connection features of the first substrate; and

5 an electronic component positioned at a surface of the second substrate and electrically connected to one or more of the conductive features,

the surface of the second substrate facing the first substrate, in which a separation between the surface of the second substrate and the first substrate is 500

10 µm or less.

153. An apparatus comprising:

a first substrate, a first electrical connection feature formed on a surface of the first substrate; and

a molded layer comprising an electronic component and a conductive element

15 encapsulated within a molding material, a second electrical connection feature formed on a surface of the electronic component, the second electrical connection feature of the electronic component being electrically connected to the first electrical connection feature of the first substrate through the conductive element;

20 the surface of the electronic component facing away from the surface of the first substrate.

154. The apparatus of claim 153, comprising a second substrate attached to the molded layer such that the molded layer is positioned between the first substrate and the second substrate.

25 155. The apparatus of claim 154, in which at least a portion of the conductive element is in physical contact with the surface of the second substrate.

156. The apparatus of claim 155, in which the conductive element comprises a first conductive feature and a second conductive feature, the first conductive feature formed along a surface of the second substrate, and the second conductive feature formed through a thickness of the molded layer.

5 157. The apparatus of claim 154, in which the second substrate is releasably attached to the molded layer.

158. The apparatus of claim 157, in which the second substrate is attached to the molded layer with a temporary bonding material.

159. The apparatus of claim 158, in which the temporary bonding material has an
10 adhesion that changes responsive to application of a stimulus.

160. The apparatus of claim 157, in which the second substrate is removable from the molded layer by one or more of wet etching, dry etching, and mechanical removal.

161. The apparatus of claim 154, comprising a third substrate attached to the second substrate such that the molded layer and second substrate are positioned between the first
15 substrate and the third substrate.

162. The apparatus of claim 161, in which the third substrate is releasably attached to the second substrate.

163. The apparatus of claim 162, in which the third substrate is attached to the second substrate with a temporary bonding material.

20 164. The apparatus of claim 155, comprising a second conductive element formed through a thickness of the second substrate and electrically connected to the portion of the conductive element.

165. The apparatus of claim 164, comprising a second electronic component electrically connected to the second conductive element, in which the second substrate is disposed between the molded layer and the second electronic component.

166. The apparatus of claim 164, comprising a second molded layer disposed such that 5 the molded layer is between the second molded layer and the first substrate,

the second molded layer comprising a second electronic component and a third conductive element encapsulated within a molding material, a third electrical connection feature of the second electronic component formed on a surface of the second electronic component, the third electronic 10 feature of the electronic component being electrically connected to the second conductive element of the second substrate through the third conductive element.

167. The apparatus of claim 166, in which the surface of the second electronic component faces away from the first molded layer.

15 168. The apparatus of claim 153, comprising a second substrate disposed such that the molded layer is between the first substrate and the second substrate, the second substrate comprising one or more third electrical connection features electrically connected to one or more of the first electrical connection features of the first substrate.

169. The apparatus of claim 168, comprising a second electronic component disposed 20 on the second substrate and electrically connected to one or more of the third electrical connection features.

170. The apparatus of claim 168, in which the third electrical connection features are formed through a thickness of the second substrate and in which one or more of the first electrical connection features of the first substrate are formed through a thickness of the 25 first substrate.

171. The apparatus of claim 170, in which the surface of the first substrate faces the second substrate, and comprising a second electronic component disposed on a second surface of the first substrate, the second electronic component electrically connected to one or more of the third electrical connection features.

5 172. The apparatus of claim 153, in which the second electrical connection feature of the electronic component is connected to the conductive element through an interconnection system.

173. The apparatus of claim 153, in which the conductive element comprises a first conductive element and a second conductive element.

10 174. The apparatus of claim 173, in which the first conductive element is oriented parallel to the molded layer and the second conductive element is oriented perpendicular to the molded layer.

175. The apparatus of claim 173, in which a first end of the first conductive feature is in physical contact with an interconnection system that is in contact with the second
15 electrical connection feature of the electronic component, and a second end of the first conductive feature is in physical contact with a first end of the second conductive feature.

176. The apparatus of claim 175, in which a second end of the second conductive feature includes an interconnection structure.

177. The apparatus of claim 176, in which the interconnection structure comprises one
20 or more of solder cap, solder ball, pillar, stud, bump, pad, conductive particle.

178. The apparatus of claim 177, in which the interconnection structure comprises a conductive adhesive.

179. The apparatus of claim 176, in which the interconnection structure is in physical contact with the first electrical connection feature of the first substrate.

180. The apparatus of claim 276, in which the second end of the second conductive feature is flush with a bottom surface of the molded layer.

181. The apparatus of claim 173, in which the second conductive feature is formed through a thickness of the molded layer.

5 182. The apparatus of claim 173, in which the first conductive feature is exposed on a top surface of the molded layer, the top surface facing away from the first substrate.

183. The apparatus of claim 182, in which a top surface of the first conductive feature is coplanar with the top surface of the molded layer.

184. The apparatus of claim 182, comprising a second electronic component disposed
10 on the top surface of the molded layer, in which an electrical connection feature of the second electronic component is electrically connected to the exposed first conductive feature.

185. The apparatus of claim 153, in which the electronic component comprises an ultra-thin electronic component.

15 186. The apparatus of claim 153, comprising an underfill in a gap between the molded layer and the first substrate.

187. The apparatus of claim 153, comprising an assembly including a second electronic component, the assembly disposed on the molded layer such that the molded layer is positioned between the assembly and the first substrate.

20 188. The apparatus of claim 187, in which the molded layer comprises multiple conductive elements, and in which the second electronic component is electrically connected to the first substrate through a conductive element.

189. The apparatus of claim 153, in which the molded layer comprises multiple electronic components encapsulated within the molding material.

190. The apparatus of claim 189, in which the multiple electronic components are disposed between the conductive element and the first substrate.

191. An apparatus comprising:

a first substrate;

5 a molded layer disposed on the first substrate such that a first surface of the molded layer is in contact with the first substrate, the molded layer comprising:

an electronic component encapsulated within a molding material, the electronic component having electrical connection features, the

10 electronic connection features facing the first substrate; and

conductive elements, each conductive element electrically connected to a corresponding electrical connection feature of the electrical component;

in which first ends of the conductive elements are exposed at a second surface of

15 the molded layer and arranged in an arrangement corresponding to an arrangement of electrical contacts of a circuit board.

192. The apparatus of claim 191, in which the electronic component comprises an ultra-thin electronic component.

193. The apparatus of claim 191, comprising a second substrate attached to the first

20 substrate such that the first substrate is positioned between the molded layer and the second substrate.

194. The apparatus of claim 193, in which the second substrate is releasably attached to the first substrate.

195. The apparatus of claim 194, in which the second substrate is attached to the first

25 substrate with a temporary bonding material.

196. The apparatus of claim 191, in which the first substrate is releasably attached to the molded layer.

197. The apparatus of claim 196, in which the first substrate is removable from the molded layer by one or more of wet etching, dry etching, and mechanical removal.

5 198. The apparatus of claim 196, in which the first substrate is attached to the molded layer with a temporary bonding material

199. The apparatus of claim 191, comprising an interconnection structure in physical and electrical contact with each of the first ends of the conductive elements.

200. The apparatus of claim 199, in which the interconnection structure comprises one
10 or more of solder cap, solder ball, pillar, stud, bump, pad, and conductive particle.

201. The apparatus of claim 199, in which the interconnection structure comprises a conductive adhesive.

202. The apparatus of claim 191, in which second ends of the conductive elements are in physical and electrical contact with an anisotropic conductive adhesive that is in
15 electrical contact with the electrical connection features of the electronic component.

203. The apparatus of claim 191, in which each conductive element comprises a first portion formed on a surface of the first substrate and a second portion formed through a thickness of the molded layer.

204. The apparatus of claim 191, comprising an interconnection structure disposed at
20 the first end of each conductive element.

205. The apparatus of claim 191, comprising a second conductive element formed through a thickness of the first substrate and electrically connected to at least one of the conductive elements of the molded layer.

206. The apparatus of claim 205, comprising a second electronic component electrically connected to the second conductive element, in which the first substrate is disposed between the molded layer and the second electronic component.

207. An apparatus comprising:

5 a molded layer comprising:

an electronic component encapsulated within a molding material, the electronic component having electrical connection features, the electronic connection features facing a first surface of the molded layer; and

10 conductive elements, each conductive element electrically connected to a corresponding electrical connection feature of the electrical component;

in which first ends of the conductive elements are exposed at a second surface of the molded layer and arranged in an arrangement corresponding to an
15 arrangement of electrical contacts of a circuit board.

208. The apparatus of claim 207, in which a portion of each conductive element is exposed at the first surface of the molded layer.

209. The apparatus of claim 208, comprising a second electronic component disposed on the first surface of the molded layer.

20 210. The apparatus of claim 209, in which the second electronic component is electrically connected to one or more of the exposed portions of the conductive elements.

211. The apparatus of claim 209, in which the second electronic component comprises one or more of a passive component, a battery, and a sensor.

212. The apparatus of claim 209, comprising an interconnection structure in physical
25 and electrical contact with each of the first ends of the conductive elements.

213. The apparatus of claim 212, in which the interconnection structure comprises one or more of solder cap, solder ball, pillar, stud, bump, pad, and conductive particle.

214. The apparatus of claim 212, in which the interconnection structure comprises a conductive adhesive.

5 215. The apparatus of claim 209, in which second ends of the conductive elements are in physical and electrical contact with an anisotropic conductive adhesive that is in electrical contact with the electrical connection features of the electronic component.

216. The apparatus of claim 208, comprising a second molded layer disposed facing the first surface of the molded layer, the second molded layer comprising:

10 a second electronic component encapsulated within a molding material, the second electronic component having second electrical connection features, the second electrical connection features facing a first surface of the second molded layer; and

second conductive elements, a second end of each second conductive element 15 electrically connected to a corresponding second electrical connection feature of the electrical component,

in which first ends of the second conductive elements are exposed at a second surface of the second molded layer and arranged in an arrangement corresponding to an arrangement of the exposed portions of the conductive 20 elements.

217. An apparatus comprising:

a molded layer comprising:

multiple electronic components encapsulated within a molding material, each electronic component having electrical connection features 25 facing a first surface of the molded layer; and

multiple sets of conductive elements, each set corresponding to one of the electronic components, each conductive element of a set electrically connected to a corresponding electrical connection feature of the corresponding electronic component;

5 in which first ends of the conductive elements are exposed at a second surface of the molded layer.

218. The apparatus of claim 217, comprising a substrate, in which the molded layer is disposed on the substrate such that the first surface of the molded layer is in contact with the substrate.

10 219. The apparatus of claim 218, comprising a support substrate, in which the substrate is disposed on the support substrate such that the substrate is between the support substrate and the molded layer.

220. The apparatus of claim 217, comprising multiple interconnection structures, each interconnection structure in physical and electrical contact with the first ends of a
15 corresponding set of conductive elements.

221. The apparatus of claim 220, in which each interconnection structure comprises one or more of solder cap, solder ball, pillar, stud, bump, pad, conductive particle.

222. The apparatus of claim 217, comprising a second electronic component disposed on the first surface of the molded layer.

20 223. The apparatus of claim 222, in which the second electronic component is in electrical contact with at least one of the conductive elements of one of the sets of conductive elements.

224. The apparatus of claim 222, comprising multiple second electronic components disposed on the first surface of the molded layer, each second electronic component in
25 electrical contact with at least one of the conductive elements of a corresponding set of conductive elements.

225. The apparatus of claim 223, in which the second electronic component comprises one or more of a passive component, a battery, and a sensor.

226. A method comprising:

attaching an interposer substrate to a support substrate, in which multiple sets of conductive features are formed on a surface of the interposer substrate;

electrically connecting each of multiple electronic components to a corresponding set of conductive features;

forming a molded layer on the surface of the interposer substrate, the molded layer comprising an encapsulant covering the electronic components and sets of conductive features;

thinning the molded layer to expose ends of the conductive features, in which thinning the molded layer includes thinning the electronic components; and

separating the thinned molded layer into multiple packages, each package including at least one of the electronic components, and the corresponding set of conductive features.

227. The method of claim 226, in which thinning the electronic components comprises forming ultra-thin electronic components.

228. The method of claim 226, comprising forming an interconnection structure at the exposed end of each of one or more of the conductive features.

229. The method of claim 228, in which the interconnection structure comprises one or more of a solder cap, a solder ball, a pillar, a stud, a bump, a pad, and a conductive particle.

230. The method of claim 226, comprising attaching the interposer substrate to the support substrate with a temporary bonding material.

231. The method of claim 226, comprising connecting one of the packages to a device substrate.

232. The method of claim 231, in which connecting the package to the device substrate comprises electrically connecting the conductive features of the package to respective
5 electrical connection features of the device substrate.

233. The method of claim 232, comprising removing the support substrate from the interposer substrate of the connected package.

234. The method of claim 226, in which separating the thinned molded layer into multiple packages comprises dicing the interposer substrate and the support substrate
10 such that each package includes a portion of the interposer substrate and a portion of the support substrate.

235. The method of claim 234, comprising connecting one of the packages to a device substrate and removing the portion of the support substrate from the portion of the interposer substrate of the connected package.

15 236. The method of claim 235, in which connecting the package to the device substrate comprises orienting the package such that the electronic component is between the portion of the interposer substrate and the device substrate.

237. The method of claim 235, comprising assembling a second molded layer onto the portion of the interposer substrate, the second molded layer comprising a second
20 electronic component encapsulated within a molding material.

238. The method of claim 234, in which assembling the second molded layer comprises electrically connecting the second electronic component to a conductive feature formed through a thickness of the portion of the interposer substrate.

239. The method of claim 226, comprising removing the support substrate from the
25 interposer substrate after thinning the molded layer.

240. The method of claim 239, in which separating the thinned molded layer into multiple packages comprises dicing the interposer substrate such that each package includes a portion of the interposer substrate.

241. The method of claim 240, comprising connecting one of the packages to a device
5 substrate such that the electronic component is between the portion of the interposer substrate and the device substrate.

242. The method of claim 239, comprising assembling a second molded layer onto the portion of the interposer substrate, the second molded layer comprising a second electronic component encapsulated within a molding material.

10 243. The method of claim 242, in which assembling the second molded layer comprises electrically connecting the second electronic component to a conductive feature formed through a thickness of the interposer substrate.

244. The method of claim 226, comprising removing the support substrate from the interposer substrate after forming the molded layer.

15 245. The method of claim 244, comprising removing the interposer substrate from the molded layer.

246. The method of claim 245, comprising removing the interposer substrate by one or more of wet etching, dry etching, and mechanical removal.

247. The method of claim 245, comprising attaching the molded layer to a second
20 support substrate.

248. The method of claim 247, in which thinning the molded layer comprises thinning the molded layer attached to the second support substrate.

249. The method of claim 247, in which separating the thinned molded layer into multiple packages comprises dicing the second support substrate such that each package includes a portion of the second support substrate.

250. The method of claim 249, comprising connecting one of the packages to a device
5 substrate such that the electronic component is between the portion of the second support substrate and the device substrate.

251. The method of claim 250, comprising removing the portion of the second support substrate from the connected package.

252. The method of claim 251, in which when the portion of the second support
10 substrate is removed, one or more electrical connection features of the electronic component are exposed on a surface of the electronic component facing away from the device substrate.

253. The method of claim 252, comprising assembling one or more second electronic components onto a surface of the electronic component facing away from the device
15 substrate.

254. The method of claim 252, comprising assembling a second molded layer onto the molded layer, the second molded layer comprising a second electronic component encapsulated within a molding material.

255. The method of claim 254, in which assembling the second molded layer
20 comprises electrically connecting the second electronic component to one or more of the conductive features in the molded layer.

256. The method of claim 248, comprising removing the second support substrate from the thinned molded layer.

257. The method of claim 256, in which when second support substrate is removed, the ends of the conductive features are exposed on a first surface of the molded layer and one or more electrical connection features of the electronic component are exposed on a second surface of the molded layer.

5 258. The method of claim 257, comprising assembling one or more second electronic components onto the second surface of the molded layer.

259. The method of claim 258, comprising assembling a second molded layer onto the molded layer, the second molded layer comprising a second electronic component encapsulated within a molding material.

10 260. The method of claim 259, in which assembling the second molded layer comprises electrically connecting the second electronic component to one or more of the conductive features in the molded layer.

261. The method of claim 258, in which assembling the second electronic component comprises electrically connecting the second electronic component to at least one of the
15 electrical connection features exposed on the second surface of the molded layer.

262. The method of claim 257, comprising connecting one of the packages to a device substrate such that the first surface of the molded layer of the package faces the device substrate.

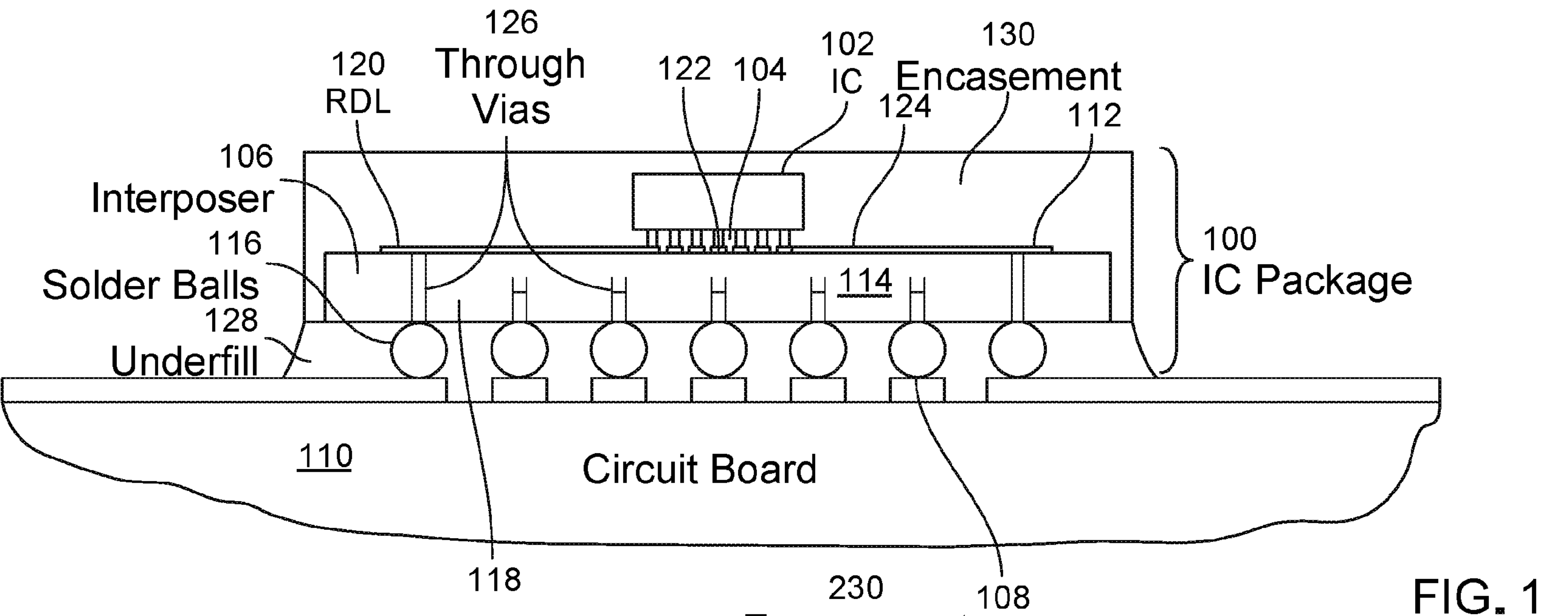


FIG. 1

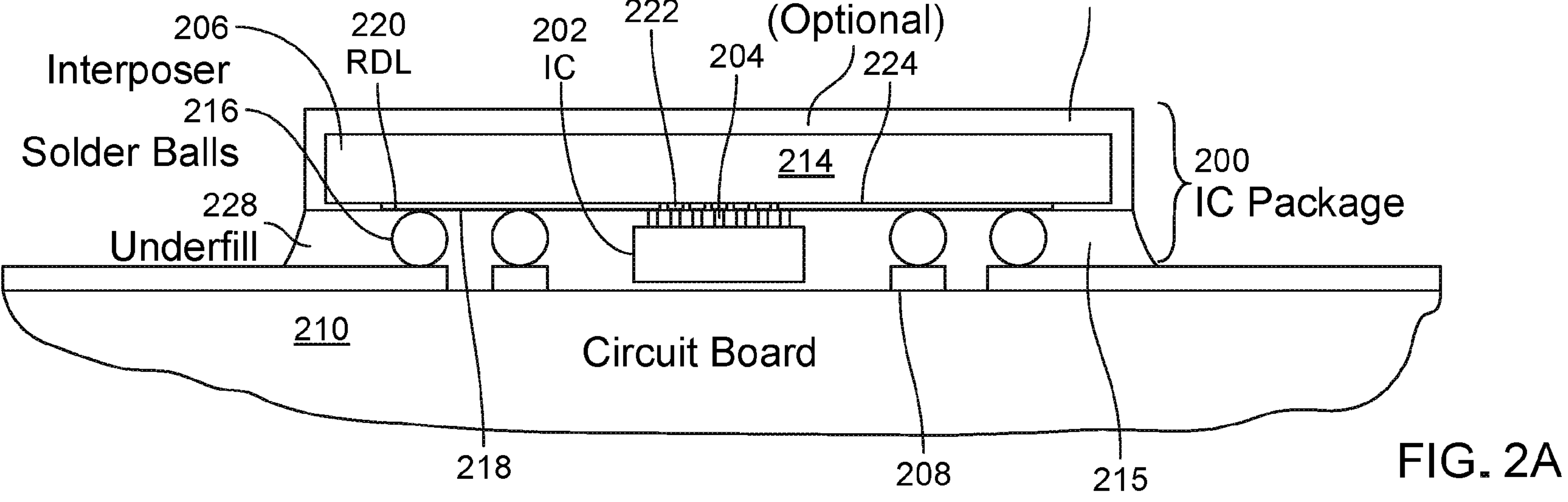


FIG. 2A

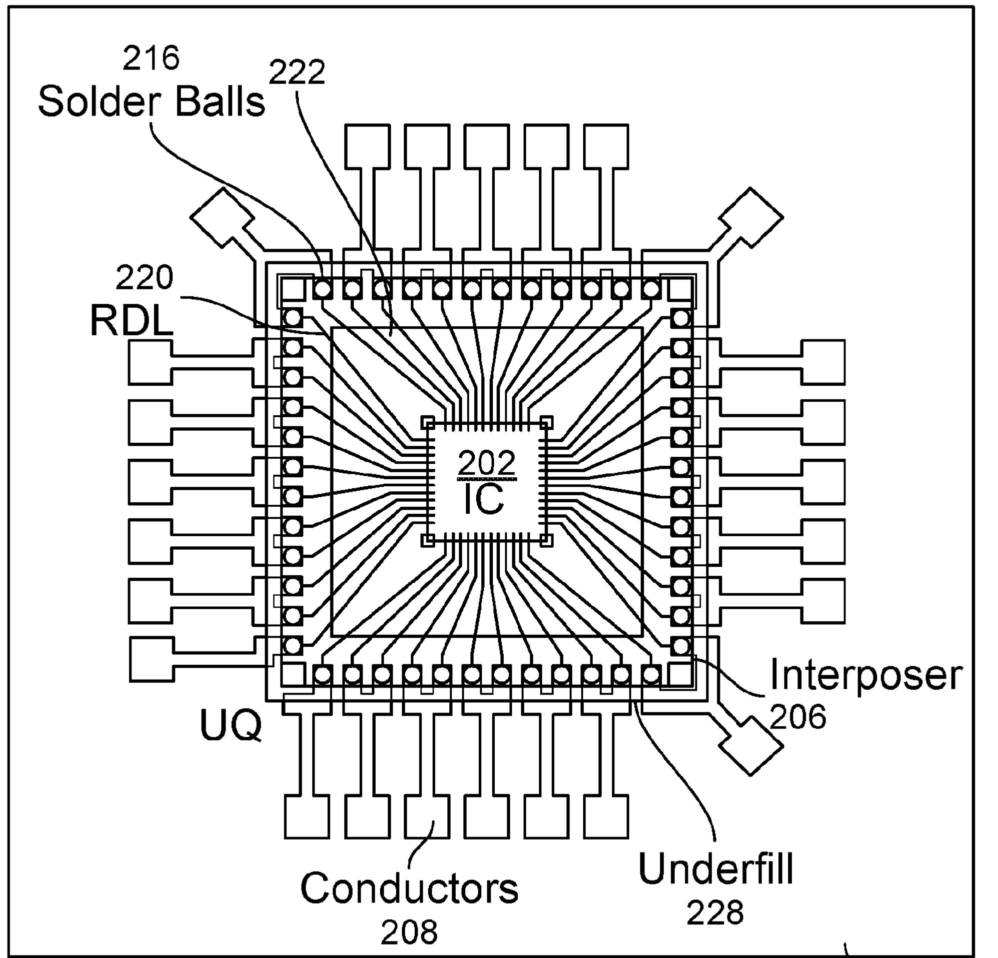


FIG. 2B

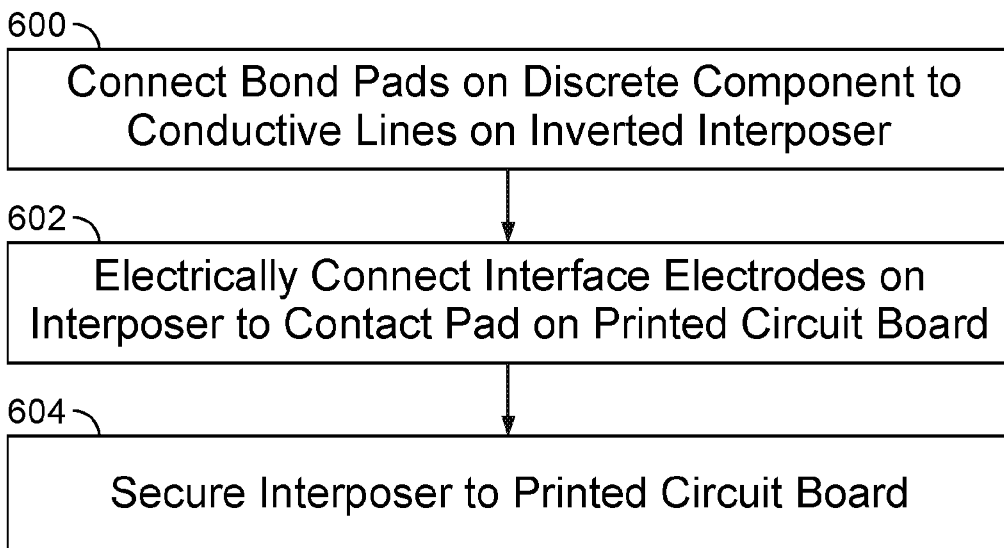


FIG. 3

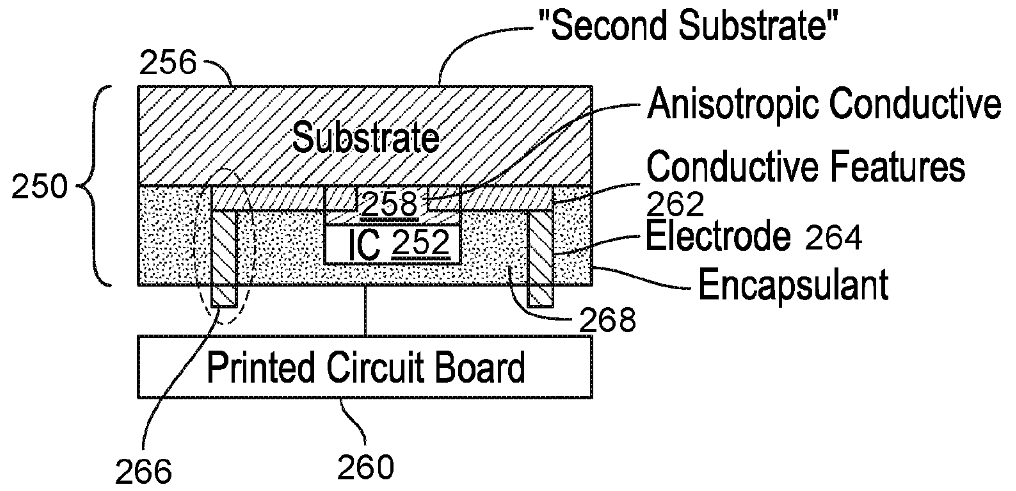


FIG. 4A

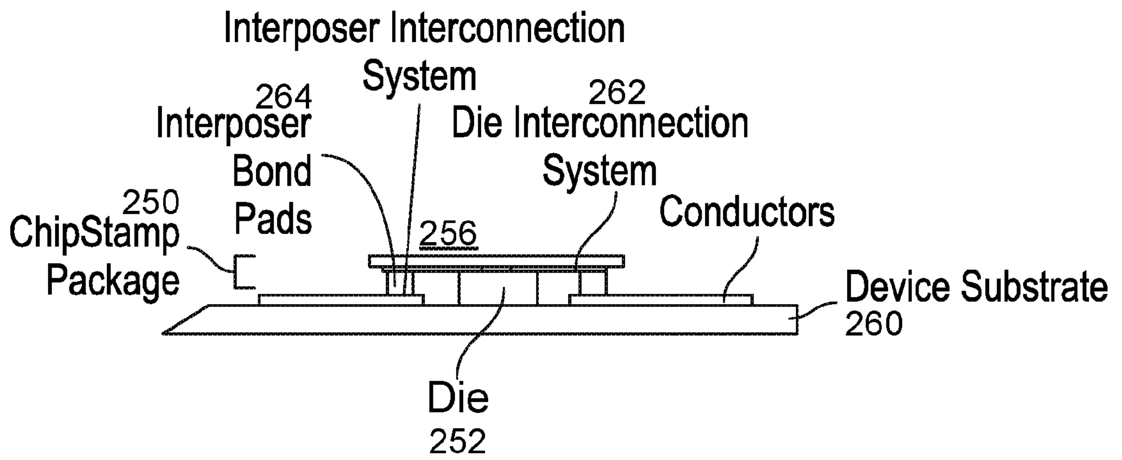


FIG. 4B

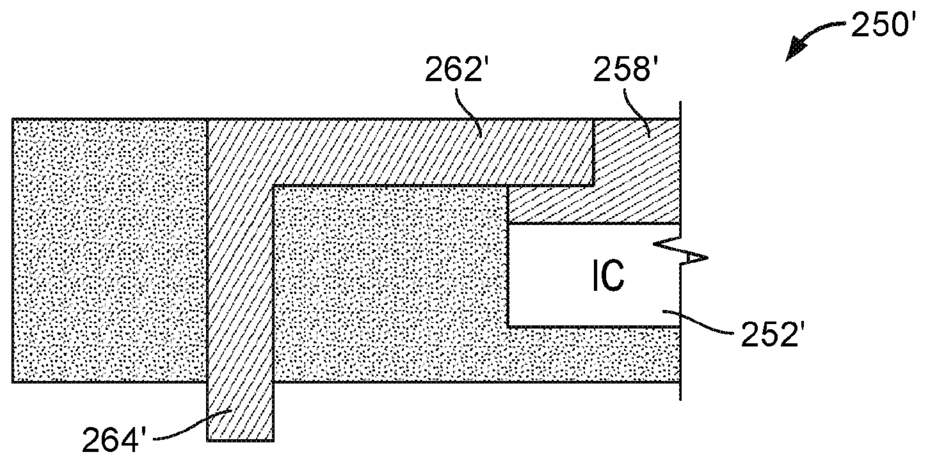


FIG. 4C

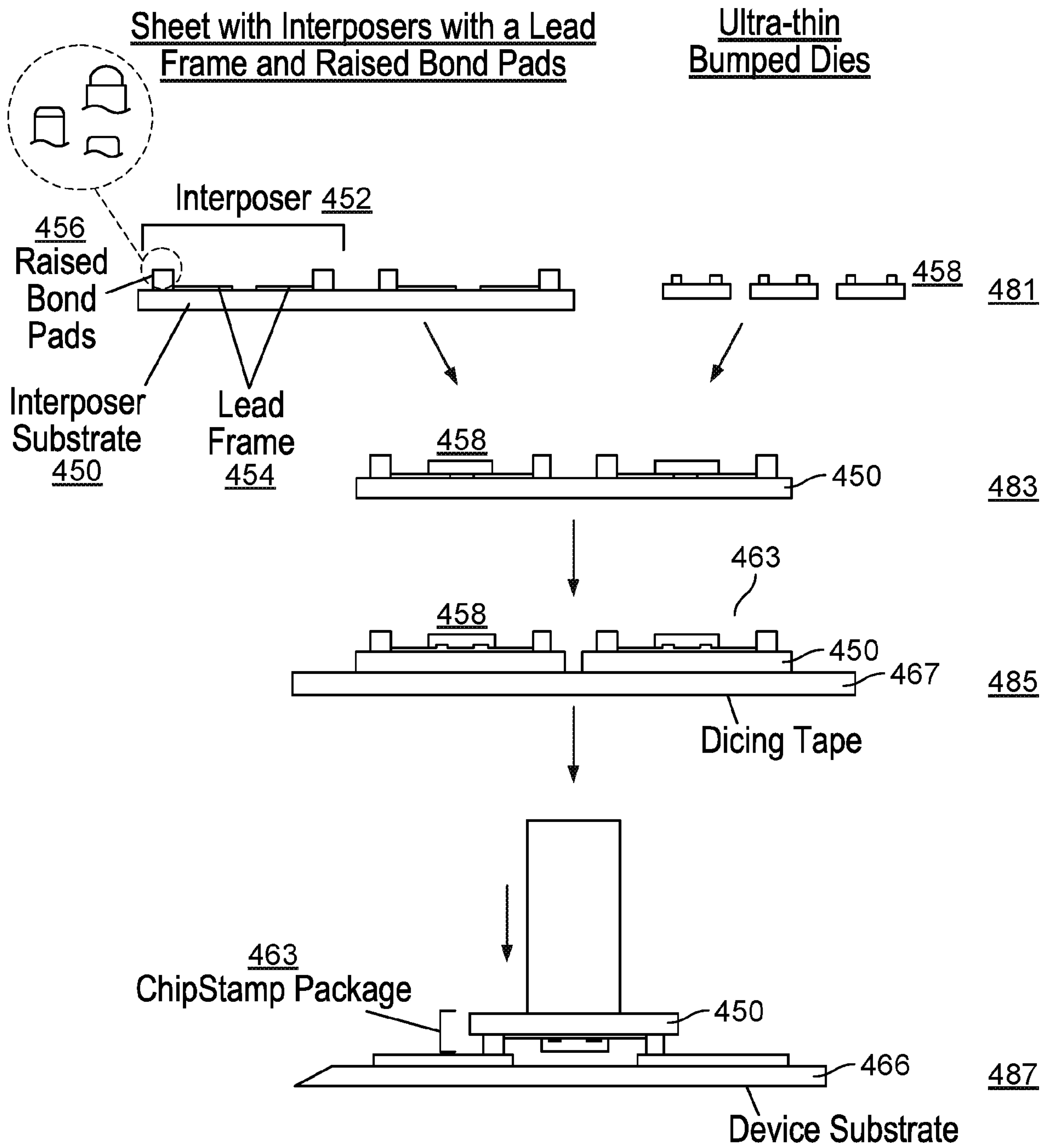


FIG. 5

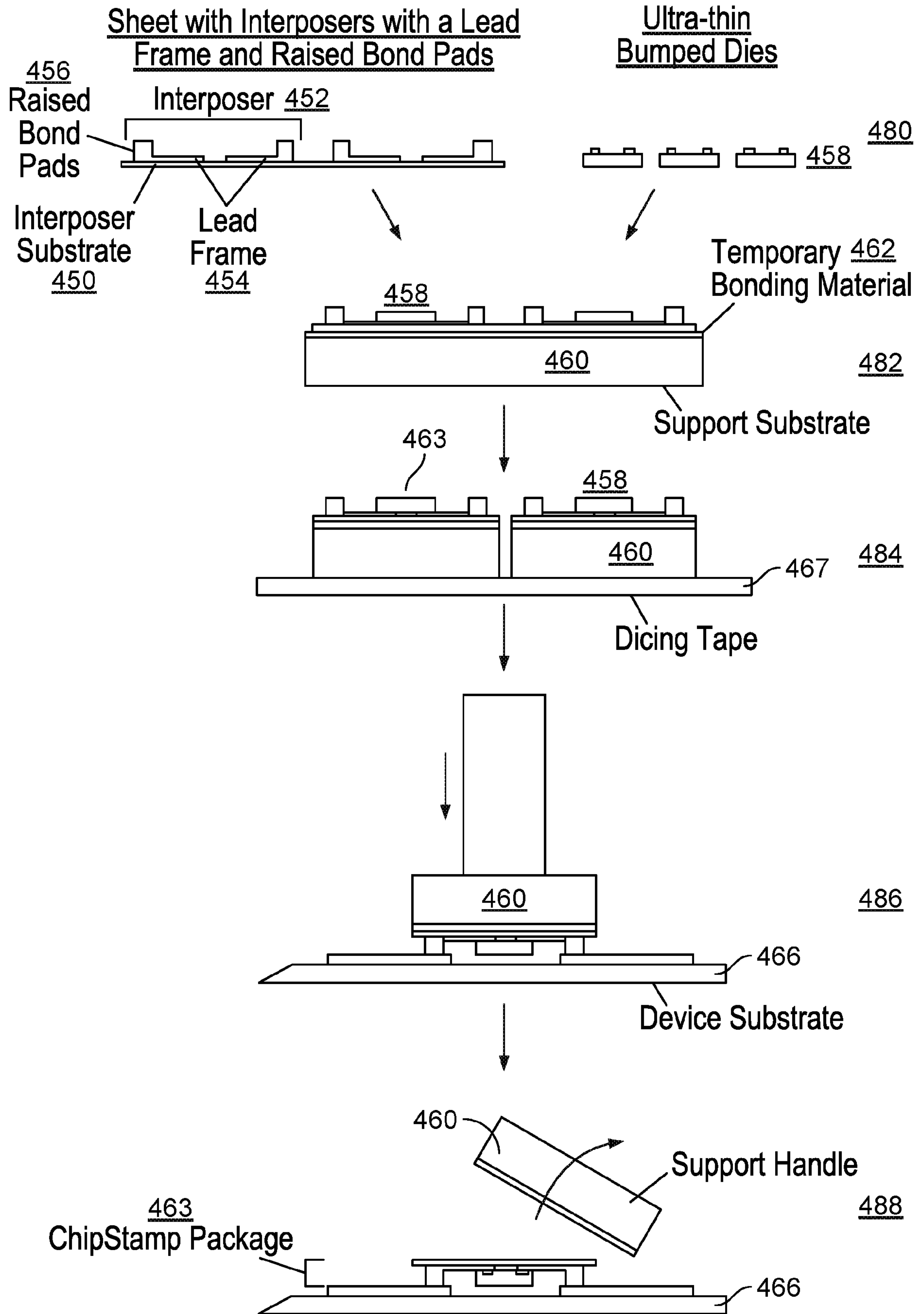


FIG. 6

6/20

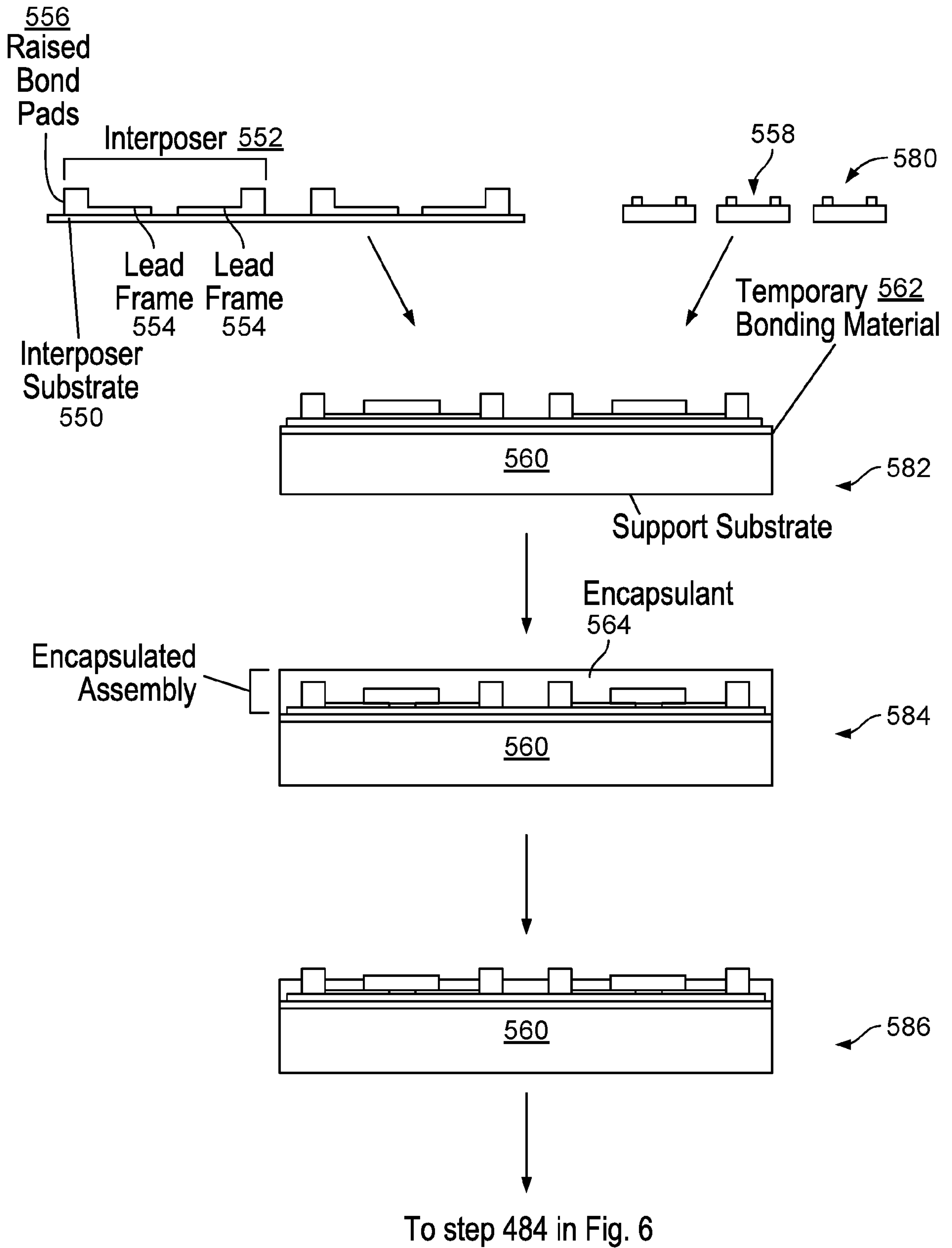


FIG. 7

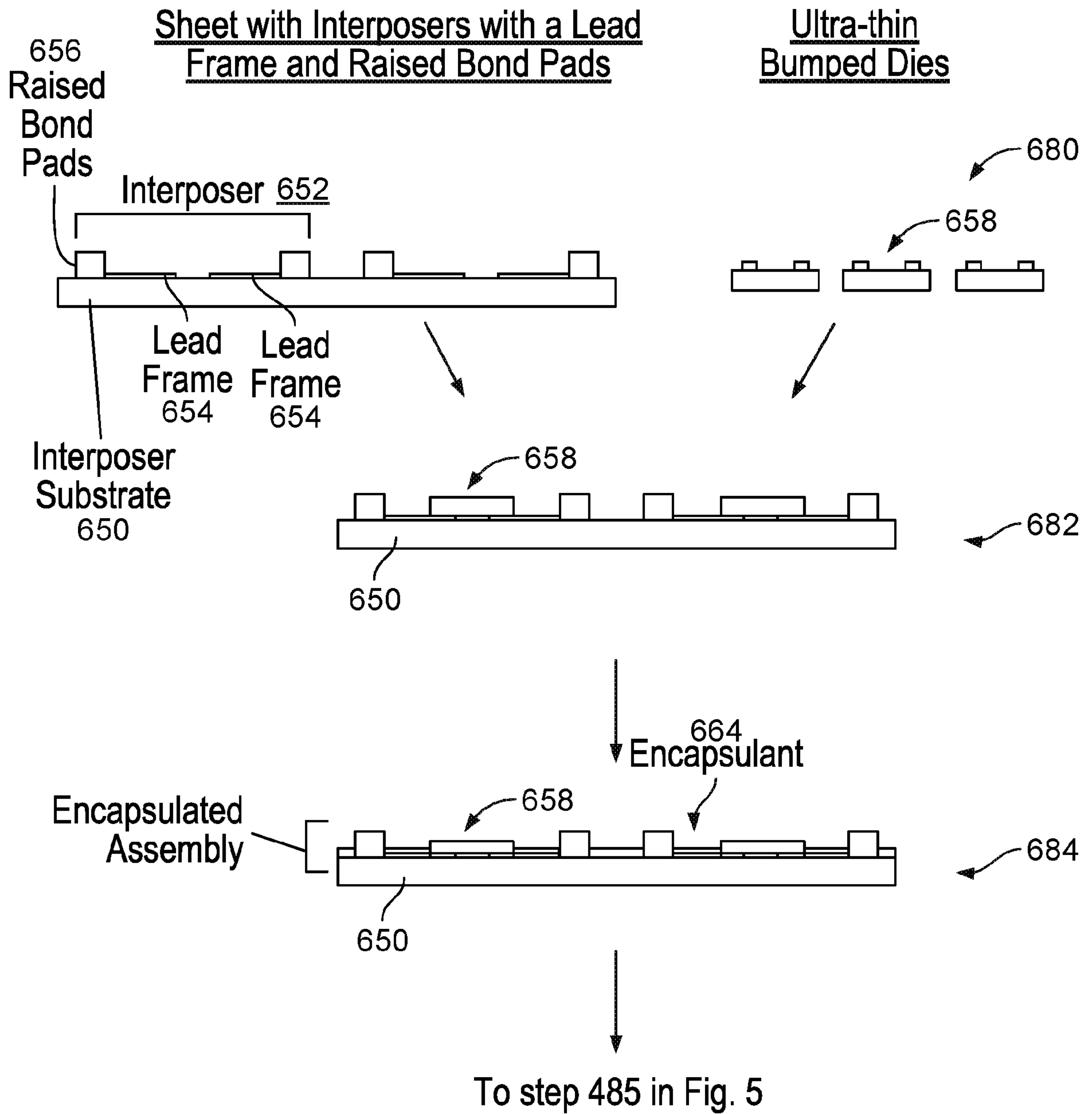


FIG. 8

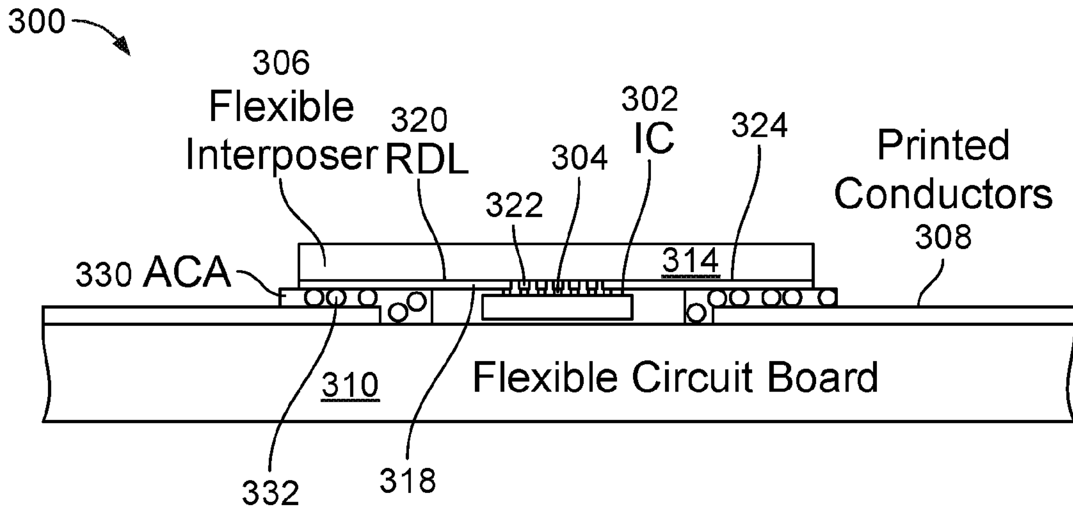


FIG. 9A

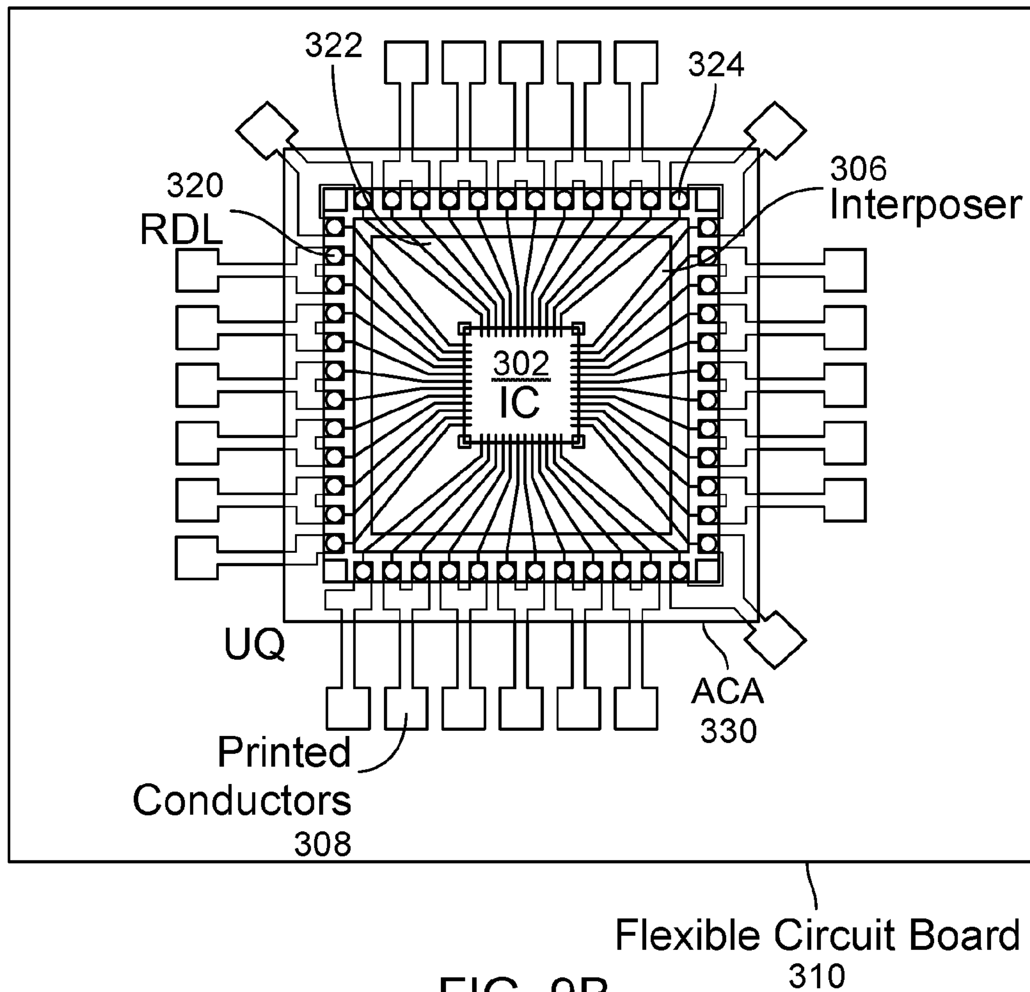


FIG. 9B

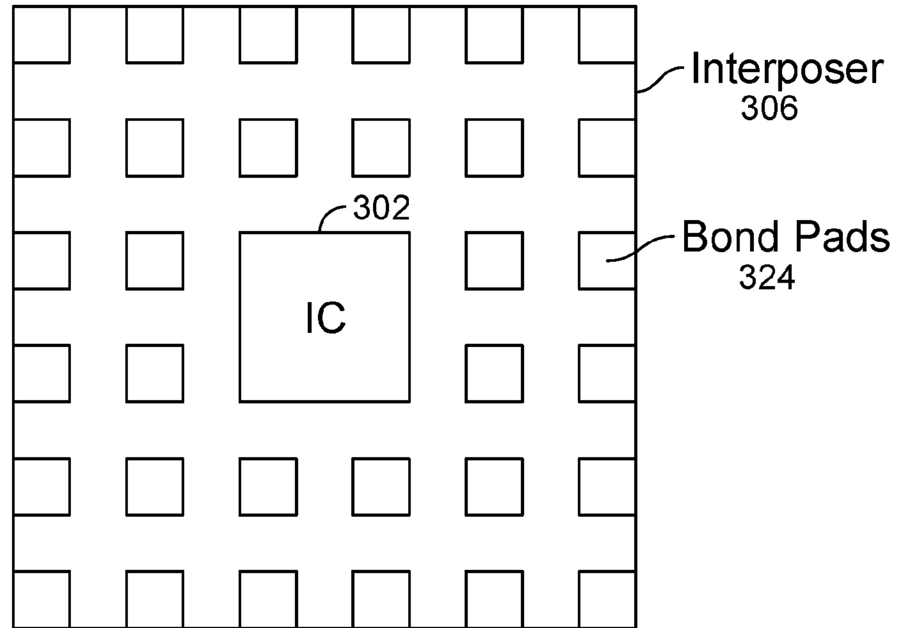


FIG. 10

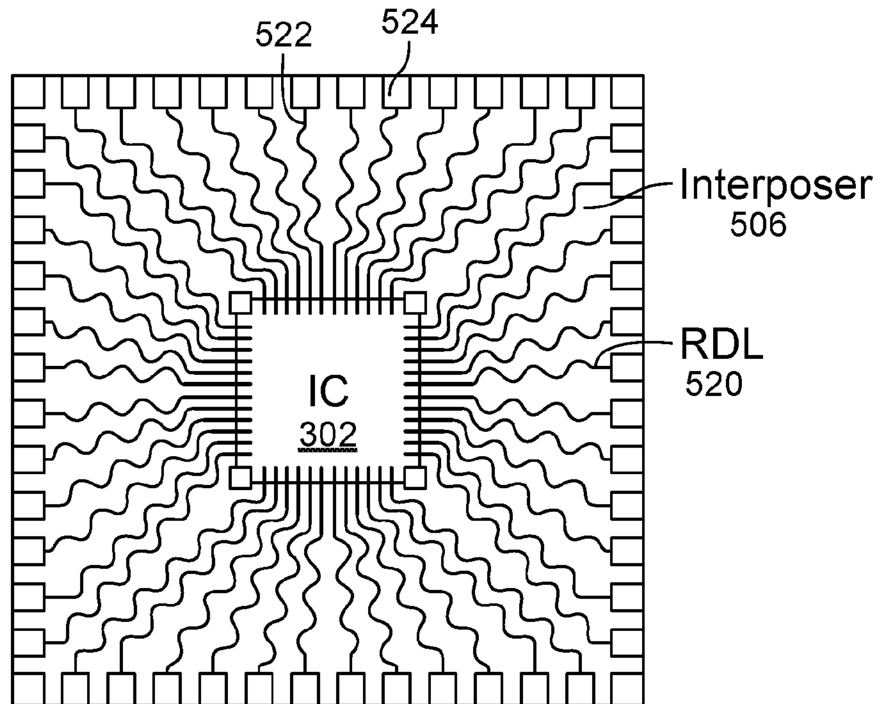


FIG. 11

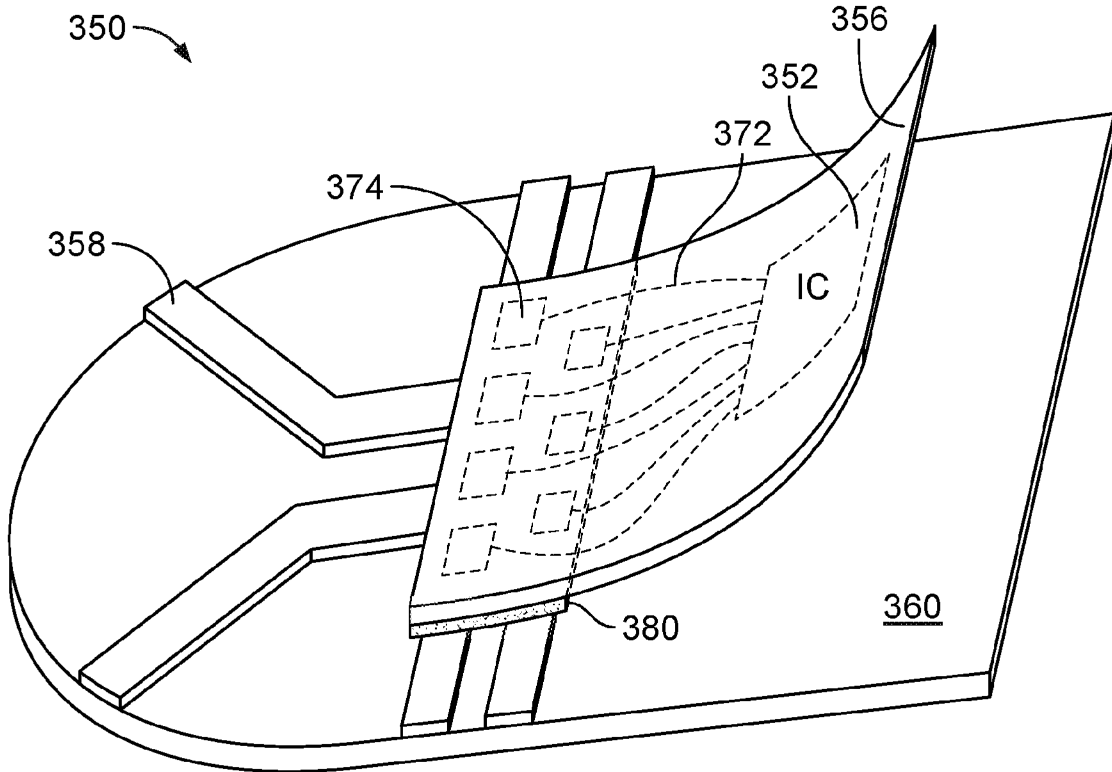


FIG. 12

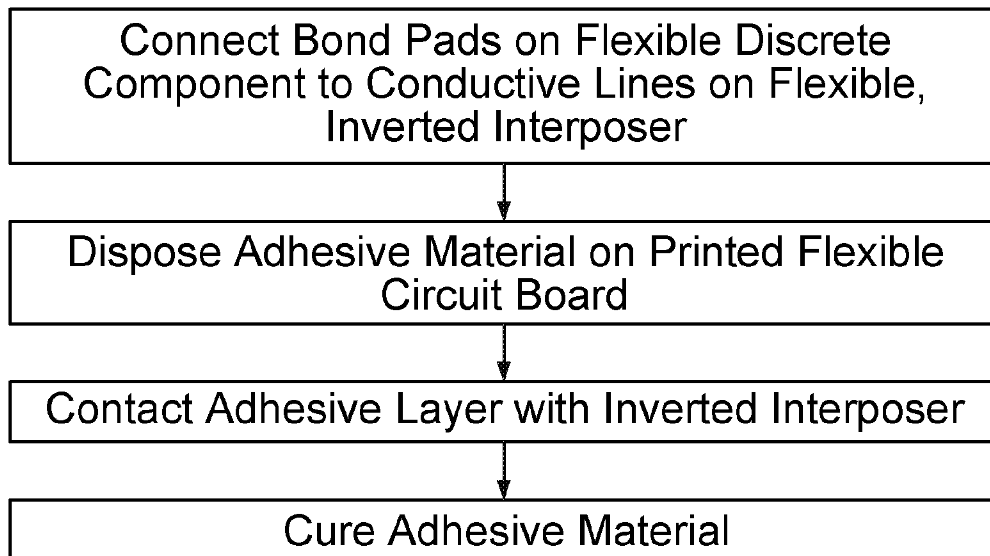


FIG. 13

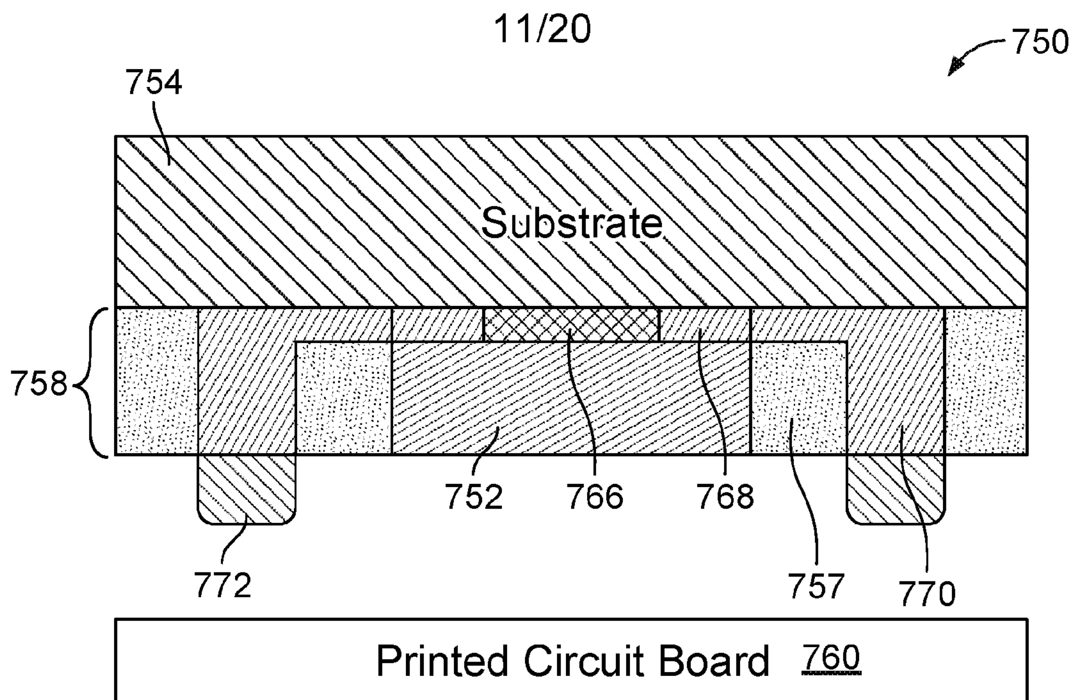


FIG. 14

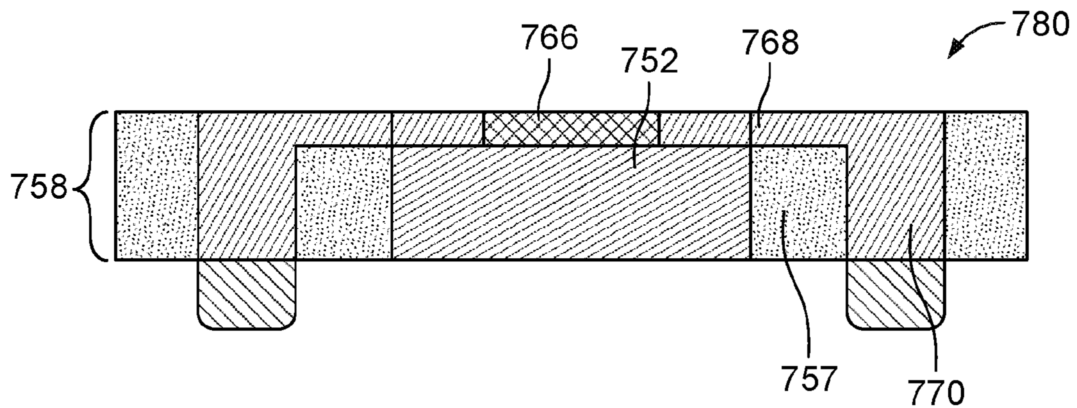


FIG. 15

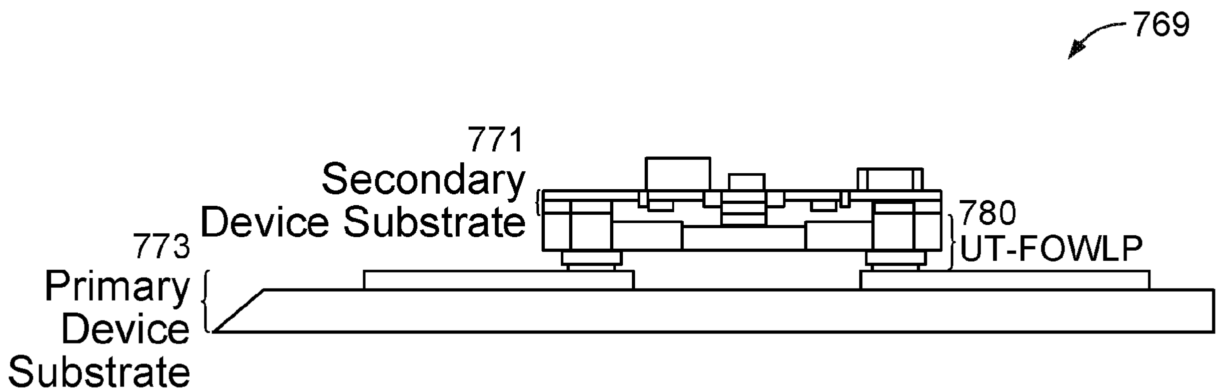


FIG. 16

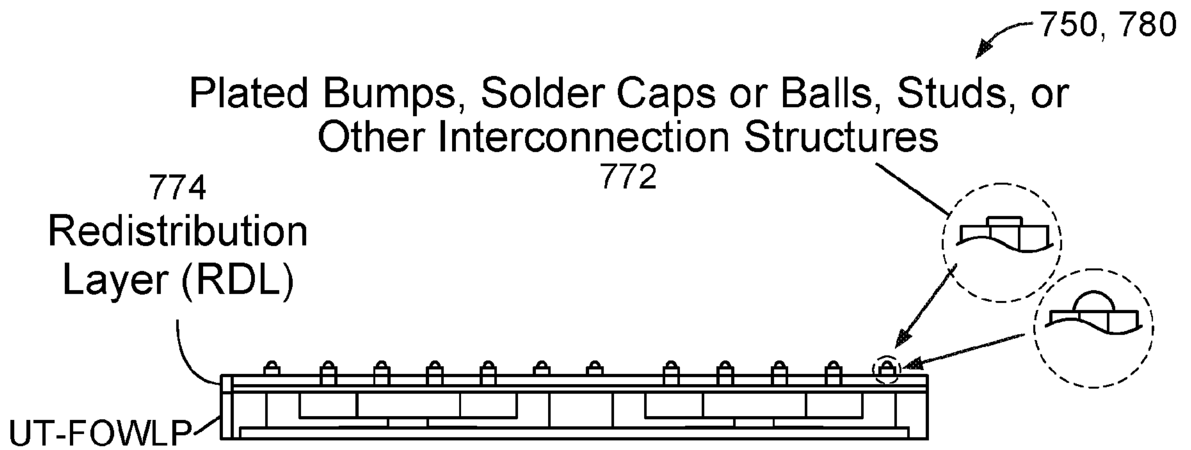


FIG. 17

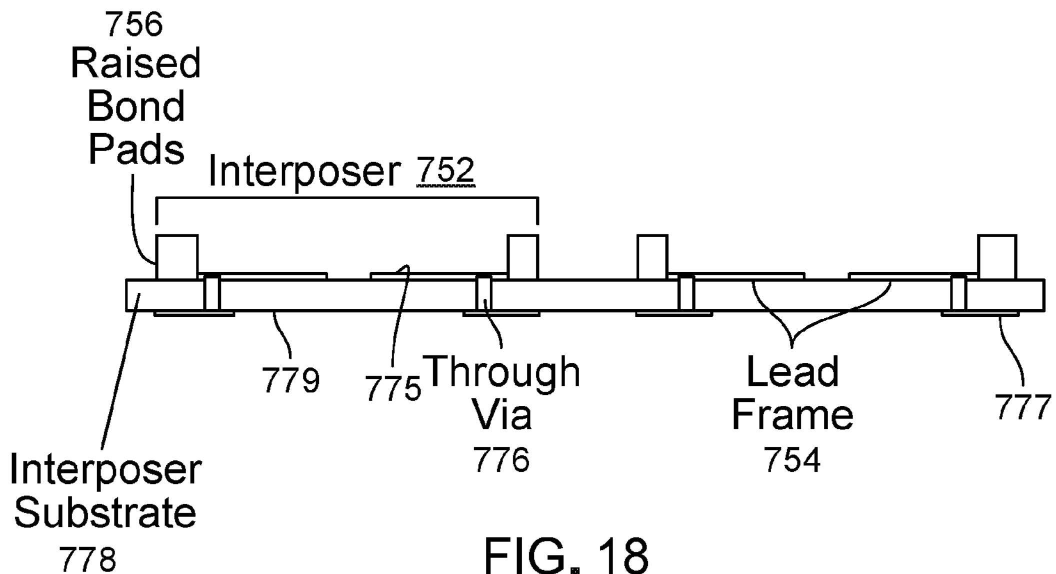


FIG. 18

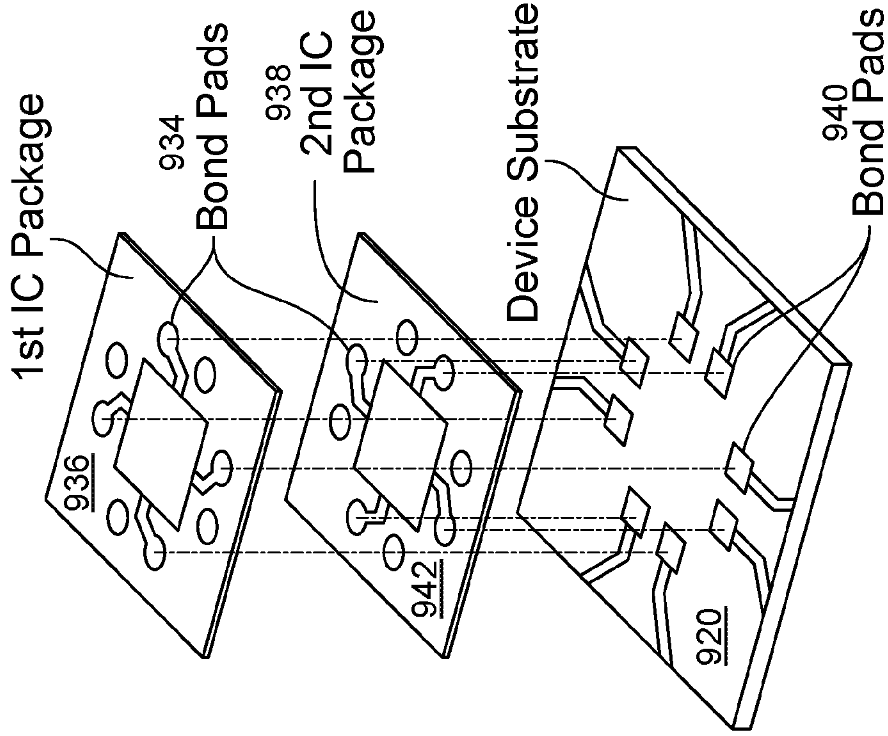


FIG. 19C

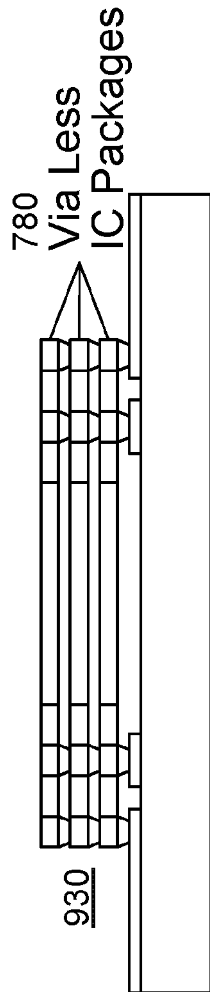


FIG. 19A

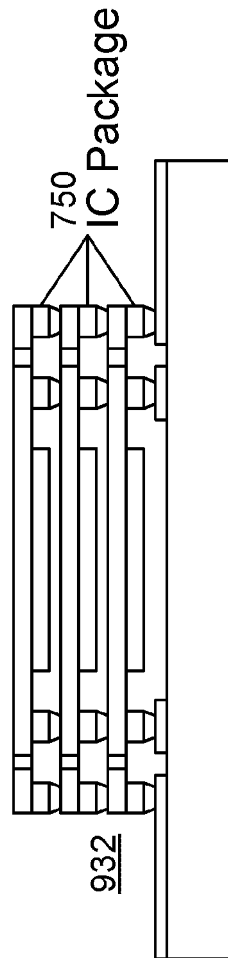


FIG. 19B

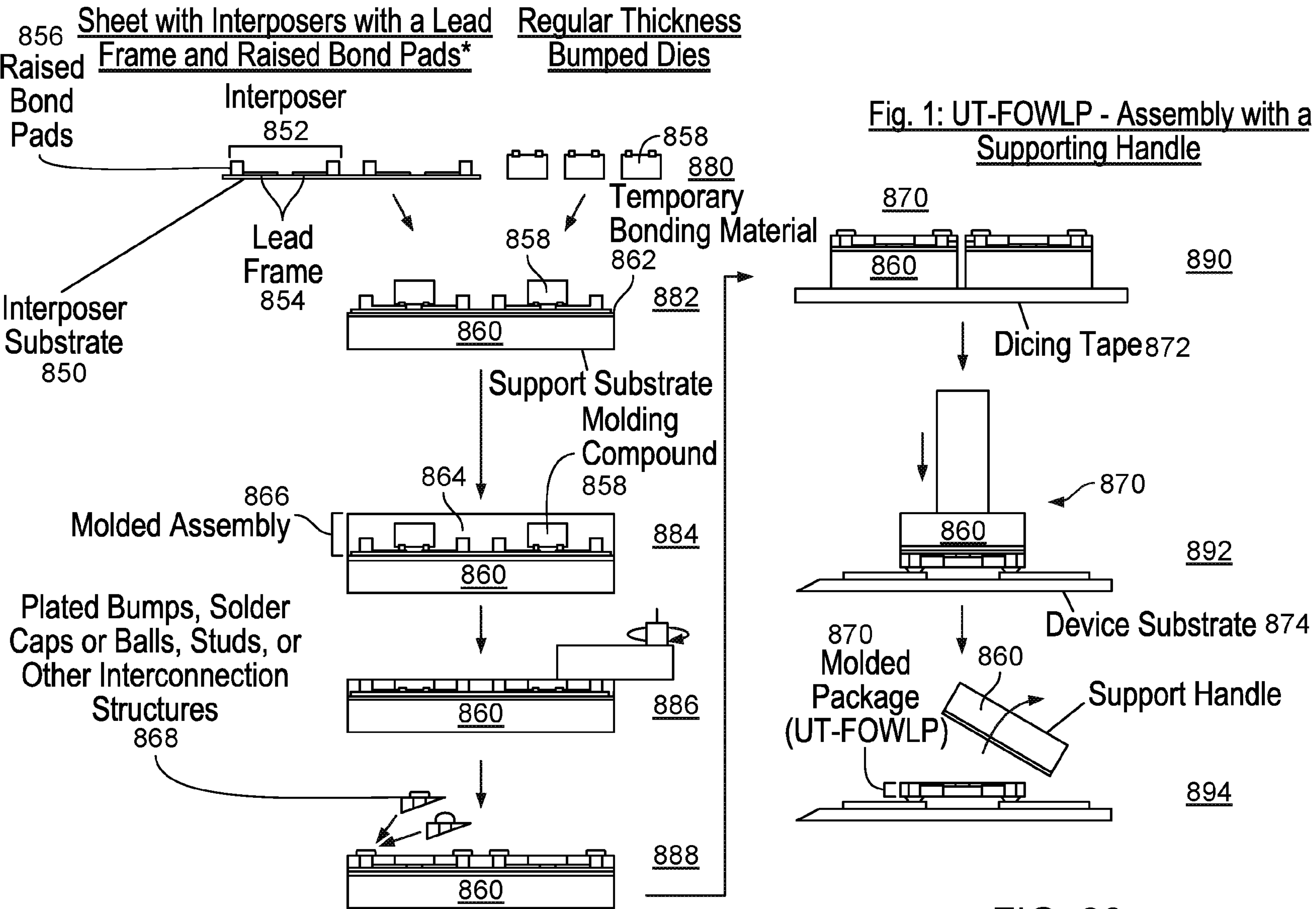


FIG. 20

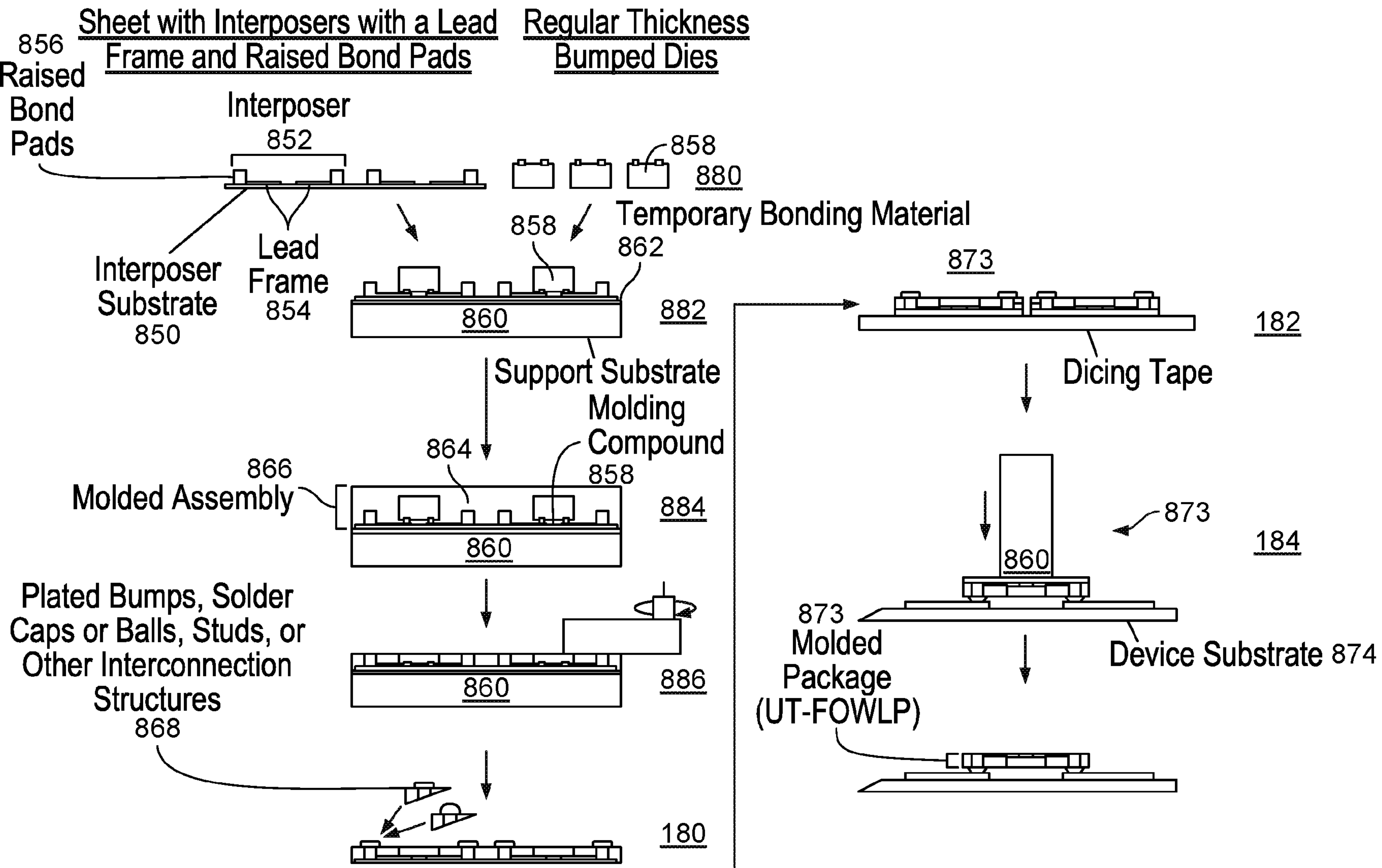


FIG. 21

856
Raised
Bond
Pads

Sheet with Interposers with a Lead Frame and Raised Bond Pads

Regular Thickness Bumped Dies

Interposer 852

858

880

Interposer Substrate 850

Lead Frame 854

858

Temporary Bonding Material

862

860

882

1st Support Substrate

Molding Compound 858

864

866

860

884

858

270

Plated Bumps, Solder Caps or Balls, Studs, or Other Interconnection Structures 868

876

272

2nd Support Substrate

876

274

878

876

276

Dicing Tape

878

876

278

Device Substrate 874

878 Molded Package (UT-FOWLP)

876

Support Handle

280

Package Backside

FIG. 22

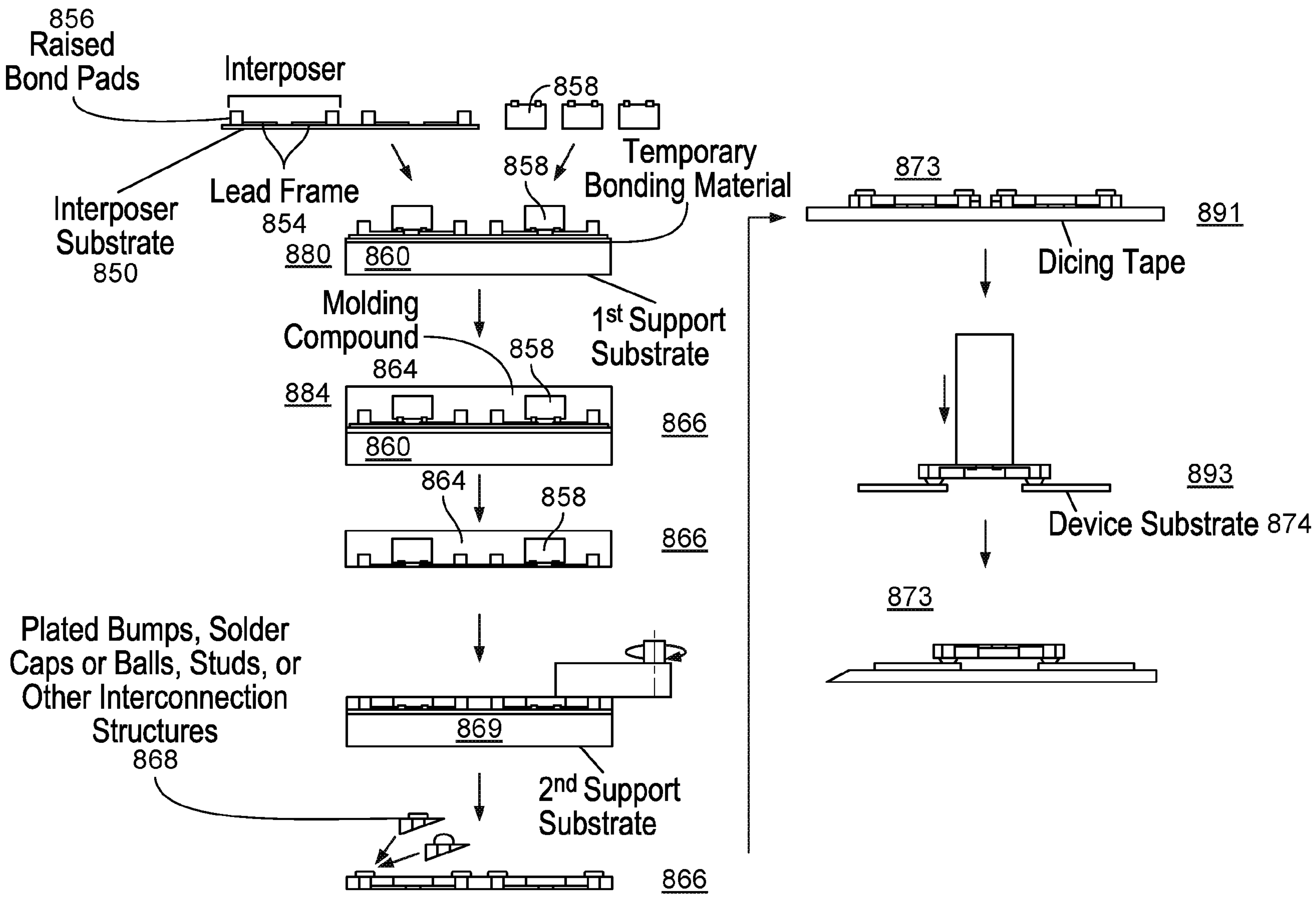


FIG. 23

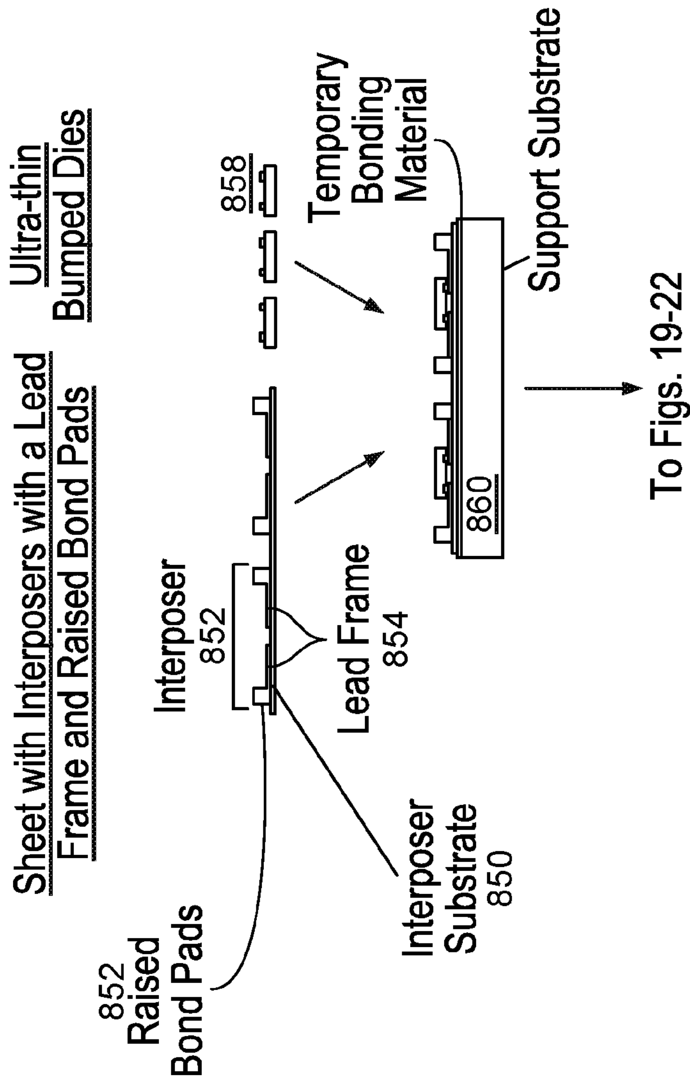


FIG. 24

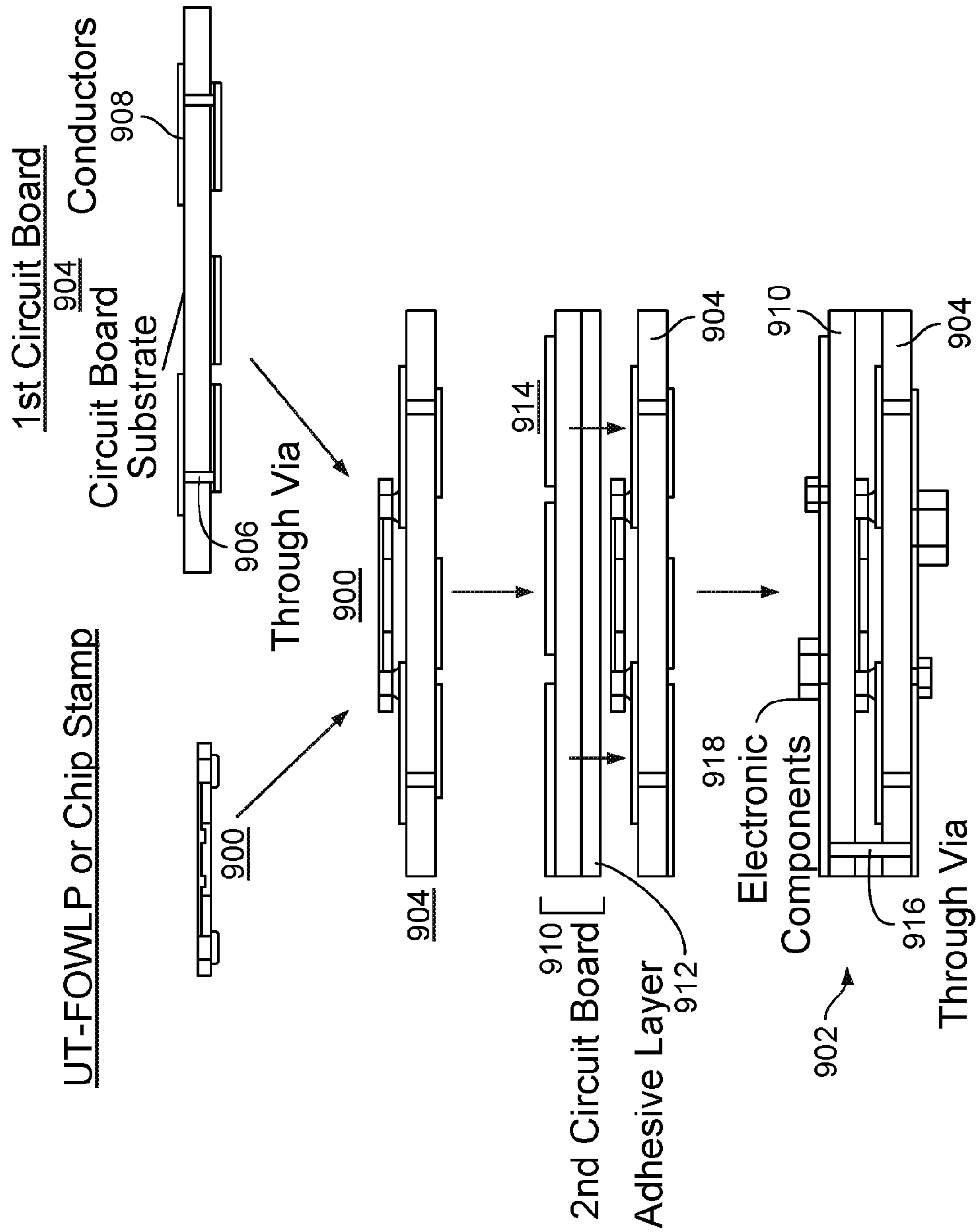


FIG. 25

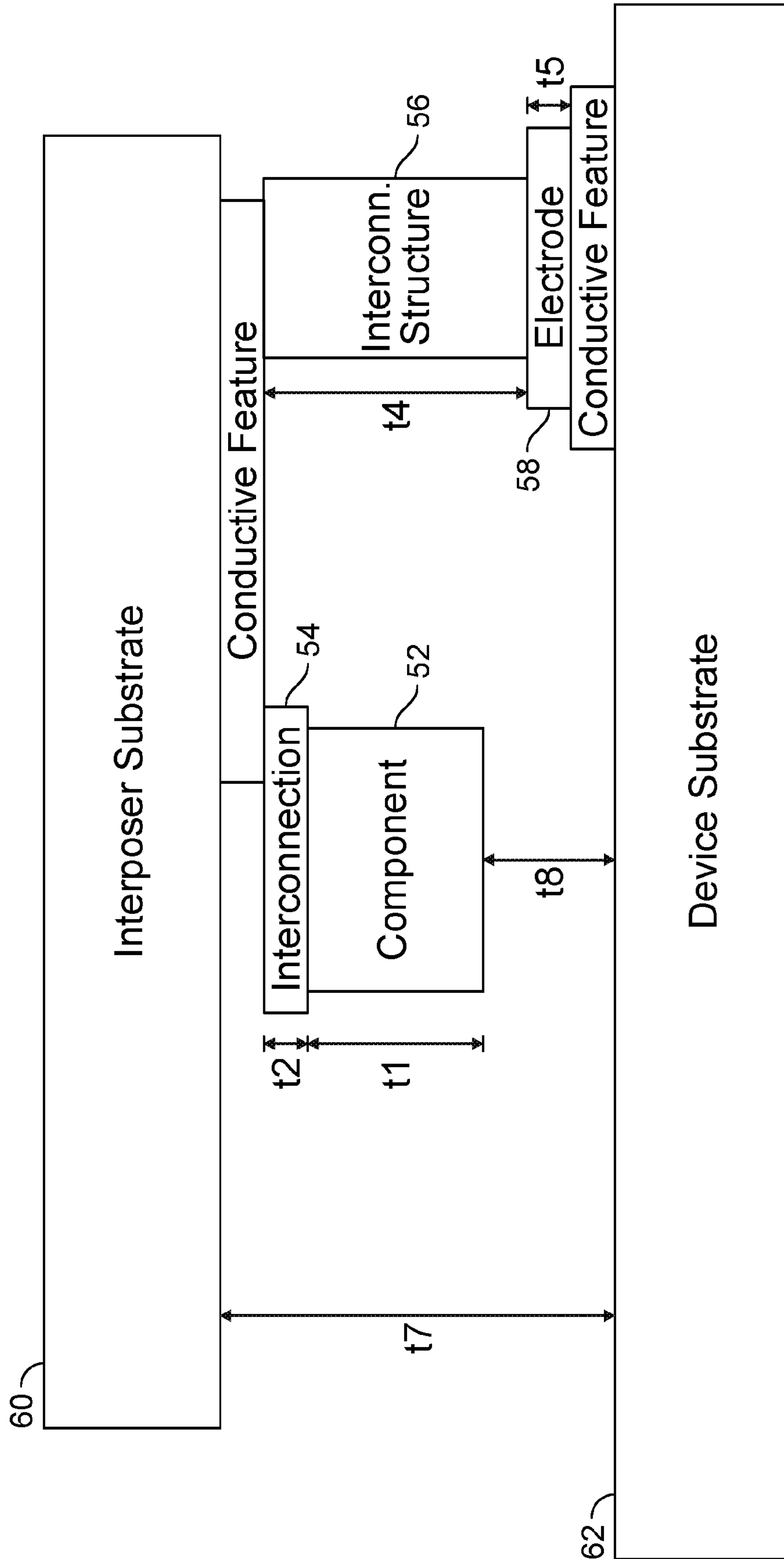


FIG. 26

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 17/28964

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/489, H01L 23/52, H01P 5/04, H05K 1/18, H05K 3/30, H05K 3/40 (2017.01)
CPC - H01L 21/0243, H01L 21/44, H01L 21/48, H01L 21/4814, H01L 21/4825, H01L 21/56, H01L 21/563, H01L 21/7806, H01L 23/498, H01L 23/49811, H01L 23/49822, H01L 23/5383, H01L 23/5386, H01L 24/02, H01L 24/07, H01L 24/10, H01L 51/0097, H01L 2224/33104, H01L 2924/15151, H01L 2924/381, H01L 2924/384, H01P 5/04, H05K 1/186, H05K 1/188, H05K 3/303, H05K 3/24, H05K 3/40, H05K 2201/10378

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2004/0246065 A1 (ROBERSON et al.) 09 December 2004 (09.12.2004), Figs. 1, 3, 4, 8; para [0008], [0009], [0026]-[0032], [0035], [0036], [0039], [0050], [0051], [0054]-[0057]	1-8, 12-15, 17-47, 62-65, 67-69, 90-92, 97,102,152 --- 9-11, 16, 48-61, 66, 93-96, 98-101
Y	US 2011/0285023 A1 (WEN-WEI et al.) 24 November 2011 (24.11.2011), para [0007], [0016], [0017]	9-11, 16, 101
Y	US 2004/0198033 A1 (LEE et al.) 07 October 2004 (07.10.2004), para [0012], [0015], [0034], [0039], [0041], [0043], [0052]	48-49, 54-61, 66, 93-96, 98-100
Y	US 2003/0003779 A1 (RATHBURN) 02 January 2003 (02.01.2003), Fig. 10A; para [0009], [0051], [0052], [0054], [0058], [0061], [0064], [0077], [0093]	48, 50-53, 58, 60, 61, 66

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search
22 August 2017

Date of mailing of the international search report
08 SEP 2017

Name and mailing address of the ISA/US
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450
Facsimile No. 571-273-8300

Authorized officer:
Lee W. Young
PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 17/28964

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I: Claims 1-69, 90-102, and 152, drawn to an apparatuses and methods comprising a separation.

Group II: Claims 70-89 and 103-151, drawn to assemblies and methods comprising an interposer.

Group III: Claims 153-262, drawn to apparatuses and a method comprising molded layers.

-- Please See Supplemental Box --

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-69, 90-102, 152

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 17/28964

Continued from Box No. III, Observations where unity of invention is lacking,

The inventions listed as Groups I, II, and III do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Special Technical Features

Groups II and III do not require an apparatus comprising: a first substrate and an assembly including: a second substrate; conductive features in contact with the second substrate; and an electronic component between the second substrate, that is required by Group I.

Groups I and III do not require an interposer, a second surface of the electronic component is 100 micrometers or less from the surface of the substrate; disposing the interposer substrate on a device substrate, including positioning the electronic component between the interposer substrate and the device substrate, conductive features formed on a surface of the substrate, each conductive feature having a first end and a second end on the first side of the substrate, in which at least a portion each conductive feature extends away from the substrate, in which each conductive feature extends to a height of 500 micrometers or less from the surface of the substrate, as required by Group II.

Groups I and II do not require a molded layer comprising an electronic component and a conductive element encapsulated within a molding material, a second electrical connection feature formed on a surface of the electronic component, the second electrical connection feature of the electronic component being electrically connected to the first electrical connection feature of the first substrate through the conductive element; a molded layer disposed on the first substrate such that a first surface of the molded layer is in contact with the first substrate, the molded layer comprising: an electronic component encapsulated within a molding material, the electronic component having electrical connection features, the electronic connection features facing the first substrate; and first ends of the conductive elements are exposed at a second surface of the molded layer and arranged in an arrangement corresponding to an arrangement of electrical contacts of a circuit board; multiple electronic components encapsulated within a molding material, each electronic component having electrical connection features facing a first surf ace of the molded layer; and forming a molded layer on the surface of the interposer substrate, the molded layer comprising an encapsulant covering the electronic components and sets of conductive features; thinning the molded layer to expose ends of the conductive features, in which thinning the molded layer includes thinning the electronic components, as required by Group III.

Shared Common Features

The only feature shared by Groups I, II, and III that would otherwise unify the groups is a first substrate; an electronic component; conductive features formed on a surface of the substrate, each conductive feature having a first end and a second end on the first side of the substrate, in which each conductive feature extends to a height of 500 micrometers or less from the surface of the substrate. However, this shared technical feature does not represent a contribution over prior art, because the shared technical feature is anticipated by US 2004/0246065 A1 to Roberson, et al. (hereinafter 'Roberson'). Roberson discloses a first substrate (Fig. 1; para [0029], [0030], first substrate, 29, second substrate, 30, and solder bumps therebetween, 16.); an electronic component (para [0015], [0034]); conductive features formed on a surface of the substrate, each conductive feature having a first end and a second end on the first side of the substrate (Fig. 2; para [0008], [0009], [0028], coupled conductive microstrips, 22, and 24, and solder bumps, 16, providing electrical connectivity between substrates located at ends of sides as shown... and bumps providing connectivity between strips.), in which each conductive feature extends to a height of 500 micrometers or less from the surface of the substrate (Fig. 1; para [0029], solder bumps of 100 micrometers.).

The only feature shared by Groups I and II that would otherwise unify the groups is an apparatus comprising: a first substrate including one or more electrical connection features; an electronic component disposed on the surface of the substrate, one or more connection elements on a first surface of the electronic component each electrically connected to the first end of a corresponding one of the conductive features, one or more of which are electrically connected to corresponding electrical connection features of the first substrate; and an electronic component in which a separation between the first substrate and a surface is 500 micrometers or less; a second surface of the electronic component is 500 micrometers or less from the surface of the substrate, and in which the height of the conductive features is greater than or equal to the separation between the second surface of the electronic component and the surface of the substrate. However, this shared technical feature does not represent a contribution over prior art, because the shared technical feature is anticipated by Roberson. Roberson discloses an apparatus comprising: a first substrate including one or more electrical connection features (Fig. 1; para [0029], [0030], first substrate, 29, second substrate, 30, and solder bumps therebetween, 16.); an electronic component disposed on the surface of the substrate, one or more connection elements on a first surface of the electronic component each electrically connected to the first end of a corresponding one of the conductive features (Fig. 2; para [0008], [0009], [0028], coupled conductive microstrips, 22, and 24, and solder bumps, 16, providing electrical connectivity between substrates located at ends of sides as shown... and bumps providing connectivity between strips.), conductive features one or more of which are electrically connected to corresponding electrical connection features of the first substrate (Figs. 1, 2; para [0008], [0028], [0034], coupled conductive microstrips, 18 and 20, providing electrical connectivity between substrates.); and an electronic component between the second surface and the first substrate and electrically connected to one or more of the conductive features (Fig. 2; para [0028], [0034], coupled conductive microstrips, 18, 20, 22, and 24, and substrates, 29 and 30, providing electrical connectivity between substrates.), in which a separation between the first substrate and the second surface is 500 micrometers or less (Fig. 1; para [0029], solder bumps of 100 micrometers.); a second surface of the electronic component is 500 micrometers or less from the surface of the substrate, and in which the height of the conductive features is greater than or equal to the separation between the second surface of the electronic component and the surface of the substrate (para [0029], solder bumps of 100 micrometers.).

-- Please See Supplemental Box --

Continued from Box No. III, Observations where unity of invention is lacking,

The only feature shared by Groups I and III that would otherwise unify the groups is conductive features arranged to each be in electrical contact with a corresponding electrical contact of a circuit board. However, this shared technical feature does not represent a contribution over prior art, because the shared technical feature is anticipated by Roberson. Roberson discloses a conductive features arranged to each be in electrical contact with a corresponding electrical contact of a circuit board (para [0025], [0026], coupling device for high speed network... flip-chip substrate.).

The only feature shared by Groups II and III that would otherwise unify the groups is disposing one or more electronic components, in which at least a portion each conductive feature extends away from the substrate, an electronic component having a first surface at which a pattern of electrical connection features are exposed; ends of conductive features/elements; an interposer substrate disposed on a support substrate, in which multiple sets of conductive features are formed on a surface of the interposer substrate; electrically connecting each of multiple electronic components to a corresponding set of conductive features; separating the a substrate into multiple packages, each package including a portion of the substrate, one or more of the electronic components, and the corresponding set of conductive features. However, this shared technical feature does not represent a contribution over prior art, because the shared technical feature is obvious over Roberson. Roberson further discloses disposing one or more electronic components, in which at least a portion each conductive feature extends away from the substrate (Fig. 2; para [0008], [0009], [0028], coupled conductive microstrips, 22, and 24.), an electronic component having a first surface at which a pattern of electrical connection features are exposed; ends of conductive features/elements (Fig. 2; para [0008], [0009], [0028], coupled conductive microstrips, 22, and 24, and solder bumps, 16, providing electrical connectivity between substrates located at ends of sides as shown... and bumps providing connectivity between strips.); an interposer substrate disposed on a support substrate, in which multiple sets of conductive features are formed on a surface of the interposer substrate (Fig. 3; para [0035], dielectric layers, 39.); electrically connecting each of multiple electronic components to a corresponding set of conductive features (Fig. 2; para [0008], [0009], [0028], coupled conductive microstrips, 22, and 24, and solder bumps, 16, providing electrical connectivity between substrates... and bumps providing connectivity between strips.); but does not specifically disclose separating the a substrate into multiple packages, each package including a portion of the substrate, one or more of the electronic components, and the corresponding set of conductive features. However, Roberson further discloses stacked wafer substrates (para [0036]), integrating the substrate as a module (para [0050]) and reduced circuit size (para [0050]). To a person of ordinary skill in the art, it would have been obvious through routine experimentation to select amongst known methods of producing stacked wafers substrates in order to optimize the cost of manufacturing chips from a wafer substrate.

As the technical features were known in the art at the time of the invention, this cannot be considered a special technical feature that would otherwise unify the groups.

Groups I, II, and III therefore lack unity under PCT Rule 13 because they do not share a same or corresponding special technical feature.

Note:

claim 180 improperly depending from non-existent claim 276. For the purpose of completing this LOU analysis, claim 180 has been assumed it is depending from claim 176.