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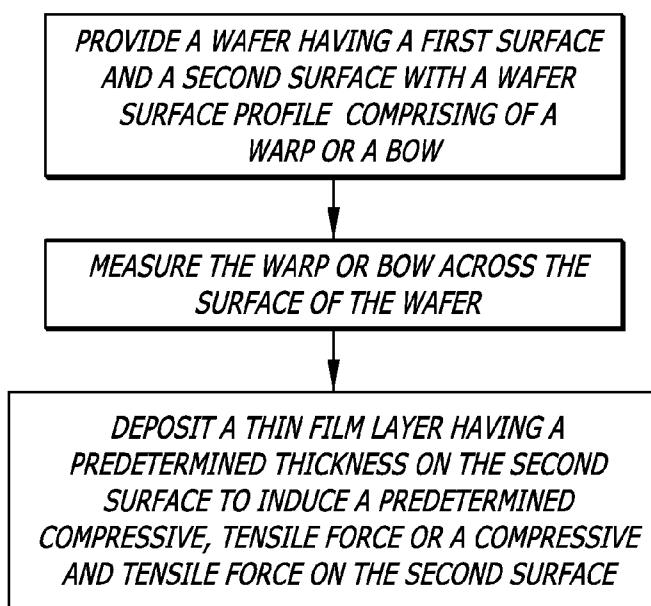
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(54) Title: METHODS FOR IMPROVING WAFER PLANARITY AND BONDED WAFER ASSEMBLIES MADE FROM THE METHODS

FIG. 1A



(57) Abstract: A method to improve the planarity of a semiconductor wafer and an assembly made from the method. In a preferred embodiment of the method, a compressive PECVD oxide layer such as SiO₂ having a predetermined thickness or pattern is deposited on the second surface of a semiconductor wafer having an undesirable warp or bow. The thickness or pattern of the deposited oxide layer is determined by the measured warp or bow of the semiconductor wafer. The compressive oxide layer induces an offsetting compressive force on the second surface of the semiconductor wafer to reduce the warp and bow across the major surface of the semiconductor wafer.



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METHODS FOR IMPROVING WAFER PLANARITY AND BONDED WAFER ASSEMBLIES MADE FROM THE METHODS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Patent Application No.

5 62/268,262 filed December 16, 2015.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention generally relates to semiconductor fabrication methods. More specifically, the invention relates to: 1) a method for enhancing the flatness, i.e.; the 10 planarity of a warped or bowed semiconductor wafer using oxide deposition techniques to increase semiconductor wafer and die yields, and, 2) a bonded semiconductor wafer assembly made from the method.

2. Prior Art

Industry-standard semiconductor wafers and in particular, GaN-on-sapphire 15 semiconductor wafers, substrates or templates, are common in photonic applications but often have surface non-planarity. The undesirable non-planarity of a semiconductor wafer can be characterized by warp and/or bowing. Typical warp and/or bow measurements on semiconductor wafers are affected by measurement method and edge exclusion region 20 definition. The smaller the edge exclusion region, the higher the measured warp and/or bow. Semiconductor wafer warp and/or bow are also affected by the diameter of the semiconductor wafer and by the thicknesses of the underlying substrate and grown epitaxial layers on standard semiconductor wafers. Semiconductor wafer warp may be on the order of 100 μm or greater across the surface of a 4-in. substrate and such non-planarity is an impediment in many semiconductor processes.

25 Undesirable non-planar semiconductor wafer profiles are generally convex and it is important to minimize or eliminate such non-planarity to improve processing yields in later fabrication steps. In standard applications, warp in a substrate is desirably reduced to at

least less than 80 μm across a 4-in. semiconductor wafer and greater reductions of warp/bow further improve semiconductor wafer bonding properties in subsequent processing steps.

The warp of a 4-in. photonic semiconductor wafer should be less than 80 μm to be accepted by a typical photolithographic stepper, such as a Canon stepper for example, in terms of mechanical handling (e.g.; vacuum arm and chuck), which in turn improves the local planar focus. Commonly, semiconductor wafer bow negatively affects vacuum arm pick up of the semiconductor wafer (from a cassette for example) and excessive semiconductor wafer warp negatively affects the suction of the semiconductor wafer onto the chuck. It is desired that any residual bow remains convex on the first semiconductor wafer surface rather than concave for improved subsequent processing of the semiconductor wafer.

An inexpensive process for reducing non-planarity and improving semiconductor wafer shape profile of the aforementioned semiconductor wafers is needed to improve yields in subsequent semiconductor wafer processing steps.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a process flow chart of a preferred set of steps of the method of the invention.

Fig. 1B is a cross-section of a semiconductor wafer having a convex warp or bow.

Fig. 1C is a cross-section of the semiconductor wafer after having a thin film layer deposited on its second surface.

Fig. 1D illustrates a pair of semiconductor wafers that have been processed according to the method of the invention and fusion bonded to form a semiconductor wafer assembly.

Fig. 2A is a wafer planarity map of a semiconductor wafer with a warp or bow that has not been processed according to the method of this invention.

Fig. 2B is a wafer planarity map of the semiconductor wafer of Fig. 2A after being processed according to the method of the invention.

Fig. 3A is a second surface of a semiconductor wafer that has been patterned with a thin film layer according to a method of the invention.

5 Fig. 3B is a second surface of a semiconductor wafer that has been patterned with two thin film layers according to another method of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In existing semiconductor fabrication steps, it is generally desired that the warp and/or bow of an unprocessed semiconductor wafer be as low as possible before processing 10 by a semiconductor photolithographic stepper and semiconductor wafer bonding equipment.

A preferred method of this invention comprises the step of an engineered patterning and deposition of a compressive dielectric material thin film layer (such as, without limitation, a PECVD oxide such as silicon oxide-SiO₂) of a predetermined thickness, pattern and composition, or a tensile layer of such material, to provide an offsetting compressive or 15 tensile force across the surface of a semiconductor wafer to reduce undesirable warp and bow in the semiconductor wafer. The planarizing effect of the above offsetting dielectric layer has been measured by Applicant herein and has been shown to materially improve the warp and/or bow properties of a non-planar photonic semiconductor wafer, resulting in improved yields during follow-on photolithography and semiconductor wafer bonding 20 steps.

In a first aspect of the invention as depicted in Figs. 1A-1D, a method is disclosed for reducing warp and/or bow in a semiconductor wafer comprising the steps of providing a semiconductor wafer 1 having a first surface and a second surface 10 wherein the surface profile of semiconductor wafer 1 comprises a warp and/or a bow as illustrated in Fig. 1B. 25 Normally, the first surface of the semiconductor wafer will be the surface of the semiconductor wafer in or on which the circuitry or other electronic or electrical devices are formed, though that is not a limitation of the invention, and in some cases electronic or electrical devices may be formed on the second surface or both surfaces of the semiconductor wafer. The warp and/or bow are measured across a surface of

semiconductor wafer 1, normally but not necessarily across the convex surface of the semiconductor wafer. A thin film layer 15 having a predetermined thickness, pattern or coefficient of thermal expansion ("CTE") is deposited on the second surface 10 to induce a predetermined strain-modifying compressive or tensile force or a compressive and tensile force on and across the second surface 10 of semiconductor wafer 1. In the specific embodiment illustrated in Figs. 1B and 1C, the thin film layer 15 is deposited on the second surface 10 to induce a predetermined strain-modifying tensile force on and across the second surface 10 of semiconductor wafer 1, causing the semiconductor wafer to substantially flatten, though preferably to leave a slight convex semiconductor wafer profile, as opposed to a semiconductor wafer profile that is a bit high in some locations and a bit low in other locations. The thin film layer 15 may comprise an oxide layer, metal layer, metal oxide layer or ceramic material layer or equivalent layer materials. The thickness, pattern or CTE of thin film layer 15 may be calculated and determined based on the measured warp and/or bow. As one example, thin film layer 15 may comprise an SiO₂ layer. Thin film layer 15 may be deposited using a PECVD process. Thin film layer 15 may have a thickness of about 1 μm per about 5 μm to about 8 μm of warp or bow. Semiconductor wafer 1 may comprise a GaN layer on a sapphire semiconductor wafer, substrate or template.

In a further aspect of the invention depicted in Fig 1D, a pair of semiconductor wafers 1, wherein one or both semiconductor wafers 1 have been processed according to the method of the invention, are bonded together, such as by fusion bonding or equivalent bonding methods as are known to persons skilled in the semiconductor wafer bonding arts, to provide a high quality bonded semiconductor wafer assembly. While the semiconductor wafers are shown bonded with a specific stacking relationship, in some applications one semiconductor wafer might be reversed, surface to surface, as again the greater planarity of each semiconductor wafer resulting from the application of the present invention improves the quality of the bond and accuracy of the relative location of the two semiconductor wafers, yielding a greater yield and better performance of the final product.

By way of example and not by limitation, a 4-in. semiconductor wafer desirably has a warp of less than about 80 μm for processing in industry-standard stepper equipment. For instance, when a semiconductor wafer is accepted by a Canon stepper, acceptable warpage or bowing is typically desired to be less than about 40-50 μm warp or bow across the

surface of the semiconductor wafer. Warpage or bowing below 40-50 μm semiconductor wafer warp/bow is further desired, particularly for subsequent semiconductor wafer fusion bonding applications. Any remaining warpage/bow is desirably convex across the first surface of the semiconductor wafer. Similarly, subsequent processing of such 5 semiconductor wafers that includes bonding with other semiconductor wafers demands a high level of wafer planarization. For example, the bonding of 4-in. semiconductor wafers using either direct fusion bonding or eutectic bonding would typically require less than 40-50 μm warp or bow across the surface of the semiconductor wafers, with flatter semiconductor wafers typically yielding reduced edge exclusion in the bonding process.

10 Unfortunately, conventional photonic semiconductor wafers, such as III-nitride semiconductor wafers on sapphire or silicon substrates, are frequently supplied with a semiconductor wafer surface profile having a least some degree of warpage and/or bowing.

15 Applicant herein discloses a method for minimizing semiconductor wafer warp and bowing. In a preferred set of the process steps of the invention, the steps are carried out using a deposition process with a plasma-enhanced chemical vapor deposition (PECVD) tool to deposit a silicon dioxide or "SiO₂" ("oxide" herein), thin film layer 15 having a predetermined thickness and composition on second (non-circuit bearing) surface 10 of 20 semiconductor wafer 1. It is expressly noted that the invention is not limited to the use of SiO₂ as a planarizing thin film layer 15 and different materials, such as those noted below and their equivalents, can be used as planarizing thin film layers 15 in the instant invention.

25 In a preferred embodiment of this invention, the atomic spacing of the oxide thin film layer 15 deposited on the second surface 10 of the semiconductor wafer 1 is greater than the atomic spacing of the substrate or template, such as sapphire, upon which the photonic material, such as III-nitride material, is deposited. The different atomic spacing creates a lattice mismatch between the two materials, resulting in an induced tension on the second surface of the semiconductor wafer 1. As a result, the deposited oxide thin film 30 layer 15 seeks a larger surface area than is provided by the sapphire substrate or template, creating a strain tending to enlarge the second surface of the semiconductor wafer, which in turn tends to flatten the sapphire as the oxide thin film layer 15 seeks to expand the second surface area 10. The foregoing assumes of course that the first surface of the semiconductor wafer was convex. Thus the layer 15 in this and other embodiments acts as a strain-

modifying layer reducing the warp or bow across the first and second surfaces of the semiconductor wafer compared to the warp or bow across the surface of the semiconductor wafer before the layer 15 is deposited.

In addition to lattice mismatch-related strain, thermal expansion mismatch-related
5 strain plays a significant role in changing a semiconductor wafer 1 shape which phenomenon is exploited in an alternative embodiment of the instant invention. As earlier indicated, there are two primary mechanisms involved in an induced film stress; atomic spacing (i.e.; lattice mismatch) and coefficient of thermal expansion ("CTE") differences. CTE may be considered as the amount volumes and linear dimensions change with respect
10 to temperature. CTE is mathematically defined as: $\alpha = (1/D) (\Delta D / \Delta T)$ where α is the CTE; D is volume, area or a linear dimension and T is temperature. Normally materials expand when heated though these dimensional changes vary from material to material.

CTE itself is a physical phenomenon and is exploited in a preferred embodiment as a semiconductor wafer planarizing method, particularly when certain thin film layer 15
15 materials are deposited on a semiconductor wafer 1 surface at a temperature other than room temperature. CTE occurs due to the fact that as temperature increases, higher level quantum states in a material become more populated in the asymmetric potential wells. These higher level quantum states have probability densities that increase at values greater than the equilibrium radius. In other words, on a time average, atoms spend more time at a
20 farther distance away from each other as temperature increases. If there is a CTE mismatch between two materials, the amount of average atomic spacing change with temperature is different for each material. A basic example of CTE film stress (neglecting lattice mismatch) is where a film with a larger CTE than the host substrate is deposited at an elevated temperature. At the deposition temperature, the structure is stress-neutral but once
25 the structure cools, thin film layer 15 will contract more than the substrate, causing thin film layer 15 to be in tensile or compressive stress (depending on the film material CTE) across second surface 10.

A preferred set of process steps for a oxide deposition of the invention may comprise the following parameters as set forth in Table 1:

Temperature = about 100 to 400 °C
Deposition Pressure = about 100 to 2000 mTorr
N ₂ Flow = about 10 to 2000 sccm
95% N ₂ /5% SiH ₄ Flow = about 10 to 2000 sccm
-or-
100% SiH ₄ Flow = about 0.5 to 50 sccm
N ₂ O Flow = about 100 to 3000 sccm
RF Power = about 100 to 1000W at about 13.56 MHz
Deposition rate = about 500 to 5000 Å/min
BOE (6:1 Buffered Oxide Etchant) rate of resultant oxide = about 500 to 5000 Å/min
Oxide Film Stress = about 100 to 1000 MPa compressive on Si(100)

Table 1 Exemplar Process Parameters

The deposited oxide thin film layer 15 preferably has a non-uniformity of less than about 10%. Processing temperatures during oxide thin film layer 15 deposition are not a substantial processing constraint as it has been observed that an oxide thin film layer 15 deposited within the range of about 300 °C and 400 °C exhibits an acceptable compressive effect.

Using the above exemplar process parameters, the preferred embodiment of this invention results in roughly about 5-8 µm of warp or bow relief per 1 µm of oxide thin film layer 15 deposited.

Referring to Figs. 2A and 2B, a graphical depiction of warp and bow adjustment data from semiconductor wafer metrology measurements conducted using Sigmatech back-pressure semiconductor wafer shape measurement equipment is set forth showing planarity improvement from an unprocessed semiconductor wafer (Fig. 2A) to the same semiconductor wafer that has been processed according to the method of this invention (Fig. 2B). This planarity improvement manifests itself in the lower range of the measurements in the legend of these Figs.

Experimental practice of a preferred embodiment of this invention resulted in an average warp reduction of about 6.3 µm for 1 µm of oxide thin film layer 15 deposited on 4-

in. semiconductor wafers 1 that were processed according to the methods of this invention, with an average bow reduction of about 3.4 μm for 1 μm oxide deposited.

Total thickness variation or "TTV" can increase or decrease roughly by the non-uniformity of the deposited oxide thin film layer 15 and such semiconductor wafer 1 thickness scales at about 80-90% of the target deposited oxide thickness.

In a sample semiconductor wafer processing run using the steps of the invention, after a target 2 μm oxide thin film layer 15 deposition, semiconductor wafer warp was shown to decrease from 56.5 to 43.3 μm ; bow was shown to decrease from 29.2 to 22.7 μm ; TTV was shown to increase from 6.8 to 7.4 μm ; and semiconductor wafer thickness shown to increase from 662.9 to 664.7 μm . Further exemplar warp reduction data is shown in Table 2 below.

Wafer 384G		Wafer 385G	
Oxide Deposited (μm)	Warp (μm)	Oxide Deposited (μm)	Warp (μm)
0	88.3	0	86.4
2	75.1	2	74.2
4	64.4	4	63.7
6	52.7	6	52.1
8	39.3	7	43.8

Table 2. Change in Wafer Warp with Second Surface Oxide Deposition Thickness

It is noted that once a second surface warp and bow adjustment oxide thin film layer 15 is deposited, it is preferable that semiconductor wafer 1 not be exposed to buffered oxide etchants or "BOE" and HF, unless a warp and bow adjust oxide thin film layer 15 deposition step is repeated.

Further, deposited thin film layer 15 oxide thickness uniformity may have some effect on subsequent processing steps such as laser liftoff (LLO) uniformity, for example. LLO uniformity may be affected by the quarter-wavelength interference condition of the UV laser light caused by oxide thin film layer 15 uniformity and not by UV absorption of the layer 15.

It is expressly noted that the methods of this invention need not be practiced solely using the exemplar preferred compressive PECVD oxide thin film layer 15 deposited on c-plane sapphire which is the example used for illustration and discussion purposes and not by way of limitation. The method and claims of the invention expressly encompass the use of 5 any high-stress thin film layer 15 deposited on any surface of any semiconductor wafer 1 so as to manipulate the shape, warp and bow of semiconductor wafer 1. The deposited thin film layer 15 is thus not limited to silicon dioxide material; any suitable thin film layer 15 that may be deposited on a semiconductor wafer 1 surface at a predetermined thickness that is sufficient to induce a predetermined compressive, tensile force or a compressive and 10 tensile force due to lattice mismatch or differing CTEs on the second surface 10, may be used.

Alternate methods are illustrated in Figs. 3A and 3B. In Fig. 3A, the thin film layer 15 is patterned to form elongated strips of the thin film layer, which provides a dominant axis for the strain-modifying effect, whether the thin film layer 15 is chosen to exert 15 compressive forces or tensile forces on the adjacent surface 10 of the semiconductor wafer 1. This can be useful when the bow or warp is about a single axis, or predominately about a single axis. If however the bow or warp is about two axes, but unequal, a second patterned thin film layer 15 may be deposited and oriented about a second axis as shown in Fig. 3B. Note also that unequal strains may be also obtained by simply choosing the width of the 20 strips of layer 15 in Fig. 3A. Also in Fig. 3B, the vertical and horizontal strips may be of the same or different thin film layer materials. In that regard, in some cases, the bow or warp may be in opposite directions about the two axes, in which case different thin film layer materials will be used, one to induce compressive forces on the adjacent semiconductor substrate and one to induce tensile forces on the adjacent substrate.

25 Numerous suitable thin film layer 15 materials which may be deposited on a semiconductor wafer 1 surface are commercially available that are of dissimilar composition and, as such, impart sufficient semiconductor wafer surface strain, thus changing the semiconductor wafer 1 surface profile. Silicon oxide is well-suited for such applications because it is simple to deposit on a semiconductor wafer 1 surface and can be 30 grown in a stress state that reshapes the bow and warp of semiconductor wafer 1 but in alternative embodiments, materials such as silicon nitride, ceramic, metal, or metal oxide thin film layers 15 may be used and are contemplated as within the scope of the method of

the invention. Further, the above-referenced semiconductor wafer 1 may be regarded as having a generic shape and the methods of this invention function to flatten any generic substrate shape by the deposition of a strain-modifying or compression-modifying thin film layer 15 or films on second surface 10 of semiconductor wafer 1. Thus the primary 5 variables for the thin film layer are material, thickness and thin film layer pattern, together with the coefficient of thermal expansion that is a characteristic of the material, which in some cases may be different for different film thicknesses of interest for the same material.

In the previously-discussed preferred embodiment of c-plane GaN-on-sapphire, semiconductor wafer 1, as viewed with epitaxial surface up, often tends to be fairly 10 uniformly convex, i.e.; the highest point is toward the center of the GaN surface. In such instances, the earlier-described deposition of a blanket compressive oxide thin film layer 15 on the second surface of semiconductor wafer 1 is particularly effective. It is expressly noted however that deposited thin film layer 15 need not be limited to an SiO₂ material and that the deposited thin film layer material may be any material that imparts an opposite 15 curvature to semiconductor wafer 1 as compared to the GaN or semiconductor wafer material.

In an instance where semiconductor wafer 1 is concave, rather than applying a compressive thin film layer 15 to the second surface of the semiconductor wafer as in the aforementioned convex down non-planarity, a deposited thin film layer 15 may be applied 20 that imparts tensile stress to the sapphire. GaN itself is a suitable candidate for this embodiment of the invention.

In the generic case of semiconductor wafer 1 having different curvatures in different crystallographic directions, such as semipolar GaN grown on m-plane sapphire, this invention enables a reduction in the bow along one axis but may increase it in the 25 perpendicular direction.

To address this concern, an alternate embodiment is disclosed in which a "shadow mask" as is known in the semiconductor arts, may be utilized to selectively deposit a strain-modifying thin film layer 15 having predetermined strain-modifying or tensile characteristics on different portions or areas of second surface 10 of semiconductor wafer 1.

An equivalent effect may also be achieved by depositing a blanket planarizing thin film layer 15 to second surface 10 of semiconductor wafer 1, patterning semiconductor wafer 1 using photolithography with a predetermined thin film layer 15 pattern such as the exemplar pattern illustrated in Fig. 4, and then selectively removing predetermined areas or 5 portions of the planarizing thin film layer 15 to induce a desired change in the wafer planarity.

By way of example and not by limitation, by using a shadow mask having a predetermined strain-modifying pattern thereon, a user may deposit a compressive thin film layer 15 oxide as strips consisting of, for example, two-thirds of the semiconductor wafer 10 area and, for example, a tensile nitride on the central third of semiconductor wafer 1 to modify the shape differently along different axes (Figs. 3A and 3B).

The differing or varying compressive/tensile layer pattern may be determined using, for instance, strain modeling software based on a given semiconductor wafer shape to model an optimum modifying thin film layer or layers 15 combination pattern for a 15 particular semiconductor wafer bow.

Many alterations and modifications may be made by those having ordinary skill in the art without departing from the spirit and scope of the method of the invention herein. Therefore, it must be understood that the illustrated embodiment has been set forth only for the purposes of example and that it should not be taken as limiting the invention as defined 20 by any claims in any subsequent application claiming priority to this application.

For example, notwithstanding the fact that the elements of such a claim may be set forth in a certain combination, it must be expressly understood that the invention includes other combinations of fewer, more or different elements, which are disclosed in above even when not initially claimed in such combinations.

25 The words used in this specification to describe the invention and its various embodiments are to be understood not only in the sense of their commonly defined meanings, but to include by special definition in this specification structure, material or acts beyond the scope of the commonly defined meanings. Thus, if an element can be understood in the context of this specification as including more than one meaning, then its

use in a subsequent claim must be understood as being generic to all possible meanings supported by the specification and by the word itself.

The definitions of the words or elements of any claims in any subsequent application claiming priority to this application should be, therefore, defined to include not only the
5 combination of elements which are literally set forth, but all equivalent structure, material or acts for performing substantially the same function in substantially the same way to obtain substantially the same result. In this sense, it is therefore contemplated that an equivalent substitution of two or more elements may be made for any one of the elements in such claims below or that a single element may be substituted for two or more elements in such a
10 claim.

Although elements may be described above as acting in certain combinations and even subsequently claimed as such, it is to be expressly understood that one or more elements from a claimed combination can in some cases be excised from the combination and that such claimed combination may be directed to a subcombination or variation of a
15 subcombination.

Insubstantial changes from any subsequently claimed subject matter as viewed by a person with ordinary skill in the art, now known or later devised, are expressly contemplated as being equivalently within the scope of such claims. Therefore, obvious substitutions now or later known to one with ordinary skill in the art are defined to be
20 within the scope of the defined elements.

Any claims in any subsequent application claiming priority to this application are thus to be understood to include what is specifically illustrated and described above, what is conceptually equivalent, what can be obviously substituted and also what essentially incorporates the essential idea of the invention.

CLAIMS

What is claimed is:

1. A method for reducing warp or bow in a semiconductor wafer comprising:
providing a semiconductor wafer having a first surface and a second surface wherein
5 a semiconductor wafer surface profile comprises a warp or bow;
measuring the warp or bow across a surface of the semiconductor wafer; and;
depositing an oxide layer having a predetermined thickness on the second surface to
induce a predetermined compressive force, tensile force or combined compressive and
tensile forces on the second surface, reducing the warp or bow in the semiconductor wafer
10 surface profile compared to the warp or bow in the semiconductor wafer surface profile
before the oxide layer is deposited.
2. The method of claim 1 wherein the oxide layer thickness is predetermined
based on the measured warp or bow in the semiconductor wafer surface profile.
3. The method of claim 1 wherein the oxide layer is an SiO₂ layer.
- 15 4. The method of claim 1 wherein the oxide layer is deposited in a PECVD
process.
5. The method of claim 1 wherein the oxide layer has a thickness of 1 μm per 5
μm to 8 μm of warp or bow.
- 20 6. The method of claim 1 wherein the semiconductor wafer is a GaN on
sapphire wafer, substrate or template.
7. A method of reducing warp or bow in a semiconductor wafer comprising:
providing a semiconductor wafer having a first surface and a second surface wherein
a semiconductor wafer surface profile comprises a warp or bow;
measuring the warp or bow across the surface of the semiconductor wafer; and;
25 depositing at least one strain-modifying layer having a predetermined thickness on
the second surface to induce a predetermined compressive force, tensile force or a
compressive and tensile force on the second surface, the at least one strain-modifying layer

reducing the warp or bow across the surface of the semiconductor wafer compared to the warp or bow across the surface of the semiconductor wafer before the at least one strain-modifying layer is deposited.

8. The method of claim 7 wherein the oxide layer thickness is determined at 5 least in part based on the measured warp or bow.

9. The method of claim 7 wherein the at least one strain-modifying layer is a silicon nitride layer.

10. The method of claim 7 wherein the at least one strain-modifying layer is a metal oxide material.

10 11. The method of claim 7 wherein the at least one strain-modifying layer is a group III-nitride.

12. The method of claim 7 wherein the at least one strain-modifying layer is deposited in a PECVD process.

15 13. The method of claim 7 wherein the at least one strain-modifying layer is deposited in a physical vapor deposition process.

14. The method of claim 7 wherein the at least one strain-modifying layer has a thickness of 1 μm per each about 5 μm to 8 μm of warp or bow.

15 15. The method of claim 7 wherein the at least one strain-modifying layer is patterned.

20 16. The method of claim 7 further comprising fusion bonding the semiconductor wafer to one or more other semiconductor wafers that have also been subjected to the method of claim 7.

17. A semiconductor wafer comprising:
a semiconductor wafer having a first surface and a second surface, and;

at least one strain-modifying layer on the second surface inducing a compressive force, tensile force or compressive and tensile forces on the second surface to reduce the warp or bow of the semiconductor wafer to below the warp or bow of the semiconductor wafer before the at least one strain-modifying layer is applied.

5 18. The semiconductor wafer of claim 17 wherein the at least one strain-modifying layer comprises first and second strain-modifying layers.

10 19. The semiconductor wafer of claim 18 wherein the first strain-modifying layer is patterned to form a plurality of elongated layer segments extending in a first direction on the semiconductor wafer, and the second strain-modifying layer is patterned to form a plurality of elongated layer segments extending in a second direction on the semiconductor wafer.

20. The semiconductor wafer of claim 19 wherein one strain-modifying layer applies a compressive force on the second surface and the second strain-modifying layer applies a tensile force on the second surface.

15 21. The semiconductor wafer of claim 17 wherein the at least one strain-modifying layer is selected from the group consisting of SiO₂, silicon nitride, a metal oxide material or a group III-nitride.

20 22. The semiconductor wafer of claim 17 wherein the semiconductor wafer is a GaN on sapphire wafer, substrate or template, and the strain modifying layer is an SiO₂ layer.

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FIG. 1A

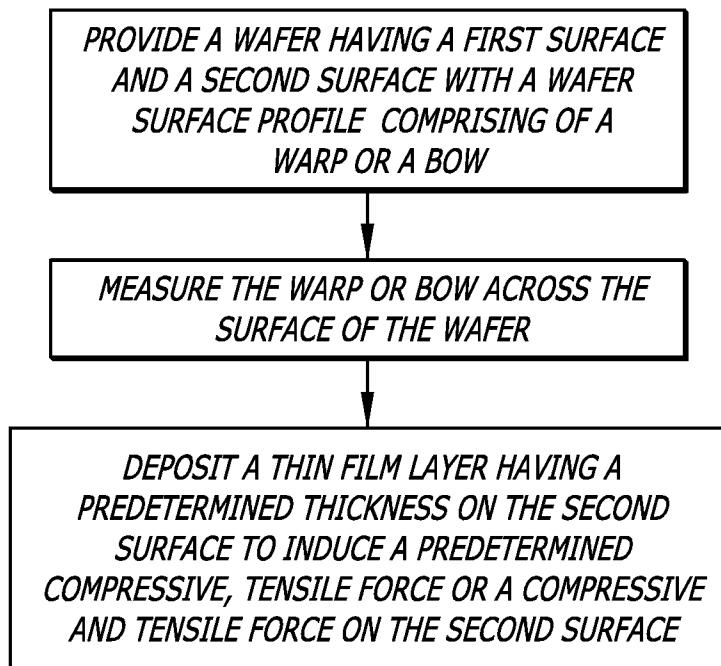


FIG. 1B

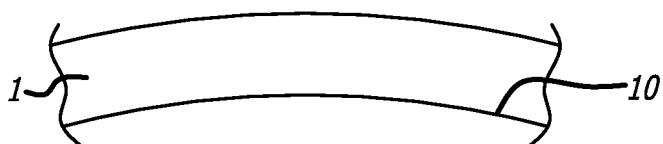


FIG. 1C

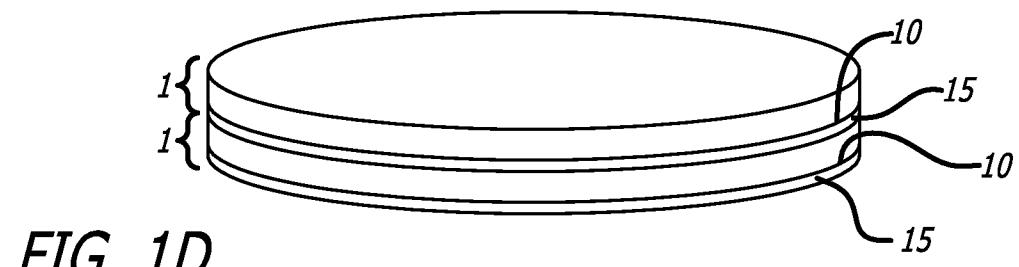
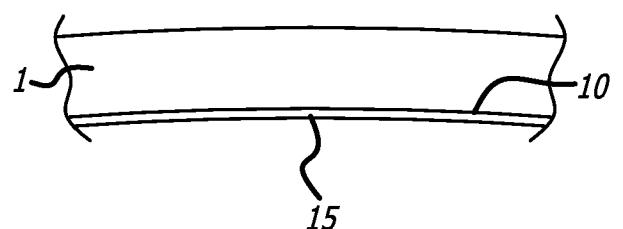
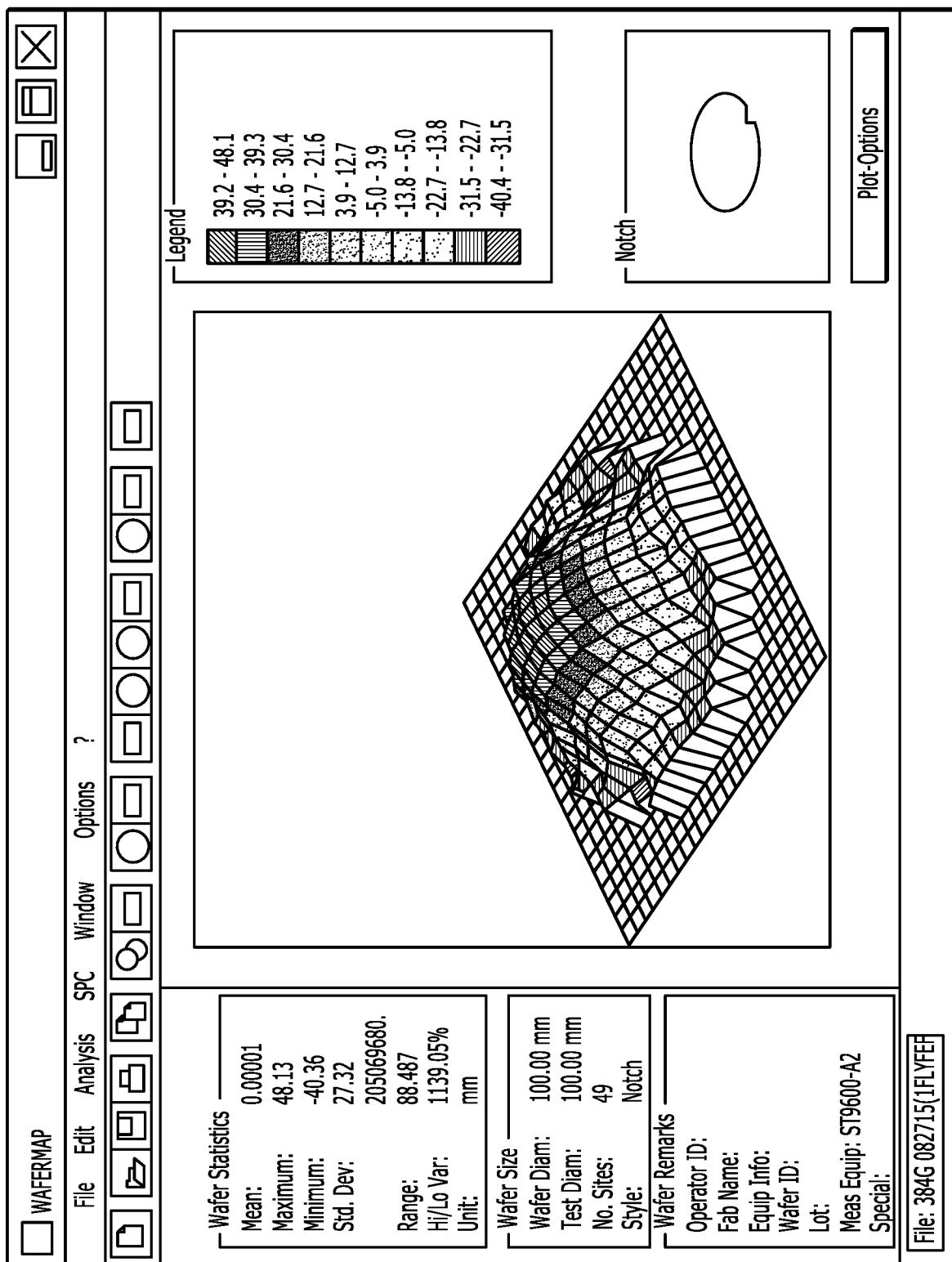


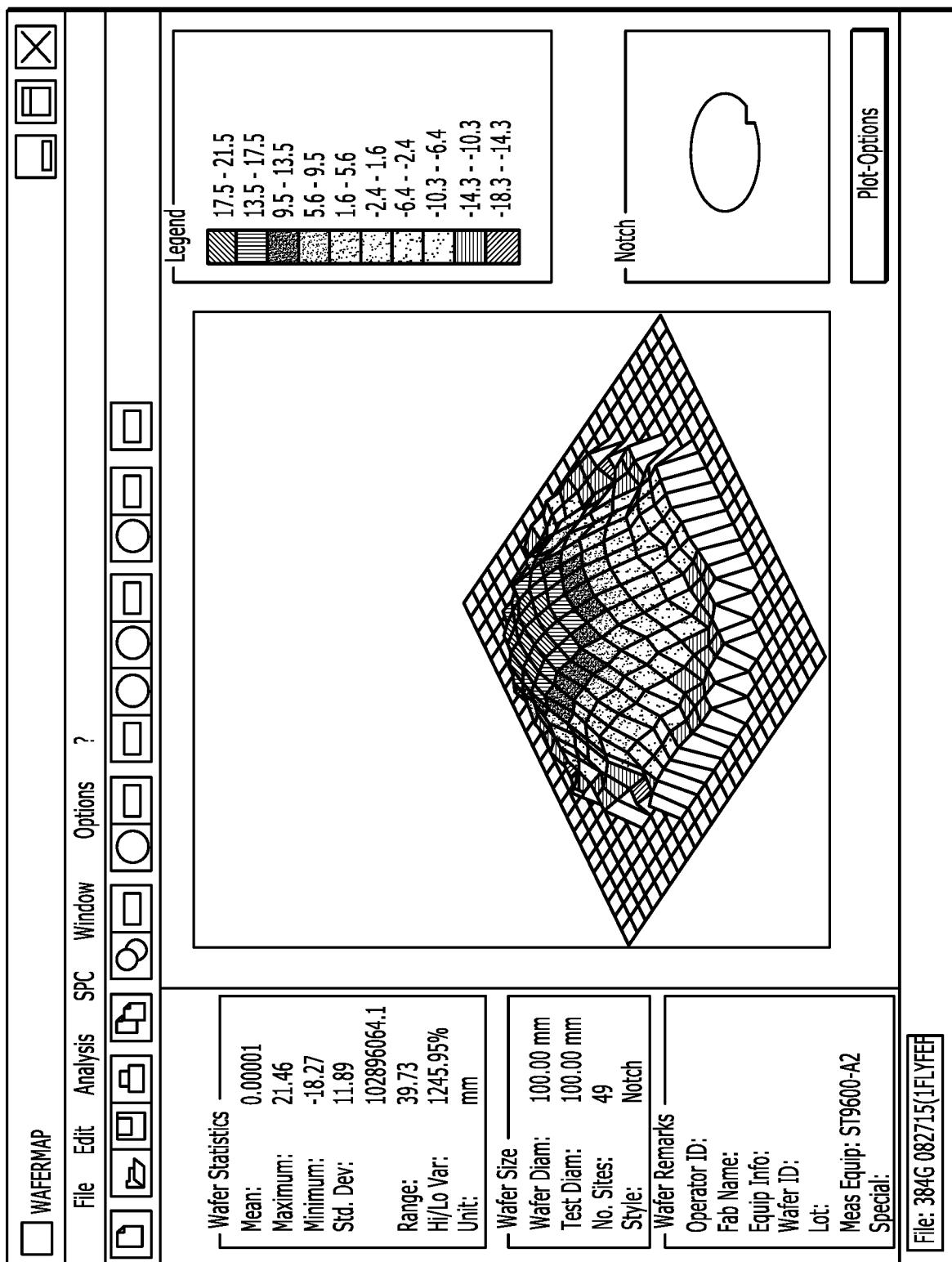
FIG. 1D

FIG. 2A



3/4

FIG. 2B



4/4

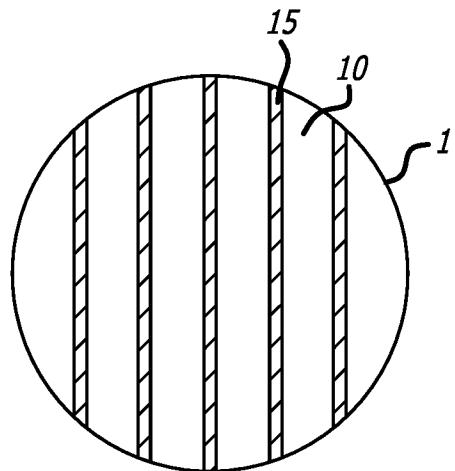


FIG. 3A

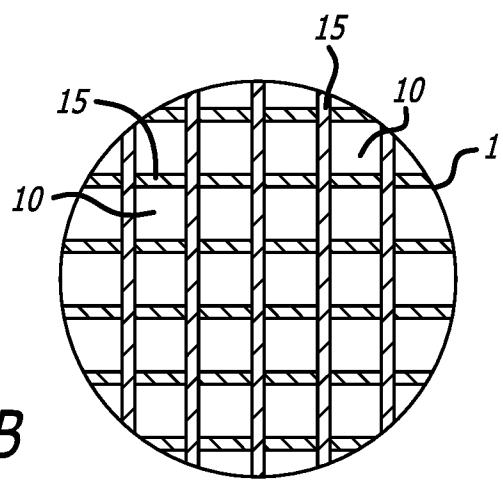


FIG. 3B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2016/067379

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 21/822; H01L 21/02; H01L 21/06; H01L 21/20; H01L 21/38; H01L 21/67 (2017.01)

CPC - H01L 21/31612; H01L 21/02; H01L 21/18; H01L 21/316; H01L 21/31604; H01L 21/31608; H01L 21/31616; H01L 21/31654; H01L 21/31675; H01L 21/3185; H01L 2924/00; H01L 2924/10 (2017.02)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7,880,278 B2 (JENG et al) 01 February 2011 (01.02.2011) entire document	1-5, 7-9, 12-15, 17-21
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Y		6, 10, 11, 16, 22
Y	US 2007/0194342 A1 (KINZER) 23 August 2007 (23.08.2007) entire document	6, 22
Y	US 4,790,920 A (KRZANICH) 13 December 1988 (13.12.1988) entire document	10
Y	US 6,652,356 B1 (ARIGA) 25 November 2003 (25.11.2003) entire document	11
Y	US 5,286,671 A (KURTZ et al) 15 February 1994 (15.02.1994) entire document	16

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	"&" document member of the same patent family

Date of the actual completion of the international search

30 January 2017

Date of mailing of the international search report

24 FEB 2017

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