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(54) METAL-INSULATOR-METAL (MIM) CAPACITOR

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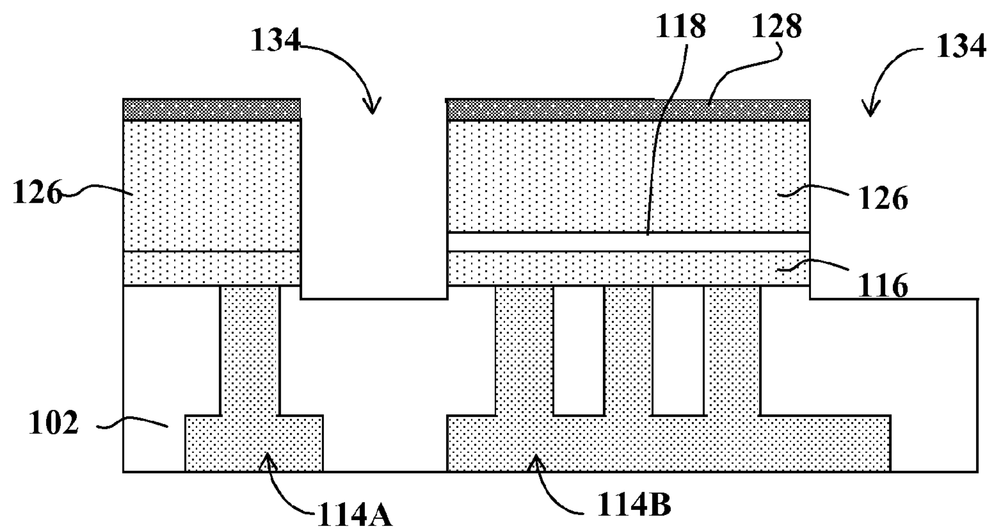
CPC ***H01L 28/40*** (2013.01)
USPC **257/532**; 438/396

(57) **ABSTRACT**

There is disclosed a metal-insulator-metal, MIM, capacitor. The MIM capacitor comprises a MIM stack formed within an interconnect metal layer. The interconnect metal layer is utilised as an electrical connection to a metal layer of the MIM stack.



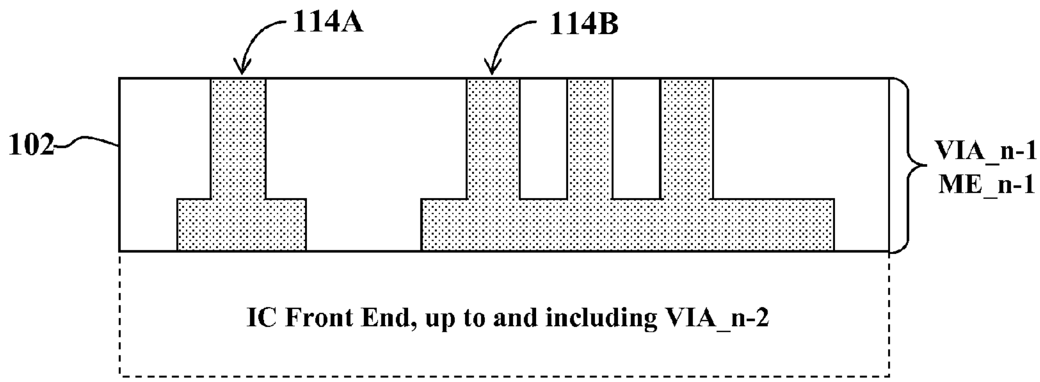

114A
114B
102
VIA_n-1
ME_n-1
IC Front End, up to and including VIA_n-2

FIG. 1

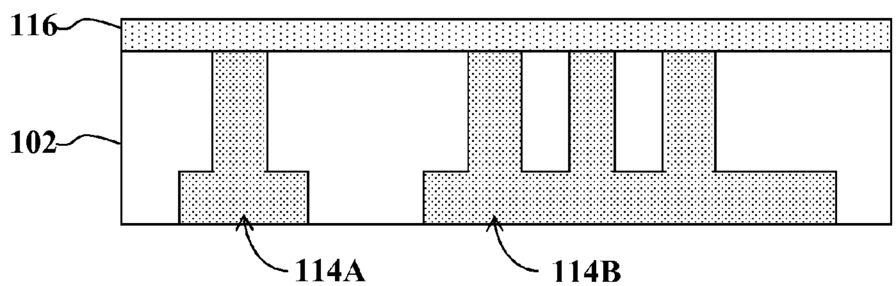

116
102
114A
114B

FIG. 2

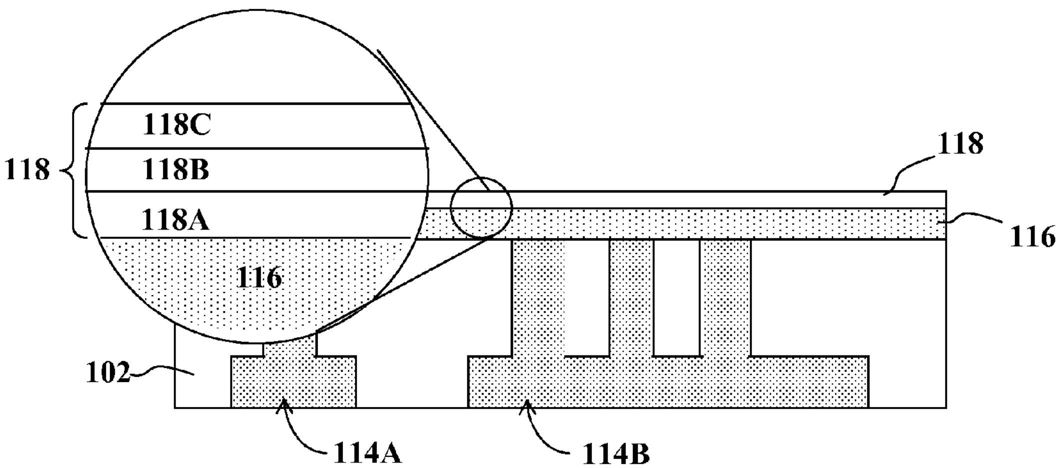


FIG. 3

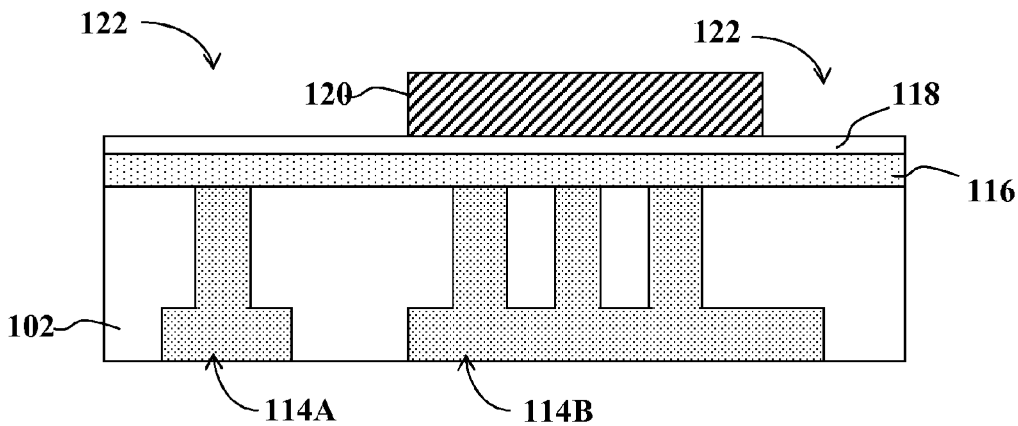


FIG. 4

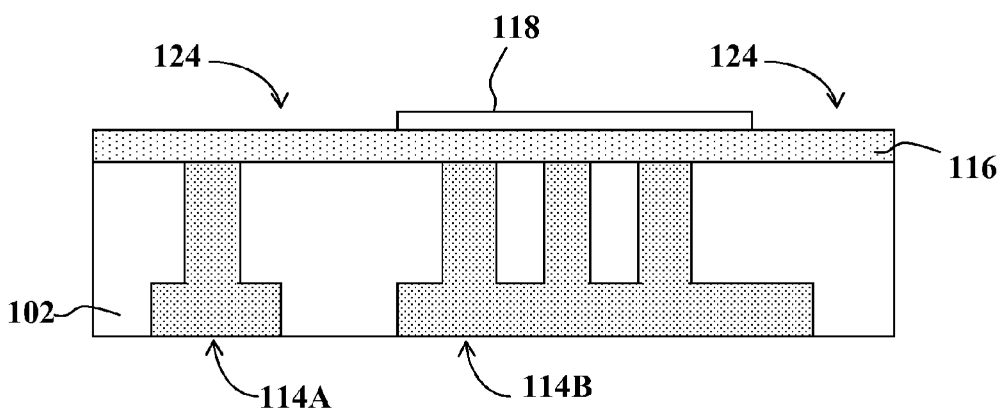


FIG. 5

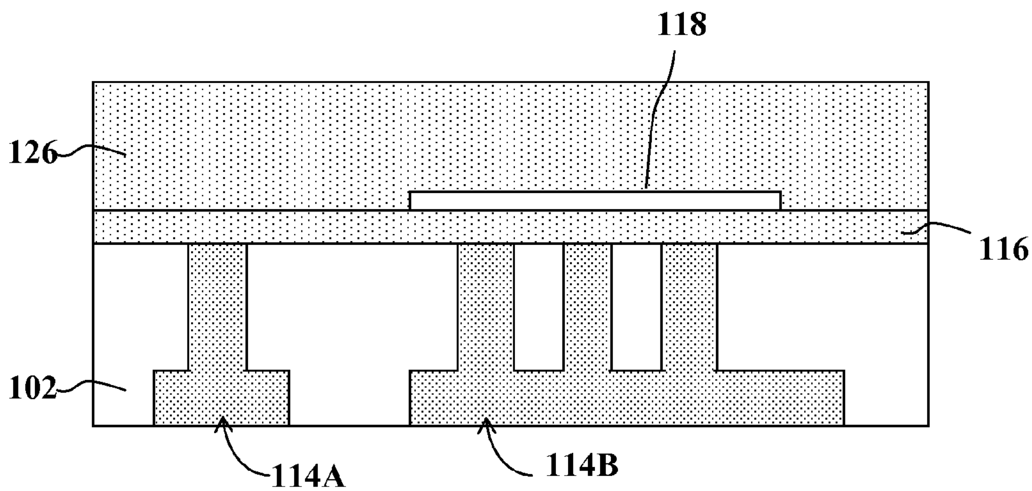


FIG. 6

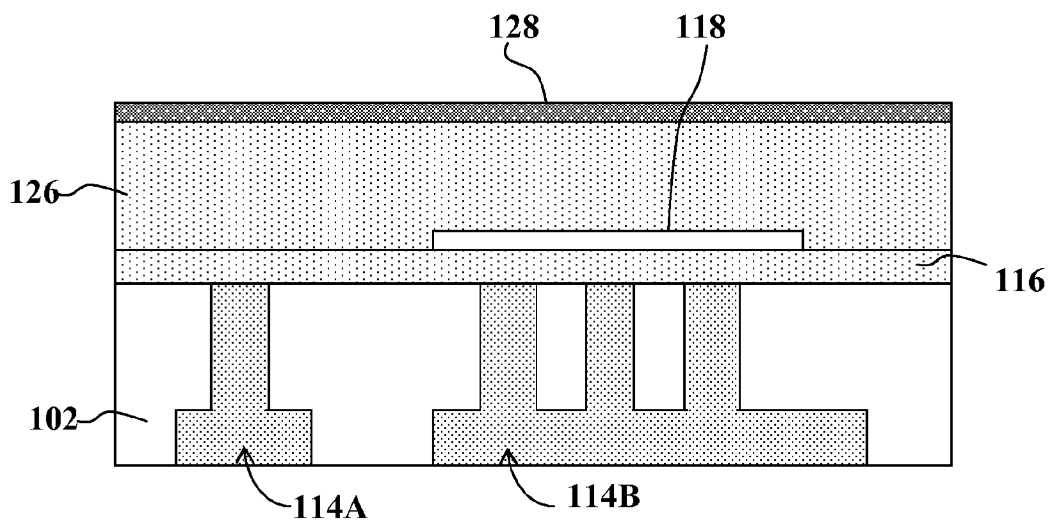


FIG. 7

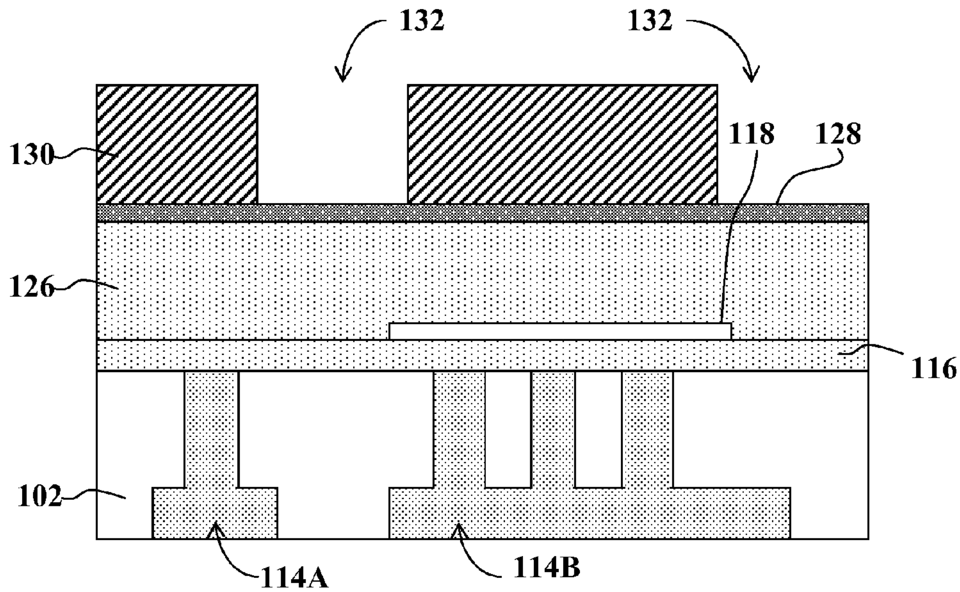

132
132
130
118
128
126
116
102
114A
114B

FIG. 8

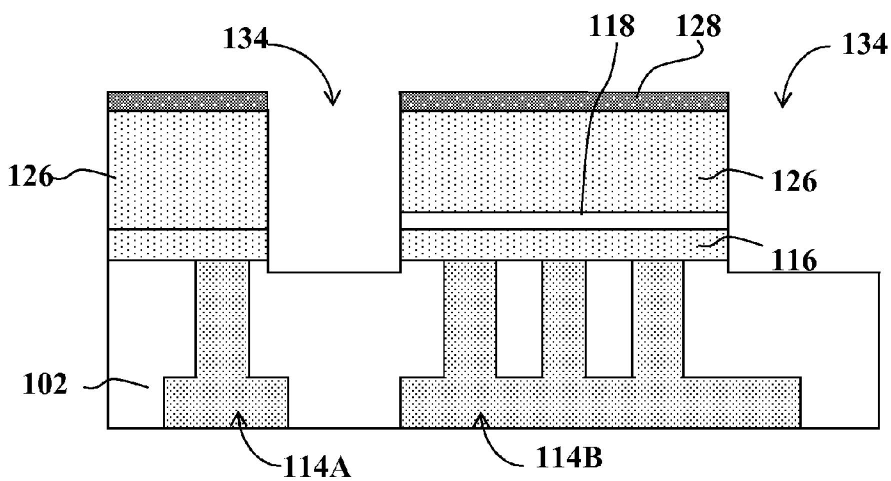

134
118
128
134
126
126
116
102
114A
114B

FIG. 9

METAL-INSULATOR-METAL (MIM) CAPACITOR

[0001] This invention relates to semiconductor structures and manufacturing. More particularly, the invention relates to the formation of metal-insulator-metal (MIM) capacitors.

[0002] MIM capacitors are widely available and are known for state-of-the art BiCMOS processes.

[0003] Currently, a MIM capacitor in a BiCMOS Integrated Circuit (IC) is made using the interconnect metal layer (otherwise referred to as the nth metal layer, MetalN or ME_n (i.e. the uppermost metal layer of n metal layers)) as the bottom plate of the MIM capacitor. The MIM dielectric and the MIM top plate are deposited on top of ME_n layer and patterned using an additional masking step to form the Capacitor Top Metal (CTM) layer. The MIM capacitor is connected with a via which is formed to make contact with both the top plate (i.e. the CTM layer) and the bottom plate (i.e. the ME_n layer).

[0004] A number of problems exist with this MIM capacitor manufacturing method. Firstly, the via etching process reaches the CTM layer much faster than the ME_n layer, thus resulting in over-etching which penetrates the CTM layer. Any roughness of the metal layer underlying the CTM layer can result in etching through the MIM stack, thereby creating a short when the via is formed. Secondly, etching of the CTM may leave residues in grooves (also due to metal roughness), which can result in a short between the CTM layer and the vias connecting the bottom plate.

[0005] According to an aspect of the invention there is provided a MIM capacitor according to independent claim **1**.

[0006] Proposed is method of manufacturing a MIM capacitor for a BiCMOS IC by depositing the MIM stack within the interconnect metal layer. In other words, the sandwich arrangement of metal-insulator-metal layers (i.e. the MIM stack) forming the MIM capacitor is formed below at least part of a top layer/portion of an nth metal layer (ME_n). The interconnect metal layer may thus be adapted to provide an electrical connection to a metal layer of the MIM stack, such as the top metal layer of the MIM for example.

[0007] By avoiding formation of the MIM stack on top of the nth Metal layer (ME_n), the roughness of the nth metal layer (ME_n) is avoided and the maximum roughness experienced when forming the MIM stack is determined by intermetal dielectric (IMD) layer (which is much smoother that the MetalN layer).

[0008] Connection to both terminals of the MIM capacitor may be made using vias formed below the nth Metal layer, which may be formed prior to depositing the MIM stack, and using vias formed on the (thicker) top interconnect metallization layer. Thus, the risk of the via etching process penetrating through the MIM capacitor is eliminated.

[0009] The MIM stack may be patterned in a single masking step, thereby avoiding the formation of residues (which can create shorts circuits).

[0010] Examples of the invention will now be described in detail with reference to the accompanying drawings, in which:

[0011] FIGS. **1-9** illustrate a process for manufacturing a MIM capacitor according to an embodiment of the invention.

[0012] The terms, chip, integrated circuit, monolithic device, semiconductor device, and microelectronic device, are often used interchangeably in this field. The present invention is applicable to all the above as they are generally understood in the field.

[0013] The terms metal line, interconnect line, trace, wire, conductor, signal path and signalling medium are all related. The related terms listed above, are generally interchangeable, and appear in order from specific to general. In this field, metal lines are sometimes referred to as traces, wires, lines, interconnect or simply metal. Metal lines, generally aluminum (Al), copper (Cu) or an alloy of Al and Cu, are conductors that provide signal paths for coupling or interconnecting, electrical circuitry. Conductors other than metal are available in microelectronic devices. Materials such as doped polysilicon, doped single-crystal silicon (often referred to simply as diffusion, regardless of whether such doping is achieved by thermal diffusion or ion implantation), titanium (Ti), molybdenum (Mo), and refractory metals are examples of other conductors.

[0014] The terms contact and via, both refer to structures for electrical connection of conductors at different interconnect levels. These terms are sometimes used in the art to describe both an opening in an insulator in which the structure will be completed, and the completed structure itself. For purposes of this disclosure contact and via refer to the completed structure.

[0015] The term vertical, as used herein, means substantially orthogonal to the surface of a substrate. Also, terms describing positioning or location (such as above, below, top, bottom, etc) are to be construed in conjunction with the orientation of the structures illustrated in the diagrams.

[0016] FIG. **1** illustrates a device **100**, having a substrate **102**, typically comprised of silicon. Substrate **102** can have formed therein a plethora of microelectronic or micromechanical structures, as would be apparent to a person skilled in the semiconductor art. The substrate is provided with Tungsten (W) vias **114** using known IC processing techniques. Any excess Tungsten on the upper or lower surface of the substrate **102** may be removed by Chemical Metal Polishing (CMP), or other known techniques. Thus, FIG. **1** shows first **114**A and second **114**B vias formed in the substrate, and this is the n−1th metal layer (ME_n−1) and n−1th via layer (VIA_n−1).

[0017] An IC front end can be provided below the substrate **102** layers up to and including the n−2th metal layer (ME_n−2) and the n−2th via layer (VIA_n−2).

[0018] Subsequent formation of a first (lower) metal interconnect layer **116** covering the upper surface of the substrate **102** is illustrated in FIG. **2**. The first metal interconnect layer **116** is a standard (i.e. conventional) Ti/TiN/AlCu interconnect layer forming part of the nth metal layer (ME_n). Here, the thickness of the first metal interconnect layer **116** is in the range of 50-150 nm, and so therefore thinner than the total ME_n layer thickness. Other suitable materials and/or thicknesses may be used, as would be apparent to a person skilled in the art.

[0019] A MIM stack **118** is then formed on the first metal interconnect layer **116** as shown in FIG. **3**. Here, the MIM stack **118** is formed from depositing a first 20 nm layer of TiN **118**A on the first metal interconnect layer **116**, then depositing a 40 nm layer of Ta_2O_5 **118**B on the TiN layer **118**A, and finally depositing a second 20 nm layer of TiN **118**C on the Ta_2O_5 layer **118**B. Thus, the first 20 nm layer of TiN **118**A forms the bottom metal layer of the MIM stack **118**, the Ta_2O_5 layer **118**B forms the dielectric layer of the MIM stack **118**, and the second 20 nm layer of TiN **118**C forms the top metal layer of the MIM stack **118**. Other suitable materials and/or thicknesses may be used for the MIM stack **118**, as would be apparent to a person skilled in the art. For example, the thickness of the TiN layers may be in the range of 5-150 nm, preferably in the range of 5-100 nm, and even more preferably in the range of 10-40 nm. Also, the thickness of the Ta_2O_5 layer may be in the range of 5-150 nm, preferably in the range of 10-100 nm, and even more preferably in the range of 30-50 nm.

[0020] As shown in FIG. **4**, a further mask layer **120** (e.g., photoresist or simply "resist") is formed on the top surface of the MIM stack **118** and is patterned according to known photolithographic techniques to form exposed areas **122** (and leave a region of the further mask layer **120** above the second via **114**B). Here, it is preferred that the horizontal dimensions of the further mask layer **120** after being patterned (i.e. the region of the further mask layer **120** above the second via **114**B) are larger than a later-used mask which defines the dimensions of the MIM capacitor (as will be described below in conjunction with FIG. **8**). The further mask layer **120** is also referred to as a patterned masking layer or a second patterned masking layer.

[0021] Spaces **124** in the MIM stack **118** are then chemically etched at the exposed areas **122**, and the further mask layer **120** is then removed, resulting is the structure illustrated in FIG. **5**.

[0022] A second (upper) metal interconnect layer **126** is deposited to cover the upper surface of the first (lower) metal interconnect layer **116** and the MIM stack **118** as illustrated in FIG. **6**. The top metal interconnect layer **126** is formed from ALCu and forms the remaining part of the nth metal layer (ME_n). Here, the thickness of the top metal interconnect layer **126** is in the range of 1-2 μm, but other suitable materials and/or thicknesses may be used, as would be apparent to a person skilled in the art. It will therefore be understood the first (lower) metal interconnect layer **116**, the MIM stack **118**, and the second (upper) metal interconnect layer **126** form the nth metal layer (ME_n), wherein the MIM stack **118** is formed below at least a portion of the second (upper) metal interconnect layer **126** and above the first (lower) metal interconnect layer **116**. In other words, the MIM stack is formed within the nth metal layer (ME_n)

[0023] A TiN Anti-Reflective Coating (ARC) layer **128** is deposited on the top surface of the top metal interconnect layer **126** above the MIM stack as shown in FIG. **7**. The ARC layer **128** is part of the nth metal layer (MEn).

[0024] A final mask layer **130** (e.g., photoresist or simply "resist") is formed on the upper surface of the top metal interconnect layer **126** substrate **102** and the ARC layer **128** to form exposed areas **132** as shown in FIG. **8**. As mentioned above, the horizontal dimensions of the final mask layer **130** above the MIM stack **118** are smaller than the MIM stack **118** and the ARC layer **128**. Thus, when the exposed areas are etched **132**, the final mask layer **130** does not cover (i.e. is not vertically above) portions of the ARC layer **128** and portions of the MIM stack **118**. In this way, the horizontal dimensions of the final masking layer **130** above the MIM stack **118** will define the horizontal dimension of the MIM capacitor after etching.

[0025] Trenches **134** in the substrate **102** are chemically etched (through the ARC layer **128** and the nth metal layer (ME_n)) at the exposed areas **132**, and the final mask layer **130** is then removed using known techniques, resulting is the structure illustrated in FIG. **9**.

[0026] From FIG. **9** it will be seen that a MIM capacitor is formed with an electrical connection to the bottom plate of the MIM capacitor being made with the vias **114**B in the n−1th layer. Thus, unlike a conventional MIM capacitor, a MIM capacitor according to an embodiment of the invention does not require connections in the n+1th metal layer (ME_n+1) and can therefore be significantly smaller and exhibit smaller parasitic capacitances.

[0027] Also, since the bottom plate of the MIM capacitor includes a (low resistive) AlCu layer, a plurality or grid of vias may not be needed which helps to reduce the parasitic capacitance to the substrate **102**.

[0028] Further, the roughness of the thick AlCu top metal interconnect layer **126** is not an issue in embodiments of the invention because the MIM stack **118** forming the MIM capacitor is situated under (i.e. below) the AlCu top metal interconnect layer **126**.

[0029] To improve electro-migration properties, conventional AlCu interconnect metal layers are typically deposited at a higher temperature, in the range of 400-500° C. In this regime, large grains are formed, which helps to reduce electro migration. However, since this also results in increased roughness, when a conventional MIM capacitor is formed on top of a particular interconnect metal layer, this interconnect metal layer needs to be deposited at a lower temperature (typically in the range of 200-300° C.) to reduce the surface roughness. This comes at the cost of worse electro-migration properties.

[0030] Since, in proposed embodiments, the MIM stack is not formed on top, but is instead formed within the interconnect metal layer, the surface roughness on top of the interconnect metal layer is of no concern, and the layer can be deposited at the desired temperature to reach the required electro-migration properties. This means that, unlike a conventional MIM capacitor, cold deposition processes are not needed to ensure MIM integrity in embodiments, thus leading to improved electro-migration properties.

[0031] Embodiments also provide improved MIM reliability through avoidance of early breakdown or leakage that would otherwise be caused by spikes in the bottom plate or residue on the top plate resultant from roughness of the top metal interconnect layer.

[0032] The MIM capacitor is formed from dielectric sandwiched between two metal layers. To have good electrical performance, and especially to be symmetric with respect to positive or negative voltage bias, it is preferable that both interfaces (bottom metal to dielectric, and dielectric to top-metal) are identical. Conventional use of a TiN ARC layer thus results in the bottom interface being TiN to dielectric. Hence, in conventional arrangements, the top interface is also arranged to be dielectric to TiN. However, in proposed embodiments the ARC layer is no longer used as a bottom plate, therefore providing i) more freedom, and ii) the ARC is of no particular interest for the MIM (although it has been described in the embodiment of FIGS. **1-9** simply for regular interconnect processing).

[0033] Unlike conventional manufacturing processes which require two patterned masking layers to define the horizontal dimensions of the MIM capacitor, embodiments of the invention may only needs a single patterned masking layer (e.g. the final masking layer **130** shown in FIG. **8**) to define the horizontal dimension of the MIM capacitor.

[0034] Various modifications will be apparent to those skilled in the art.

1. A metal-insulator-metal, MIM, capacitor, comprising:
a MIM stack formed within an interconnect metal layer, wherein the interconnect metal layer is adapted to provide an electrical connection to a metal layer of the MIM stack.

2. The MIM capacitor of claim 1, wherein the interconnect metal layer is an Nth metal layer for a BiCMOS process having an N+1th interconnect metal layer.

3. The MIM capacitor of claim 1, further comprising:
a first metal layer formed on a substrate, wherein the MIM stack is formed on the first metal layer;
an opening formed in the substrate that exposes at least one portion of the first metal layer below a region of the MIM stack; and
a via metal layer formed in the opening of the substrate so as to form a via connecting to the first metal layer,
wherein the at least part of interconnect metal layer is formed on the MIM stack.

4. The MIM capacitor of claim 1 further comprising an anti-reflective coating layer formed on the interconnect metal layer, wherein the anti-reflective coating layer comprises titanium or titanium alloy.

5. The MIM capacitor of claim 1, wherein the interconnect metal layer comprises aluminum, aluminum alloy, copper, or copper alloy.

6. The MIM capacitor of claim 1, wherein at least one of the metal layers of the MIM stack comprises titanium or titanium alloy, and wherein the insulator layer of the MIM stack comprises a metal oxide or silicon nitride.

7. A method manufacturing a metal-insulator-metal, MIM, capacitor, comprising:
forming a MIM stack within an interconnect metal layer, wherein the interconnect metal layer forms an electrical connection to a metal layer of the MIM stack.

8. The method of claim 7, wherein the interconnect metal layer is an Nth metal layer for a BiCMOS process having an N+1th interconnect metal layer.

9. The method of claim 7, further comprising:
forming an opening in a substrate;
forming a via metal layer in the opening of the substrate so as to form a via in the substrate;
forming a first metal layer on the substrate;
forming the MIM stack on the first metal layer; and
forming at least part of the interconnect metal layer on the MIM stack.

10. The method of claim 7, further comprising forming an anti-reflective coating layer on the interconnect metal layer, wherein the anti-reflective coating layer comprises titanium or titanium alloy.

11. The method of claim 7, wherein the interconnect metal layer comprises aluminum, aluminum alloy, copper, or copper alloy.

12. The method of claim 7, wherein at least one of the metal layers of the MIM stack comprises titanium or titanium alloy, and wherein the insulator layer of the MIM stack comprises a metal oxide or silicon nitride.

13. The method of claim 7, further comprising:
forming a mask layer on the interconnect metal layer;
patterning the mask layer to expose at least one region of the interconnect layer and to retain at least one portion of the mask layer above the MIM stack; and
etching the exposed at least one region through the interconnect metal layer and the first metal layer to form at least one trench in the substrate.

14. The method of claim 13, wherein a horizontal dimension of the at least a portion of the mask layer above the MIM stack is less than the corresponding horizontal dimension of the MIM stack, such that the step of etching comprises etching through the MIM stack.

15. A BiCMOS integrated circuit comprising a MIM capacitor according to claim 1.

* * * * *