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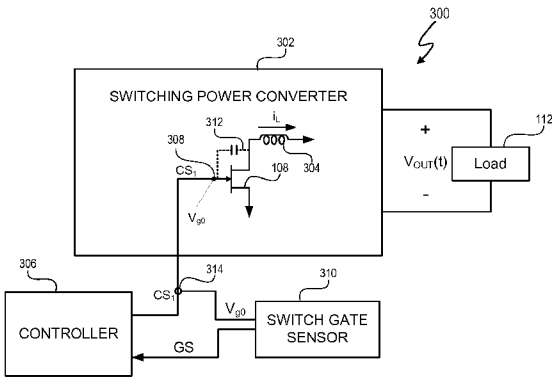

Figure 3

(57) **Abstract:** A method and system (300) monitor gate charge characteristics of one or more field effect transistors (108) in a switching power converter (302) to detect an end of an inductor flyback time interval. The switching power converter (302) includes a switch (108) coupled to an inductor (304) to control current flow (IL) in the inductor (304). When the switch (108) turns OFF, a collapsing magnetic field causes the inductor current (IL) to decrease and the inductor voltage to reverse polarity. When the magnetic field completely collapses, the inductor current (IL) goes to zero. At the end of the inductor flyback time interval, a voltage is induced across a Miller capacitance (312) of the switch (108). The voltage can be detected as a transient change in the gate voltage (Vgo) of the switch (108). A switch gate sensor (310) detects the gate voltage change associated with the end of the inductor flyback time interval and provides a signal (GS) indicating an end of the inductor flyback time interval.

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SYSTEM AND METHOD WITH INDUCTOR FLYBACK DETECTION USING SWITCH GATE CHARGE CHARACTERISTIC DETECTION

John L. Melanson

Cross-reference to Related Application

(1) This application claims the benefit under 35 U.S.C. § 119(e) and 37 C.F.R. § 1.78 of U.S. Provisional Application No. 60/915,547, filed May 2, 2007, and entitled "Power Factor Correction (PFC) Controller Apparatuses and Methods," and is incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

(2) The present invention relates in general to the field of signal processing, and, more specifically, to a system and method with inductor flyback detection using switch gate charge characteristic detection.

DESCRIPTION OF THE RELATED ART

(3) Switching power converters, such as switching power supplies, switch mode converters, switch mode transformers, and switching amplifiers, control power output using one or more switches. Often the switching power converters include inductors. The inductors are initially charged with an inductor current that induces a magnetic field in the inductor and a voltage across the inductor. The voltage across the inductor opposes the inductor current. When the inductor current is interrupted, for example, by opening a switch, a magnetic field created by the inductor current begins to collapse. The collapsing magnetic field causes the inductor current to ramp-down, and the inductor voltage reverses. The reversed inductor voltage is commonly referred to as a "flyback" voltage. The time during which the inductor current begins ramping down until it stops decreasing is referred to as the inductor flyback time interval. The switching power converter operates in discontinuous current mode if the switching power converter allows the induced magnetic field to completely collapse and, thus, allows the inductor current to reach zero (0) amps. The switching power converter operates in continuous current mode if the

switching power converter begins increasing the inductor current before the induced magnetic field completely collapses.

(4) Figure 1 depicts a power control system 100 that utilizes an inductor 110. The inductor 110 generates an inductor current when switch 108 is nonconductive, i.e. is "OFF". The power control system 100 includes a switching power converter 102. The switching power converter 102 performs power factor correction and provides regulated voltage power to load 112. Voltage source 101 supplies an alternating current (AC) input voltage $V_{in}(t)$ to a full, diode bridge rectifier 103. The voltage source 101 is, for example, a public utility, and the AC voltage $V_{in}(t)$ is, for example, a 60 Hz/110 V line voltage in the United States or a 50 Hz/220 V line voltage in Europe. The rectifier 103 rectifies the input voltage $V_{in}(t)$ and supplies a rectified, time-varying, line input voltage $V_x(t)$ to the switching power converter 102.

(5) The switch 108 of switching power converter 102 regulates the transfer of energy from the line input voltage $V_x(t)$, through inductor 110, to capacitor 106. The inductor current i_L ramps 'up' (i.e. increases) when the switch 108 conducts, i.e. is "ON". Switch 108 is a field effect transistor (FET). Switch 108 is depicted as an n-channel device but can also be a p-channel device. The inductor current i_L ramps down when switch 108 is OFF, and supplies inductor current i_L to recharge capacitor 106. In at least one embodiment, the switching power converter 102 operates in discontinuous current mode, i.e. the inductor current i_L ramp up time plus the inductor flyback time interval is less than the period of switch 108. Capacitor 106 supplies stored energy to load 112 while the switch 108 conducts. The capacitor 106 is sufficiently large so as to maintain a substantially constant output voltage $V_c(t)$, as established by a power factor correction (PFC) and output voltage controller 114 (as discussed in more detail below). The output voltage $V_c(t)$ remains substantially constant during constant load conditions. However, as load conditions change, the output voltage $V_c(t)$ changes. The PFC and output voltage controller 114 responds to the changes in $V_c(t)$ and adjusts the control signal CS_0 to maintain a substantially constant output voltage as quickly as possible. The PFC and output voltage controller 114 includes a small capacitor 115 to filter any high frequency signals from the line input voltage $V_x(t)$.

(6) The power control system 100 also includes a PFC and output voltage controller 114 to control the switch 108 and, thus control power factor correction and regulate output power of the switching power converter 102. The goal of power factor correction technology is to make the switching power converter 102 appear resistive to the voltage source 101. Thus, the PFC and

output voltage controller 114 attempts to control the inductor current i_L so that the average inductor current i_L is linearly and directly related to the line input voltage $V_x(t)$. Prodić, *Compensator Design and Stability Assessment for Fast Voltage Loops of Power Factor Correction Rectifiers*, IEEE Transactions on Power Electronics, Vol. 22, No. 5, Sept. 2007, pp. 1719-1729 (referred to herein as "Prodić"), describes an example of PFC and output voltage controller 114. The PFC and output voltage controller 114 supplies a pulse width modified (PWM) control signal CS_0 to control the conductivity of switch 108. In at least one embodiment, switch 108 is a field effect transistor (FET), and control signal CS_0 is the gate voltage of switch 108. The values of the pulse width and duty cycle of control signal CS_o depend on two feedback signals, namely, the line input voltage $V_x(t)$ and the capacitor voltage/output voltage $V_c(t)$.

(7) PFC and outpuat voltage controller 114 receives two feedback signals, the line input voltage $V_x(t)$ and the output voltage $V_c(t)$, via a wide bandwidth current loop 116 and a slower voltage loop 118. The current loop 116 operates at a frequency f_c that is sufficient to allow the PFC and output controller 114 to respond to changes in the line input voltage $V_x(t)$ and cause the inductor current i_L to track the line input voltage to provide power factor correction. The current loop frequency is generally set to a value between 20 kHz and 150 kHz. The voltage loop 118 operates at a much slower frequency f_v, typically 10-20 Hz. The capacitor voltage $V_c(t)$ includes a ripple component having a frequency equal to twice the frequency of input voltage $V_{in}(t)$, e.g. 120 Hz. Thus, by operating at 10-20 Hz, the voltage loop 118 functions as a low pass filter to filter the ripple component.

(8) Figure 2 depicts a class D amplifier 200, which represents another embodiment of a switching power converter. The class D amplifier 200 includes a controller 202 to generate respective control signals CS_0 and CS_1. Switches 208 and 210 are n-channel FETs but can also be p-channel devices. Control signals CS_0 and CS_1 charge and discharge the respective gates 204 and 206 of switches 208 and 210. When control signals CS_0 and CS_1 charge the respective gates 204 and 206, the respective gate voltages V_{g0} and V_{g1} increase and cause switches 208 and 210 to turn ON. When control signals CS_0 and CS_1 discharge respective gates 204 and 206, the respective gate voltages V_{g0} and V_{g1} decrease and cause switches 208 and 210 to turn OFF. Control signals CS_0 and CS_1 control switches 208 and 210 in a 'non-overlapping' manner so that switches 208 and 210 are not ON at the same time.

(9) When switch 208 turns ON and switch 210 is OFF, an inductor current is supplied by voltage source V+ and generates a magnetic field in the inductor 212. The magnetic field

induces a voltage across the inductor that opposes the inductor current. When switch 208 turns OFF and switch 210 turns ON, an inductor current is supplied by voltage source V-. The inductor current induces a reverse voltage across the inductor 212. Capacitor 214 provides a low pass filtering function and stabilizes the output voltage V_{out}. The class D amplifier 200 provides power to load 216, such as one or more audio speakers.

(10) Detecting a time at which the inductor flyback time ends ("inductor flyback end time") can be useful, for example, to control switch timing and ensuring a device operates in continuous current mode or discontinuous current mode. However, detection of the inductor flyback end time can be difficult and/or costly.

SUMMARY OF THE INVENTION

(11) In one embodiment of the present invention, an apparatus to detect an end of an inductor flyback time interval of a switching power converter, wherein the switching power converter includes an inductor to couple to an input voltage node and a field effect transistor (FET) switch coupled to the inductor, includes a switch gate sensor to couple to a gate of the switch, wherein during operation of the switch gate sensor. The switch gate sensor is configured to detect a charge characteristic on a gate of the switch associated with an end of the inductor flyback time interval and generate a switch gate sensor signal indicating an end of the inductor flyback time interval.

(12) In another embodiment of the present invention, a method to detect an end of an inductor flyback time interval of a switching power converter, wherein the switching power converter includes an inductor to couple to an input voltage node and a field effect transistor (FET) switch coupled to the inductor, includes detecting a charge characteristic on a gate of the switch associated with an end of the inductor flyback time interval. The method further includes generating a switch gate sensor signal indicating an end of the inductor flyback time interval.

(13) In a further embodiment of the present invention, an apparatus to detect an end of an inductor flyback time interval of a switching power converter, wherein the switching power converter includes an inductor to couple to an input voltage node and a field effect transistor (FET) switch coupled to the inductor, includes means for detecting a charge characteristic on a gate of the switch associated with an end of the inductor flyback time interval. The apparatus further includes means, coupled to the means for detecting, for generating a switch gate sensor signal indicating an end of the inductor flyback time interval.

BRIEF DESCRIPTION OF THE DRAWINGS

(14) The present invention may be better understood, and its numerous objects, features and advantages made apparent to those skilled in the art by referencing the accompanying drawings. The use of the same reference number throughout the several figures designates a like or similar element.

(15) Figure 1 (labeled prior art) depicts a power control system with power factor correction and output voltage regulation.

(16) Figure 2 (labeled prior art) depicts a class D amplifier.

(17) Figure 3 depicts a switching power converter with a switch gate sensor.

(18) Figure 4 depicts a power control system with a switching power converter and a switch gate sensor.

(19) Figure 5 depicts a time domain graph of a voltage feedback signal, an inductor current i_L, and corresponding states of a switching power converter switch.

(20) Figure 6 depicts a graph of a feedback signal and corresponding ideal and actual gate voltages and actual currents of a switching power converter switch.

(21) Figure 7 depicts a switch gate sensor for a switching power converter.

(22) Figure 8 depicts a class D amplifier with a switch gate sensor.

DETAILED DESCRIPTION

(23) A method and system monitor gate charge characteristics of one or more field effect transistors in a switching power converter to detect an end of an inductor flyback time interval. The switching power converter includes a switch coupled directly or indirectly to an inductor. The conductive state of the switch controls current flow in the inductor. When the switch turns OFF, i.e. is nonconductive, a collapsing magnetic field causes the inductor current to decrease and the inductor voltage to reverse polarity. When the magnetic field completely collapses, the inductor current goes to zero. A parasitic "Miller" capacitance exists between a gate and source of the switch. At the end of the inductor flyback time interval, a voltage is induced across the Miller capacitance, and the voltage can be detected as a transient change in the gate voltage of the switch. A switch gate sensor detects the gate voltage change associated with the end of the inductor flyback time interval and provides a signal indicating an end of the inductor flyback

time interval. The end of the inductor flyback time interval can be used to, for example, detect an input voltage, an output voltage, or both from a switching power converter, which can in turn be used to determine a control signal to control the switching power converter. In at least one embodiment, detecting the inductor flyback end time from the gate voltage can reduce terminal counts in PFC and output voltage controllers or permit reallocation of terminals.

(24) Figure 3 depicts a power control system 300. The power control system 300 includes a switching power converter 302. The switching power converter 302 can be any switching power converter 302, such as a switching power supply, a switch mode converter, a switch mode transformer, or a switching amplifier. The switching power converter 302 includes a switch 108 to control the inductor current i_L. Figure 3 depicts an exemplary connection configuration between switch 108 and inductor 304. The particular connection configuration between switch 108 and inductor 304 is a design choice.

(25) A controller 306 generates a control signal CS_1 that charges and discharges the gate of switch 108. When control signal CS_1 charges gate 308, the gate voltage V_{g0} increases and causes switch 108 to turn ON. When control signal CS_1 discharges gate 308, the gate voltage V_{g0} decreases and causes switch 108 to turn OFF. The conductive state of switch 108 controls the inductor current i_L. In at least one embodiment, when switch 108 conducts, the inductor current i_L creates a magnetic field associated with inductor 304 and induces an inductor voltage that opposes the inductor current i_L. When switch 108 turns OFF, the inductor current decreases as the magnetic field collapses, and the voltage across the inductor concurrently reverses polarity. The time interval during which the inductor current decreases is referred to as the "inductor flyback time interval".

(26) A switch gate sensor 310 detects changes in the charge on gate 308. The changes in the gate 308 charge include, in at least one embodiment, transient charge fluctuations on the gate 308 at the end of the inductor flyback time. The switch 108 has a parasitic gate-to-drain "Miller" capacitance 312 between the gate and source of switch 108. At the end of the inductor flyback time interval, a transient gate charge fluctuation associated with the Miller capacitance 312 occurs on the gate of switch 108. The switch gate sensor 310 includes a probe 314 coupled to the gate of switch 108 to allow the switch gate sensor 310 to detect the charge fluctuations on the switch 108 gate. In at least one embodiment, the gate charge fluctuations can be detected as a change in the gate voltage V_{g0} at the end of the inductor flyback time interval. In at least one embodiment, the gate voltage V_{g0} is at or near a common voltage during the inductor flyback

time interval and decreases below the common voltage at the end of the inductor flyback time interval.

(27) The switch gate sensor 310 generates a switch gate sensor signal GS upon detection of the gate charge fluctuations on the gate of switch 108 and provides the signal GS to the controller 306. The controller 306 receives the gate sensor signal GS and can use the detection of the inductor flyback time interval end as indicated by the gate sensor signal GS to, for example, determine the duration of the inductor flyback time interval and determine when to sample one or more feedback signals (not shown) from the switching power converter to the controller as, for example, discussed in commonly assigned U.S. Patent Application entitled "Power Factor Correction Controller With Feedback Reduction", inventor John L. Melanson, assignee Cirrus Logic, Inc., and attorney docket number 1756-CA ("Melanson I") and U.S. Patent Application entitled "Power Factor Correction Controller With Switch Node Feedback", inventor John L. Melanson, assignee Cirrus Logic, Inc., and attorney docket number 1757-CA ("Melanson II"). Melanson I and Melanson II are incorporated herein by reference in their entireties.

(28) In at least one embodiment, the switch gate sensor 310 is incorporated within an integrated circuit with the controller 306. By incorporating the switch gate sensor 310 in the same integrated circuit, one or more additional pins that would otherwise be used to detect the end of the inductor flyback interval can be eliminated or reallocated. In at least one embodiment, additional switch gate sensors are included in power control system 300 to detect additional gate charge fluctuations associated with other switches.

(29) Figure 4 depicts power control system 400 having a power factor correction (PFC) and output voltage controller 404 to control power factor correction and output voltage regulation of the switching power converter 102. Power control system 400 includes switch gate sensor 310 to detect charge fluctuations on the gate of switch 108. The switch gate sensor 310 provides the switch gate sensor signal GS to PFC and output voltage controller 404. In at least some embodiments, the PFC and output voltage controller 404 represents an embodiment of the PFC and output voltage controllers described in Melanson I and Melanson II, and PFC and output voltage controller 404 utilizes the switch gate sensor signal GS and the feedback signal(s) V_{FB} to generate the control signal CS_1. The PFC and output voltage controller 404 can utilize a programmable pulse width and period control processor. An exemplary programmable pulse width and period control processor is described in U.S. Patent Application entitled

"Programmable Power Control System", inventor John L. Melanson, assignee Cirrus Logic, Inc., and attorney docket number 1759-CA, which is incorporated herein by reference in its entirety.

(30) Referring to Figures 4 and 5, Figure 5 provides an exemplary depiction of inductor flyback time intervals in the context of the voltage $V_S(t)$ at the SWITCH NODE of switching power converter 102 and the inductor current i_L. More specifically, Figure 5 depicts time domain graphs 500 of (i) the voltage feedback signal $V_S(t)$ from the SWITCH NODE (graph 502), (ii) inductor current i_L (graph 504), and (iii) corresponding states of switch 108 (graph 506). Referring to Figures 4 and 5, the state of switch 108 is controlled by control signal CS_1. Control signal CS_1 has a frequency equal to $1/TT_x$, where TT_x is the period of control signal CS_1 for the x^{th} frame, and "x" is an integer marker. The frequency f_{CS1} of control signal CS_1 can be controlled by PFC and output voltage controller 404. In at least one embodiment, PFC and output voltage controller 404 varies the frequency f_{CS1} to provide a regulated output voltage $V_c(t)$ and in accordance with a predetermined spread spectrum strategy to, for example, reduce electromagnetic interference emissions. The frequency of control signal CS_1 is preferably between 20 kHz and 150 kHz, which respectively avoids audio frequencies and inefficient switching frequencies.

(31) During an inductor current i_L ramp-up time interval T1, i.e. when switch 108 is "ON" (i.e. conducts), the inductor current i_L ramps up and the voltage $V_S(t)$ at the SWITCH NODE decreases to at least approximately 0. (The terms "at least approximately" include an exact value and an approximate value). In at least one embodiment, the voltage $V_S(t)$ decreases to approximately 0 because small, non-ideal voltage drops can occur, such as a voltage drop across switch 108 when switch 108 is conducting or a voltage drop across diode 111, so that the voltage of feedback signal $V_S(t)$ differs from, for example, line input voltage $V_x(t)$ or output voltage $V_c(t)$ by such non-ideal voltage drops. However, unless otherwise indicated, for purposes of this application determining or obtaining a line input voltage $V_x(t)$ and/or an output voltage $V_S(t)$ of switching power converter 102 includes determining or obtaining an approximate or scaled line input voltage and/or an approximate or scaled output voltage of switching power converter 102.

(32) During inductor flyback time interval T2 when switch 108 is "OFF" (i.e. nonconductive), diode 111 conducts, the inductor current i_L ramps down to zero (0) amps, and the voltage $V_S(t)$ increases to $V_c(t)$. After the inductor current i_L ramps down to zero (0) amps, diode 111 stops conducting, the voltage drop across inductor 110 is approximately zero, and the voltage of feedback signal $V_S(t)$ equals $V_x(t)$. When the inductor current i_L reaches zero, parasitic

impedances, such as the parasitic capacitance across inductor 110, cause a decaying ripple 508 at the SWITCH NODE.

(33) Power control system 400 determines the end of inductor flyback time interval T2 by monitoring the gate charge characteristics of switch 108 to detect the end of inductor flyback time interval T2. Figure 6 depicts a graph 600 of feedback signal $V_S(t)$ and corresponding ideal and actual gate voltages V_g and actual gate currents i_g. Referring to Figures 4 and 6, ideally during each period of control signal CS_1, the gate voltage V_g has a logical HIGH pulse 602 corresponding to the switch 108 ON time and is otherwise a logical LOW. Likewise, ideally during each period of control signal CS_1, the gate current i_g has a brief pulse 604 to charge the gate of switch 108 and has a brief pulse 606 to discharge the gate of switch 108. Ideally, pulses 604 and 606 are the only pulses of the gate current i_g.

(34) The parasitic Miller capacitance 312 causes transient voltage signals 608 and transient current signals 610 at the gate of switch 108 when the feedback signal $V_S(t)$ at the SWITCH NODE transitions from voltage $V_c(t)$ to voltage $V_x(t)$ at the end of the inductor flyback time interval T2. (The transient signals are not necessarily drawn to scale in Figure 6, and the magnitudes of the transient signals will vary depending upon the components used to implement switching power converter 102.) The transient voltage and current signals each represent embodiments of transient charge fluctuations 612 that are detected by switch gate sensor 310. Upon detection of the transient charge fluctuations, PFC and output voltage controller 404 can determine the inductor flyback time interval T2 by determining the beginning of inductor flyback time interval T2 and determining the elapsed time until the transient signal(s) are detected as described in Melanson I and Melanson II.

(35) Figure 7 depicts switch gate sensor 700, which represents one embodiment of switch gate sensor 310. The switch gate sensor 700 detects the gate voltage V_g, and comparator 702 compares the gate voltage with a reference voltage V_{REF1}. The reference voltage V_{REF1} is predetermined and set between the steady state gate voltage V_g during the inductor flyback time interval T2 and the minimum voltage of the transient 608. In at least one embodiment, V_{REF1} is set at -0.5 V. When the feedback signal $V_S(t)$ transitions from voltage $V_c(t)$ to voltage $V_x(t)$, the gate voltage V_g transient 608 decreases below the reference voltage V_{REF1}, and the output signal V_{SENSE_1} of comparator 702 changes from a logical HIGH to a logical LOW. The transition of the comparator output signal V_{SENSE_1} of comparator 702 from logical HIGH to logical LOW indicates an end of the inductor flyback time interval T2.

(36) Figure 8 depicts an embodiment of a class D amplifier 800. The amplifier 800 represents one embodiment of a class D switching power converter. Amplifier 800 is identical to amplifier 200 except amplifier 800 includes switch gate sensor 802. Switch gate sensor 802 is identical to switch gate sensor 310, except switch gate sensor 802 detects charge fluctuations on the gates of switch 208 and switch 210. In at least one embodiment, switch gate sensor 802 incorporates duel implementations of switch gate sensor 700 to generate respective switch gate sensor signals GS_0 and GS_1. Switch gate sensor signals GS_0 and GS_1 represent detection of the charge fluctuations on respective gates 204 and 206 and can, thus, detect when switches 208 and 210 are conductive and non-conductive. In at least one embodiment, controller 202 operates switches 208 and 210 with non-overlapping conduction cycles to prevent switches 208 and 210 from conducting at the same time and, thus, creating a low impedance path between voltage sources V+ and V-. Thus, controller 202 turns switch 208 OFF before turning switch 210 ON and vice versa.

(37) The interim time when switches 208 and 210 are both OFF can create distortion in the output voltage V_{out}. To minimize the distortion, in at least one embodiment, controller 202 minimizes the time when both switches 208 and 210 are OFF. Detecting the charge fluctuations on the respective gates 204 and 206 of switches 208 and 210 allows controller 202 to detect when switch 208 is non-conductive and immediately turn ON switch 210 and vice versa. Thus, detecting the charge fluctuations on the respective gates 204 and 206 of switches 208 and 210 allows controller 202 to operate switches 208 and 210 with non-overlapping conduction cycles with a minimal amount of time when both switches 208 and 210 are non-conductive, thus, minimizing distortion.

(38) Thus, a method and system detect charge fluctuations on a gate of a switch in a switching power converter. The detected charge fluctuations indicate an end of a inductor flyback time interval and, in at least one embodiment, can be used in the process of generating a switching power converter control signal.

(39) Although the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made hereto without departing from the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. An apparatus to detect an end of an inductor flyback time interval of a switching power converter, wherein the switching power converter includes an inductor to couple to an input voltage node and a field effect transistor (FET) switch coupled to the inductor, the apparatus comprising:

a switch gate sensor to couple to a gate of the switch, wherein during operation of the switch gate sensor, the switch gate sensor is configured to:

detect a charge characteristic on a gate of the switch associated with an end of the inductor flyback time interval; and

generate a switch gate sensor signal indicating an end of the inductor flyback time interval.

2. The apparatus of claim 1 wherein the charge characteristic associated with an end of the inductor flyback time interval comprises a gate voltage fluctuation on the gate of the switch.

3. The apparatus of claim 2 wherein the switch gate sensor comprises:

a comparator having a first input terminal to couple to the gate of the switch and a second input terminal to couple to a reference voltage, wherein the comparator is configured to generate the switch gate sensor signal when a comparison of the gate voltage to the reference voltage by the comparator indicates the end of the inductor flyback time interval.

4. The apparatus of claim 3 wherein the comparator is configured to generate the switch gate sensor signal when the comparison of the gate voltage to the reference voltage indicates the gate voltage is less than the reference voltage.

5. The apparatus of claim 1 wherein the switch gate sensor is further configured to provide the switch gate sensor signal to a power factor correction and output voltage controller.

6. The apparatus of claim 1 wherein the switching power converter is a member of a group consisting of: switching power supplies, switch mode converters, switch mode transformers, and switching amplifiers.

7. The apparatus of claim 1 further comprising a PFC and output voltage controller coupled to the switch gate sensor to receive the switch gate sensor signal.

8. A method to detect an end of an inductor flyback time interval of a switching power converter, wherein the switching power converter includes an inductor to couple to an input voltage node and a field effect transistor (FET) switch coupled to the inductor, the method comprising:

detecting a charge characteristic on a gate of the switch associated with an end of the inductor flyback time interval; and

generating a switch gate sensor signal indicating an end of the inductor flyback time interval.

9. The method of claim 8 wherein detecting a charge characteristic on a gate of the switch associated with an end of the inductor flyback time interval comprises detecting a gate voltage fluctuation on the gate of the switch.

10. The method of claim 8 wherein generating a switch gate sensor signal indicating an end of the inductor flyback time interval comprises:

comparing a gate voltage of the switch to a reference voltage; and

generating the switch gate sensor signal indicating the end of the inductor flyback time interval when the comparison of the gate voltage to the reference voltage indicates the end of the inductor flyback time interval.

11. The method of claim 10 wherein generating the switch gate sensor signal further comprises:

generating the switch gate sensor signal when the comparison of the gate voltage to the reference voltage indicates the gate voltage is less than the reference voltage.

12. The method of claim 8 further comprising:
providing the switch gate sensor signal to a power factor correction and output voltage controller.

13. The method of claim 8 further comprising:
maintaining a voltage on the gate of the switch during the inductor flyback time interval that prevents the switch from conducting.

14. The method of claim 8 wherein the switching power converter is a member of a group consisting of: switching power supplies, switch mode converters, switch mode transformers, and switching amplifiers.

15. An apparatus to detect an end of an inductor flyback time interval of a switching power converter, wherein the switching power converter includes an inductor to couple to an input voltage node and a field effect transistor (FET) switch coupled to the inductor, the apparatus comprising:
means for detecting a charge characteristic on a gate of the switch associated with an end of the inductor flyback time interval; and
means, coupled to the means for detecting, for generating a switch gate sensor signal indicating an end of the inductor flyback time interval.

16. The apparatus of claim 15 wherein the charge characteristic associated with an end of the inductor flyback time interval comprises a gate voltage fluctuation on the gate of the switch.

17. The apparatus of claim 15 wherein the means for generating comprises:
means for comparing a gate voltage of the switch to a reference voltage; and
means, coupled to the means for comparing, for generating the switch gate sensor signal indicating the end of the inductor flyback time interval when the comparison of the gate voltage to the reference voltage indicates the end of the inductor flyback time interval.

18. The apparatus of claim 17 wherein means for generating the switch gate sensor signal further comprises means for generating the switch gate sensor signal when the comparison of the gate voltage to the reference voltage indicates gate voltage is less than the reference voltage.

19. The apparatus of claim 15 further comprising:

means, coupled to the means for generating, for providing the switch gate sensor signal to a power factor correction and output voltage controller.

20. The apparatus of claim 15 further comprising:

means for maintaining a voltage on the gate of the switch during the inductor flyback time interval that prevents the switch from conducting.

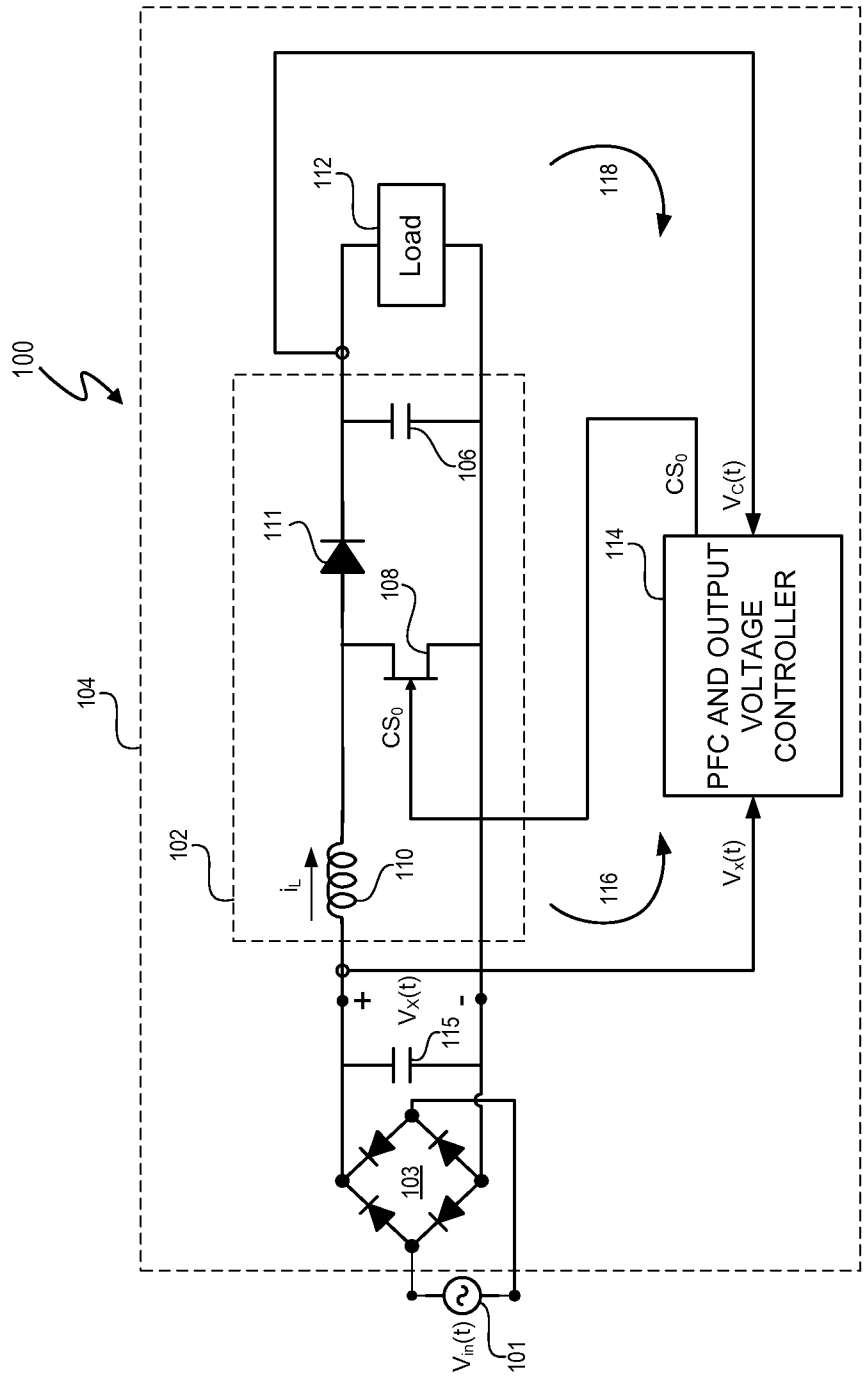

Figure 1 (prior art)

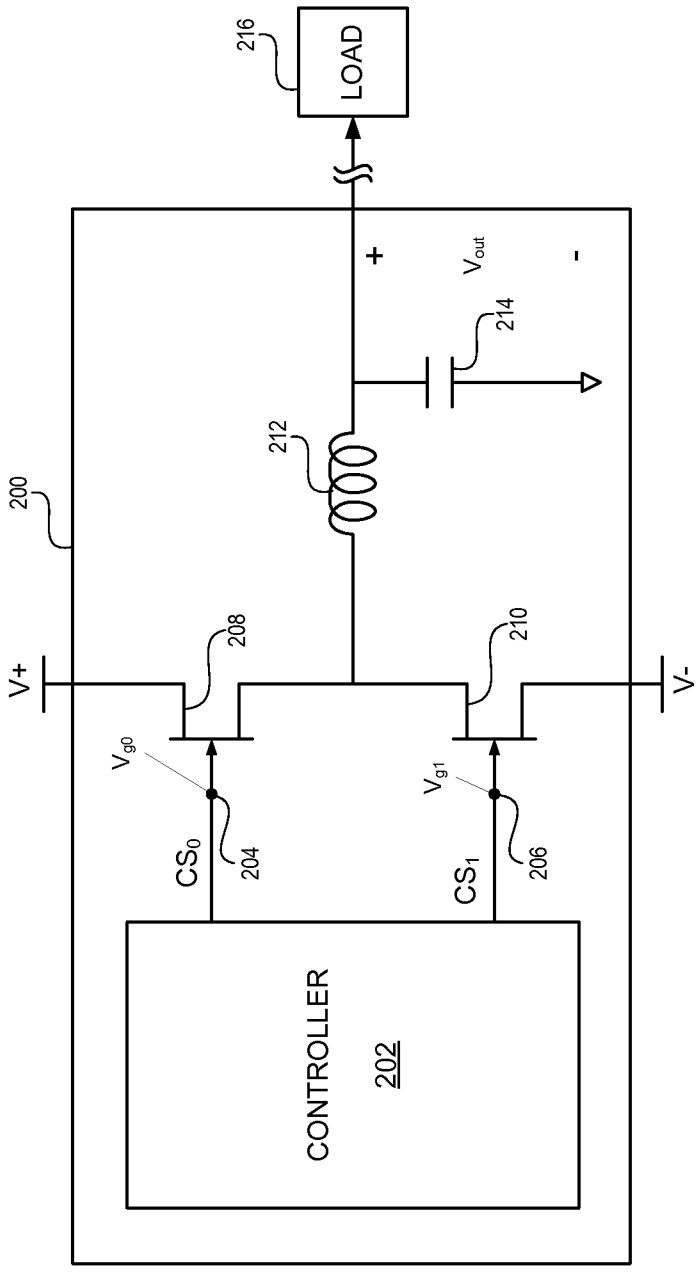

Figure 2 (prior art)

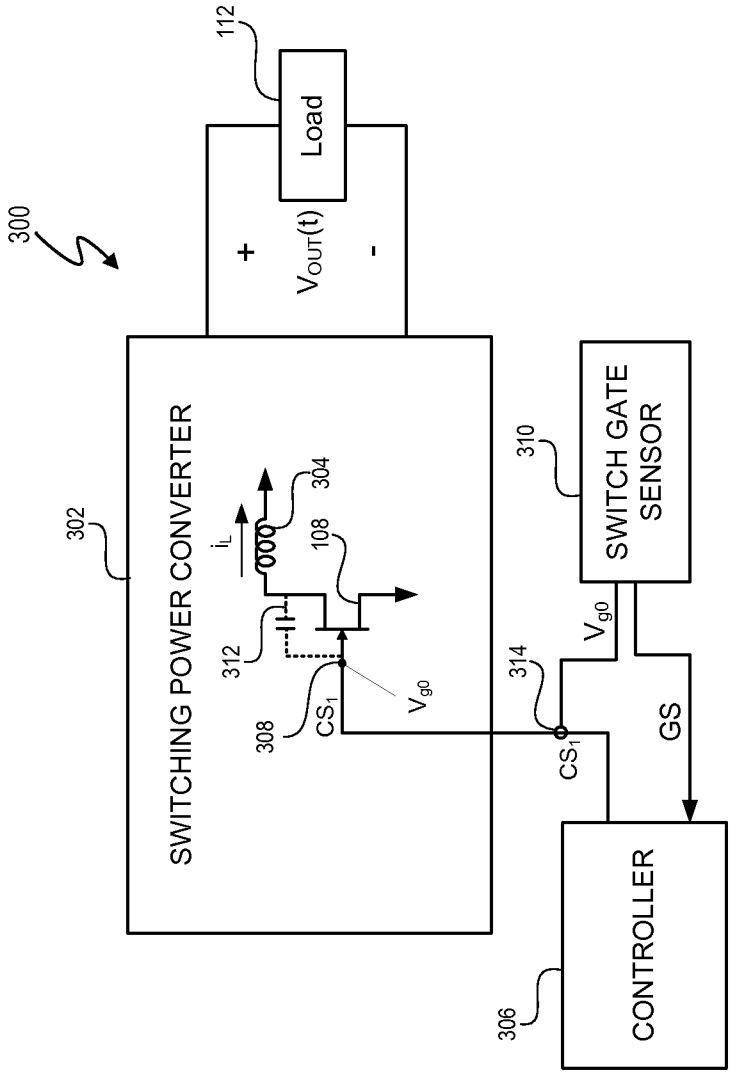
300
112
Load
+
$V_{OUT}(t)$
-
SWITCHING POWER CONVERTER
302
i_L
304
108
312
308
CS_1
V_{g0}
310
SWITCH GATE SENSOR
V_{g0}
314
CS_1
GS
CONTROLLER
306

Figure 3

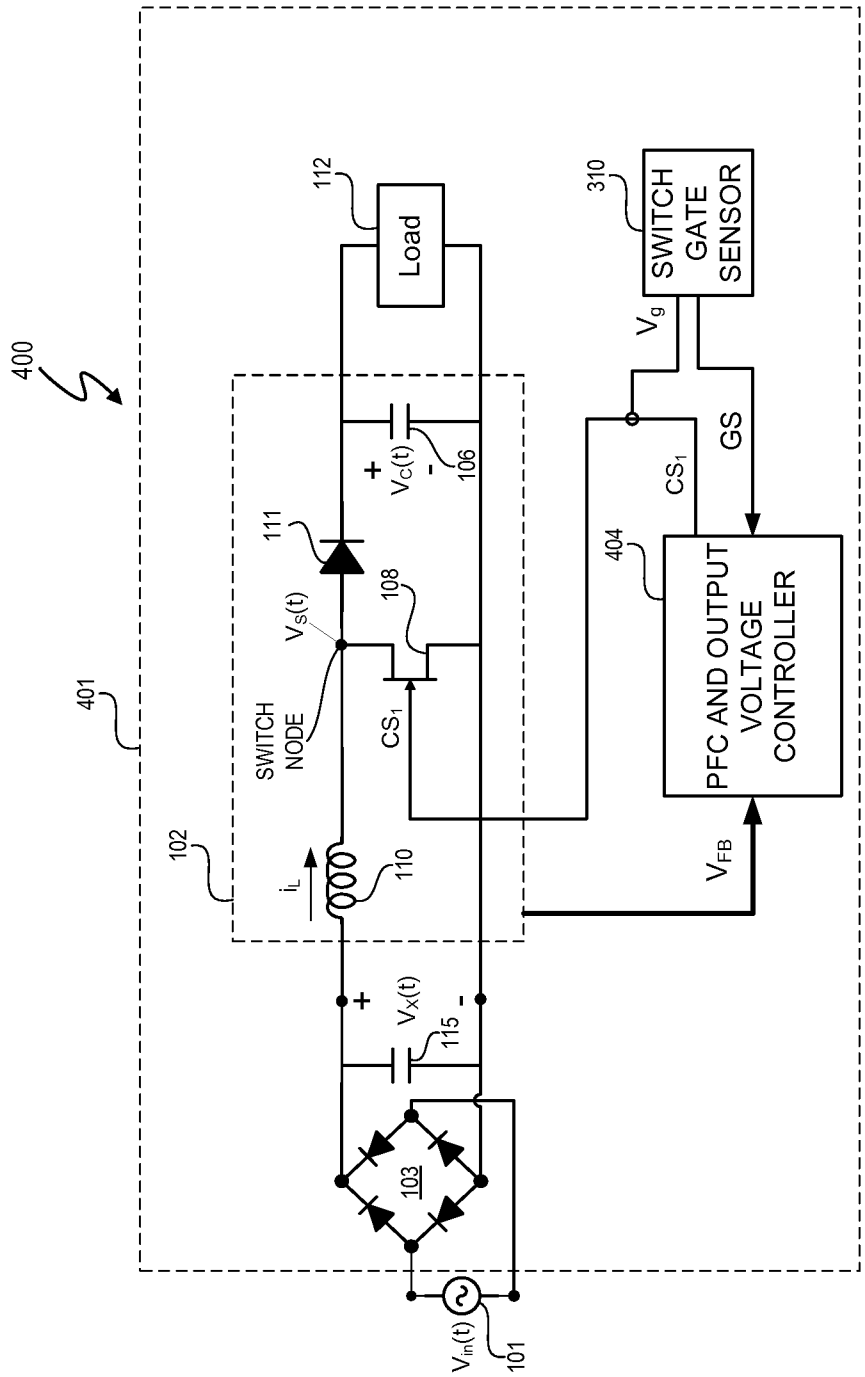
400
401
102
112
Load
310
SWITCH GATE SENSOR
V_g
GS
CS_1
404
PFC AND OUTPUT VOLTAGE CONTROLLER
V_{FB}
$V_C(t)$
106
111
108
$V_S(t)$
SWITCH NODE
CS_1
i_L
110
$V_X(t)$
115
103
$V_{in}(t)$
101

Figure 4

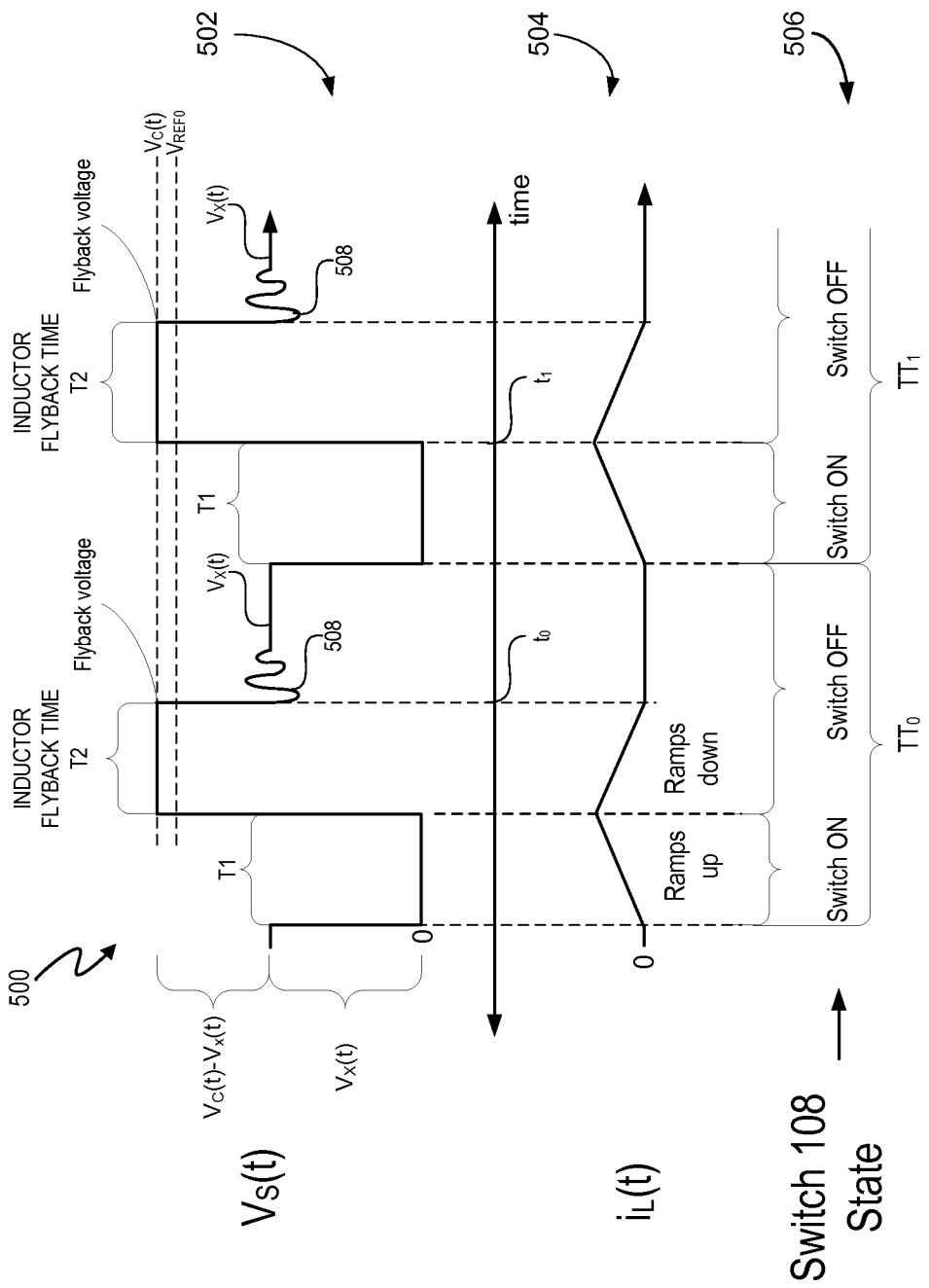
500
502
504
506
$V_S(t)$
$i_L(t)$
Switch 108 State
$V_C(t)$-$V_x(t)$
$V_X(t)$
$V_C(t)$
V_{REF0}
Flyback voltage
INDUCTOR FLYBACK TIME
T2
T1
$V_X(t)$
508
time
t_0
t_1
Ramps up
Ramps down
Switch ON
Switch OFF
TT_0
TT_1
0

Figure 5

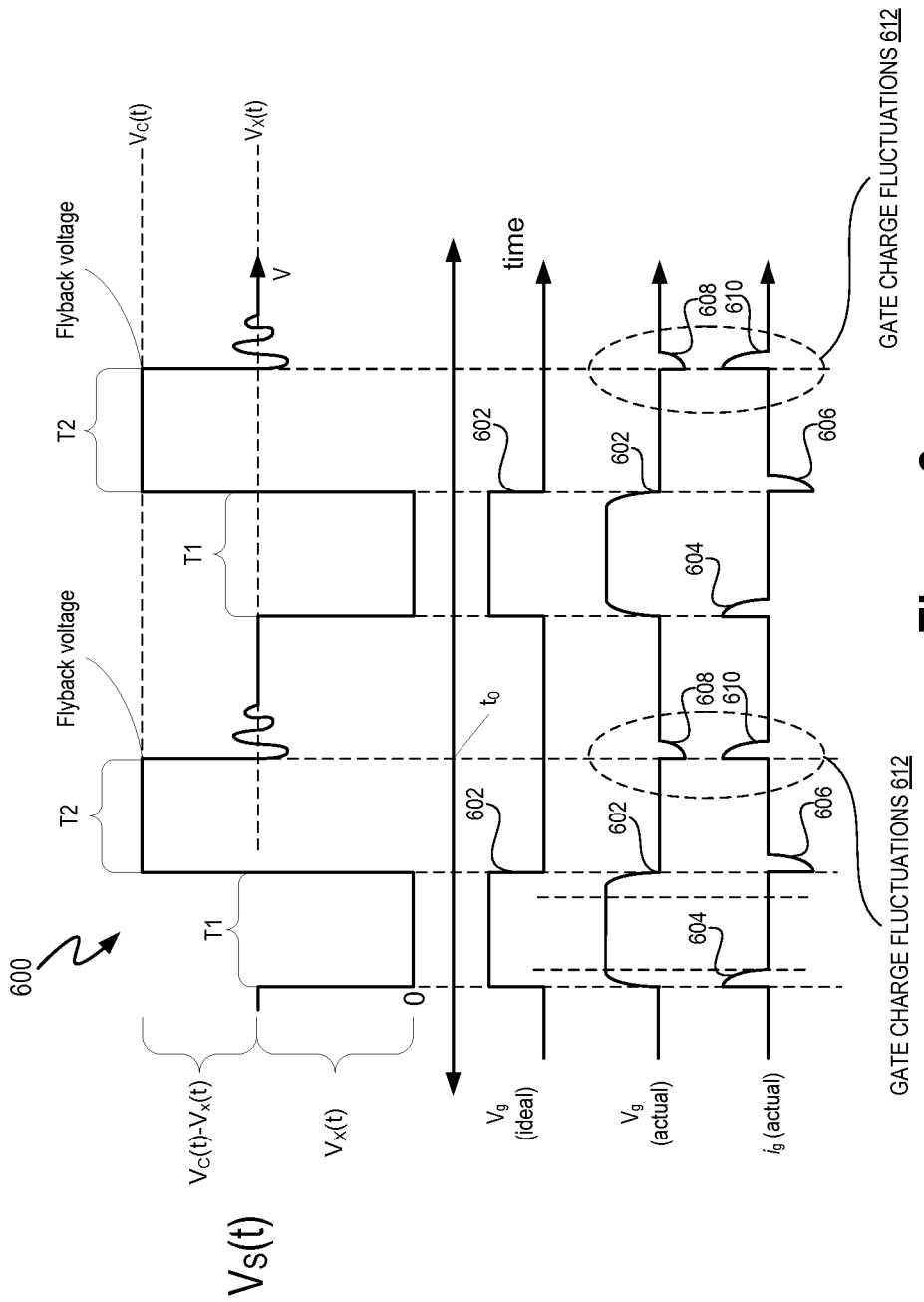
600
Vs(t)
Vc(t)-Vx(t)
Vx(t)
Vg (ideal)
Vg (actual)
ig (actual)
T1
T2
Flyback voltage
Vc(t)
Vx(t)
V
0
time
to
602
604
606
608
610
GATE CHARGE FLUCTUATIONS 612

Figure 6

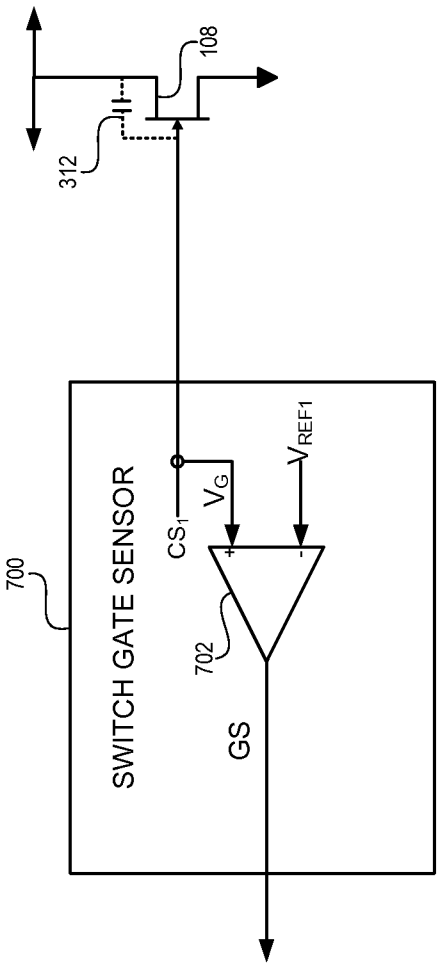

Figure 7

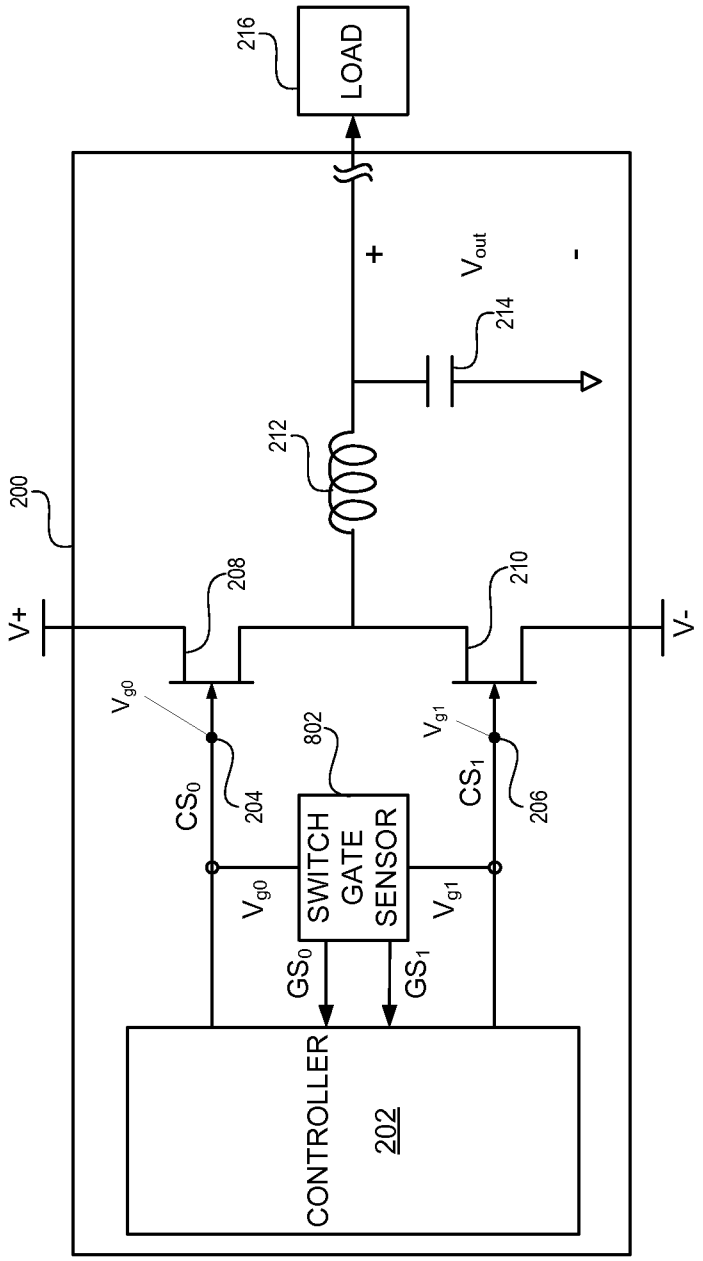
216
LOAD
+
V_{out}
-
214
212
200
208
210
V+
V-
V_{g0}
802
V_{g1}
CS_0
204
SWITCH GATE SENSOR
CS_1
206
V_{g0}
V_{g1}
GS_0
GS_1
CONTROLLER
202

Figure 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/062381

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M1/42 H02M1/08 H03K5/153

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED.

Minimum documentation searched (classification system followed by classification symbols)
H02M H03K H03F G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal; WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 043 633 A (LEV ARIE [IL] ET AL) 28 March 2000 (2000-03-28) abstract column 6, line 28 - column 11, line 58; figures 3-15	1-20
A	EP 1 213 823 A (SANKEN ELECTRIC CO LTD [JP]) 12 June 2002 (2002-06-12) abstract; figures 1,2	1-20
A	US 2004/085117 A1 (MELBERT JOACHIM [DE] ET AL MELBERT JOACHIM [DE] ET AL) 6 May 2004 (2004-05-06) abstract paragraphs [0107], [0108], [0130] - [0139]	1-20

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 August 2008	09/09/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Braccini, Roberto

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/062381

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002/166073 A1 (NGUYEN JAMES HUNG [US] ET AL NGUYEN JAMES HUNG [US] ET AL) 7 November 2002 (2002-11-07) abstract; figures 2,4	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2008/062381

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EP 1213823 A	12-06-2002	CN 1365181 A	21-08-2002
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		WO 0247265 A2	13-06-2002
US 2002166073 A1	07-11-2002	NONE	