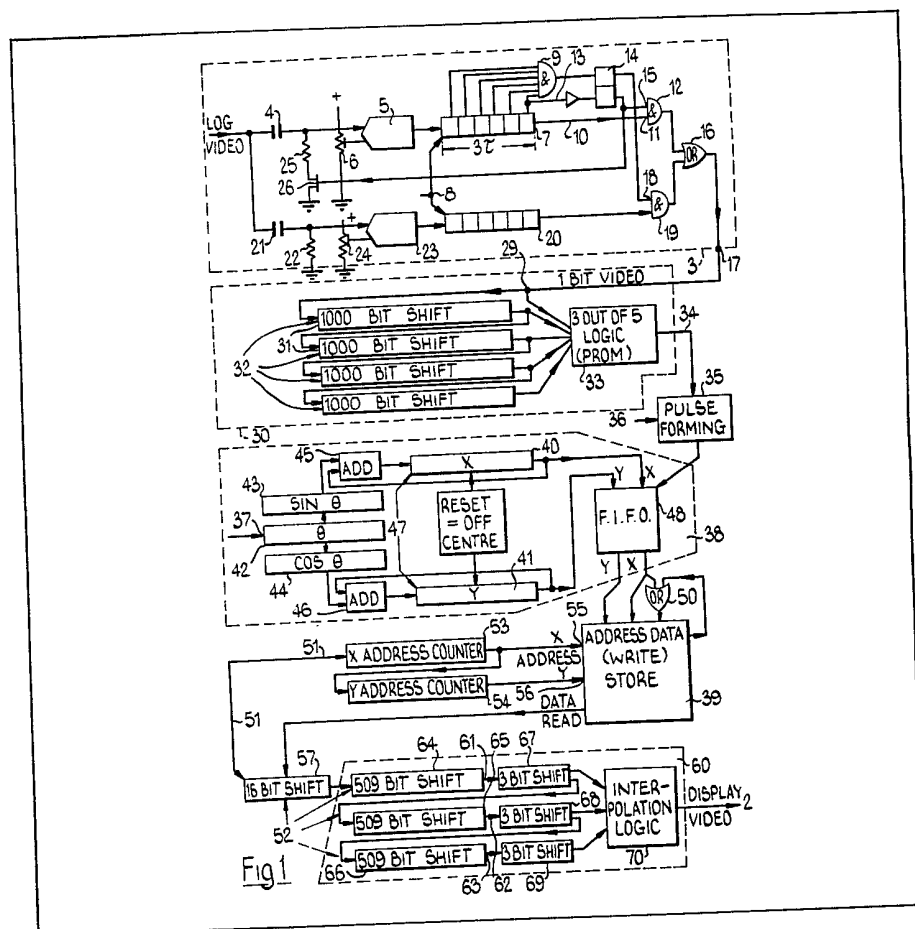


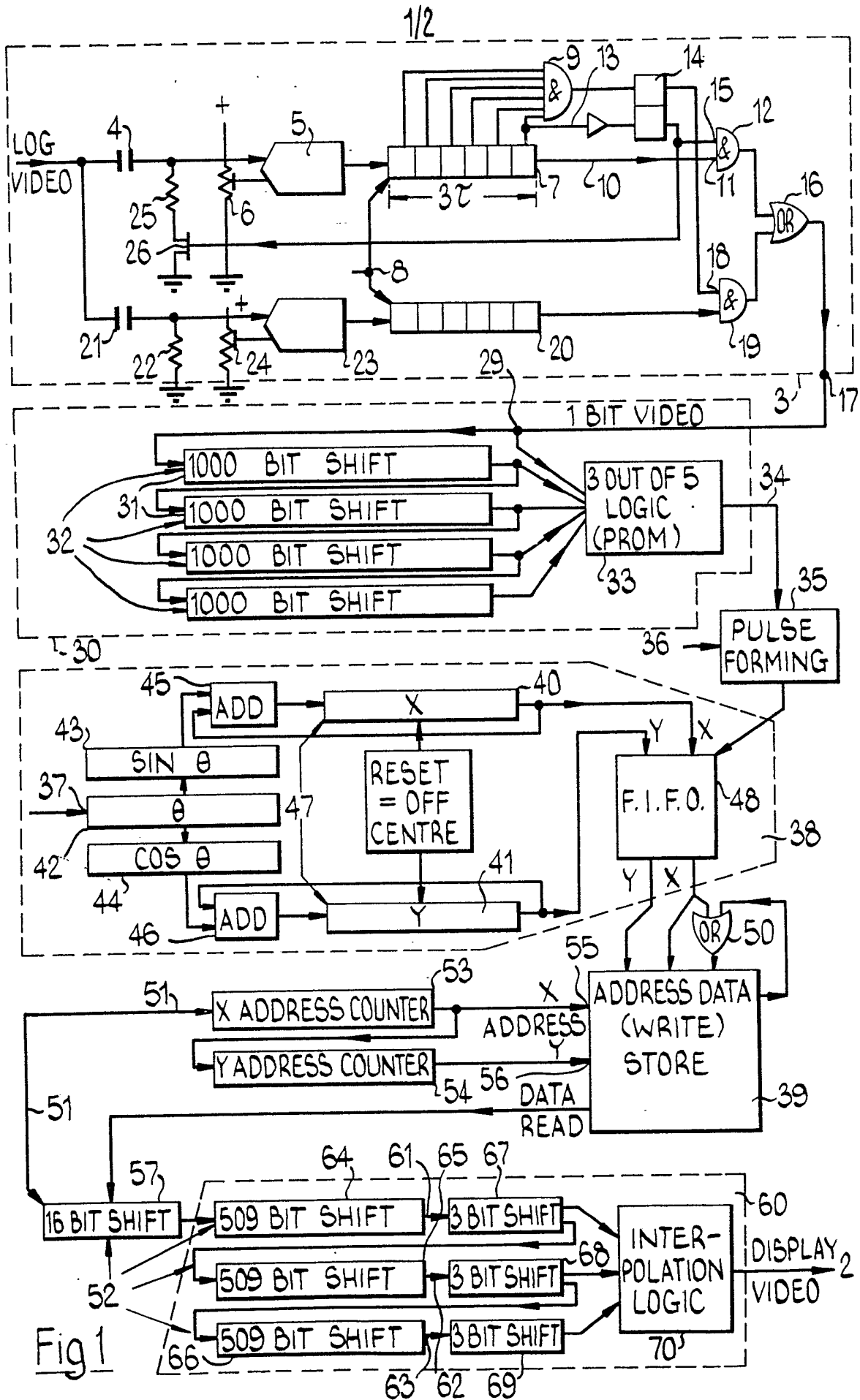
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(54) Scan converter for a television display

(57) A digital raster scan converter for converting elements of picture information available according to a first format to a second format suitable for display on a TV screen comprises a rectangular coordinate memory store (39) into which 1-bit video information according to the first format is written. The information from the store (39) is read out sequentially into three shift registers (61, 62, 63). An interpolation logic circuit (70) is connected to the last three bits of each of the three shift registers and is so arranged as to interpolate additional in-line and inter-line picture information to thereby provide a flicker-free display on a TV screen. The incoming information may be in polar coordinate form from a radar system.



The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.



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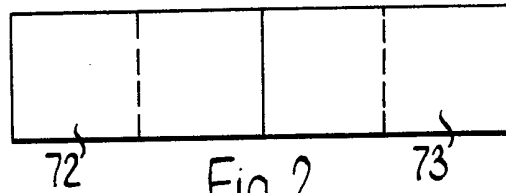
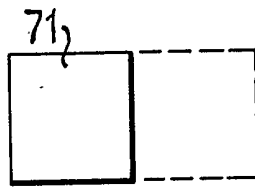


Fig. 2

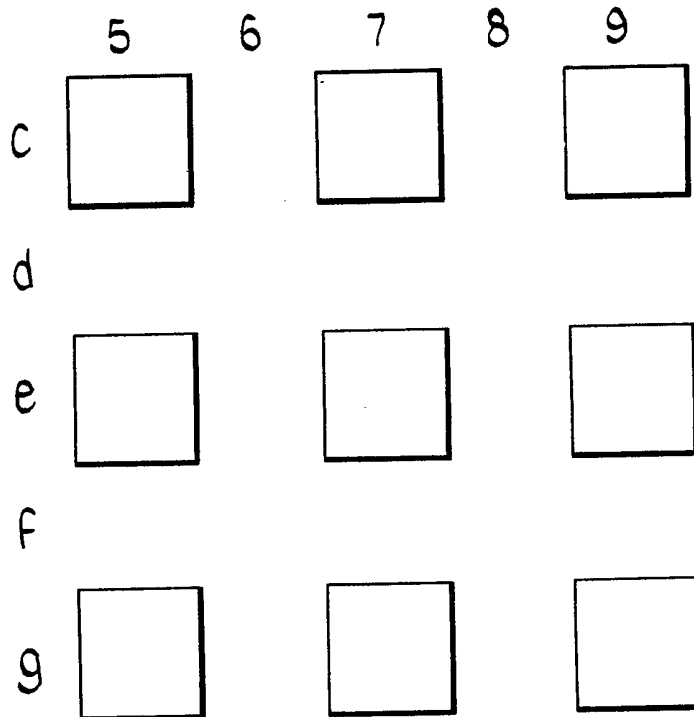


Fig. 3

SPECIFICATION

Improvements in or relating to raster scan converters

- 5 This invention relates to digital raster scan converters wherein scan information in one format is converted to scan information in a second format. 5

Scan converters are commonly used to convert radar information obtained in polar co-ordinates at a scan rate determined by the rotation of the radar antenna into a form suitable for display on a TV screen. By such means there can be provided a bright steady picture which can be viewed in normal lighting conditions. The

- 10 disadvantage of the prior art digital scan converters is that large data stores are required to retain the definition of modern radars. The radar information must be stored over a whole revolution of the radar antenna and to provide a resultant picture which is indistinguishable in quality from that of a directly viewed display typically requires 3 million bits of storage ie 1000 x 1000 picture elements each having 3 bits (8 levels) of brightness. A flicker-free display of this stored data requires the data to be read out 25 times a second ie at a bit rate of 75 mega-bits. Using word lengths of 24 bits, this requires a store cycle time of 320 nanoseconds for read-out, neglecting the time necessary to refresh with new data. 15

It is an object of the present invention to provide a flicker-free radar picture on a TV raster using appreciably less storage than heretofore possible as well as a longer store cycle time, while retaining good picture quality.

- 20 The present invention provides a digital raster scan converter for converting elements of picture information available according to a first format to a second format suitable for display on a TV screen comprising a rectangular co-ordinate memory store into which the information according to the first format can be written, means to read out the information from said memory store in a raster manner and means to interpolate additional in-line and inter-line information to provide a flicker-free display on a TV screen. 20

- 25 Preferably the means to interpolate comprises two or more shift registers in which successive lines read out from said memory store can be temporarily stored. Alternatively the information according to the first format can be written into separate blocks in the memory store so that interpolation can be achieved by cyclically addressing appropriate locations in the store blocks. In one preferred embodiment the raster scan converter is used in a radar system wherein radar picture information in polar co-ordinates obtained from a rotatable directional antenna is transformed into rectangular co-ordinates to provide said first format. 30

- Advantageously said radar picture information is 1-bit video information produced by applying the received radar signal to a discriminator whereby a radar signal pulse output is produced whenever said received radar signal amplitude exceeds a predetermined value. Preferably there is provided means to discriminate against received clutter radar signals, clutter being received signals having pulse lengths longer than the transmitted radar pulses. Whenever such clutter signals are detected it is possible to arrange for differentiation of the clutter signal so that there is not a complete loss of information from areas of clutter. Preferably also the 1-bit video information from successive sweeps of the antenna is correlated to eliminate noise and interference signals which do not correlate in range. The 1-bit video information may be transformed from polar co-ordinates to rectangular co-ordinates according to said first format by continuous operation of two multiplier circuits wherein the range measured by a range clock is multiplied respectively by the sine and cosine of the angular bearing of the antenna, said rectangular co-ordinates being connected to the address lines of the memory store whereby a received radar pulse is stored at the appropriate rectangular co-ordinate location in the memory store. 40

- In a preferred arrangement of the interpolation means for processing 1-bit video information three shift registers connected in series are provided wherein each register has a capacity equal to one line of stored video information and an interpolation logic circuit is connected to nine bits consisting of three adjacent bits in corresponding positions in each shift register. The nine bits thus represent a rectangular element of the field view comprising a three by three matrix of picture elements. The interpolation logic circuit may be arranged so that "1"s corresponding to radar pulses are generated at intermediate positions on a line that can be drawn through any three bits of said nine bits wherein said three bits are filled with radar pulses. 50

- Whenever there are only two adjacent bits of said nine bits which are filled with radar pulses, the interpolation logic may be arranged so as to cancel the said two adjacent pulses and to generate a "1" at the single intermediate point. By this interpolation means the output is able to reproduce horizontal, vertical and diagonal lines but discriminates against the reproduction of short lines resulting from a single received radar pulse being stored in two adjacent locations in the memory store. 55

In order that the invention may be more fully understood, one embodiment thereof will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a schematic block diagram of a scan converter according to the invention;

Figure 2 illustrates a timing consideration involved in the interpolation logic;

- 60 *Figure 3* is a schematic diagram to illustrate the interpolation logic embodied in the invention. 60

In *Figure 1* there is shown schematically a circuit arrangement for processing input signal information 1 from a rotating radar antenna to produce an output signal 2 in a form suitable for a TV raster scan. The input signal 1 obtained from a log amplifier (not shown) is processed by means of circuitry 3 to produce 1-bit video data whereby the input signal is compared with an amplitude threshold and a "1" is generated whenever the

- 65 threshold is crossed. The input signal is connected through capacitor 4 to an amplitude comparator circuit 5 65

whose threshold is fixed by means of a variable resistor 6. A leak resistor 25 is connected at one end to earth via a normally conducting FET 26 and at the other end to the connection between the capacitor 4 and the comparator 5. The values of the capacitor 4 and leak resistor 25 are chosen to provide a long time constant so that there is little differentiation of the input signal 1. The output from the comparator 5 produced whenever the input signal 1 exceeds the comparator threshold is passed to a 6-bit shift register 7. The shift register 7 has an input from a clock 8 which provides pulses at such a frequency that the time between successive pulses is equal to half the pulse length of the transmitted radar pulses. Shift register 7 is arranged in such a way that the 1-bit video circuitry 3 discriminates against clutter which might be present in the input signal 1. For this means clutter is defined as an input signal having a pulse length at least three times that of the radar signal. Each bit of the shift register 7 is connected to an AND gate 9. The 1-bit video data is transmitted through the shift register 7 and via path 10 to one input 11 of an AND gate 12. The data is also transmitted via the parallel path 13 to a bistable gate 14. In the absence of clutter there will be at least one zero present at an input to AND gate 9 causing bistable gate 14 to be set such that a "1" is simultaneously transmitted to the inputs 11 and 15 of AND gate 12. The data is thus transmitted through AND gate 12 to an OR gate 16 the output of which is connected to the output 17 of the 1-bit video circuitry 3.

In the presence of clutter a "1" signal will be simultaneously present at each input of the AND gate 9 from the 6-bit register 7. The output from AND gate 9 changes the state of the bistable gate 14. This causes a "1" to be transmitted to an input 18 of an AND gate 19 and a "0" to input 15 of the AND gate 12. The clutter signal cannot therefore pass directly to the output 17 of the circuit 3 through the AND gate 12. The "1" pulse transmitted to the input 18 of AND gate 19 enables the input signal 1 to be transmitted via a shift register 20 connected in parallel with shift register 7 to the AND gate 19 and thence via OR gate 16 to the output 17 of the 1-bit video circuitry 3. The input signal 1 before transmission to shift register 20 is first differentiated by a short time constant circuit comprising capacitor 21 and resistor 22 to suppress the clutter and then passes to a comparator circuit 23, similar to comparator 5, wherein the discrimination level is set by the variable resistor 24. The 1-bit video circuitry 3 thereby operates normally using a fixed threshold determined by comparator 5 but in the presence of a clutter signal when the fixed threshold is crossed continuously for a time equivalent to three radar pulse lengths the circuit switches automatically to the differentiated signal thereby suppressing the clutter. By reducing the clutter signal to that of noise radar echos above the clutter level can be detected. However by differentiation of the input signal 1 the signal to noise ratio is reduced making weak targets difficult to see. Differentiation is therefore only applied in cluttered areas. In order that the extent of cluttered areas can be shown, and hence the areas of degraded radar performance, in the output signal 2 for the TV display, the two thresholds for the direct and differentiated signals in comparators 5 and 23 are respectively set at different levels relative to their means by the variable resistors 6 and 24. The thresholds will thus have different mean probabilities of being crossed and will thereby produce a different mean brilliance on the TV display, contrasting the cluttered and uncluttered areas. To prevent capacitor 4 being charged through the leak resistor 25 during blocks of clutter and thus changing the mean level of signal applied to comparator 5, the leak is disconnected by providing between the leak resistor 25 and earth an FET 26 which is biased to the off condition by means of a logic "0" from bistable gate 14.

The lower the thresholds the greater is the sensitivity to weak echos but these become increasingly difficult to see due to the greater mean density of the noise spots making visual range correlation more difficult. In order to reduce the noise the output 17 from the circuitry 3 generating the 1-bit video signal is connected to the input 29 of an automatic correlator 30 of the three out of five variety. The correlator 30 employs four 1000-bit shift registers 31 connected in series. The 1000-bit shift registers 31 are chosen so as to be capable of storing information corresponding to the maximum range of the radar. The shift registers 31 have common parallel inputs from an interrupted clock 32, similar to clock 8 in producing pulses such that the time between successive pulses is equal to half that of the radar pulses. At the commencement of each sweep of the radar antenna the clock 32 is started and is interrupted when the number of output pulses just equals the 1000-bit capacity of the shift registers 31. "1"s which appear at the input 29 become stored in the first of the series-connected shift registers 31 during one sweep of the radar antenna and are then shifted into corresponding positions in the second of the series-connected shift registers 31 during the subsequent sweep of the radar antenna. The inputs to each shift register 31 and the output of the final shift register are connected to the address lines of a Programmable Read Only Memory (PROM) 33. The PROM 33 has a "1" stored at addresses corresponding to acceptable patterns so that whenever the signals in three of the five PROM address lines correlate in range a "1" is passed to the output 34 of the PROM 33. The automatic correlator 30 thus reduces signals which do not correlate: this reduces the noise residue and also interference signals from, for example, other radars. As will be apparent, automatic correlators other than the three out of five variety can be used to reduce the noise.

The output 34 from PROM 33 is connected to a pulse forming circuit 35, which circuit in addition to shaping also lengthens the pulse so that it is the same length as the radar transmitted pulse. A range clock 36 connected to the pulse forming circuit 35 is set to zero by the transmission of a radar pulse and is stopped by the appearance of a received pulse at the pulse forming circuit 35. The time thus recorded by the range clock 36 between transmission and reception of a reflected pulse is proportional to twice the range from the transmitter of the pulse reflecting target.

The range determined by the range clock 36 and the bearing of the antenna 37 give the polar co-ordinates of the target. The bearing and range are converted from polar to cartesian X, Y co-ordinates for presentation

on a TV display by the conversion circuitry 38. A rectangular co-ordinate memory store 39 is provided in which the video "1" from the pulse forming circuit 35 are injected into the appropriate X, Y locations. This is done by keeping an up-to-date address of the store location in which a "1" if present in the output from circuit 35 should be put. The up-to-date address is maintained by running two binary rate multipliers 40 and 41 at rates proportional to the displayed range scale multiplied by the sine and cosine of the antenna bearing. One multiplier 40 then gives the X address and the other multiplier 41 gives the Y address of the appropriate store location. Circuit 42 is arranged in cooperation with the radar antenna 37 to hold the instantaneous angle θ of the radar in the plane of rotation thereof. A digital signal representing the angle θ is applied to the inputs of sine and cosine circuits 43 and 44 respectively whereby the outputs thereof represent the sine and cosine of the antenna direction. The digital sine and cosine outputs are transmitted through ADD circuits 45 and 46 to the respective inputs of the binary rate multipliers 40 and 41. Range pulses 47, at half the range clock 36 rate are also applied to each binary rate multiplier such that the respective output from the multipliers 40 and 41 represent the X and Y coordinates of the radar-reflecting target. The X and Y coordinates are stored temporarily in a "first in first out" (FIFO) store 48 for transfer to the rectangular coordinate store 39. At the end of each radar sweep the binary rate multipliers are arranged to be reset by means of reset circuit 49. If it is desired that the display should be offset, the reset value determined by reset circuit 49 is made equal to the algebraic sum of the offset and the X, Y address. Whenever a "1" appears at the output of the pulse forming circuit 35 the X and Y coordinates of the radar-reflecting target are applied to the address lines of the rectangular coordinate store 39 and a "1" is entered in the appropriate X, Y location. OR gate 50 is provided at the input to the store 39 so that any "1" which is already stored is not destroyed by an incoming "1".

In the arrangement shown the store 39 has a capacity of 16,384 16-bit words. The nine most significant bits of the address word define the Y address, the next five bits define the coarse X address and the remaining 4 bits of the X address are used to define the position of the "1" in the 16-bit word. In order to provide a flicker-free display the picture field stored in the rectangular coordinate store 39 is arranged to be read out 50 times a second to provide interlacing of the picture fields. The readout is therefore done at about 820 K words per second. A read-out clock 51 operating at a frequency of about 820 K Hz, derived by dividing the output of a display clock 52 by 16, is applied serially to an X address counter 53 and a Y address counter 54. The outputs from the counters 53 and 54 are applied respectively to the X and Y address lines 55 and 56 of the store 39. The store is therefore scanned sequentially through the X lines and the 16-bit words are read out and temporarily stored in a 16-bit shift register 57. Each 16-bit word is then shifted out of the register 57 by means of the display clock 52, operating at a frequency of about 13 MHz, to the input of an interpolation circuitry 60 the output of which provides the video display. The interpolation circuit 60 comprises three 512-bit shift registers 61, 62 and 63 which are serially fed from the output of the store 39 via the 16-bit shift register 57 such that three successive lines for display can be stored in the shift registers. The three shift registers consist of first 509-bit registers 64, 65 and 66 serially connected to second 3-bit registers 67, 68 and 69 respectively. An interpolation logic circuit 70 is connected to each of the 3-bit registers 67, 68 and 69 and is so arranged as to generate intermediate data points in each video line as well as intermediate video lines.

Referring also to Figure 2 a processed video pulse 71 while in polar format as produced by the 1-bit video circuitry 3 is compared schematically with two successive indexing pulses 72 and 73 produced by the X, Y address counters 53 and 54. If the duration of the processed video pulse 71 is made half of the indexing rate of the X, Y address counters 53 and 54 there will be a 50% probability of the pulse 71 straddling the time barrier between two successive addresses and thus being stored in both addresses in the store 39. The interpolation logic circuit 70 is arranged to recognise this and thus whenever two adjacent store locations are occupied (either horizontally, vertically or diagonally) the circuit generates a "1" in the intermediate picture element only ie when an intermediate spot is produced as a result of two adjacent filled store locations, no spot will be generated in either of the positions corresponding to the two adjacent store locations. Whenever three successive store locations are filled (in any direction) the intermediate spots are generated since these form part of a line of spots. When a "1" appears in an isolated store location the interpolation logic circuit 70 will generate a single "1" for transmission to the output 2. The interpolation logic 70 is shown diagrammatically in Figure 3. The columns numbered 5 to 9 and the rows numbered c to g represent data locations of the second output format to provide the output signal 2 for a TV raster scan. The odd-numbered columns 5, 7 and 9 and the odd-numbered lines c, e and g represent stored data positions in three adjacent data locations in the three successive lines stored in the 3-bit shift registers 67, 68 and 69.

Intermediate positions in the even-numbered columns 6 and 8 and in the even-numbered lines d and f are generated by the interpolation logic circuit 70. The logic is arranged as follows:

a. Intermediate position on stored lines will be set to "1" if adjacent stored bits are "1"s eg on line e : e8 = 1 if e7 and e9 = 1. On an intermediate line - say line f:

f7 = 1 if e7 and g7 = 1

and f8 = 1 if e7 and g9 = 1

or e9 and g7 = 1

b. Where an intermediate position has been set to "1", the stored "1"s producing it will be suppressed unless the stored position is part of a continuous line ie there is a "1" on each side of it.

Consequently a "1" in position e7 will be suppressed unless: c5, c7, c9, e9, g9, g7, g5 and e5 are all zero (ie when no intermediate "1" has been generated).

or c5 and (e9 or g9 or g7) are "1"s

or c7 and (g9 or g7 or g5) are "1"s

5 or c9 and (g7 or g5 or e5) are "1"s

or e9 and (g5 or e5) are "1"s

or e5 and g9 are "1"s.

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The output 2 from the interpolation circuitry 60 thus described comprises 1024 lines each containing 1024 picture elements, which are presented on an inter-laced picture, the alternate picture field both using direct and interpolated data from the store 39. The method of inter-lacing the alternate fields is well known in the art and is not shown.

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The rectangular coordinate store 39 would gradually fill with "1"s as data from successive antenna scans is accumulated unless an erase facility is included. This can be done by continuously erasing "1"s throughout the store on a pseudo-random basis. If the erase rate is adjusted so that all locations are erased in a time corresponding to five antenna scans a radar light spot on the current scan would be gradually eroded away during the following five scans, thus giving tails to echos from moving targets. The tails will give an indication of the speed and direction of targets.

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The embodiment of the invention previously described provides a 1024 line picture employing a memory store of only 512 x 512 bits. The above description illustrates the principle of the invention within which variation will be apparent to those skilled in this art. It is not essential, for example, that successive lines of data be transferred from the memory store, one to each of several successive shift registers, in order to carry out the interpolation of the data. Instead it is possible for the store 39 to be arranged in blocks such that a read-out logic circuit can be provided to cyclically address appropriate locations in the store blocks so as to interpolate additional data as previously described.

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25 CLAIMS

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1. A digital raster scan converter for converting elements of picture information available according to a first format to a second format suitable for display on a TV screen comprising a rectangular co-ordinate memory store into which the information according to the first format can be written, means to read out the information from said memory store in a raster manner and means to interpolate additional in-line and inter-line information to provide a flicker-free display on a TV screen.

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2. A digital raster scan generator as claimed in claim 1 wherein the means to interpolate comprises two or more shift registers in which successive lines read out from said memory store can be temporarily stored.

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3. A digital raster scan generator as claimed in claim 1 wherein the information according to the first format is written into separate blocks in the memory store so that interpolation can be achieved by cyclically addressing appropriate locations in the store blocks.

4. A digital raster scan generator according to any one of claims 1 to 3 wherein the picture information is 1-bit video information.

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5. A digital raster scan generator according to claim 4 wherein the interpolation means for processing 1-bit video information comprises three shift registers connected in series wherein each register has a capacity equal to one line of stored video information and an interpolation logic circuit is connected to nine bits consisting of three adjacent bits in corresponding positions in each shift register such that the nine bits represent a rectangular element of the field of view comprising a three by three matrix of picture elements.

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6. A digital raster scan generator according to claim 5 wherein the interpolation logic circuit is arranged so that "1"s corresponding to radar pulses are generated at intermediate positions on a line that can be drawn through any three bits of said nine bits wherein said three bits are filled with radar pulses and whenever there are only two adjacent bits of said nine bits filled with radar pulses, the interpolation logic is arranged to cancel the said two adjacent pulses and to generate a "1" at the single intermediate point.

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7. A radar system employing a digital raster scan generator according to any one preceding claim wherein radar picture information in polar co-ordinates obtained from a rotatable directional antenna is transformed into rectangular co-ordinates to provide said first format.

8. A radar system as claimed in claim 7 wherein the radar picture information is 1-bit video information produced by applying the received radar signal to a discriminator whereby a radar signal pulse output is produced whenever said received radar signal amplitude exceeds a predetermined value.

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9. A radar system as claimed in any one of claims 6 to 8 wherein there is provided means to discriminate against received clutter radar signals.

10. A radar system as claimed in claim 9 wherein the clutter signal is differentiated so that there is not a complete loss of information from areas of clutter.

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11. A radar system as claimed in any one of claims 8 to 10 wherein the 1-bit video information from successive sweeps of the antenna is correlated to eliminate noise and interference signals which do not correlate in range.

12. A radar system as claimed in any one of claims 8 to 10 wherein the 1-bit video information is transformed from polar co-ordinates to rectangular co-ordinates according to said first format by continuous operation of two multiplier circuits wherein the range measured by a range clock is multiplied respectively

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by the sine and cosine of the angular bearing of the antenna, said rectangular co-ordinates being connected to the address lines of the memory store whereby a received radar pulse is stored at the appropriate rectangular co-ordinate location in the memory store.

13. A digital raster scan generator substantially as described with reference to Figures 1 to 3 of the accompanying drawings.

14. A radar system including a digital raster scan generator substantially as described with respect to Figures 1 to 3 of the accompanying drawings.