July 21, 1970 W. F. BARTLETT ET AL 3,521,036

BINARY CODED DECIMAL COUNTER

Filed Nov. 1, 1966 3 Sheets-Sheet 1

FIG. 1.

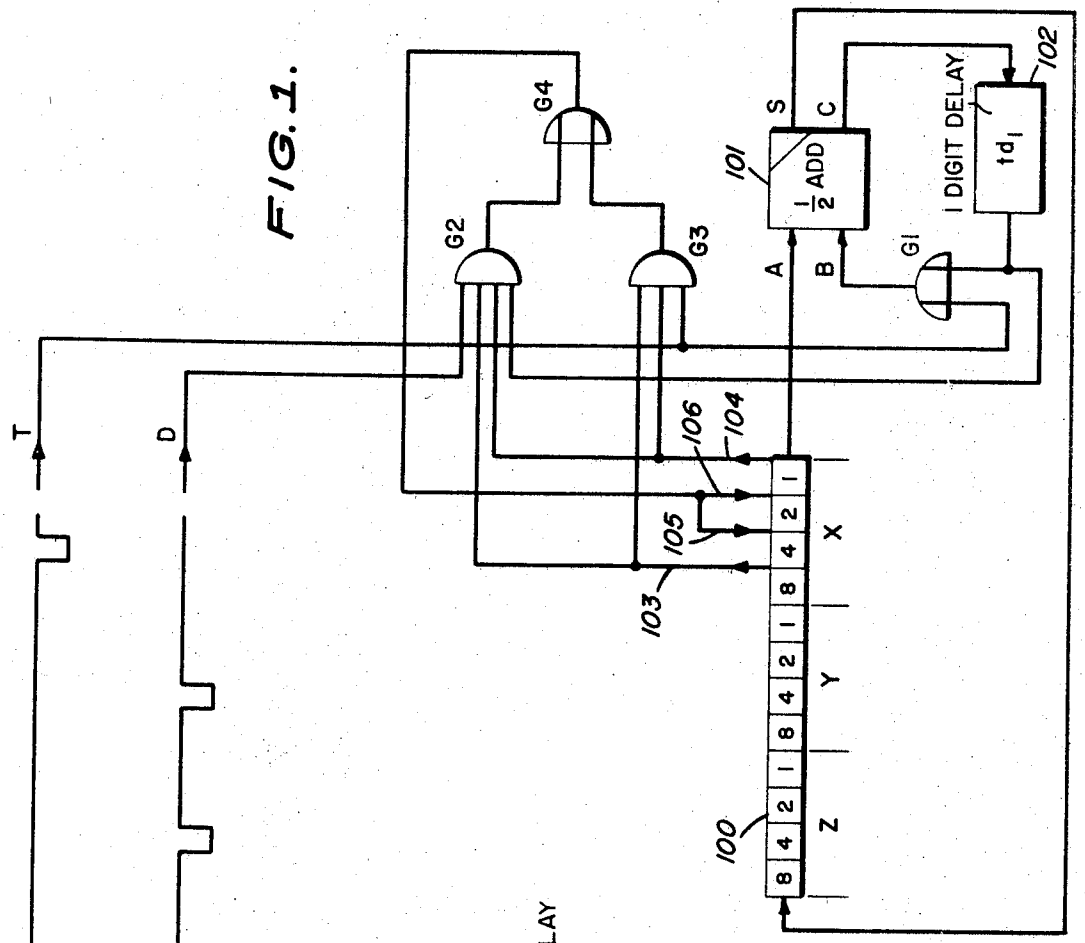
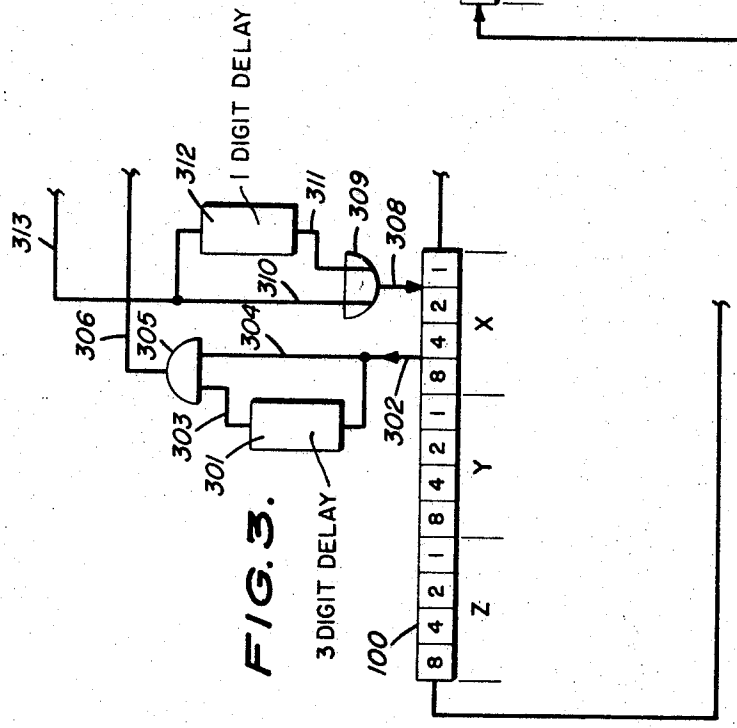


FIG. 3.



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BINARY CODED DECIMAL COUNTER

Filed Nov. 1, 1966 3 Sheets-Sheet 2

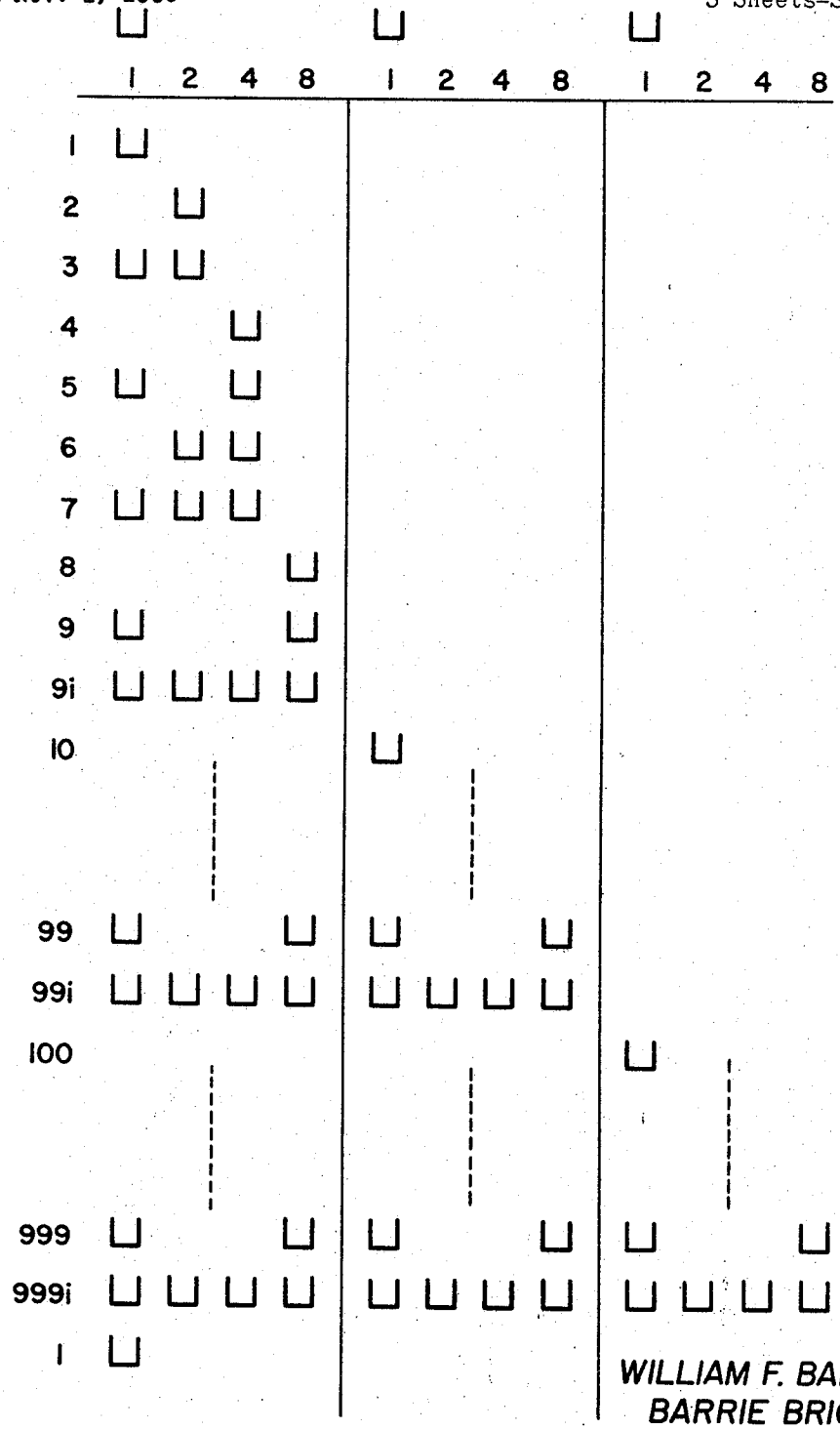


FIG. 2.

WILLIAM F. BARTLETT
BARRIE BRIGHTMAN
INVENTORS

BY Dicke + Craig
ATTORNEYS

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BINARY CODED DECIMAL COUNTER

Filed Nov. 1, 1966 3 Sheets-Sheet 3

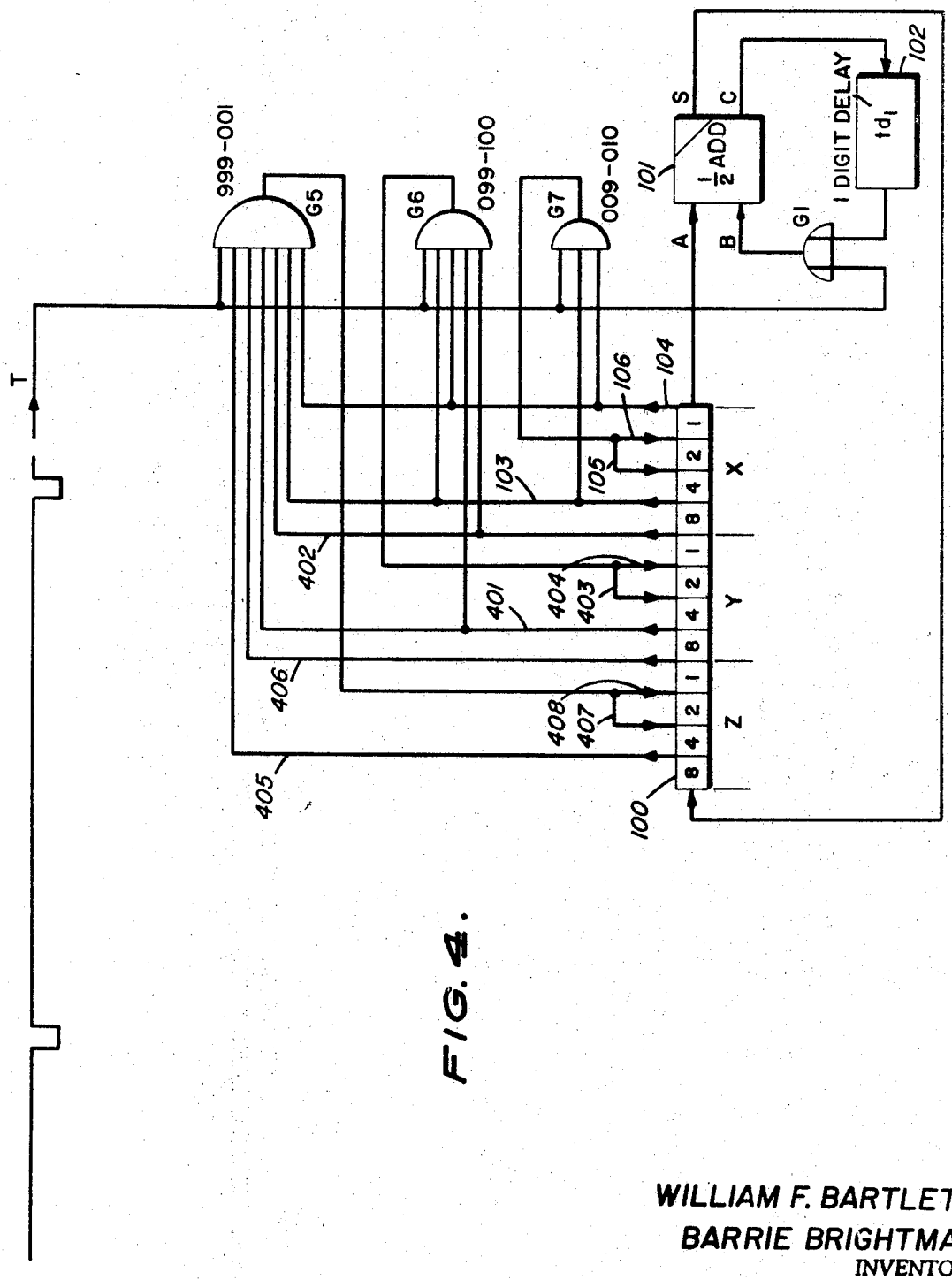


FIG. 4.

WILLIAM F. BARTLETT
BARRIE BRIGHTMAN
INVENTORS

BY Dicke & Craig
ATTORNEYS

United States Patent Office 3,521,036 Patented July 21, 1970

3,521,036

BINARY CODED DECIMAL COUNTER

William F. Bartlett, Rochester, and Barrie Brightman, Webster, N.Y., assignors to Stromberg-Carlson Corporation, Rochester, N.Y., a corporation of Delaware

Filed Nov. 1, 1966, Ser. No. 591,208
Int. Cl. H03k 27/02
U.S. Cl. 235—92 12 Claims

ABSTRACT OF THE DISCLOSURE

Binary coded decimal counter including a delay line forming a plurality of form digit delay units, a half adder, a one digit delay line and an OR gate to provide binary counting. A suitable gating arrangement is also provided for eliminating the binary states **11** through **16** in between the 9th and 10th binary states of each delay unit so that after the 9th binary state, the unit will automatically be set to a count of zero and will carry a single pulse to the next highest order delay unit.

The present invention relates in general to electronic counters, and more particularly, to a binary coded decimal counter using pulse advancing techniques.

To provide an economical binary coded decimal counter, it is necessary to use a binary counter employing either pulse advancing, pulse feedback or pulse blocking techniques. The special techniques must be employed in connection with these counters primarily because the bistable devices or switching elements which are used to perform the counting operations operate only in one or another of two discrete states, which represent the maximum and minimum output current levels of these devices. As can be appreciated, these switching elements are very suitable for counters operating in the straight binary number system, which requires only first and second states for counting. However, because of the almost universal acceptance of the decimal number system, it is necessary to provide electronic counters which are capable of counting in this number system. The disparity thereby presented between the binary nature of the elements used in electronic counters and the numerical system within which the results must be obtained require the use of special techniques to adapt the binary electronic elements to the power of 10 or decimal number system. The compromise is a counter commonly known as the binary coded decimal counter.

A circuit containing four binary elements provides a total of sixteen possible operating states which may be made to correspond to the number of pulses applied thereto. In order to perform a decade counting operation using such binary counting elements, it is necessary to eliminate six of the sixteen possible operating states of the four element circuit. The special techniques referred to above relate to the manner in which the six extraneous operating states are eliminated in the circuit. In the case of counters using pulse feedback or pulse blocking techniques, successive feedback of signals is employed for eliminating the undesirable operating states, which arrangement not only appreciably reduces the speed of the counter, but also increases the complexity of this circuitry. Ideally, the elimination of the unnecessary operating states of the binary counter should be effected in a single operation providing control signals at one instant in the counting operation to advance the counter so as to permit a more rapid counting to take place. Circuits have been proposed for performing in this manner; however, these circuits still relay upon pulse blocking or feedback techniques, and are therefore of necessarily complex configuration.

It is an object of the present invention to provide a binary coded decimal counter which avoids, or otherwise altogether eliminates, the disadvantages inherent in known circuit arrangements of a similar nature.

It is another object of the present invention to provide a binary coded decimal counter based upon pulse advancing techniques.

It is a further object of the present invention to provide a binary coded decimal counter which is of simple configuration providing dependability and economy in manufacture and use.

It is still another object of the present invention to provide a binary coded decimal counter which will operate at greater counting speeds than known arrangements of a similar nature.

In accordance with the exemplary embodiment of the present invention disclosed herein, a twelve digit delay line is utilized as a combination of three separate delay units, each consisting of four binary elements representing one binary coded decimal digit. The twelve digit delay line is provided in association with a half adder, a one digit delay line, and an OR gate to provide a straight binary count upon application of suitable impulses thereto. This combination is then associated with a suitable gating arrangement for eliminating the binary states **11** through **16** in between the 9th and 10th binary states of a binary counter unit, so that after the 9th binary state the counter unit will automatically be set to a count of zero and will carry a single pulse to the next highest order delay unit in the delay line.

These and other objects, features and advantages of the present invention will become more apparent from the following detailed description of the invention, when taken with the accompanying drawings, which illustrate several embodiments of the present invention, and wherein:

FIG. 1 is a schematic circuit diagram of one embodiment of a binary coded decimal counter in accordance with the present invention;

FIG. 2 is a chart illustrating the manner in which the counter of FIG. 1 progresses in its operation;

FIG. 3 is a schematic circuit diagram of a second embodiment of a binary coded decimal counter in accordance with the present invention; and

FIG. 4 is a schematic circuit diagram of a third embodiment of a binary coded decimal counter in accordance with the present invention.

Referring now to the drawing wherein like reference numerals have been used throughout the several views to designate like components, wherever possible, and particularly to FIG. 1, one embodiment of the binary coded decimal counter in accordance with the present invention includes a 12 digit delay line **100**, which may be of any known configuration, such as a magnetostrictive delay line or other delay device capable of operating at high speeds. The output of the delay line **100** is connected to one input A of a pair of inputs A and B to a conventional half adder circuit **101**. The half adder circuit has a pair of outputs S and C, with the output S being connected to the input of the 12 digit delay line **100**. The C output from the half adder **101** is connected to the input of a one digit delay line **102**, which is in turn connected to the input of an OR gate G1, whose output is connected back to the B input of the half adder. A second input to the OR gate G1 serves as the input T to the counter circuit providing the pulses to be counted thereby.

The combination of the 12 digit delay line **100**, the half adder **101**, the one digit delay line **102** and the OR gate G1 provide a straight binary counter for producing

a binary count of the pulses applied via the input T to tthe gate G1. However, for purposes of providing a binary coded decimal counter, the 12 digit delay line **100** can be considered as a combination of three delay lines X, Y and Z each of four digit length. Thus, the delay line **100**, as illustrated in FIG. 1, is subdivided into three units of four digits, with each unit X, Y and Z including digits designated **1**, **2**, **4** and **8**. Each of the four digit delay units is capable of providing sixteen binary states, so that with provision of suitable gating circuits for eliminating the operating states **11** through **16**, each of the four digit delay units will provide 10 binary states representing successive impulses **1** through **10**. By then controlling the carry of a single pulse from the first delay unit X after reaching a count of 9 therein to the second delay unit Y and so on, the three units of four binary digits can be made to represent the units, tens and hundreds digits of a decimal number. Of course, provision for a higher count may be effected in connection with each of the embodiments described herein by merely increasing the length of delay line **100**.

The gating arrangement provided in accordance with the present invention in association with the embodiment thereof illustrated in FIG. 1, includes a pair of AND gates G2 and G3 responsive to the combination of signals circulating in the delay line **100** for applying an output in response to coincident receipt of impulses on the input line T or control line D to the system for producing an output applied through an OR gate G4 to insert signals into the delay line to effect an elimination of the unnecessary states in each of the four digit delay units. As will be apparent from the following detailed description of the circuit of FIG. 1, the gate G3 serves as a means of eliminating the binary states **11** through **16** in the first or "units" delay unit X thereby stepping this unit directly from a count of 9 to a count of 0 and provides for application of a carry to the second or "tens" delay unit Y of the delay line. The gate G2 operates in conjunction with the gate G3 and serves as the means for eliminating the operating states **11** through **16** in the second or "tens" unit Y of the delay line and the third or "hundreds" unit Z of the delay line, but only when a carry is produced in connection with the preceding delay unit indicating that it also has reached a count of 9. This carry indication is provided through connection of the output of the single digit delay line **102** directly to the input of gate G2. The monitoring of impulses in each delay unit as they progress through the delay line **100** is provided by the pulses applied through input D to the system.

The invention will now be described in connection with the operation of the circuit of FIG. 1. Assuming that the delay line **100** and the single digit delay line **102** are empty, the next pulse to be counted which is received at input line T to the system will pass the OR gate G1 and be applied to the input B to the half adder **101**. It may be recalled that the conventional half adder provides an output on line S in response to an input applied either to input A or B, but provides no output on the lead C under these conditions. However, coincident receipt of impulses on inputs A and B to the half adder will result in an output pulse applied to the output lead C without application of a corresponding pulse on the output S. Thus, as there is no input on the lead A to the half adder at this time, the output pulse will appear at the S output of the half adder only and will be inserted into the 12 digit delay line **100**.

After 12 digit delays the pulse will reappear at the output of the delay line **100** and will be applied to the A input of the half adder. However, as there is no input on the B lead to the half adder at this time, the pulse will appear once again at the S output and will be reinjected back into the delay line **100**. The pulse will recirculate in this fashion through the 12 digit delay line **100** until another drive pulse is applied via the input T to the system where it will pass through the OR gate G1 to the input B of the half adder **101**.

The length or total delay time of the delay line **100** is chosen so that the drive pulses applied to the input T are spaced by an interval greater than the total delay time of the delay line **100** but are coincident in time with the lowest order digit in the 12 digit delay line. Thus, if an impulse is circulating in the delay line in the lowest order digit therein, the application of a drive pulse to the system via input T will coincide with the recirculating pulse at the inputs A and B to the half adder **101**. The coincidence of this second drive pulse and the output of the delay line at the inputs A and B to the half adder will result in a carry output from the C terminal of the half adder with no pulse provided at the S output therefrom at this time. The pulse of the C output of the half adder will be applied through the single digit delay line **102** to the input of the OR gate G1 where it is applied through the second digit time of the delay line **100** to the B input of the half adder **101**. This pulse will emerge from the half adder **101** at the S output thereof to be applied to the 12 digit delay line **100** in the second digit position. In this manner, sequential impulsing of the system from the input line T will result in the building up of a binary count in the delay line **100**.

The binary counting operation described above can be additionally illustrated from the chart set forth in FIG. 2. The chart is divided into three vertical sections representing the three delay units X, Y and Z of the delay line **100** with each section having four columns representing the four digits of the delay unit, designated respectively, **1**, **2**, **4** and **8**. A pulse symbol is provided above the number **1** column of each section to indicate the pulses received either on input T to the system (which controls the first delay unit) or the impulses received on the input D to the system (which controls the second and third delay units). As indicated in the above description, the first impulse received on input T is inserted via the half adder **101** into the delay line in the first position of the first delay unit X, as indicated in line **1** of the chart. The second impulse is then applied at the input of the half adder **101** in coincidence with the recirculating pulse to provide an output from line C of the half adder through the single digit delay line **102** and back to the input B of the half adder where it is inserted into the delay line **100** in the second digit position of the delay line as represented by line **2** of the chart. It is noted at this time that the pulse recirculating in the first digit of the delay line has been erased in the half adder **101** upon coincidence with the second received impulse applied via the input T.

The third impulse received via the input T will be applied through the OR gate G1 to the half adder **101** one digit ahead of the recirculating pulse in the delay line **100** so that no coincidence will occur at the input to the half adder and the impulse will be inserted into the delay line in the first digit position, leaving the other recirculating pulse in the second digit position. This condition is indicated in line **3** of the chart. Receipt of the fourth impulse at input T will produce coincidence at the input of the half adder **101** with the recirculating pulse in the first position in the delay line thereby producing an impulse or the output line C from the half adder which is recirculated through the single digit delay line **102** and applied back to the input B of the half adder through OR gate G1. The recirculating pulse formerly in the first digit position is thereby erased and the impulse is passed once again to the output line C. Upon appearance of the impulse derived from the output C of the half adder at the B input thereof, a coincidence will occur with the recirculating pulse in the second digit position of the delay line so that this recirculating pulse is erased and an output is placed once again at the line to be recirculated to the single digit delay line **102** and applied back to the input B of the half adder. This pulse is then placed at the output S of the half adder and inserted into the third digit position of the first delay unit of the delay line as indicated in line **4** of the chart.

It should be apparent at this point that the operation of the half adder in combination with the OR gate G1 and the single digit delay line **102** results in a build up of a binary count in the delay line **100** with coincidence at the input of the half adder **101** resulting in an erasing of the recirculating impulse to provide a carry digit through the single digit delay line for insertion into the next digit position of the delay line.

When the counter has proceeded in the described fashion to a natural count of 9, as indicated in line **9** of the chart, the pulse advancing circuit is required to advance the counter by six steps upon recognition of the next drive pulse so as to limit the counter to ten operational states for purposes of keeping a decimal count of the binary operation. This is accomplished in the following way. Two output taps are provided in the 12 digit delay line, one of the output taps is provided at the output of the line and extended to both of the AND gates G2 and G3, and the second output tap is provided three digits from the end of the delay line, i.e., between the third digit position and the fourth digit position of the first delay unit X and is applied once again to both of the AND gates G2 and G3. In addition, two parallel inputs to the delay line **100** are provided, with one input being provided one digit from the end of the delay line, i.e., between the number one digit and the number two digit of the first delay unit X, and the other input provided two digits from the end of the delay line, i.e., between the number **2** digit and the number **4** digit of the first delay unit X. These inputs are derived from the output of OR gate G4 and provide a means for inserting digits or impulses into the appropriate positions in the delay line for immediately shifting a detected count of 9 to an intermediate count of 16. As a result, the received impulse to the system on line T will shift the first delay unit X of the delay line **100** to a count of 0 with a carry to the next delay unit Y rather than the normally provided count of the binary 10 (0101). This is indicated in the chart of FIG. 2 at lines **9**, **9***i* and **10**. It is noted from line **9** that a count of 9 includes an impulse in the first digit position and the fourth or number **8** digit position with no impulses appearing at the number **2** and number **4** digit positions of the unit. Thus, in order to advance the count by six digits, it is necessary to insert impulses into the number **2** and number **4** digit positions of the first delay unit X, thereby advancing the count to binary **16**, so that the next advance of the delay line will produce a count of 0 in the first delay unit X with a carry to the number **1** digit of the second delay unit Y, as indicated in line **10** of FIG. 3.

The operation above is carried out by the AND gate G3 in combination with the OR gate G4. Detection of an impulse in the number **1** and number **8** digit positions of the first delay unit X of the delay line **100** will produce an output on lines **103** and **104** from the delay line to the AND gate G3 so that upon coincidence of an impulse on input line T, the AND gate G3 will be enabled and an output will be provided through the OR gate G4 to the inputs **105** and **106** at the number **2** and number **4** digit positions of the first delay unit X, thereby inserting impulses into these digit positions to instantaneously advance the binary count in the delay unit to binary **16**. This injection of the drive pulses into the second and third order digit positions effectively adds six drive pulses (binary **2** and binary **4**) to the existing state of the counter. Pulses will then exist in the first four digit orders of the 12 digit delay line **100**, in the **1**, **2**, **4** and **8** positions of the first delay unit. The addition of the drive pulse to this count will result in the first four orders of the line returning to the 0 state and a carry pulse being stored in the fifth order position of the line **100**.

As previously described, the 12 digit delay line **100** can be considered as three separate delay units X, Y and Z, each consisting of four binary elements. It can further be considered that these three separate delay units represent the units, tens and hundreds digits of a decimal number. The pulse advancing just described has therefore advanced the counter from a count of 9 in the first delay unit of the delay line to a count of 0 in this group, and at the same time has carried a count of 1 into the Y unit, providing a binary coded decimal count of 10 in the first and second delay units X and Y of the delay line **100**.

The foregoing describes the advance of a carry from the "units" to the "tens" units in the delay line; however, it is also necessary to advance of a carry from the "tens" unit to the "hundreds" unit and back again from the "hundreds" unit to the "units" unit. These advances and the intermediate state of the 12 digit delay line **100** associated with the advances are shown in the chart of FIG. 2. The manner in which this is implemented by the circuitry of FIG. 1 will now be described. The advance in the delay line from a count of decimal 099 to 100 and from decimal 999 to 001 is performed in the same fashion as previously described in connection with the advance from 009 to 010; however, it is necessary for the second and third advances that a carry be detected in the first delay unit X and the second delay unit Y, respectively, to indicate that these delay units have reached the final count requiring an advance to the next delay unit Z. Thus, these second and third advances are provided under the control of the drive pulses received from input D and the carry lead C from the output of the half adder **101** is applied through the single digit delay line **102** to the input of the AND gate G2.

As indicated in the chart in FIG. 2, the drive pulses received from the input D to the system are coincident with the first digit position in the second and third delay units Y and Z, respectively, and due to the connection of the output of the one digit delay line **102** to the input of AND gate G2, an advance will take place from the second delay unit Y to the third delay unit Z, and from the third delay unit Z back to the first delay unit X, only if a carry is detected in coincidence with application of the impulse at the D input of the system. The reason for this requirement should be obvious from the conditions illustrated in the chart of FIG. 2. For example, in line **98** of the chart, it is seen that the count in the second delay unit Y is a binary count of 1001 representing a tens digit of 9 in connection with the decimal indication and detection of this count via lines **103** and **104** to the AND gate G2 provide two of the required conditions for effecting a carry into the third or "hundreds" delay unit Z of the delay line **100**. However, the generation of a carry into a third delay unit is not appropriate at this time, since the count in the first delay unit X has only reached a count of 8 (0001) and generation of a carry into the third delay unit Z would effectively result in omission of the count 99. As a result, in addition to the timing pulse derived from the input D to the AND gate G2, the presence of a carry condition at the output of the single digit delay line **102** must also be detected at the input of the gate G2, indicating that the count in the first delay unit has reached the count of 9 making a carry to the next higher order possible at that time.

In this way the impulses received on line T will be progressively counted with each delay unit providing a binary representation of a respective decimal position of the count. The count may be read out from delay line **100** in any known manner, either serially or in parallel, in accordance with conventional data processing techniques, and so a specific read-out system will not be described herein.

A modification of the circuit of FIG. 1 to simplify the interconnection between the gating circuitry and the 12 digit delay line **100** is illustrated in FIG. 3. Since much of the system provided in accordance with this modification is identical to the system illustrated in FIG. 1 only the modifications with the 12 digit delay line **100** are illustrated in FIG. 3.

This embodiment of the present invention reduces the number of parallel taps on the 12 digit delay line **100** by

employing a serial three digit delay **301** in connection with a single output tap **302** positioned between the third order and fourth order digits of the first delay unit X of the 12 digit delay line **100**. The output tap **302** is split into two lines **303** and **304** connected to an AND gate **305**, with the line **303** containing the three digit delay line **301**. The output of the AND gate **305** in the form of a control line **306** extends to each of the AND gates G2 and G3, for example, as provided in FIG. 1. It is noted that due to the provision of a single output tap **302** in connection with the delay line **100** only a single control line is connected to each of the gates G2 and G3 rather than the pair of lines **103** and **104**, as provided in the embodiment of FIG. 1.

This embodiment of the present invention further provides for but a single input tap **308** to the 12 digit delay line **100**, which tap is connected between the first and second orders of the first delay unit X of the delay line. This tap **308** is connected to the output of an OR gate **309** to which is connected a pair of control lines **310** and **311**, with the control line **311** containing a single digit delay line **312**. The control lines **310** and **311** are connected to a single control line **313** which is in turn connected to the output of the OR gate G4, such as provided in connection with the embodiment of FIG. 1.

The embodiment of FIG. 3 operates as follows. An impulse in the fourth order digit of the first delay unit X will provide an output at the tap **302** which is applied in turn to the three digit delay line **301** and to the input AND gate **305**. The impulse connected directly to the AND gate **305** will not pass through the gate due to lack of coincidence of the impulse in line **303** resulting from the interposed delay line **301**. It should be remembered at this time that the AND gates G2 and G3 are enabled only upon application thereto of the control pulses applied via lines T and D, which pulses coincide with the time slot of the first digit position of the first delay unit X and the first digit position of the second and third units Y and Z, respectively. Thus, while all recirculating digits in the delay line **100** will be detected at the output tap **302**, as they progressively pass down the delay line, only the impulses naturally appearing in the fourth order of the delay line as determined by the timing of the input control pulses on lines T and D will provide effective control of the system. Therefore, for digits **1** through **7** which do not contain an impulse in the fourth order, no control of the system will be effected by the impulses detected at the output tap **302**. In addition, since gate **305** is an AND gate, no output will appear on line **306** unless coincident signals are received via lines **303** and **304**, a condition which can prevail only if an impulse is stored in both the first and fourth orders of the delay unit X. Thus, in connection with the number 8 (binary 0001) wherein a single impulse is stored in the fourth order of the delay unit, the impulse will be detected at the tap **302** and will be applied to the three digit delay line **301** and the AND gate **305**; however, the impulse applied directly to the AND gate **305** will not pass the gate since no coincident signal appears on line **303** at this time.

For the count of 9 wherein an impulse is stored in both the first and fourth orders of the first delay unit X, appearance of the impulse of the first digit order at the tap **302** will result in application of the impulse to both the three digit delay line **301** and the AND gate **305**. The impulse will not pass the AND gate at this time, but three digits later when the impulse in the fourth order of the first delay unit appears at the output tap **302**, this impulse will be applied directly to the AND gate **305** in coincidence with the first digit impulse now appearing at the output of the three digit delay line **301** to enable the AND gate and apply a control signal via line **306** to the AND gate G3. At the same time, a control impulse is received via the input line T to the AND gate G3 enabling the AND gate and applying an impulse through the OR gate G4 to the control line **313**. This control pulse is applied immediately via line **310** and OR gate **309** to the input tap **308** for storage in the second digit of the first delay unit X of the delay line **100**, and is also applied to the single digit delay line **312** at this time. A single digit later the impulse received via line **313** and applied to the single digit delay line **312** will emerge on line **311** and be applied via the OR gate **309** to the delay line **100** where it is inserted into the third digit order of the first delay unit thereby resulting in the advancing of the count to the intermediate count of line **9***i* in FIG. 2. The counter will then automatically clear the first delay unit X and provide a carry to the second delay unit Y for a count of 10, as described in connection with the embodiment of FIG. 1.

A third embodiment of the present invention is illustrated in FIG. 4. This embodiment of the invention is similar to that provided in FIG. 1 but eliminates the need for a separate drive D by providing taps to and from the digit orders in each of the first, second, and third delay units of the delay line **100**. However, this arrangement requires the use of three separate pulse advancing circuits represented by AND gates G5, G6 and G7. The output lines **103** and **104** connected to the AND gate G7 detect the digit **9** in the first delay unit X of the delay line **100** providing an output to lines **105** and **106** to insert impulses in the second and third digit order of the delay unit to advance this unit to the intermediate count as indicated in line **9***i* of FIG. 2.

Output control lines **401** and **402** are provided in this embodiment for connection to AND gate G6 along with the output lines **103** and **104** from the first delay unit indicating 9's in both the first and second delay units and providing an output from the gate G6 to insert impulses in the second and third digit orders of the second delay unit Y in coincidence with the insertion of impulses in the second and third digit orders of the first delay unit to advance the count to the intermediate state indicated in line **9***i* in FIG. 2.

In control of the third delay unit, there is provided control lines **405** and **406** connected to the AND gate G5 along with lines **401**, **402**, **403** and **404** from the first and second delay units. Coincidence of impulses on all of the lines into the gate G5 along with the timing impulse from the input T indicates a count of 999 and effects an output from the gate G5 in coincidence with the gates G6 and G7 to insert impulses in the second and third digit orders of the respective delay units thereby advancing the count to the intermediate step indicated in line **999***i* of FIG. 2.

It should be apparent from the foregoing description that each of the embodiments of the invention disclosed satisfies the objects of the present invention in providing a simplified, accurate high speed binary coded decimal counter using pulse advancing techniques and these embodiments avoid many, if not all, of the disadvantages inherent in known counters of a similar nature.

While we have shown and described several embodiments in accordance with the present invention, it is understood that the same is not limited thereto, but is susceptible of numerous changes and modifications as known to a person skilled in the art and we therefore do not wish to be limited to the details shown and described herein; but intend to cover all such changes and modifications as are within the ability of one of ordinary skill in the art to which this invention pertains.

We claim:

1. A binary coded decimal counter comprising a delay line $4n$ bits delay, where n is an integral number of decimal places in a decimal number, first means for applying input pulses to and recirculating said pulses through said delay line including second means for controlling said recirculation of pulses to said delay line to provide for storage of successively applied pulses in a binary progression, and gating means connected to selected points on said

delay line for automatically advancing the state of said binary progression in each group of four bit positions in one operation from a state of binary nine to a state of zero with a carry to the next adjacent group.

2. The combination defined in claim 1 wherein said second means includes a half adder circuit having a first input and a first output connected respectively to the output and input of said delay line, respectively, an OR circuit, and a single digit delay line connected between a second output of said half adder and an input of said OR circuit, the output of said OR circuit being connected to a second input to said half adder, and a source of pulses to be counted connected to a second input of said OR circuit.

3. The combination defined in claim 2 wherein said gating means includes a first AND gate responsive to detection of a state of binary nine in the first four digit positions of said delay in coincidence with receipt of an input pulse to advance the state therein to an intermediate state by filling the first four digit positions with impulses.

4. The combination defined in claim 3 wherein said delay line is divided into *n* delay units of four bits each, the first delay unit forming the output of the delay line having a first output tap at said output and a second output tap connected between the third and fourth digit positions thereof, said first and second output taps being connected to said first AND gate.

5. The combination defined in claim 4 further including a source of timing pulses providing a pulse coincident with the first digit position of each delay unit of said delay line subsequent to said first delay unit, said gating means further including a second AND gate responsive to coincident receipt of signals on said first and second output taps, said timing signal and an output from said single digit delay line to advance the then state of said first delay unit to an intermediate state by filling the digit positions thereof with impulses.

6. The combination defined in claim 5 wherein said gating means further includes an OR gate connected to the output of each of said AND gates, said delay line having first and second input taps connected between the first and second digit positions, and the second and third digit positions, of said first delay unit, respectively, the output of said OR gate being connected to both of said first and second input taps.

7. The combination defined in claim 3 wherein said delay line is divided into *n* delay units of four bits each, the first delay unit forming the output of the delay line and having an output tap connected between the third and fourth digit positions thereof, a third AND gate and a three digit delay line, said output tap being connected on the one hand directly to said third AND gate and on the other hand through said three digit delay line to said third AND gate, said third AND gate being connected to said first AND gate.

8. The combination defined in claim 7 further including a source of timing pulses providing a pulse coincident with the first digit position of each delay unit of said delay line subsequent to said first delay unit, said gating means further including a second AND gate responsive to coincident receipt of signals from said third AND gate, from said source of timing signals, and from the output of said single digit delay line to advance the then state of said first delay unit to an intermediate state by filling the digit positions thereof with impulses.

9. The combination defined in claim 8 wherein said gating means further includes a first OR gate connected to the output of each of said AND gates, said delay line having an input tap connected between the first and second digit position of said first delay unit, an additional single digit delay line and a second OR gate connected to said input tap, the output of said first OR gate being connected on the one hand directly to said second OR gate and on the other hand through said additional single digit delay line to said second OR gate.

10. The combination defined in claim 3 wherein said delay line is divided into *n* delay units of four bits each, each of said delay units having a first output tap at the output from the first digit position thereof and a second output tap connected between the third and fourth digit positions thereof, second an third AND gates each connected to said source of input pulses, the first and second output taps of each of said delay units being connected to said first, second and third AND gates, respectively.

11. The combination defined in claim 10 wherein said output taps of said first delay unit are also connected to said second and third AND gates, and said output taps of said second delay unit are also connected to said third AND gates.

12. The combination defined in claim 11 wherein each of said delay units further includes a first input tap connected between the first and second digit position thereof and a second input tap connected between the second and third digit positions thereof, the outputs of said first, second and third AND gates being connected to the first and second input taps of the first, second and third delay units of said delay line, respectively.

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MAYNARD R. WILBUR, Primary Examiner

J. M. THESZ, JR., Assistant Examiner

U.S. Cl. X.R.

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