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(54) **Title**: A VOLTAGE-GATED BIPOLAR TRANSISTOR FOR POWER SWITCHING APPLICATIONS

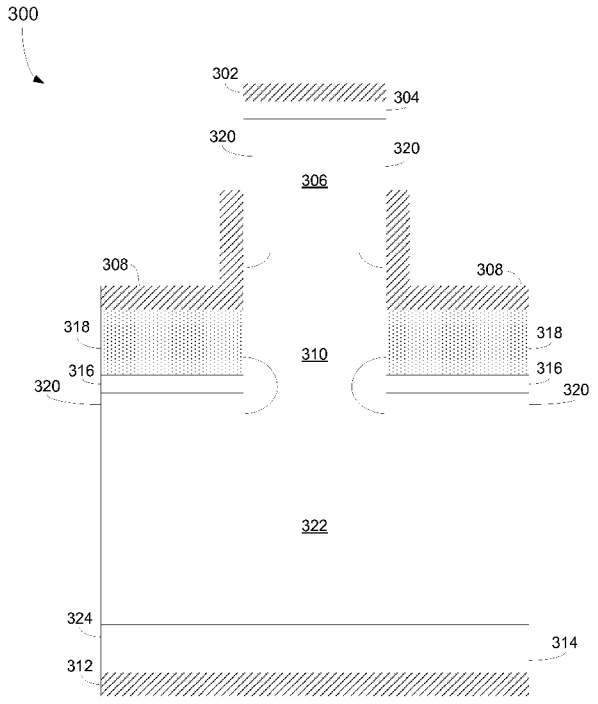

FIGURE 3

(57) **Abstract**: An assembly includes a collector, an emitter, and a gate. The assembly further includes a channel positioned between the collector and the emitter, a depletion layer positioned between the collector and the emitter, a plurality of second N^+ doped regions positioned about the channel to establish a junction between the collector and the gate, and an N^+ doped substrate positioned between the emitter and the depletion layer. The depletion layer includes buried anodes and a plurality of first N^+ doped regions. The plurality of first N^+ doped regions are configured such that they are normally closed, thereby impeding current flow through the vertical channel between the collector and the emitter. In response to a voltage difference between the collector and the gate exceeding a threshold level, the plurality of first N^+ doped regions open, thereby resulting in current flow between the collector and emitter.

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A VOLTAGE-GATED BIPOLAR TRANSISTOR FOR POWER SWITCHING APPLICATIONS

RELATED APPLICATION

[0001] This application hereby claims priority to U.S. Provisional Patent Application No. 61/558,415 filed November 10, 2011, entitled "VOLTAGE-GATED BIPOLAR TRANSISTOR FOR POWER SWITCHING APPLICATIONS," the disclosure of which is incorporated herein by reference.

BACKGROUND

[0002] The present disclosure is related to bipolar transistors for power switching applications. More specifically, the present disclosure is related to a voltage-gated bipolar transistor.

[0003] Electronics based power supplies are becoming increasingly common in commercial industry applications. Recent reports have indicated that the commercial market for discrete power semiconductor devices will continue to drastically increase in the coming years, due in part to increased demand from hybrid electric vehicle manufacturers, the solar power industry, the wind energy industry, and other similar developing industries.

[0004] Currently, the majority of the semiconductor market is dominated by Metal-Oxide-Semiconductor Field-Effect Transistors ("MOSFETs") and Insulated Gate Bipolar Transistors ("IGBTs"). Typically, these components were manufactured from silicon ("Si"). However, silicon carbide ("SiC") has emerged as a viable replacement for conventional Si due to various advantages. For example, SiC is over 700 times better than conventional Si for power semiconductor switching. Additionally, SiC typically improves efficiency of a

switching device by over 20% while providing for design and fabrication of switching devices having a smaller form factor than those using conventional Si.

[0005] However, despite the advantages, SiC switching devices have several drawbacks. For example, a SiC IGBT typically suffers from three fundamental problems: (1) low gate oxide reliability; (2) long term threshold voltage drift; and (3) low channel mobility.

SUMMARY

[0006] In one general respect, the embodiments disclose an assembly. The assembly includes a collector terminal, an emitter terminal, and a gate terminal; a vertical channel positioned between the collector terminal and the emitter terminal, wherein the gate is positioned adjacent to the vertical channel; a depletion layer positioned between the collector terminal and the emitter terminal, and adjacent to the vertical channel; a plurality of second N^+ doped regions positioned about the vertical channel and configured to establish a junction between the collector terminal and the gate; and an N^+ doped substrate positioned between the emitter terminal and the depletion layer. The depletion layer includes a plurality of buried anodes, and a plurality of first N^+ doped regions, at least one N^+ doped region adjacent to each of the plurality of buried anode. The plurality of first N^+ doped regions are configured such that they are normally in a closed position, thereby impeding current flow through the vertical channel between the collector terminal and the emitter terminal. In response to a voltage difference between the collector terminal and the gate terminal exceeding a threshold level, the plurality of first N^+ doped regions move into an open position.

[0007] According to an alternative embodiment, the assembly as described above may also include a drift layer positioned between the depletion layer and the N^+ doped substrate. In

another embodiment wherein the drift layer has a P doping. In a specific example, the P doping of the drift layer is about 2 X 10^{14} cm^{-3}.

[0008] According to an alternative embodiment, the assembly as described above may also include an insulation layer positioned between the gate terminal and the plurality of first N^+ doped regions. In one or more additional embodiment, the insulation layer is constructed from at least one of silicon oxide, silicate, and one or more polymers.

[0009] According to an alternative embodiment, the depletion layer may have a P doping. In one or more additional embodiments, the P doping of the depletion layer may be about 5 X 10^{16} cm^{-3}.

[0010] According to an alternative embodiment, the collector terminal may be positioned adjacent to a P^{++} doped mesa component.

[0011] According to an alternative embodiment, the N^+ doped substrate may include 4H silicon carbide.

[0012] According to an alternative embodiment, the gate terminal may further include a gate drive input. In one or more additional embodiments, the gate drive input may be supplied by an output of a junction gate field-effect transistor.

BRIEF DESCRIPTION OF THE FIGURES

[0013] FIG. 1 is a schematic illustration of an exemplary IGBT including a MOSFET.

[0014] FIG. 2 is a schematic illustration of an exemplary voltage-gated bipolar transistor.

[0015] FIG. 3 is a cross-sectional view of an exemplary voltage-gated bipolar transistor.

[0016] FIG. 4 is a detailed cross-sectional view of an exemplary voltage-gated bipolar transistor.

[0017] FIG. 5 is a graph depicting an off-state mode of an exemplary voltage-gated bipolar transistor.

[0018] FIG. 6 is a graph depicting on-state characteristics of an exemplary voltage-gated bipolar transistor.

[0019] FIGS. 7 and 8 each comprise a graph depicting effects of opening a vertical channel in an exemplary voltage-gated bipolar transistor.

[0020] FIGS. 9 and 10 each comprises a graph depicting effects of spreading layer doping concentrations in an exemplary voltage-gated bipolar transistor.

DETAILED DESCRIPTION

[0021] This disclosure is not limited to the particular systems, devices and methods described, as these may vary. The terminology used in the description is for the purpose of describing the particular versions or embodiments only, and is not intended to limit the scope.

[0022] As used in this document, the singular forms "a," "an," and "the" include plural references unless the context clearly dictates otherwise. Unless defined otherwise, all technical and scientific terms used herein have the same meanings as commonly understood by one of ordinary skill in the art. Nothing in this disclosure is to be construed as an admission that the embodiments described in this disclosure are not entitled to antedate such disclosure by virtue of prior invention. As used in this document, the term "comprising" means "including, but not limited to."

[0023] The present disclosure is directed to a Voltage-Gated Bipolar Transistor ("VGBT") that offers the desired characteristics of an IGBT without the fundamental problems addressed above. In general, SiC power devices have advantageous properties including, but not limited to, a wider band gap, larger critical electrical field, and higher thermal conductivity that allows them to operate at higher temperatures and voltages, in addition to higher power and current densities, over conventional Si devices. These properties allow the SiC devices to operate at much higher voltage levels. SiC based devices also result in reduced conduction and switching losses, thus offering higher efficiencies in electronic systems.

[0024] However, as addressed above, typical SiC devices have several fundamental problems, including low gate oxide reliability, long term threshold voltage drift, and low channel mobility. FIG. 1 illustrates an exemplary conventional IGBT **100**. In the IGBT **100**, a MOSFET **108** provides base current to an integrated NPN Bipolar Junction Transistor ("BJT") **101**. The BJT **101** includes a collector terminal **102**, an emitter terminal **104**, and a gate terminal **106**. Typically, a gate drive connects to the gate terminal **106**, while the collector terminal **102** and the emitter terminal **104** are connected to a power portion of a circuit. As the voltage increases on the gate drive, the voltage between the gate terminal **106** and the emitter terminal **104** increases above a threshold level (e.g., about 5 volts). Once the threshold level is exceeded, the BJT **101** turns on, thereby activating the IGBT **100**.

[0025] In typical IGBTs, the overall voltage tolerance of the components used is low. As such, a typical IGBT may not be useful in high voltage circuits. To increase the voltage tolerance levels, a MOSFET **108** may be used to provide the gate drive voltage. The MOSFET **108** includes a drive terminal **110**, a source terminal **112**, a gate terminal **114**, and a body terminal **116**. However, as shown in FIG. 1, the body terminal **116** is typically

connected to the source terminal **112**, thereby resulting in a three terminal device, similar to the BJT **101**.

[0026] As shown in FIG. 1, the source terminal **112** of the MOSFET **108** may be used as the gate drive of the BJT **101**. This arrangement provides a switching device configured to operate at higher voltage and thermal levels as the MOSFET **108** is capable of operating at operational levels higher than that of a conventional BJT.

[0027] FIG. 2 illustrates an exemplary VGBT **200**. VGBT **200** may include a Junction Gate Field-Effect Transistor ("JFET") **208** for providing a base current to an integrated NPN BJT **201**. The BJT **201** may include a collector terminal **202**, an emitter terminal **204**, and a gate terminal **206**. Typically, a gate drive connects to the gate terminal **206**, while the collector terminal **202** and the emitter terminal **204** are connected to a power portion of a circuit. As the voltage increases on the gate drive, the voltage between the gate terminal **206** and the emitter terminal **204** increases above a threshold level. As a result, the BJT **201** turns on, thereby activating the VGBT **200**. As such, the VGBT **200** is similar in operation to the IGBT **100** shown in FIG. 1.

[0028] As shown in FIG. 2, the VGBT **200** includes a JFET **208** configured to function as a switching device for controlling the gate drive of the gate terminal **206**. The JFET **208** may be configured such that electric charge flows though a semiconducting channel between a drain terminal **210** and a source terminal **212**. By applying a reverse bias voltage to a gate terminal **214** of JFET **208**, the channel may be pinched such that the electric current is impeded or switched off completely. The amount of current flow through the channel is dependent upon the electric field between the source **212** terminal and the drain **210** terminal

[0029] Construction of a JFET, including the conducting channel, is accomplished by exploiting the field effect. As a voltage between the gate and source is applied to reverse bias

the gate-source junction, a depletion layer of this junction is thereby widened, encroaching upon the conducting channel and thus restricting the cross-sectional area of the channel, impeding or switching off the current flow completely.

[0030] FIG. 3 illustrates a cross-sectional view of an exemplary VGBT **300**, similar in function and component arrangement as VGBT **200** of in FIG. 2. The VGBT **300** may include an anode **302**, similar to the collector terminal **202** of FIG. 2. The anode **302** may be positioned on a P^+ mesa **304**. The P^+ mesa **304** is positioned above a vertical channel **306**. A gate **308** may be positioned adjacent to the vertical channel **306** and a depletion layer **310**. A cathode **312**, similar to the emitter terminal **204** of FIG. 2, may be positioned adjacent to a substrate layer **314**. The substrate layer **314** may be an N^+ doped layer formed from a one or more polytypes of SiC. For example, 4H-SiC may be used to construct the substrate layer **314** as 4H polytypes of SiC provide high electron mobility. Embodiments of the present invention are not limited in this regard.

[0031] Additional buried anodes **316** may be positioned adjacent each other within the depletion layer **310**. The anodes **316** may be isolated from the gate **308** by an insulation layer **318**. The insulation layer **318** may be constructed from a material having a high insulation rating such as silicon oxide, a silicate such as mica, one or more polymers such as thermoplastic, rubber, or other various insulating materials.. However, it should be noted that these materials are listed by way of example only.

[0032] Multiple N^+ doped regions **320** may be integrated within the VGBT **300** as well. For example, a pair of N^+ doped regions **320** may be positioned adjacent to each other in the channel **306**. Additionally, a pair of N^+ doped regions **320** may be positioned about the buried anodes **316** within the depletion layer **310**.

[0033] The gate **308** may be operably connected to the N+ doped regions **320** positioned adjacent to each other in the channel **306** via one or more ohmic gate contacts (not shown). An ohmic gate contact is a low interference contact typically used in JFET manufacture. For example, an ohmic gate contact may be manufactured out of alternative thin layers of gold and zinc at a total thickness of about 3000 angstroms. Such an ohmic gate contact may have a contact resistance of about 3.7 X 10^{-5} ohms/cm^2, thereby maintaining a relatively unobstructed junction between the gate **308** and the collector terminal **302**.

[0034] A drift layer **322** may be constructed from, for example, a lightly doped P^- material. Also, the drift layer **322** may be positioned adjacent the depletion layer **310** and separated from the N^+ substrate **314** by a buffer layer **324**. It should be noted that the arrangement of the components as shown in FIG. 3 is by way of example only.

[0035] In order to manufacture the VGBT as shown in FIG. 3, typical integrated circuit manufacturing techniques such as pick and place assembly or complimentary metal-oxide-semiconductor (CMOS) assembly techniques may be used. For example, the individual components as shown in FIG. 3 may be assembled in a stacking fashion, beginning with the cathode **312** and assembling each layer or component sequentially, moving from the bottom to the top of FIG. 3. Various masks and doping materials may be used to manufacture the doped layers per standard manufacturing techniques.

[0036] In typical transistor production, doping intentionally introduces impurities into an extremely pure semiconductor, such as the silicon carbide as used herein or other semiconductor materials such as gallium arsenide, for the purposes of modulating the electrical properties of the semiconductor. For example, during synthesis of n- type doped semiconductors, a vapor-phase epitaxy process may be used. In vapor-phase epitaxy, a gas containing the negative dopant is passed over a semiconductor substrate wafer. For example,

hydrogen sulfide may be passed over the substrate wafer. During the process, sulfur is incorporated into the substrate wafer. The reaction conditions for such a vapor-phase epitaxy may be, for example, at a temperature range of 600 to 800°C for a duration of 6-12 hours.

[0037] Some dopants are added as the actual substrates as produced, giving each substrate wafer an almost uniform initial doping. To define circuit elements, selected areas, typically controlled by photolithography, are further doped by such processes as diffusion and ion implantation. When dopants are on the order of about one dopant atom per 100 million substrate atoms, the doping level is considered low or light. As the number of dopants increases, for example to one dopant atom per ten thousand substrate atoms, the doping level is referred to as high or heavy, and is typically represented as n+ for n-type doping, or p+ for p-type doping. Higher ratios of dopant atoms to substrate atoms may further be represented as n++ or p++.

[0038] For semiconductors such as silicon and silicon carbide, elements such as boron, arsenic, phosphorus and gallium are used as dopants. Boron is typically used for p-type doping of silicon and silicon carbide as it diffuses at a rate that makes junction depths easily controllable. To produce an n-type doped substrate, phosphorus may be used to dope the silicon carbide. During doping with phosphorus, extra valence electrons are added that become unbonded from individual atoms, thereby allowing the substrate to be an electrically conductive n-type semiconductor.

[0039] It should be noted that the materials and doping processes and techniques as discussed herein are by way of example only. Additional materials may be used to create the semiconductor substrate wafers used to assemble the VGBTs as discussed herein. Similarly, additional elements may be used to dope the substrate wafers to achieve a desired doping level, as determined by the intended function of the assembled VGBT.

[0040] Referring again to FIG. 3, in its off state, the VGBT **300** may have zero gate bias. The voltage applied between the collector (e.g., anode **302**) and the emitter (e.g., cathode **312**) may be supported by the N^+-P^- junction formed by the buried N^+ collectors **320** and the lightly doped P^- drift layer **322**. It should be noted that, in the off state, the space between the two adjacent N^+ collector regions **320** within the depletion layer **310** is zero, thereby closing the vertical channel **306** and eliminating any current flow through the channel. A VGBT that is designed and manufactured to be normally-off may be initially in this state.

[0041] To turn on the VGBT **300**, a positive gate bias may be applied between the gate **308** and the collector (e.g., anode **302**) until the gate bias exceeds a threshold level (e.g., 5V). When the gate bias exceeds the threshold level, the two adjacent N^+ buried connectors regions **320** open or move apart within the depletion layer **312**. Consequently, a current may pass through the vertical channel **306**.

[0042] To turn off the VGBT **300**, the positive gate bias may be removed between the gate **308** and the collector (e.g., anode **302**). Removal of the gate bias may result in the two adjacent N^+ buried connectors regions **320** moving together, thereby closing the space between the two adjacent N^+ buried collector regions and effectively closing the vertical channel **306**. By closing the channel **306**, the VGBT **300** may impede or eliminate any current flow through the channel.

[0043] As such, the VGBT **300** functions similar to an IGBT having a MOSFET. However, several of the fundamental drawbacks of the IGBT having a MOSFET are eliminated. For example, gate oxide and its related problems such as increased leakage current and increased response time are eliminate through the use of the JFET for controlling the power switching.

[0044] Referring now to FIG. 4, there is provided a schematic illustration of an exemplary VGBT **400**. The VGBT **400** may have a width **A** selected in accordance with a particular application. The width **A** may be selected based on the sizes of the individual components used during manufacture and the tolerances that the VGBT **400** may be required to operate within. In some scenarios, the VGBT **400** may have a width **A** falling within the range of 3.5 μm to 4.00 μm, inclusive. Values within the stated range (i.e., 3.5 μm to 4.00 μm) ensure that the VGBT **400** operates at up to about 200°C and provides a blocking voltage of about 15.7 kV.

[0045] An anode **402** may be positioned on a P^{++} doped mesa **404**. The P^{++} doped mesa **404** is positioned above a vertical channel **406**. The width **B** of the P^{++} doped mesa **404** may be selected in accordance with a particular application. The width **B** may be selected based on the operational tolerances of the VGBT **400**. In some scenarios, the width **B** has a value falling within a range of 1.50 μm to 2.00 μm, inclusive. Values within the stated range (i.e., 1.50 μm to 2.00 μm) ensure that the VGBT **400** operates at up to about 200°C and provides a blocking voltage of about 15.7 kV.

[0046] A gate **408** may be positioned about the vertical channel **406** and adjacent to a depletion layer **410**. The gate **408** is operably connected to the N+ doped regions **420**. The N+ doped regions **420** are positioned adjacent to each other in the vertical channel **406** via one or more ohmic gate contacts (not shown). An ohmic gate contact is a low interference contact typically used in JFET manufacture. For example, an ohmic gate contact may be manufactured out of alternative thin layers of gold and zinc at a total thickness of about 3000 angstroms. Such an ohmic gate contact may have a contact resistance of about 3.7×10^{-5} ohms/cm^2, thereby maintaining a relatively unobstructed junction between the gate **408** and the anode **402**.

[0047] The depletion layer **410** may have various doing levels dependant upon the intended functionality of the VGBT **400**. For example, to operate at up to about 200°C and provide a blocking voltage of about 15.7 kV, the depletion layer **410** may have a P doping level of about $P = 5 \times 10^{16}$ cm^{-3}. Additionally, the depletion layer **410** may be about 1.7 μm in height.

[0048] A cathode **412** may be positioned adjacent to a substrate layer **414**. The substrate layer **414** may be an N^+ doped layer, formed from a one or more polytypes of SiC. For example, 4H-SiC may be used to construct the substrate layer **414** as 4H polytypes of SiC provide high electron mobility.

[0049] Additional buried N^{++} doped anodes **416** may be positioned adjacent to each other within the depletion layer **410**. The N^{++} doped anodes **416** is isolated from the gate **408** by an insulation layer **418** constructed from one or more of various materials including, but not limited to, silicon oxide, a silicate such as mica, one or more polymers such as thermoplastic, rubber, or other various insulating materials. Additionally, multiple N^+ doped regions **420** may be integrated within the VGBT **400** as well. For example, a pair of N^+ doped regions **420** may be positioned adjacent to each other in the vertical channel **406**. Additionally, a pair of N^+ doped regions **420** may be positioned about the buried N^{++} doped anodes **416** within the depletion layer **410**.

[0050] A lightly doped drift layer **422** is positioned adjacent the depletion layer **410**. The lightly doped drift layer **422** is separated from the N^+ substrate **414** by a P doped buffer layer **424**. The lightly doped drift layer **422** and the P doped buffer layer **424** may have various doing levels dependant upon the intended functionality of the VGBT **400**. For example, to operate at up to about 200°C and provide a blocking voltage of about 15.7 kV, the lightly doped drift layer **422** may have a P doping level of about $P^- = 2 \times 10^{14}$ cm^{-3}. Also, the P

doped buffer layer **424** may have a P doping level of about P = 2 X 10^{17} cm^{-3}. Additionally, the lightly doped drift layer **422** may be about 0.7 μm in height. The P doped buffer layer **424** may be about 1.7 μm in height.

[0051] It should be noted that the arrangement of the components as shown in FIG. 4, as well as the sizing and doping information, is provided by way of example only. A VGBT designed and constructed to operate at alternative tolerance levels may have one or more components altered in size and doping levels to accommodate the alternative tolerance levels.

[0052] Referring now to FIG. 5, there is provided a graph depicting the off-state or blocking mode of the VGBT **400** of FIG. 4 operating at 200°C and having zero gate bias. As shown in the graph of FIG. 5, the maximum blocking voltage is about 15.7kV.

[0053] Referring now FIG. 6, there is provided a graph depicting the on-state or forward conduction characteristics of the VGBT **400** of FIG. 4 operating at 200°C and having zero gate bias. As shown in the graph, the $J_E = (I_{Cathode}) = 168A/cm^2$, $J_G = 1A/cm^2$ at $V_G = 2.57V$ and $V_{CE} = 5V$.

[0054] FIGS. 7 and 8 illustrate related graphs depicting effects of a vertical channel, for example vertical channel **406** of VGBT **400**. As shown in FIG. 7, as the width W_{VC} of the vertical channel **406** increases from 0.74 μm to 0.84 μm, the blocking voltage is decreased slightly. However, as shown in FIG. 8, as the width W_{VC} of the vertical channel **406** increases from 0.74 μm to 0.84 μm, the current density at the emitter J_E increases from 91 A/cm^2 to 120 A/cm^2 at $V_{CE} = 5V$.

[0055] FIGS. 9 and 10 illustrate related graphs depicting effects spreading the doping layer concentration in the depletion layer, for example depletion layer **410** of the VGBT **400**. As shown in FIG. 9, by increasing the doping concentration of the depletion layer **410** from P =

5×10^{16} cm^{-3} to $P = 1 \times 10^{16}$ cm^{-3}, the blocking voltage is increased from 15.7kV to about 16.25kV. However, as shown in FIG. 10, increasing the doping concentration of the depletion layer **410** from $P = 5 \times 10^{16}$ cm^{-3} to $P = 1 \times 10^{16}$ cm^{-3} reduces the current density at the emitter from 91 A/cm^2 to about 22 A/cm^2.

[0056] It should be noted that FIGS. 5-10 are provided by way of example only to show a specific embodiment of the VGBT **400** operating at 200°C. By altering various operation conditions, alternative results may be produced during operation of the VGBT **400**.

[0057] Various of the above-disclosed and other features and functions, or alternatives thereof, may be combined into many other different systems or applications. Various presently unforeseen or unanticipated alternatives, modifications, variations or improvements therein may be subsequently made by those skilled in the art, each of which is also intended to be encompassed by the disclosed embodiments.

CLAIMS

What is claimed is:

1. An assembly comprising:

a collector terminal, an emitter terminal, and a gate terminal;

a vertical channel positioned between the collector terminal and the emitter terminal, wherein the gate is positioned adjacent to the vertical channel;

a depletion layer positioned between the collector terminal and the emitter terminal, and adjacent to the vertical channel, the depletion layer comprising:

a plurality of buried anodes, and

a plurality of first N^+ doped regions, at least one N^+ doped region adjacent to each of the plurality of buried anodes;

a plurality of second N^+ doped regions positioned about the vertical channel and configured to establish a junction between the collector terminal and the gate; and

an N^+ doped substrate positioned between the emitter terminal and the depletion layer;

wherein the plurality of first N^+ doped regions are normally in a closed position, thereby impeding current flow through the vertical channel between the collector terminal and the emitter terminal, and

wherein the plurality of first N^+ doped regions move into an open position in response to a voltage difference between the collector terminal and the gate terminal exceeding a threshold level.

2. The assembly of claim 1, further comprising a drift layer positioned between the depletion layer and the N^+ doped substrate.

3. The assembly of claim 2, wherein the drift layer has a P doping.

4. The assembly of claim 3, wherein the P doping of the drift layer is about 2 X 10^{14} cm^{-3}.

5. The assembly of claim 1, further comprising an insulation layer positioned between the gate terminal and the plurality of first N^+ doped regions.

6. The assembly of claim 5, wherein the insulation layer is constructed from at least one of silicon oxide, silicate, and one or more polymers.

7. The assembly of claim 1, wherein the depletion layer has a P doping.

8. The assembly of claim 7, wherein the P doping of the depletion layer is about 5 X 10^{16} cm^{-3}.

9. The assembly of claim 1, wherein the collector terminal is positioned adjacent to a P^{++} doped mesa component.

10. The assembly of claim 1, wherein the N^+ doped substrate comprises 4H silicon carbide.

11. The assembly of claim 1, wherein the gate terminal further comprises a gate drive input.

12. The assembly of claim 11, wherein the gate drive input is supplied by an output of a junction gate field-effect transistor.

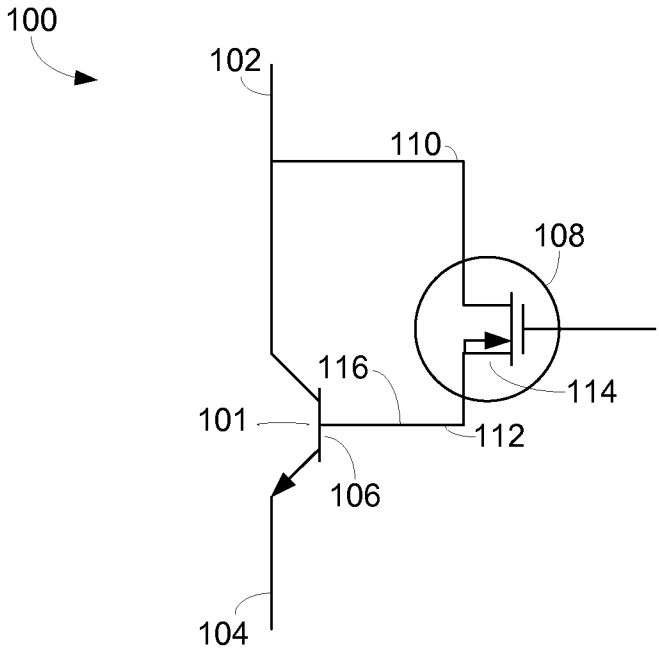

FIGURE 1

Prior Art

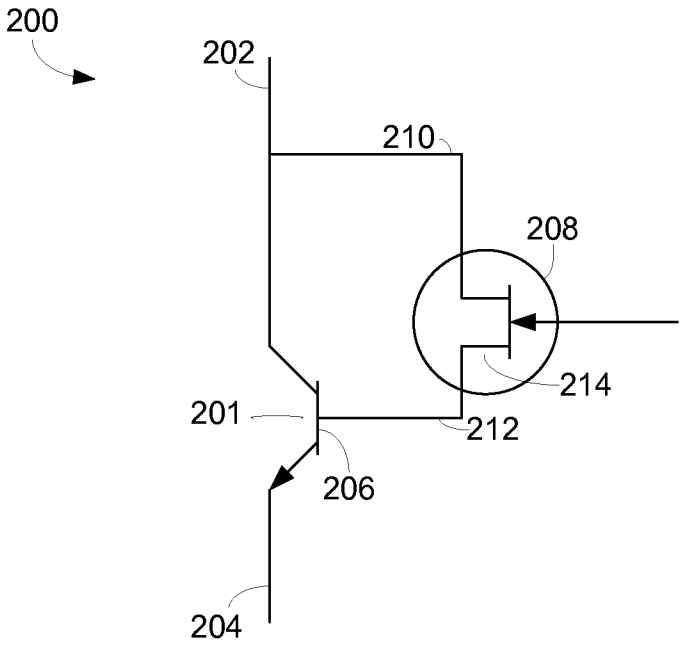

FIGURE 2

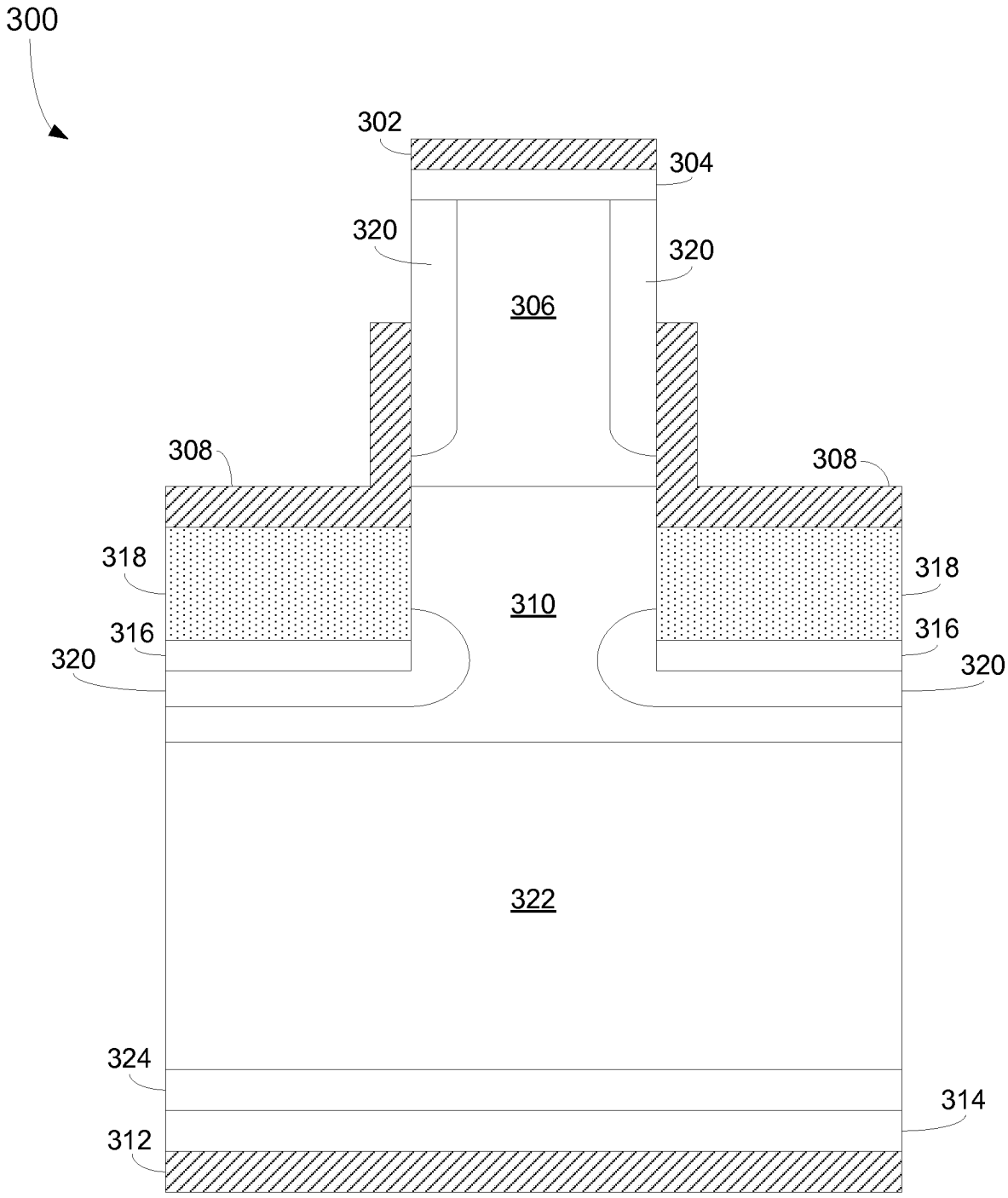
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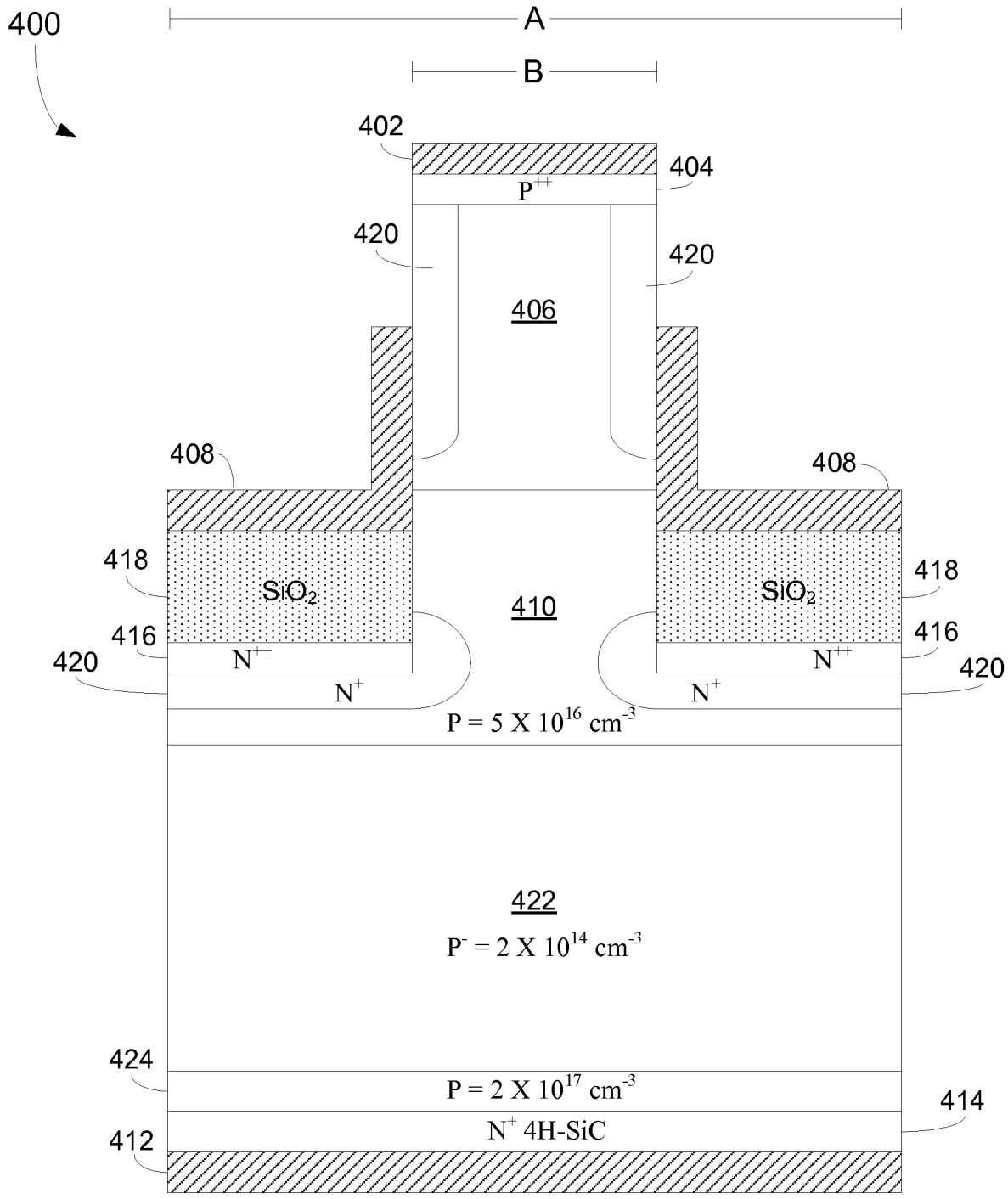
FIGURE 3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420
420
406
408
408
418
SiO2
410
SiO2
418
416
N++
N++
416
420
N+
N+
420
P = 5 X 10^16 cm^-3
422
P- = 2 X 10^14 cm^-3
424
P = 2 X 10^17 cm^-3
414
N+ 4H-SiC
412

FIGURE 4

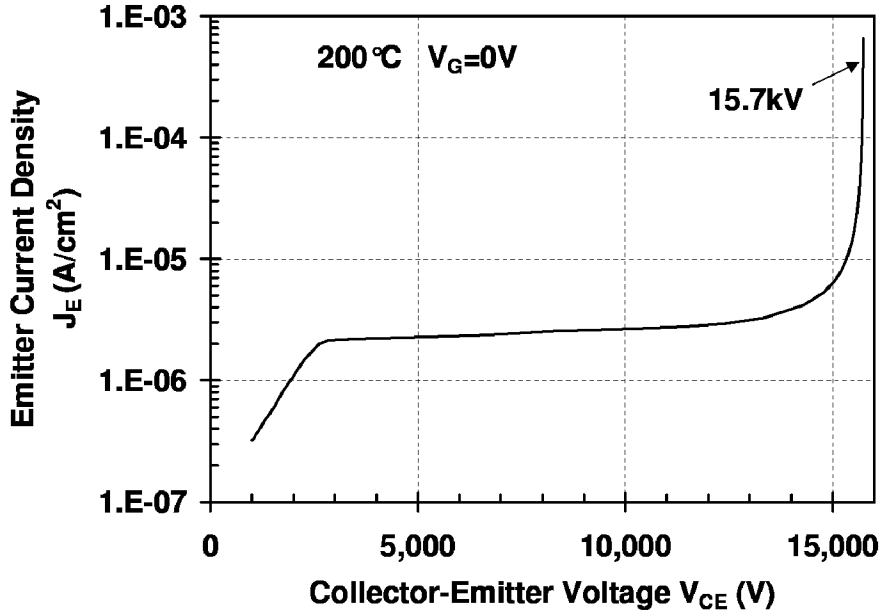

FIGURE 5

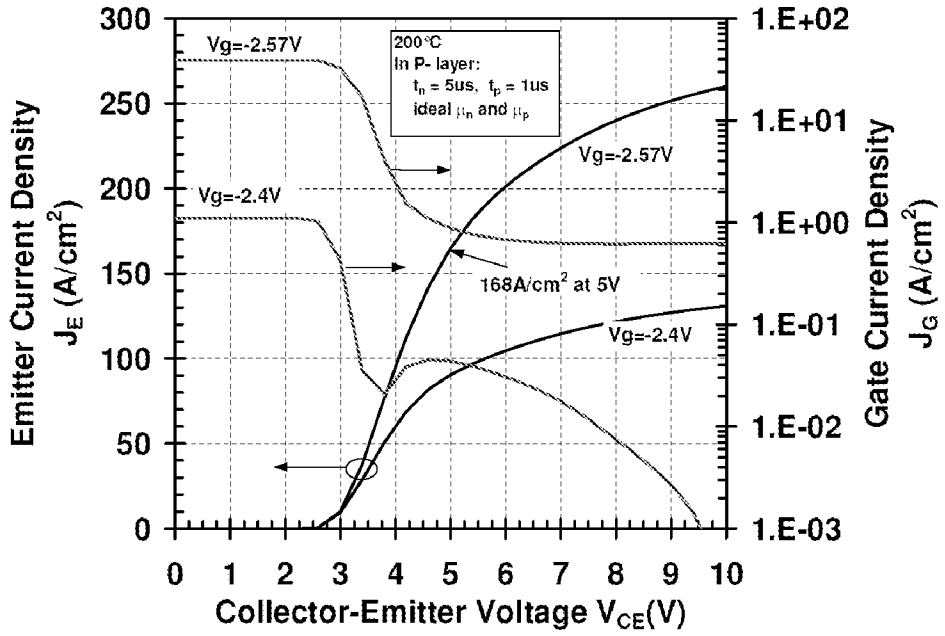

FIGURE 6

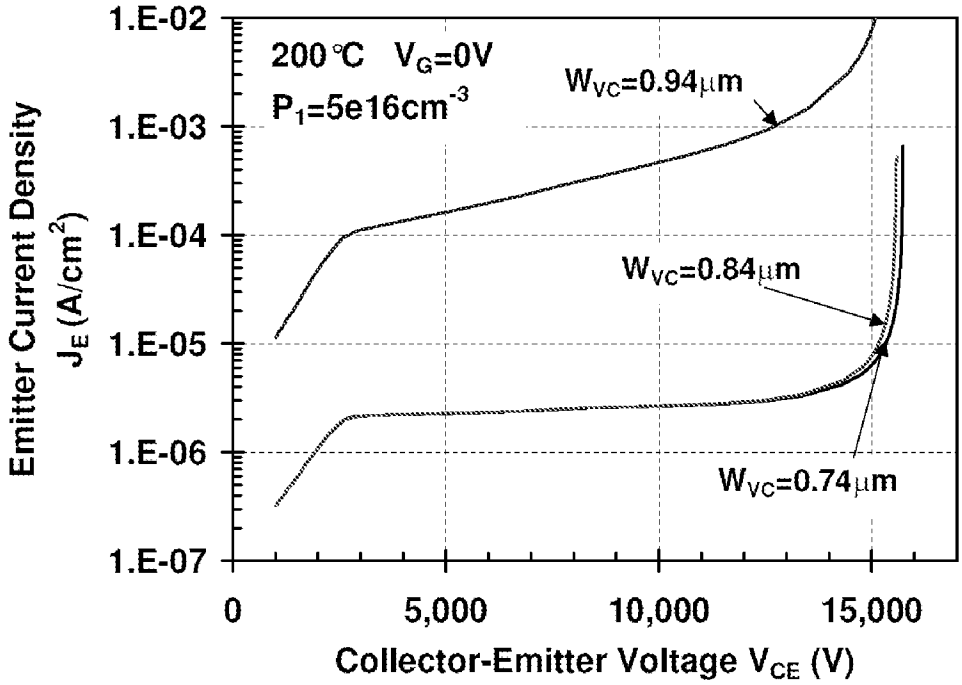

FIGURE 7

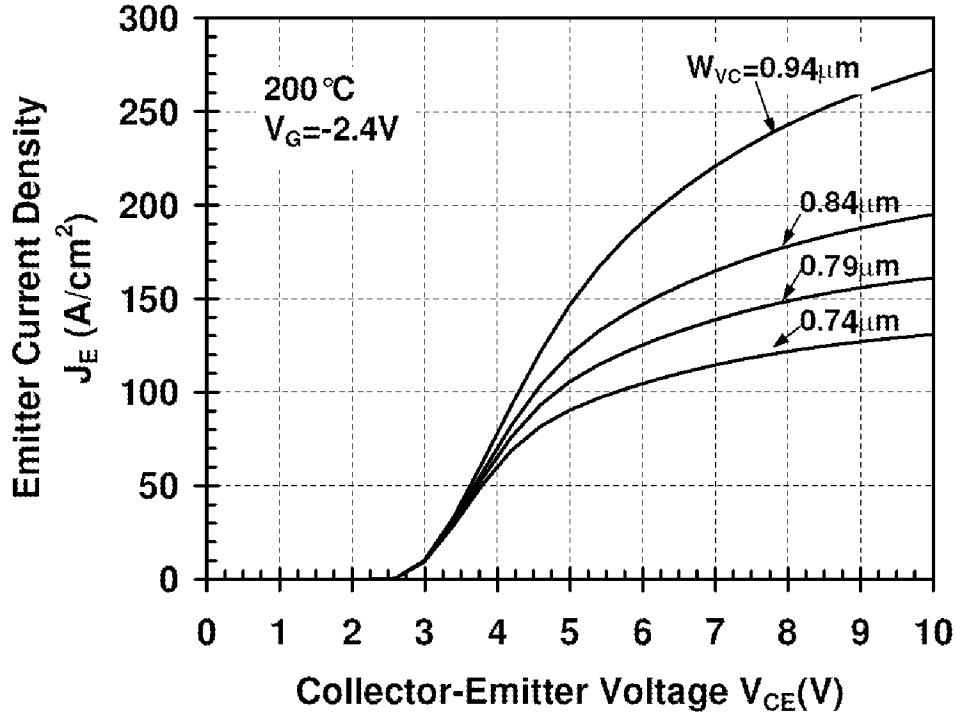

FIGURE 8

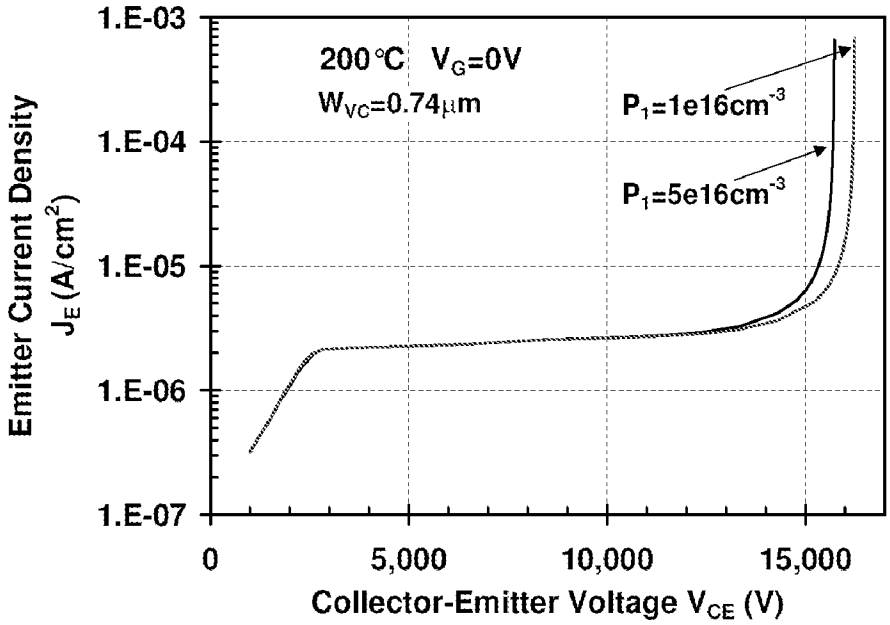

FIGURE 9

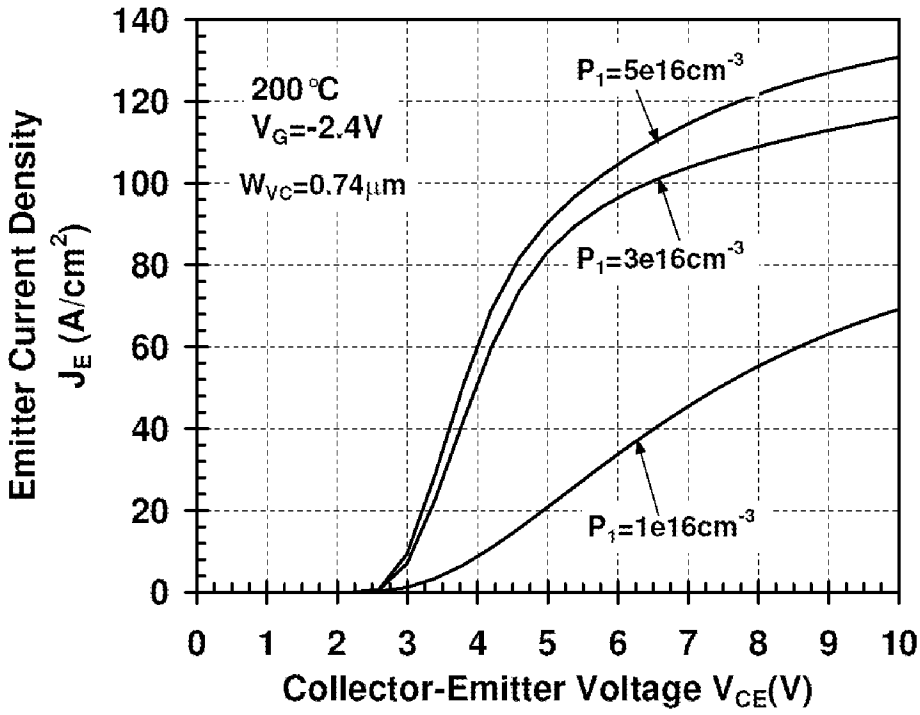

FIGURE 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US12/64315

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/74 (2012.01)
USPC - 257/134
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8): H01L 29/74; H01L 31/111 (2012.01)
USPC: 257/134; 257/135; 257/136; 327/427; 327/108; 327/109

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US-G, US-A, EP-A, EP-B, WO, JP-bib, DE-C,B, DE-A, DE-T, DE-U, GB-A, FR-A); IP.com; Google/Google Scholar; IEEE
Search Terms Used: collector and emitter and gate and drift and (mesa or ridge or vertical) and 4H adj (silicon adj carbide or sic) and voltage adj gated adj bipolar adj transistor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2005/0067630 A1 (ZHAO, J) March 31, 2005; figures 8, 11, 13, paragraphs [0021, 0025]	1-12
Y	US 2011/0254010 A1 (ZHANG, Q) October 20, 2011; figure 2B, paragraphs [0056-0058]	1-12
Y	US 5969378 A (SINGH, R) October 19, 1999; figure 2, column 8, lines 15-35	5-6
Y	US 7782118 B2 (REICHL, J et al.) August 24, 2010; figure 2, column 3, lines 21-52	12

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 December 2012 (30.12.2012)	22 JAN 2013
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)