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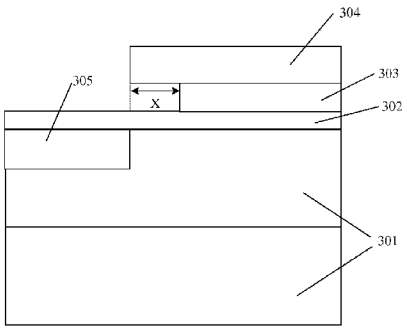
(54) **Title**: METHOD FOR MANUFACTURING METAL-OXIDE-SEMICONDUCT OR FIELD-EFFECT TRANSISTORS

FIG. 4



(57) **Abstract**: A method is disclosed for manufacturing a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). The method includes providing a substrate containing an epitaxial layer, forming a gate oxide layer and a polysilicon layer on the epitaxial layer, and forming a photoresist layer on the polysilicon layer and a gate region pattern in the photoresist layer. The method also includes forming a gate region by etching the polysilicon layer using the gate region pattern in the photoresist layer as a mask. The etching is performed in such a way that the gate region has a lateral surface receding at a predetermined length relative to the gate region pattern in the photoresist layer. Further, the method includes forming a body region by ion implantation and dopant drive-in using the photoresist layer as a mask such that an overlapping area between the body region and the gate region can be reduced based on the predetermined receding length.

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METHOD FOR MANUFACTURING METAL-OXIDE-SEMICONDUCTORFIELD-EFFECT TRANSISTORS

Description

[1] FIELD OF THE INVENTION

[2] The present invention generally relates to the field of semiconductor manufacturing and, more particularly, to methods and processes for manufacturing Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) .

[3] BACKGROUND

[4] To achieve faster operation speed, larger data storage capacity, and more functionalities, semiconductor chips have been developed in the direction towards increasingly higher device density and degrees of integration. This calls for higher standards on physical structures and manufacturing processes of semiconductor devices. For example, in a MOSFET, the size of the overlap between the gate region and the body region significantly affects the input capacitance, gate-source charge and gate-drain charge of the MOSFET. A larger size of the overlap often results in a higher input capacitance and hence worse dynamic characteristics, which further leads to a lower yield rate of the MOSFET.

[5] Figure 1 shows a partial structural diagram of a MOSFET device under a conventional manufacturing process. As shown in Figure 1,a large overlapping area exists between a body region 102 and a gate region 101 of the MOSFET device. Such large overlapping area may cause a large input capacitance and poor dynamic characteristics of the MOSFET device. Such MOSFET device may fail to meet process requirements and may reduce the yield rate as well.

[6] The disclosed methods and devices are directed to solve one or more problems set forth above and other problems.

[7] BRIEF SUMMARY OF THE DISCLOSURE

[8] One aspect of the present disclosure includesa method for manufacturing a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). The method includes providing a substrate containing an epitaxial layer, forming a gate oxide layer and a polysilicon layer on the epitaxial layer, and forming a photoresist layer on the polysilicon layer and a gate region pattern in the photoresist layer. The method also includes forming a gate region by etching the polysilicon layer using the gate region pattern in the photoresist layer as a mask. The etching is performed in such a way that the gate region has a lateral surface receding at a predetermined length relative to the gate region pattern in the photoresist layer. Further, the method includes forming a body region by ion implantation and dopant drive-in using the photoresist layer as a

mask such that an overlapping area between the body region and the gate region can be reduced based on the predetermined receding length.

[9] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

[10] BRIEF DESCRIPTION OF THE DRAWINGS

[11] Figure 1 is a partial structural diagram of a conventional MOSFET;

[12] Figure 2 illustrates a flow chart of a method for manufacturing a MOSFET consistent with the disclosed embodiments;

[13] Figure 3 illustrates a MOSFET device after forming a gate region consistent with the disclosed embodiments;

[14] Figure 4 illustrates a MOSFET device after forming a body region consistent with the disclosed embodiments;

[15] Figure 5 illustrates a MOSFET device after forming a source region consistent with the disclosed embodiments;

[16] Figure 6 illustrates diffusion functions of a body region and a source region in a cross-section of a semiconductor unit cell corresponding to different receding lengths; and

[17] Figure 7 illustrates a partial structural diagram of a MOSFET deviceconsistent with the disclosed embodiments.

[18] DETAILED DESCRIPTION

[19] Reference will now be made in detail to exemplary embodiments of the invention, which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[20] Figure 2 illustrates an exemplary process for manufacturing a MOSFET device. As shown in Figure 2, after a semiconductor substrate is provided, a gate oxide layer and a subsequent polysilicon layer are formed on a surface of an epitaxial layer of the semiconductor substrate (S201).

[21] The semiconductor substrate may include any appropriate material for making MOSFETs . For example, the substrate may include a semiconductor structure, e.g., silicon, silicon germanium (SiGe) with a monocrystalline, polycrystalline, or amorphous structure. The substrate may also include a hybrid semiconductor structure, e.g., carborundum, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide orgallium antimonide, alloy semiconductor, or a combination thereof. Further, the substrate may include a silicon-on-insulator (SOI) structure. In addition, the substrate may also include other materials, such as a multilayered structure of epitaxial layer or buried layer. Other materials may also be used.

[22] The semiconductor substrate may include an epitaxial layer. T he epitaxial layer may

be an N^--N^+ structure formed on the semiconductor substrate, and the thickness of the epitaxial layer may be determined according to the specific requirements of applications. Further, the epitaxial layer may be on the front or back of the semiconductor substrate .

[23] A gate oxide layer may be formed on the surface of the epitaxial layer of the semiconductor substrate by thermal oxidization. The gate oxide layer may include at least silicon oxide and may have a thickness of approximately 20-50 Å. Further, a polysilicon layer may be formed in various steps. For example, these steps include loading the semiconductor substrate with the gate oxide layer into a low pressure chemical vapor deposition tool, and introducing silane into the deposition chamber. When the silane decomposes, polysilicon is deposited on the surface of the gate oxide layer and the polysilicon layer may have a thickness of about 5000 Å. In addition, the polysilicon deposition process may be followed by a polysilicon doping process.

[24] After forming the gate oxide layer and the polysilicon layer (S201), a gate region is formed (S202). The gate region may be formed by first coating a photoresist layer on the polysilicon layer, forming a gate region pattern in the photoresist layer using photolithography, and then etching the polysilicon layer using the gate region pattern as a mask. The etching process on the polysilicon layer is performed in such a way that the formed gate region has a lateral surface receding at a predetermined length relative to the gate region pattern in the photoresist layer.

[25] That is, in the photoresist layer, the gate region pattern is formed through exposure and developing. Then, the polysilicon layer outside the gate region pattern is removed by erosion to form the gate region. Figure 3 shows a corresponding device after forming the gate region.

[26] As shown in Figure 3, the semiconductor substrate (not numbered) includes an epitaxial layer 301, which has an N^--N^+ structure. A gate oxide layer 302 is formed on the semiconductor substrate (i.e., the epitaxial layer 301) and a polysilicon layer is formed on the gate oxide layer 302. Further, a gate region pattern 304 is formed in a photoresist layer, which is formed on the polysilicon layer. The gate region 303 is then formed after etching the polysilicon layer using the gate region pattern 304 as a mask. After the gate region 303is formed, the formed gate region 303 has a lateral surface receding at a predetermined length *X* relative to the gate region pattern 304 in the photoresist layer.

[27] The polysilicon layer may be etched using isotropic plasma or by wet chemical etching. Because the polysilicon layer is etched at the same etching rate in all directions (e.g., an isotropic etching process), the lateral surface of the polysilicon layer directly under the gate region pattern 304 in the photoresist layer is eroded. Thus, the width of the obtained polysilicon gate 303 is less than the width of the gate region

pattern 304 in the photoresist layer. That is, the lateral surface of the formed gate region 303 recedes at a predetermined length relative to the gate region pattern in the photoresist layer.

[28] Further, a body region is formed by an ion implantation and dopant drive-inprocess (S203). The photoresist layer is used as a mask when forming the body region. In other words, the photoresist layer is not removed directly after S202. Instead, the photoresist layer is used as a mask during the ion implantation and dopant drive-in process when forming the body region. During ion implantation for the body region, the gate oxide layer on the surface of the epitaxial layer may be used to control the depth of the ion implantation.

[29] As shown in Figure 4, a body region 305 is formed by, for example,an ion implantation process.As previously explained, the etching process on the polysilicon layer is performed in such a way that the formed gate region 303 has a lateral surface receding at a predetermined length X relative to the gate region pattern 304 in the photoresist layer. During the ion implantation process forming the body region 305, because the ion implantation process uses the gate region pattern 304 in the photoresist layer as a mask, the resulting body region 305has an end away from the formed gate region 303. Thus, the overlapping area between the body region 305 and the gate region303 can be reduced.

[30] After forming the body region (S203), the photoresist layer is removed (S204). That is, after the body region is formed, the photoresist layer on the surface of the semiconductor substrate (e.g., the polysilicon layer)is no longer be used, and is removed completely. Specifically, the photoresist layer on the surface of the semiconductor substrate may be removed by wet etching, e.g., immersing the photoresist layer in a photoresist-removing solution to dissolve and remove the photoresist layer.

[31] Further, a source region is formed in the body region (S205).A portion of the gate oxide layer within a predetermined region for the source region is removed. The source region may be formed by implanting ions in the body region using the gate oxide layer as a mask. T he portion of the gate oxide layer within the source region may be removed by etching, as explained above. Figure 5 shows a corresponding device after forming the source region.

[32] As shown in Figure 5, a source region 306 is formed in the body region 305. The body region is formed in epitaxial layer 301, and the gate region 303 and the gate oxide layer 302 are formed on the epitaxial layer 301.

[33] More specifically, 'A' is the length of the overlap between the gate regionand the source regionin the prior art (K^1 with the dotted line is the edge of the body region trench in the prior art). 'B' is the length of the overlap between the gate region 303 and the source region 305 according to the disclosed embodiments (K is the edge of the

body region trench according to the disclosed embodiments). Thus, 'X' is the reduced length of the overlap between the body region and the source region according to the disclosed embodiments compared with the prior art, which is also the predetermined receding length of the lateral surface of the gate region 303 during the etching process forming the gate region 303. The threshold voltage of the device may be determined by the position of the edge K and the ion concentrationat the edge K.

[34] In certain embodiments, the predetermined length that the lateral surface of the formed gate region recedes relative to the gate region pattern in the photoresist layer depends on the type of the device. The upper limit of the predetermined length depends on the desired threshold voltage to be obtained, and the lower limit of the predetermined length depends oncharacteristics of the manufacturing process, such as the production precision and the measurement precision. In certain embodiments, the predetermined length ranges from 0.1μm to 0.5μm. The receding length may be predetermined based on the etching rate and/or time of the etching process forming the gate region 303.

[35] Figure 6 illustrates diffusion functions of the body region and the source region in a cross-section of a semiconductor unit cell corresponding to different receding lengths. As shown in Figure 6, the solid line represents the curve of the diffusion function obtained according to the prior art, the dashed line represents the diffusion function curve with the predetermined receding length of 0.5μm, and the dash-dot line represents the diffusion function curve with the predetermined receding length of 0.7μm. From the solid-line curve, the AB region or AB section is referred as a sloperegion in the body region dopant distribution, and the BC region is referred as a high-gradient concentration region of the body region dopant.

[36] Further, in the cross-section of the body region dopant distribution,there is an initial sloperegion of about 1μm in length, which intersects with the high-gradient concentration region. However, the middle of the sloperegion may be attracted by the source region, and there may be a body region sloperegion of about 0.5μm in length on the right side of the edge K of the body region. Thus, the concentration of body region dopant at the edge of the body region trench may directly determine the threshold voltage of the MOSFET device.

[37] Due to the receding distance of the polysilicon gate region relative to the photoresist pattern, while the source region dopant distribution remain the same in the cross-section,the body region dopant distribution in the cross section is farther away from the gate region. Thus, the edge the body region trench moves along with the body region dopantcross-section. When itis about 0.5μm, K moves to the end of the sloperegion; when it is larger than 0.5μm, K moves to the high-gradient concentration region of body region dopant distribution.Further, when the K is in the high-gradient con-

centration region, the repeatability of the threshold voltage of the MOSFET is significantly decreased.

[38] Additionally or optionally, in the previously described method for manufacturing the MOSFET device, before forming the gate oxide layer and the polysilicon layer, a conduction protecting region may be formed in the semiconductor substrate. The conduction protecting region may be used to protect the device and/orto implement device isolation. To form the conduction protecting region, an oxide protective layer may be first formed on the surface of the epitaxial layer of the semiconductor substrate. Further, a conduction protecting region pattern is formed in the oxide protective layer by photolithography. An ion implantation and dopant drive-in process may be used to implant certain ions and/or drive-in certain dopants to form a well region in the epitaxial layer using the conduction protecting region pattern as a mask. The will region can then be used as the conduction protecting region. Afterwards, the oxide protective layer is removed.

[39] The oxide protective layer may be obtained by introducing oxygen into a high temperature processing chamber to oxidize the silicon substrate. The oxide protective layer may be mainly used as an oxide block layer, controlling the dopingarea and doping depth during the ion implantation process, preventing contamination to the surface of the epitaxial layer, and/or avoiding severe damages to the semiconductor substrate during ion implantation.

[40] Further, a plurality of active regions may be defined in the semiconductor substrate. After removing the oxide protective layer and before forming the gate oxide layer and the polysilicon layer, the surface of the epitaxial layer of the semiconductor substrate may be oxidized to form an oxide layer. Then, an active region pattern for the plurality of active regions may be formed in the oxide layer on the surface of the epitaxial layer by photolithography.

[41] The plurality of active regions may be formed in the epitaxial layer using the active region pattern as a mask. Further, after forming the active regions, the oxide layer on the surface of the epitaxial layer is removed by etching/erosion. Multiple devices may be formed based on the plurality active regions.

[42] Furthermore, after forming the source region, other processes may be used to make the semiconductor device. For example, after the source region is formed, a dielectric layer may be formed on the surface of the epitaxial layer of the semiconductor substrate. Contact holes to the gate region and the source region may then be formed in the dielectric layer. Further, metallization (or metal contacts) is performed to obtain a gate electrode and a source electrode. In addition, a drain electrode may also be formed on a back side of the semiconductor substrate.

[43] Figure 7 shows a structural diagram of a MOSFET device . As shown in Figure 7,

similar to the device previously described in above sections, the device includes the epitaxial layer 301 of the semiconductor substrate, the gate oxide layer302, the gate region 303 formed after etching the polysilicon layer, the body region305, the source region306, the drain region309, the dielectric layer307, and the through hole 308 filled with metallic material.

[44] More specifically, the epitaxial layer may be N^--N^+ doped structure ; the source region 306 may be N^+ doped; and the body region 305 may be P^- doped. The body region may be formed by implanting boron ions and performing dopant drive-in using the gate region pattern in the photoresist layer as a mask.

[45] By using the disclosed methods and processes, the polysilicon layer in the MOSFET device may be etched in such a way that the formed gate region has a lateral surface receding at a predetermined length relative to the gate region pattern in the photoresist layer . Thus , in the subsequent process for forming the body region, because the ion implantation process uses the gate region pattern in the photoresist layer as a mask, the result ed body region may have an edge away from the formed gate region . Therefore , the MOSFET device may have a significantly reduced overlapping area between the body region and the gate region, thereby reducing the input capacitance of the device, and improving the dynamic characteristics and yield rate of the MOSFET device.

[46] It is understood that the disclosed embodiments may be applied to any semiconductor devices. Various alternations, modifications, or equivalents to the technical solutions of the disclosed embodiments can be obvious to those skilled in the art.

Claims

[Claim 1] A method for manufacturing a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) , comprising:
providing a substratecontaining an epitaxial layer;
forming a gate oxide layer and a polysilicon layer on the epitaxial layer;
forming a photoresist layer on the polysilicon layer and a gate region pattern in the photoresist layer;
forming a gate region by etching the polysilicon layer using the gate region pattern in the photoresist layer as a mask, wherein the etching is performed in such a way that the gate region has a lateral surfac-ereceding at a predetermined length relative to the gate region pattern in the photoresist layer ; and
forming a body region by ion implantation and dopant drive-in using the photoresist layer as a mask such that an overlapping area between the body region and the gate region can be reduced based on the prede-termined receding length.

[Claim 2] The method according to claim 1, wherein forming the photoresist layer and the gate region pattern further includes:
coating the photoresist layer on the polysilicon; and
forming the gate region pattern in the photoresist layer using pho-tolithography.

[Claim 3] The method according to claim 1, further including:
removing the photoresist layer ;
removing a portion of the gate oxide layer within a predetermined region for a source region; and
forming the source region in the body region based on the gate oxide layer.

[Claim 4] The method according to claim 1, wherein:
the predetermined length ranges from 0.1μm to 0.5μm.

[Claim 5] The method according to claim 1, wherein:
the polysilicon layer is etched using isotropic plasma.

[Claim 6] The method according to claim 1, wherein, before the forming the gate oxide layer and the polysilicon layer, the method further includes :
forming an oxide protective layer on the epitaxial layer;
forming a conduction protecting region pattern in the oxide protective layer by photolithography;

forming a conduction protecting region by an ion implantation and dopant drive-in process using the conduction protecting region pattern as a mask ; and

removing the oxide protective layer.

[Claim 7] The method according to claim 6, wherein, after the removing the oxide protective layer, the method further includes :

oxidizing a surface of the epitaxial layer to form an oxide layer ;

forming an active region pattern in the oxide layer;

forming a plurality of active regions using the active region pattern as a mask; and

removing the oxide layer on the surface of the epitaxial layer.

[Claim 8] The method according to claim 1, wherein, after the forming the source region, the method further includes :

forming a dielectric layer on a surface of the epitaxial layer of the substrate;

forming, in the dielectric layer, contact holes to the gate region and the source region; and

performing metallization to obtain a gate electrode and a source electrode.

[Claim 9] The method according to claim 8, further including :

forming a drain electrode on a back side of the substrate.

[Claim 10] The method according to claim 1, wherein:

the epitaxial layer is N-type doped, the body region is P-type doped, and the source region is N-doped.

[Claim 11] The method according to claim 1, wherein:

the gate oxide layer includes at least silicon oxide and has a thickness of approximately 20-50 Å.

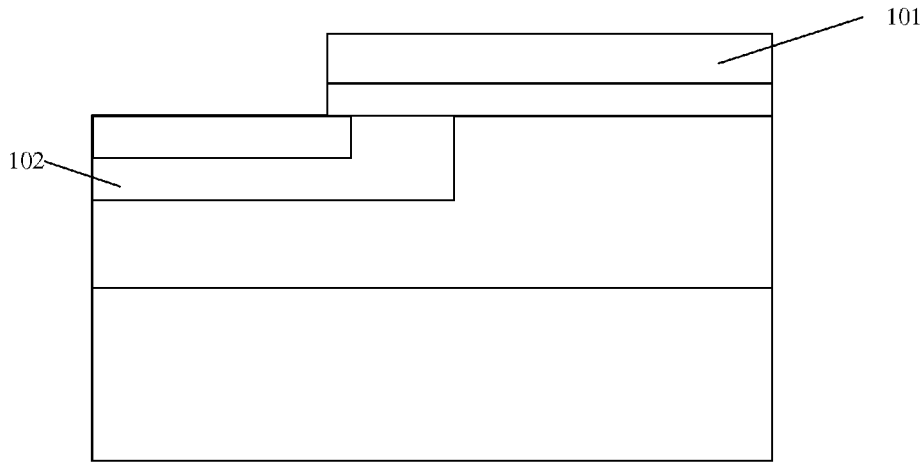
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FIG. 1

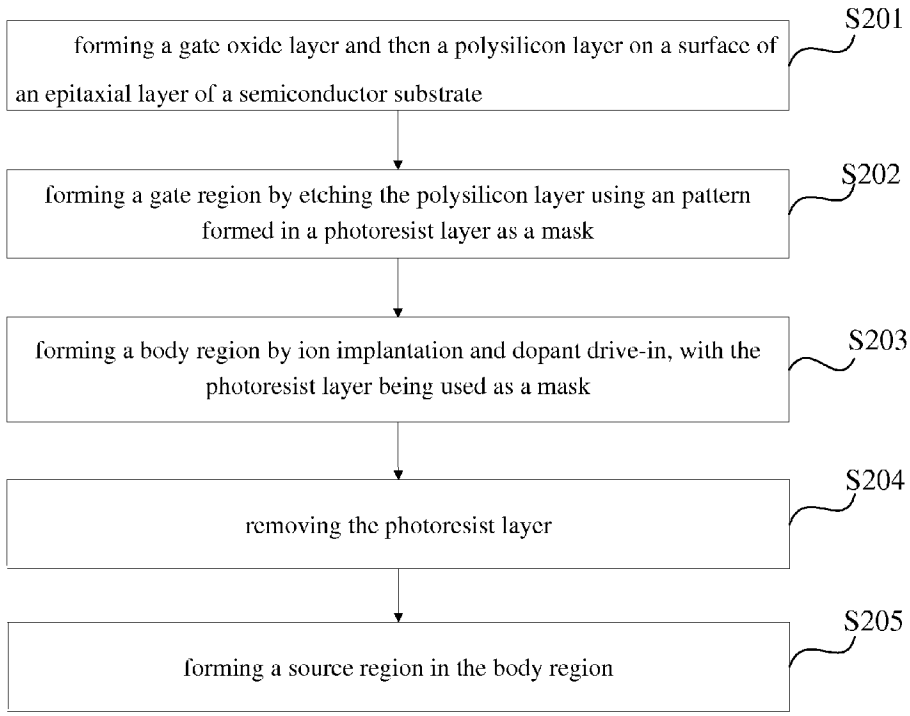
S201
forming a gate oxide layer and then a polysilicon layer on a surface of an epitaxial layer of a semiconductor substrate
S202
forming a gate region by etching the polysilicon layer using an pattern formed in a photoresist layer as a mask
S203
forming a body region by ion implantation and dopant drive-in, with the photoresist layer being used as a mask
S204
removing the photoresist layer
S205
forming a source region in the body region

FIG. 2

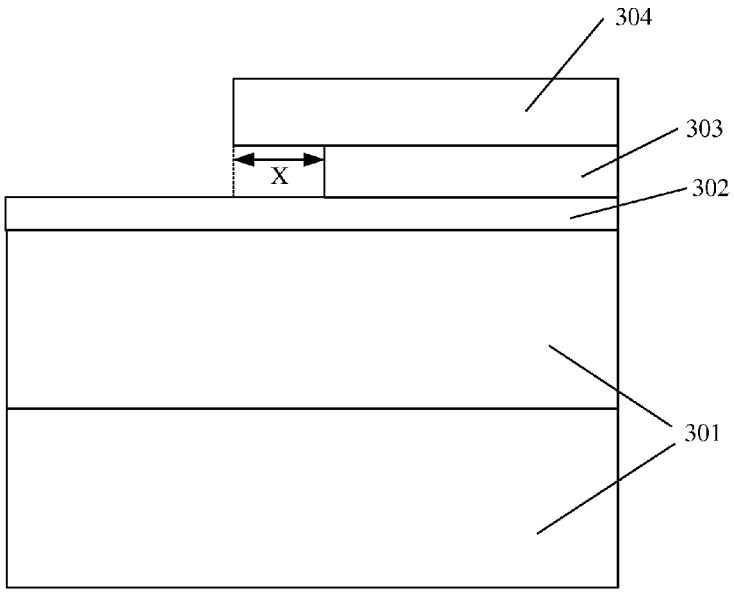

FIG. 3

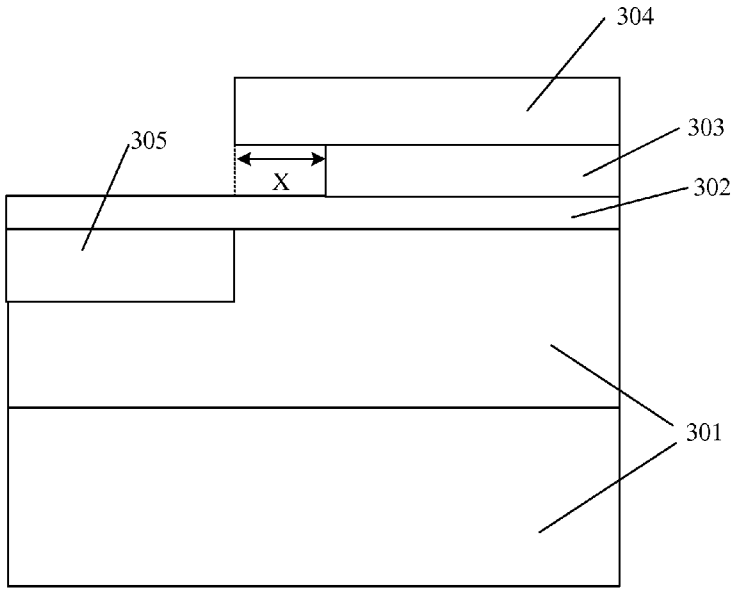

FIG. 4

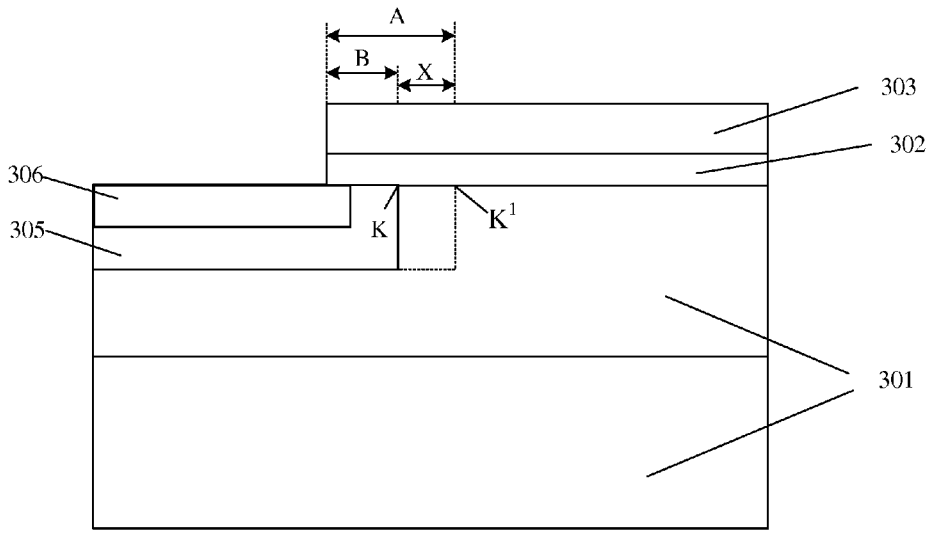

FIG. 5

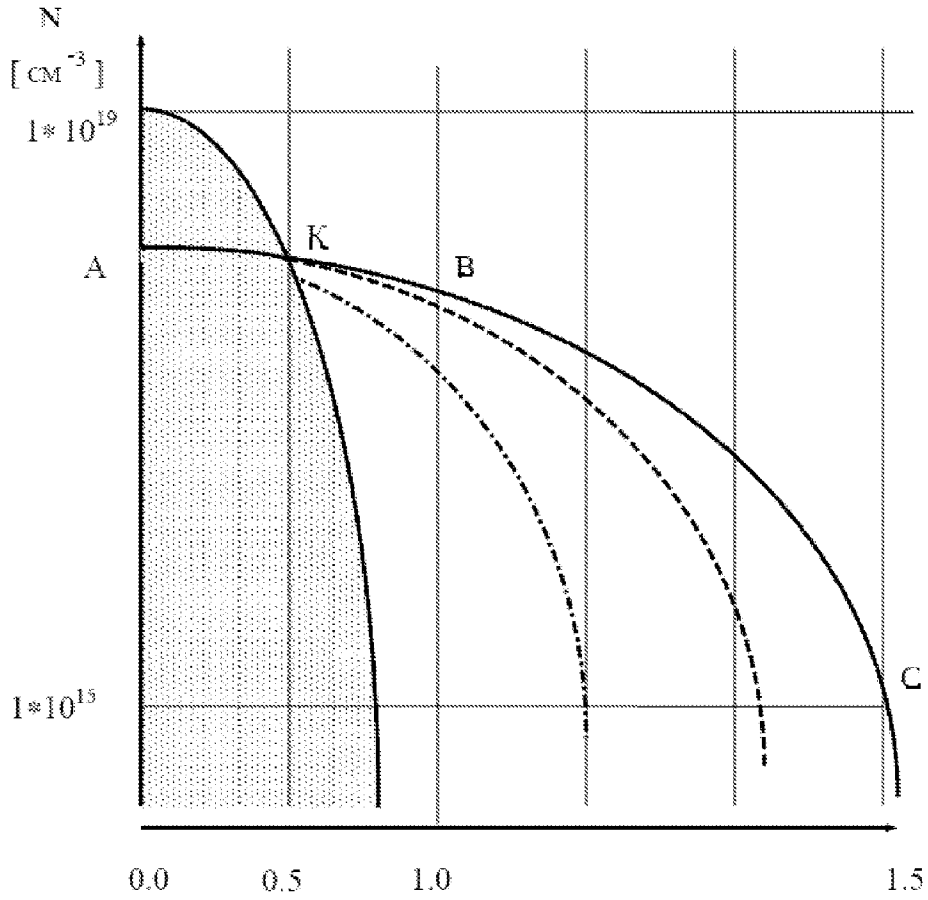

FIG. 6

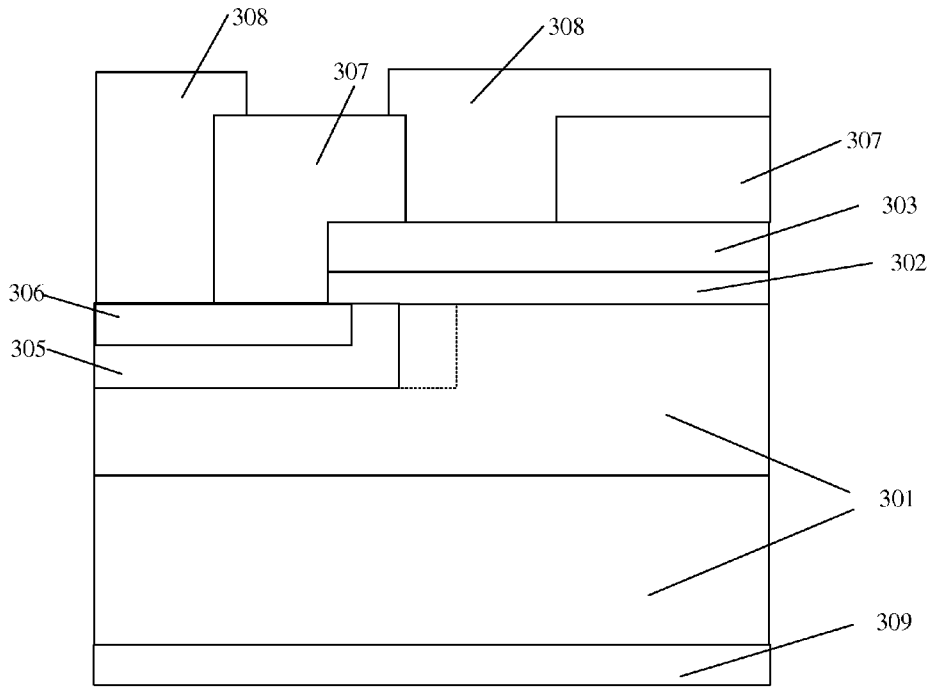

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/082419

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/336 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L21/-, H01L27/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CPRSABS, WPI: gate, etch, mask, photoresist, polysilicon, polycrystalline

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN101236904 A (SVA GROUP CO., LTD) 06 Aug. 2008 (06.08.2008) page 3 of description and figures 2a-2d	1-11
A	US6849530 B2 (BONSER et al.) 01 Feb.2005 (01.02.2005) the whole document	1-11
A	JP6275635 A (NIPPON STEEL CORP) 30 Sep. 1994 (30.09.1994) the whole document	1-11
A	CN100533692 C (YAMAHA COPR) 26 Aug.2009 (26.08.2009) the whole document	1-11

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 Jan. 2012 (11.01.2012)	**08 Mar. 2012 (08.03.2012)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer FANG, Hualong Telephone No. (86-10)62411551

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/082419

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN101236904 A	06.08.2008	none	
US6849530 B2	01.02.2005	AU2003296890 A8	03.11.2005
		TW200403733 A	01.03.2004
		US2004043590 A1	04.03.2004
		WO2004034442 A2	22.04.2004
		AU2003296890 A1	04.05.2004
JP6275635 A	30.09.1994	none	
CN100533692 C	26.08.2009	JP4725451 B2	13.07.2011
		CN101047131 A	03.10.2007
		US2007224764 A1	27.09.2007
		US7659173 B2	09.02.2010
		JP2007294836 A	08.11.2007