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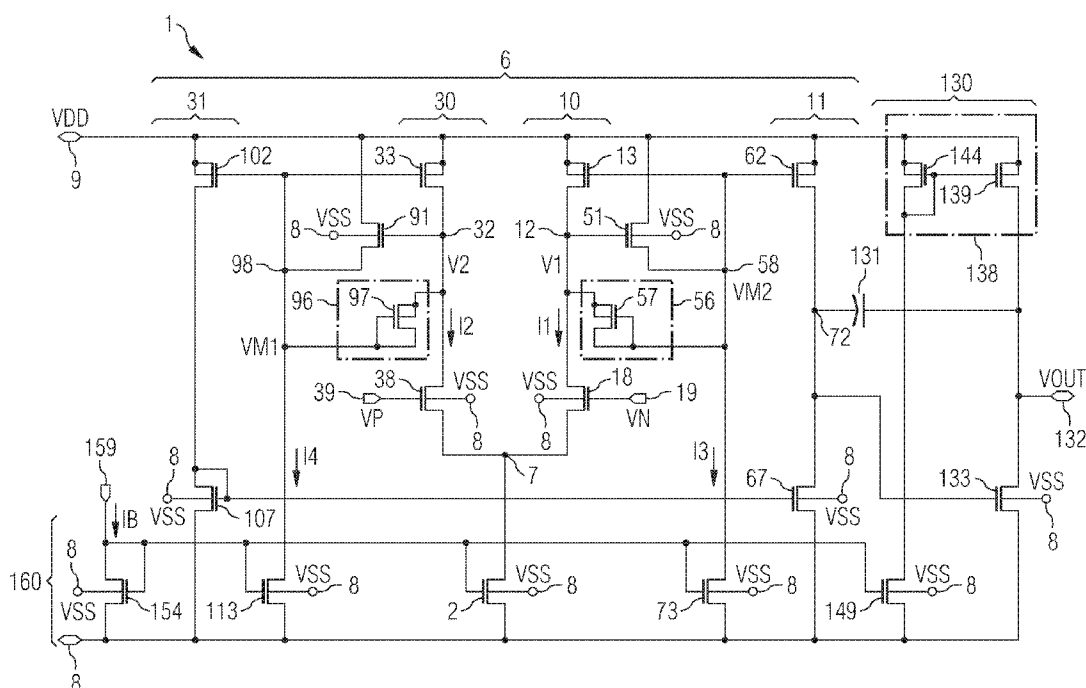
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(54) Title: **AMPLIFIER ARRANGEMENT AND METHOD FOR AMPLIFICATION**



(57) Abstract: An amplifier arrangement comprises a first transistor (18), a first bias transistor (13) and a first field-effect transistor (51). A first input signal (VN) is supplied for amplification to a control terminal of the first transistor (18). The first bias transistor (13) is coupled to the first transistor (18) via a first node (12). The first field-effect transistor (51) is coupled for clamping of a first node voltage (V1) provided at the first node (12).

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Description

Amplifier arrangement and method for amplification

- 5 The present invention relates to an amplifier arrangement, a voltage converter comprising a measurement circuit for sensing a coil current with an amplifier arrangement, and a method for amplification.
- 10 Amplifier arrangements are common in consumer electronics such as mobile phones and digital cameras, and in industrial electronics. Amplifier arrangements are also used in voltage converters which achieve an up- or a down-conversion of a supply voltage to generate an output voltage for electrical
- 15 circuits. Voltage converters for down-conversion are, for example, buck mode converters, whereas voltage converters for up-conversion are, for example, boost converters. Voltage-mode and current-mode control arrangements are used in voltage converters. A current flowing through a coil is
- 20 sensed in current-mode control arrangements.

Document "An Integrated CMOS Current-Sensing Circuit for Low-Voltage Current-Mode Buck Regulator", C. Y. Leung et al., IEEE Transactions on Circuits and Systems-II: Express Briefs,

25 volume 52, number 7, July 2005, pages 394-397, shows a buck mode converter with a current-mode control arrangement for a minimum supply voltage of 1.2 V.

It is an object of the present invention to provide an

30 amplifier arrangement, a voltage converter, and a method for amplification operating at low voltages and achieving a high amplification gain.

This object is solved by an amplifier arrangement comprising the features of claim 1, a voltage converter comprising the features of claim 14, and a method for amplification according to claim 20. Preferred embodiments are presented in
5 the respective dependent claims.

An amplifier arrangement comprises a first transistor, a first bias transistor, and a first field-effect transistor. The first bias transistor is coupled via a first node to the
10 first transistor and the first field-effect transistor is coupled to the first bias transistor.

A first input signal is applied to a control terminal of the first transistor for the purpose of amplification of the
15 first input signal. The first bias transistor provides a current to the first transistor. The first field-effect transistor achieves a clamping of a first node voltage which is provided at the first node.

20 It is an advantage of the clamping of the first node voltage at the first node that the voltage across the first bias transistor is decreased and the voltage across the first transistor is increased. Therefore, the amplifier achieves an amplification also with a low voltage supply. A gain of the
25 amplifier arrangement is high because of the relatively high voltage drop across the first transistor, even at a low supply voltage.

In an embodiment, the first field-effect transistor comprises
30 a control terminal which is connected to a terminal of the first bias transistor via the first node. The first field-effect transistor couples a control terminal of the first bias transistor to a first power supply terminal.

In a preferred embodiment, the amplifier arrangement comprises a first current path. The first current path comprises the first transistor, the first node and the first bias transistor and connects the first supply terminal to a second supply terminal.

In a preferred embodiment, the first transistor comprises a first terminal which is coupled to the second power supply terminal and a second terminal which is coupled to the first node. The first bias transistor comprises a control terminal, a first terminal which is coupled to the first power supply terminal and a second terminal which is coupled to the second terminal of the first transistor via the first node. The first field-effect transistor comprises the control terminal which is connected to the first node. Further on, the first field-effect transistor comprises a first terminal which is connected to the control terminal of the first bias transistor and is coupled to the second power supply terminal, and a second terminal which is coupled to the first power supply terminal.

In an embodiment, the first field-effect transistor is a metal-oxide-semiconductor field-effect transistor, abbreviated MOSFET. The first field-effect transistor can be a p-channel MOSFET. In a preferred embodiment, the first field-effect transistor is an n-channel MOSFET.

In a preferred embodiment, the voltage at the first supply terminal is higher than the voltage at the second supply terminal. In this preferred embodiment, the first bias transistor is realized as p-channel MOSFET, and the first transistor and the first field-effect transistor are realized

as n-channel MOSFETs. In this embodiment, the gain of the amplifier arrangement is higher when realizing the first transistor as an n-channel MOSFET.

5 In an embodiment, the amplifier arrangement comprises a second transistor, a second node, a second bias transistor and a second field-effect transistor. The second transistor is coupled to the second bias transistor via the second node. A second current path comprises the second transistor, the
10 second node and the second bias transistor. A second input signal is applied to a control terminal of the second transistor for amplification. A coupling of the second field-effect transistor to the second bias transistor is performed in such a way that clamping of a second node voltage at the
15 second node is achieved. The first and the second transistors are coupled to achieve a differential amplification of the first and the second input signals. This coupling can be realized by connecting the first terminal of the first transistor to the first terminal of the second transistor and
20 by coupling the two first terminals to the second supply terminal with a resistor, a current source or, preferably, a transistor.

In an embodiment, the second field-effect transistor
25 comprises a control terminal which is connected to a terminal of the second bias transistor via the second node. The second field-effect transistor couples a control terminal of the second bias transistor to the first power supply terminal.

30 In an embodiment, a first resistor couples the node between the first transistor and the first bias transistor to the first terminal of the first field-effect transistor. In a preferred embodiment, the resistor is realized as a first

coupling transistor. In an embodiment, a second resistor couples the node between the second transistor and the second bias transistor to the first terminal of the second field-effect transistor. In a preferred embodiment, the second
5 resistor is realized as a second coupling resistor. The coupling transistors can be n-channel MOSFETs. Preferably, the coupling transistors are p-channel MOSFETs. By use of the first and the second resistors or the first and the second coupling transistors, respectively, the influence of process
10 variations can be reduced.

In an embodiment, the amplifier arrangement comprises a third transistor and a third bias transistor which is coupled to the third transistor. The third bias transistor comprises a
15 control terminal which is connected to a control terminal of the first bias transistor. In an embodiment, an output node of the amplifier arrangement is realized as a node between the third transistor and the third bias transistor.

20 In an embodiment, the amplifier arrangement comprises an output stage which couples the node between the third transistor and the third bias transistor to an output node of the amplifier arrangement.

25 In an embodiment, the amplifier arrangement comprises a current mirror with mirror transistors. The current mirror is coupled to a current input terminal of the amplifier arrangement, to the first field-effect transistor, to the second field-effect transistor and to the node between the
30 first transistor and the second transistor.

According to an aspect of the invention, a voltage converter comprises a measurement circuit which itself comprises the

amplifier arrangement. The measurement circuit is designed for sensing a coil current. In an embodiment, the voltage converter is realized as a boost-mode converter for up-conversion of the first supply voltage. In a preferred
5 embodiment, the voltage converter is designed as a buck-mode converter, achieving a down-conversion of the first supply voltage. In a preferred embodiment, the voltage converter comprises a current-mode control arrangement. In a preferred embodiment, the measurement circuit uses the error-amplifier
10 voltage mirror principle.

In an embodiment, the voltage converter comprises a first and a second converter transistor which are coupled to a second signal input terminal of the amplifier arrangement and
15 comprises a third and a fourth converter transistor which are coupled to a first signal input terminal of the amplifier arrangement. The first and the second signal input terminals are connected to the control terminals of the first and the second transistor of the amplifier arrangement.

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In an embodiment, the first, the second, the third and the fourth converter transistor are field-effect transistors. A ratio of the channel width to the channel length of the fourth converter transistor is by a factor N greater than a
25 ratio of the channel width to the channel length of the first converter transistor. The drain-source voltages of the first and the fourth converter transistors may approximately be equal. Therefore, the current flowing through the first converter transistor is approximately by the factor N smaller
30 than a current flowing through the fourth converter transistor.

In an embodiment, the voltage converter comprises an inductance, realized as a coil, which is coupled to the fourth converter transistor. In an embodiment, the fourth converter transistor is realized in a power metal-oxide-semiconductor integration technique.

In an embodiment, the voltage converter comprises a fifth converter transistor, which is connected to the first and the second converter transistors, and a resistor. A control terminal of the fifth converter transistor is coupled to the output node of the amplifier arrangement. The resistor couples the fifth converter transistor to the first power supply terminal. The sum of the currents flowing through the first and the second converter transistors is also flowing through the fifth converter transistor and the resistor. If the first and the fourth converter transistors are switched on, the current flowing through the resistor is approximately by the factor N smaller than the current flowing through the fourth converter transistor. The voltage of an output node between the resistor and the fifth converter transistor is an output voltage of the measurement circuit which is proportional by the product of the factor N and the value of the resistor to the current flowing through the fourth converter transistor. Because the current through the fourth converter transistor approximately equals the current through the coil the current through the resistor, the voltage at the output node can be used for the measurement of the current through the coil of the voltage converter. The fifth converter transistor is preferably designed as an n-channel field-effect transistor.

In a preferred embodiment, the voltage converter with the amplifier arrangement is realized using a semiconductor body

to which the coil is coupled. Preferably, the converter transistors are realized as MOSFETs.

According to an aspect of the invention, the method for
5 amplification comprises the following steps: a first input
signal is applied to a first transistor. A current is
provided to the first transistor using a first bias
transistor. A first node voltage is provided at a first node
between the first transistor and the first bias transistor.
10 The first node voltage is clamped using a first field-effect
transistor. It is an advantage of the clamping of the first
node and, therefore, also of the first bias transistor that a
voltage across the first bias transistor is reduced and a
voltage across the first transistor is increased and,
15 therefore, a high gain of the amplification is achieved.

In an embodiment, a first node voltage is provided at the
first node and is applied to a control terminal of the first
field-effect transistor. The first field-effect transistor
20 couples a control terminal of the first bias transistor to a
first power supply terminal. A voltage at the control
terminal of the first bias transistor is advantageously
generated from a first supply voltage via the first field-
effect transistor. The first supply voltage is provided at
25 the first power supply terminal.

The following description of figures of exemplary embodiments
may further illustrate and explain the invention. Devices
with the same structure or the same effect, respectively,
30 appear with equivalent reference numerals. A description of a
part of a circuit or a device having the same function in
different figures might not be repeated in every of the
following figures.

FIG. 1 shows a schematic of an exemplary embodiment of an amplifier arrangement of the principle presented,

5 FIG. 2 shows a schematic of an exemplary embodiment of a voltage converter of the principle presented and

FIG. 3 shows an exemplary embodiment of the first, the second and the third control signals.

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FIG. 1 shows an exemplary embodiment of an amplifier arrangement 1 of the principle presented. The amplifier arrangement 1 comprises a first and a second transistor 18, 38 with first terminals which are connected to a node 7, which is coupled to a second power supply terminal 8. A first and a second bias transistor 13, 33 of the amplifier arrangement 1 comprise first terminals which are connected to a first power supply terminal 9. A second terminal of the first bias transistor 13 is connected to a second terminal of the first transistor 18 via a first node 12 and a second terminal of the second bias transistor 33 is connected to a second terminal of the second transistor 38 via a second node 32. The amplifier arrangement 1 comprises a first and a second field-effect transistor 51, 91 with second terminals which are connected to the first power supply terminal 9. A control terminal of the first field-effect transistor 51 is connected to the first node 12 and, therefore, with the second terminal of the first bias transistor 13. A first terminal of the first field-effect transistor 51 is connected to a control terminal of the first bias transistor 13. In an analogous manner, a control terminal of the second field-effect transistor 91 is connected to the second node 32, and, therefore, also with the second terminal of the second bias

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transistor 33. A first terminal of the second field-effect transistor 91 is connected to a control terminal of the second bias transistor 33.

5 A first resistor 56 of the amplifier arrangement 1 couples the first node 12 to a third node 58 which is connected to the first terminal of the first field-effect transistor 51. A second resistor 96 of the amplifier arrangement 1 couples the second node 32 to a fourth node 98 which is connected to the
10 first terminal of the second field-effect transistor 91. The first and the second resistors 56, 96 are realized as a first and a second coupling transistor 57, 97. The first terminal of the first coupling transistor 57 is connected to the first node 12. A control terminal of the first coupling transistor
15 57 is connected to a second terminal of the first coupling transistor 57 and to the first terminal of the first field-effect transistor 51. In an analogous manner, a first terminal of the second coupling transistor 97 is connected to the second node 32. A control terminal and a second terminal
20 of the second coupling transistor 97 are connected together and are connected to the first terminal of the second field-effect transistor 91.

A third and a fourth bias transistor 62, 102 of the amplifier
25 arrangement 1 each comprise a respective first terminal which is connected to the first power supply terminal 9. A control terminal of the third bias transistor 62 is connected to the control terminal of the first bias transistor 13. In an analogous manner, a control terminal of the fourth bias
30 transistor 102 is connected to the control terminal of the third bias transistor 33. A third and a fourth transistor 67, 107 of the amplifier arrangement 1 each comprise a respective first terminal which is connected to the second power supply

terminal 8. A second terminal of the third transistor 67 is connected to a second terminal of the third bias transistor 62. In a corresponding manner, a second terminal of the fourth transistor 107 is connected to a second terminal of the fourth bias transistor 102. A control terminal of the third transistor 67 is connected to a control terminal of the fourth transistor 107 and in addition also to the second terminal of the fourth transistor 107, so that a current mirror is achieved. A node 72 between the third transistor 67 and the third bias transistor 62 is an output node of the input stage 6 of the amplifier arrangement 1 comprising the first, the second, the third and the fourth transistors 18, 38, 68, 108 and the first and the second field-effect transistors 51, 91 and the first, the second, the third and the fourth bias transistors 13, 33, 62, 102. This node 72 may act also as an output node of the amplifier arrangement 1.

The amplifier arrangement further comprises an output stage 130. The output stage 130 comprises a fifth transistor 133, a current mirror 138, a capacitor 131, and an output node 132 of the amplifier arrangement 1. The node 72 is connected to a control terminal of the fifth transistor 133. A first terminal of the fifth transistor 133 is connected to the second power supply terminal 8. A second terminal of the fifth transistor 133 is connected to the output node 132 of the amplifier arrangement 1 and also to the current mirror 138. The current mirror 138 couples the second terminal 136 of the fifth transistor 133 to the first power supply terminal 9. The current mirror 138 comprises a fifth and a sixth bias transistor 139 and 144 with first terminals which are connected to the first power supply terminal 9. A second terminal of the fifth bias transistor 139 is connected to the second terminal of the fifth transistor 133. A control

terminal of the fifth bias transistor 139 is connected to a control terminal of the sixth bias transistor 144 and also to a second terminal of the sixth bias transistor 144. The second terminal of the sixth bias transistor 144 is coupled to the second power supply terminal 8. The capacitor 131 couples the node 72 to the output node 132 of the amplifier arrangement.

A second mirror of the amplifier arrangement 1 160 comprises a first, a second, a third, a fourth and a fifth mirror transistor 154, 113, 2, 73, 149 with first terminals which are connected to the second power supply terminal 8. The control terminals are connected together and are connected to the second terminal of the first mirror transistor 154 and to a current supply terminal 159. A second terminal of the second mirror transistor 113 is connected to the first terminal of the second field-effect transistor 91, and therefore, also to the control terminals of the second and the fourth bias transistors 33, 102. A second terminal of the third mirror transistor 2 is connected to the node 7 between the first and the second transistor 18, 38. A second terminal of the fourth mirror transistor 73 is connected to the first terminal of the first field-effect transistor 51. A second terminal of the fifth mirror transistor 149 is connected to the first current mirror 138 and, therefore, is connected to the second terminal of the sixth bias transistor 144.

A first input signal VN is supplied to a first signal input terminal 19 which is coupled with a control terminal of the first transistor 18 and a second input signal VP is supplied to a second signal input terminal 39 which is a control terminal of the second transistor 38. Because the node 7 between the first and the second transistors 18, 38 is

coupled to the second power supply terminal 8 via the third mirror transistor 2, the first and the second input signals VN, VP are amplified in a differential manner. The first and the second field-effect transistors 51, 91 achieve a small
5 voltage between the first and the second terminals of the first bias transistor 13 and between the first and the second terminals of the second bias transistor 33. Therefore, a voltage between the first and the second terminals of the first transistor 18 and between the first and the second
10 terminals of the second transistor 38 obtains a high value, yielding a high gain of the amplification of the first and the second input signals VN, VP. An amplified signal of the first input signal VN is applied to the control terminal of the third bias transistor 62 and, therefore, also to the node
15 72 between the third transistor 67 and the third bias transistor 62. An amplified signal of the second input signal VP is applied in an analogous manner to the control terminal of the fourth bias transistor 102. Because the third and the fourth transistors 67, 107 are coupled together, the
20 amplified signal of the second input signal VP also influences a voltage at the node 72. The voltage at the node 72 is amplified by the output stage 130 of the amplifier arrangement 1 using the fifth transistor 133 for amplification. A bias current for the fifth transistor 133 is
25 supplied by the first current mirror 138. An output voltage VOUT is provided at the output node 132 of the amplifier arrangement 1. The first and the second input signals VN, VP are amplified in a differential manner resulting in a voltage at the node 72. The voltage at the node 72 is amplified in a
30 non-differential manner so that the output voltage VOUT of the amplifier arrangement 1 is provided.

The transistors are realized as field-effect transistors in the form of MOSFETs. A first supply voltage VDD is applied at the first power supply terminal 9 and a second supply voltage VSS is provided at the second power supply terminal 8. The first supply voltage VDD is higher than the second supply voltage VSS. The first terminals of the transistors can be realized as a source terminal of the respective field-effect transistors and, therefore, the second terminals of all the transistors can be a drain terminal of the field-effect transistors. The control terminals of all the transistors are realized as gate electrodes of the field-effect transistors. The first, the second, the third, the fourth, and the fifth transistors 18, 38, 67, 107, 133 and the five mirror transistors 154, 113, 2, 73, 149 are realized as n-channel field-effect transistors. The first, the second, the third, the fourth, the fifth and the sixth bias transistors 13, 33, 62, 102, 139, 144 are realized as p-channel field-effect transistors. The first and the second coupling transistors 57, 97 are realized as p-channel field-effect transistors.

It is an advantage of the realization of the first and the second transistor 18, 83 as n-channel field-effect transistors that the amplification achieved by an n-channel transistor is higher than the amplification achieved by a p-channel field-effect transistor with the same transistor area. The input stage of the amplifier arrangement, comprising the first, the second, the third and the fourth transistors 18, 38, 67, 107, being constructed symmetrically, results in a low offset value of the amplifier arrangement. It is an advantage of the output stage 130 that it increases the gain of the amplifier arrangement.

In an alternative embodiment, the amplifier arrangement 1 does not comprise a first and a second resistor 56, 96 and the first and the second coupling transistor 57, 97.

5 FIG. 2 shows an exemplary embodiment of a voltage converter according to the principle presented. The focus of the voltage converter shown in FIG. 2 is directed to a measurement circuit which is designed for the measurement of a current through a fourth converter transistor 200 which is
10 approximately equivalent to a current through a coil 210 of the voltage converter. FIG. 2 shows the voltage converter realized as a buck-mode converter for down-conversion of the first supply voltage VDD. The voltage converter comprises the amplifier arrangement 1 of which an exemplary embodiment is
15 shown in FIG. 1. The voltage converter comprises a first, a second and a third converter transistor 242, 237, 232. The first terminals of these four converter transistors 242, 237, 232, 200 are connected to the first power supply terminal 9. A second terminal of the first converter transistor 242 and a
20 second terminal of the second converter transistor 237 are connected together and are connected to the second signal input 39 of the amplifier arrangement 1. A second terminal of the third converter transistor 232 is connected to the first signal input terminal 19 of the amplifier arrangement 1. A
25 second terminal of the fourth converter transistor 200 is coupled to the first signal input terminal 19. This coupling is achieved by a sixth converter transistor 215 with a first terminal which is connected to the second terminal of the fourth converter transistor 200. A second terminal of the
30 sixth converter transistor 215 is connected to the first signal input terminal 19.

The voltage converter further comprises a fifth converter transistor 247 and a resistor 252. A second terminal of the fifth converter transistor 247 is connected to the second terminals of the second and first converter transistors 242, 237. The control terminal of the fifth converter transistor 247 is connected to the output node 132 of the amplifier arrangement 1. A first terminal of the fifth converter transistor 247 is coupled to the second power supply terminal 8 via the resistor 252. The second terminal of the third converter transistor 232 and the second terminal 218 of the sixth converter transistor 215 are coupled via a current mirror 220 to the second power supply terminal 8. The current mirror 220 comprises an eighth and a ninth converter transistor 221, 226 with first terminals which are connected to the second power supply terminal 8. A second terminal of the eighth converter transistor 222 is connected to the second terminal of the sixth converter transistor 215. A control terminal of the eighth converter transistor 221 is connected to a control terminal of the ninth converter transistor 226 and also to a second terminal of the ninth converter transistor 206. The current mirror 220 further comprises a current source 231 which couples the ninth converter transistor 226 to the first power supply terminal 9.

The voltage converter further comprises a seventh converter transistor 205 which couples the second terminal of the fourth converter transistor 200 to the second power supply terminal 8. A second terminal of the seventh converter transistor 205 is connected to the second terminal of the fourth converter transistor 200 and to a terminal of the coil 210. A further terminal of the coil 210 is coupled to a load

of the voltage converter represented by a capacitor 211 and a resistor 212.

The first, the second, the third, the fourth and the sixth
5 converter transistors 242, 237, 232, 200, 215 are realized as
p-channel MOSFETs. The fifth, the seventh, the eighth, and
the ninth converter transistors 247, 205, 221, 226 are
realized as n-channel MOSFETs. A first control signal VP is
applied to the control terminals of the first, the fourth and
10 the sixth converter transistors 242, 200, 215. A second
control signal VXP is applied to the control terminals of the
second and the third converter transistors 237, 232. A third
control signal VN is applied to the control terminal 206 of
the seventh converter transistor 205. The mode of operation
15 is described with reference to FIG. 3.

FIG. 3 shows an exemplary embodiment of the first, the
second, and the third control signals VP, VXP, VN. The second
control signal VXP is an inverted signal of the first control
20 signal VP. The third control signal VN is approximately the
first control signal VP with a small difference: a rising
edge of the third control signal VN is by a time difference
 ΔT later than a rise of the first control signal VP and a
falling edge of the third control signal VN is by a time
25 difference $\Delta T1$ earlier than a fall of the first control
signal VP. When the first control signal VP is in a high
state, the first, the fourth and the sixth converter
transistors 242, 200, 215 are switched off. The second and
the third converter transistors 237, 232 are switched on by
30 the second control signal VXP and are generating the first
and the second input signals VN, VP for the amplifier
arrangement 1. Because the current mirror 220 is also
connected to the first input signal terminal 19 of the

amplifier arrangement 1 and because the amplifier arrangement is designed for the purpose that the first and the second input signals VN, VP are approximately equal, the output voltage VOUT of the amplifier arrangement 1 provided at the output node 132 of the amplifier arrangement 1 obtains such a value that a current ISENSE flowing through the eighth converter transistor 247 and the resistor 252 is approximately equal to the current flowing through the fourth converter transistor 200. The seventh converter transistor 205 is also switched on. If electric energy is stored in the coil 210, a coil current IL can flow from the second supply terminal 8 through the seventh converter transistor 205 and the coil 210 to the load represented by the capacitor 211 and the resistor 212.

In a second state of operation, the first control signal VPC is in a low state and, therefore, the first, the fourth and the sixth converter transistors 242, 200, 215 are switched on. The second, the third and the seventh converter transistors 237, 232, 205 are switched off during the second state of operation by the second and the third control signals VXPC, VNC. The coil current IL can now flow from the first supply terminal 9 through the fourth converter transistor 200 and through the coil 210 to the load represented by the capacitor 211 and the resistor 212.

Because a current ID flowing through the eighth converter transistor 221 of the current mirror 220 is small compared with the coil current IL, the voltage between the first and the second terminals of the sixth converter transistor 215 is small in comparison with the voltage between the first and the second terminals of the fourth converter transistor 200. Therefore, the voltage between the first and the second terminals of the fourth converter transistor 200 is

approximately equal to the voltage between the first and the second terminals of the first converter transistor 242. The fourth converter transistor 202 is realized with a ratio of the channel width to the channel length W/L . The first

5 converter transistor 242 is realized with a smaller ratio of the width of the channel to the length of the channel. The width-to-length ratios differ by a factor N . Because the voltages between the first and the second terminals of the first and the fourth converter transistors 242, 200 are

10 approximately equal and the ratios of the channel width to the channel length is smaller in the case of the first converter transistor 242, a current flows through the first converter transistor 242 which is by the factor N smaller than the current through the fourth converter transistor 200

15 which is approximately the coil current I_L . The output voltage V_{OUT} of the amplifier arrangement 1 is provided in such a way that the first and the second input signals V_N , V_P are approximately equal also in the second state of operation.

20 The current flowing through the first converter transistor 242 also flows through the resistor 252 and the fifth converter transistor 247. The output voltage V_{OUT} of the amplifier arrangement 1 controls the current through the

25 fifth converter transistor 247 in such a way that the first and the second input signals V_P , V_N for the amplifier arrangement 1 are approximately equal. Therefore, the current through the resistor 252 is proportional to the current through the fourth converter transistor 200 and the coil

30 current I_L by the factor N . The first supply voltage V_{DD} is provided to the first power supply terminal 9 and the second supply voltage V_{SS} is provided to the second power supply terminal 8. A sense current I_{SENSE} flows through the resistor

252 and a sense voltage VSENSE is provided at a node between the resistor 252 and the fifth converter transistor 247.

Therefore, the voltage converter according to FIG. 2 provides the current ISENSE and the voltage VSENSE in such a way that

5 it can be used for the measurement of the coil current I_L because a constant and known proportionality factor between the coil current I_L and the sense current ISENSE through the resistor 252 is provided.

Reference numerals

	1	amplifier arrangement
	2	third mirror transistor
5	6	input stage
	7	node
	8	second power supply terminal
	9	first power supply terminal
	10	first current path
10	11	fourth current path
	12	first node
	13	first bias transistor
	18	first transistor
	19	first signal input terminal
15	30	second current path
	31	third current path
	32	second node
	33	second bias transistor
	38	second transistor
20	39	second signal input terminal
	51	first field-effect transistor
	56	first resistor
	57	first coupling transistor
	58	third node
25	62	third bias transistor
	67	third transistor
	72	node
	73	fourth mirror transistor
	91	second field-effect transistor
30	96	second resistor
	97	second coupling transistor
	98	fourth node
	102	fourth bias transistor

	107	fourth transistor
	113	second mirror transistor
	130	output stage
	131	capacitor
5	132	output node
	133	fifth transistor
	139	fifth bias transistor
	144	sixth bias transistor
	149	fifth mirror transistor
10	154	first mirror transistor
	200	fourth converter transistor
	205	seventh converter transistor
	210	coil
	211	capacitor
15	212	resistor
	215	sixth converter transistor
	221	eighth converter transistor
	226	ninth converter transistor
	232	third converter transistor
20	237	second converter transistor
	242	first converter transistor
	247	fifth converter transistor
	252	resistor
	$\Delta T, \Delta T2$	time difference
25	I_B, I_{B2}	mirror current
	I_L	coil current
	I_{SENSE}	sense current
	I_1, I_2, I_3, I_4	current
	T	period
30	VDD	first supply voltage
	VLOAD	load voltage
	V_{M1}, V_{M2}	voltage
	VN	first input signal

VNC	third control signal
VOUT	output signal
VP	second input signal
VPC	first control signal
5 VSENSE	sense voltage
VSS	second supply voltage
VXPC	second control signal
V1	first node voltage
V2	second node voltage

Claims

1. Amplifier arrangement, comprising

- a first transistor (18) with a control terminal to which a first input signal (VN) is supplied for amplification,
- a first bias transistor (13) which is coupled to the first transistor (18) via a first node (12) and
- a first field-effect transistor (51) for clamping of a first node voltage (V1) which is provided at the first node (12), wherein the first field-effect transistor (51) comprises a control terminal which is connected to a terminal of the first bias transistor (13) via the first node (12) and the first field-effect transistor (51) couples a control terminal of the first bias transistor (13) to a first power supply terminal (9).

2. Amplifier arrangement according to claim 1,

wherein the first node voltage (V1) depends on a difference of a control voltage of the first bias transistor (13) and a control voltage of the first field-effect transistor (51).

3. Amplifier arrangement according to claim 1 or 2,

wherein the first field-effect transistor (51) is a metal-oxide-semiconductor field-effect transistor.

4. Amplifier arrangement according to one of claims 1 to 3,

wherein the first transistor (18), the first node (12) and the first bias transistor (13) are comprised by a first current path (10) between the first supply terminal (9) and a second supply terminal (8).

5. Amplifier arrangement according to one of claims 1 to 4,

wherein a first coupling transistor (57) comprises a control terminal which is connected to a second terminal of the first coupling transistor (57) and the first coupling transistor (57) couples the first node (12) to a third node (58) between
5 a first terminal of the first field-effect transistor (51) and the control terminal of the first bias transistor (13).

6. Amplifier arrangement according to claim 4 and 5,
wherein a voltage (VDD) at the first supply terminal (9) is
10 higher than a voltage (VSS) at the second supply terminal (8) and
- the first bias transistor (13) and the first coupling transistor (57) are p-channel field-effect transistors and
- the first transistor (18) and the first field-effect
15 transistor (51) are n-channel field-effect transistors.

7. Amplifier arrangement according to one of claims 1 to 6,
wherein the amplifier arrangement (1) comprises
- a second transistor (38) with a control terminal to which
20 a second input signal (VP) is supplied for amplification,
- a second bias transistor (33) which is coupled to the second transistor (38) via a second node (32) and
- a second field-effect transistor (91) for clamping of a second node voltage (V2) which is provided at the second
25 node (32),

wherein the first and the second transistors (18, 38) are coupled to each other to provide a differential amplification of the first and the second input signals (VN, VP).

30 8. Amplifier arrangement according to claim 7,
wherein the second node voltage (V2) depends on a difference of a control voltage of the second bias transistor (33) and a control voltage of the second field-effect transistor (91).

9. Amplifier arrangement according to claim 7 or 8,
wherein the second field-effect transistor (91) is a metal-
oxide-semiconductor field-effect transistor.

5

10. Amplifier arrangement according to one of claims 1 to 9,
wherein the amplifier arrangement (1) comprises a third
current path (11) with

- a third transistor (67) and
- 10 - a third bias transistor (62) which is coupled to the third
transistor (67) and which comprises a control terminal
which is connected to a control terminal of the first bias
transistor (13).

- 15 11. Amplifier arrangement according to claim 10,
wherein the amplifier arrangement (1) comprises a fourth
current path (31) with
- a fourth transistor (107) with a control terminal which is
coupled to a second terminal of the fourth transistor
 - 20 (107) and to a control terminal of the third transistor
(67) and
 - a fourth bias transistor (102) which is coupled to the
fourth transistor (107) and which comprises a control
terminal which is connected to a control terminal of the
 - 25 second bias transistor (33).

12. Amplifier arrangement according to claim 11,
wherein

- a second current path (30) comprises the second transistor
- 30 (38), the second node (32) and the second bias transistor
(33),

- a current in the fourth current path (31) is a linear function of a second current (I_2) in the second current path (30) and
- a first current (I_1) in the first current path (10) and a
5 second current (I_2) in the second current path (31) are compared by a current comparator formed by the third bias transistor (62) and the third transistor (67).

13. Amplifier arrangement according to one of claims 10 to
10 12,

wherein the amplifier arrangement (1) comprises an output stage (130), comprising

- a fifth transistor (133) with a control terminal which is coupled to a node (72) between the third transistor (67)
15 and the third bias transistor (62) and
- an output node (132) of the amplifier arrangement (1), which is coupled to a second terminal of the fifth transistor (133).

20 14. Voltage converter, comprising a measurement circuit for sensing a coil current (I_L) according to the error amplifier voltage mirror principle with an amplifier arrangement (1) according to one of claims 1 to 13.

25 15. Voltage converter according to claim 14 and including the features of claim 7, comprising

- a first converter transistor (242) which is coupled to the control terminal of the second transistor (38) of the amplifier arrangement (1) and comprises a control terminal
30 to which a first control signal (VPC) is supplied and
- a second converter transistor (237) which is coupled to the control terminal of the second transistor (38) of the

amplifier arrangement (1) and comprises a control terminal to which a second control signal (VXPC) is supplied.

16. Voltage converter according to claim 15,

5 wherein the voltage converter comprises

- a third converter transistor (232) which is coupled to the control terminal of the first transistor (18) of the amplifier arrangement (1) and comprises a control terminal to which the second control signal (VXPC) is supplied and
- 10 - a fourth converter transistor (200) which is coupled to the control terminal of the first transistor (18) of the amplifier arrangement (1) and comprises a control terminal to which the first control signal (VPC) is supplied.

15 17. Voltage converter according to claim 16,

wherein the first and the fourth converter transistors (200, 242) are field-effect transistors and wherein a ratio of the channel width to the channel length W/L of the fourth converter transistor (200) is by a factor N greater than a
20 ratio of the channel width to the channel length of the first converter transistor (242).

18. Voltage converter according to one of claims 15 to 17, wherein the voltage converter comprises

- 25 - a resistor (252) and
- a fifth converter transistor (247) which couples the resistor (252) to the control terminal of the second transistor (38) of the amplifier arrangement (1).

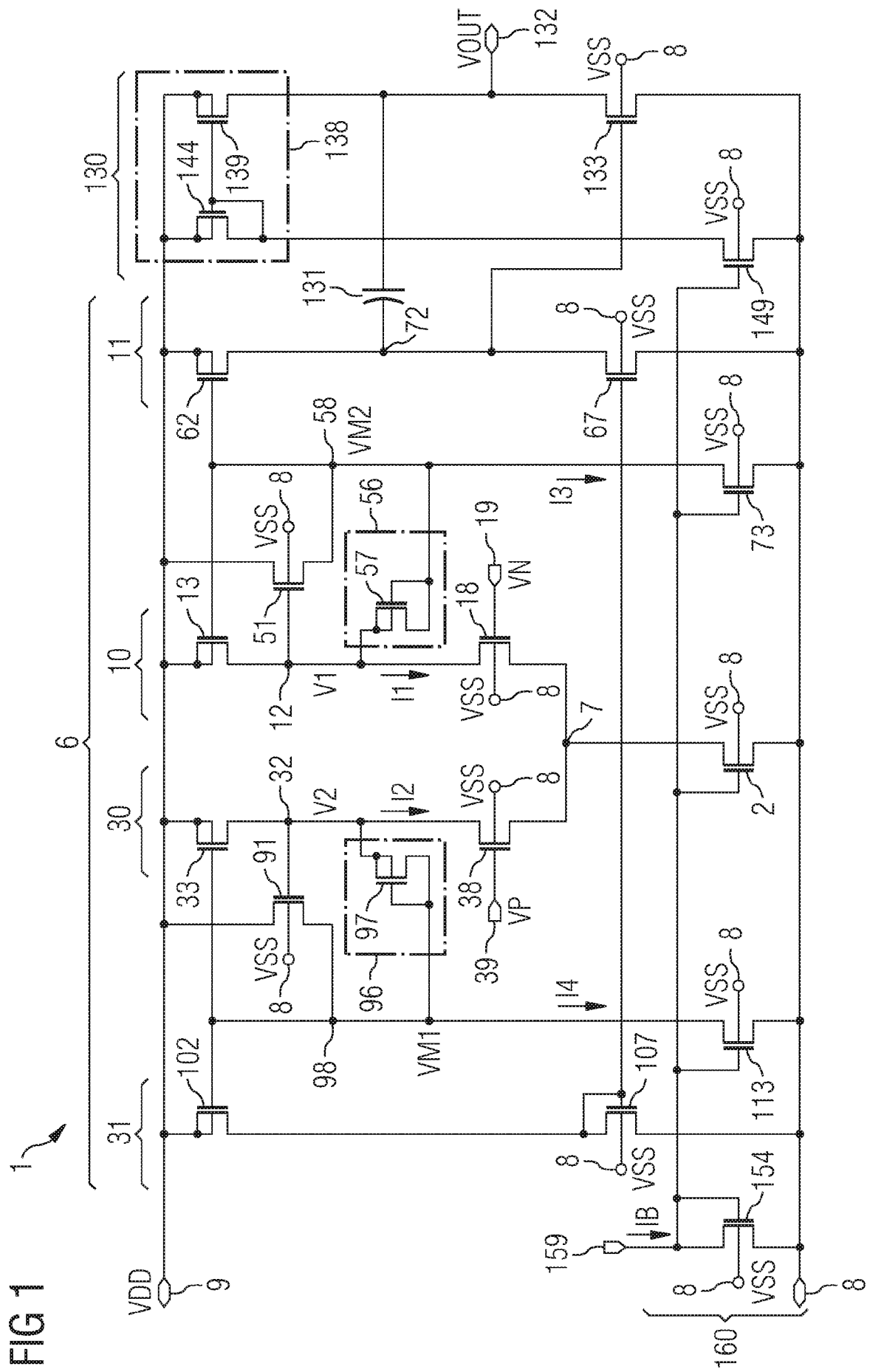
30 19. Voltage converter according to claim 18,

wherein the fifth converter transistor (247) is a n-channel metal-oxide-semiconductor field-effect transistor.

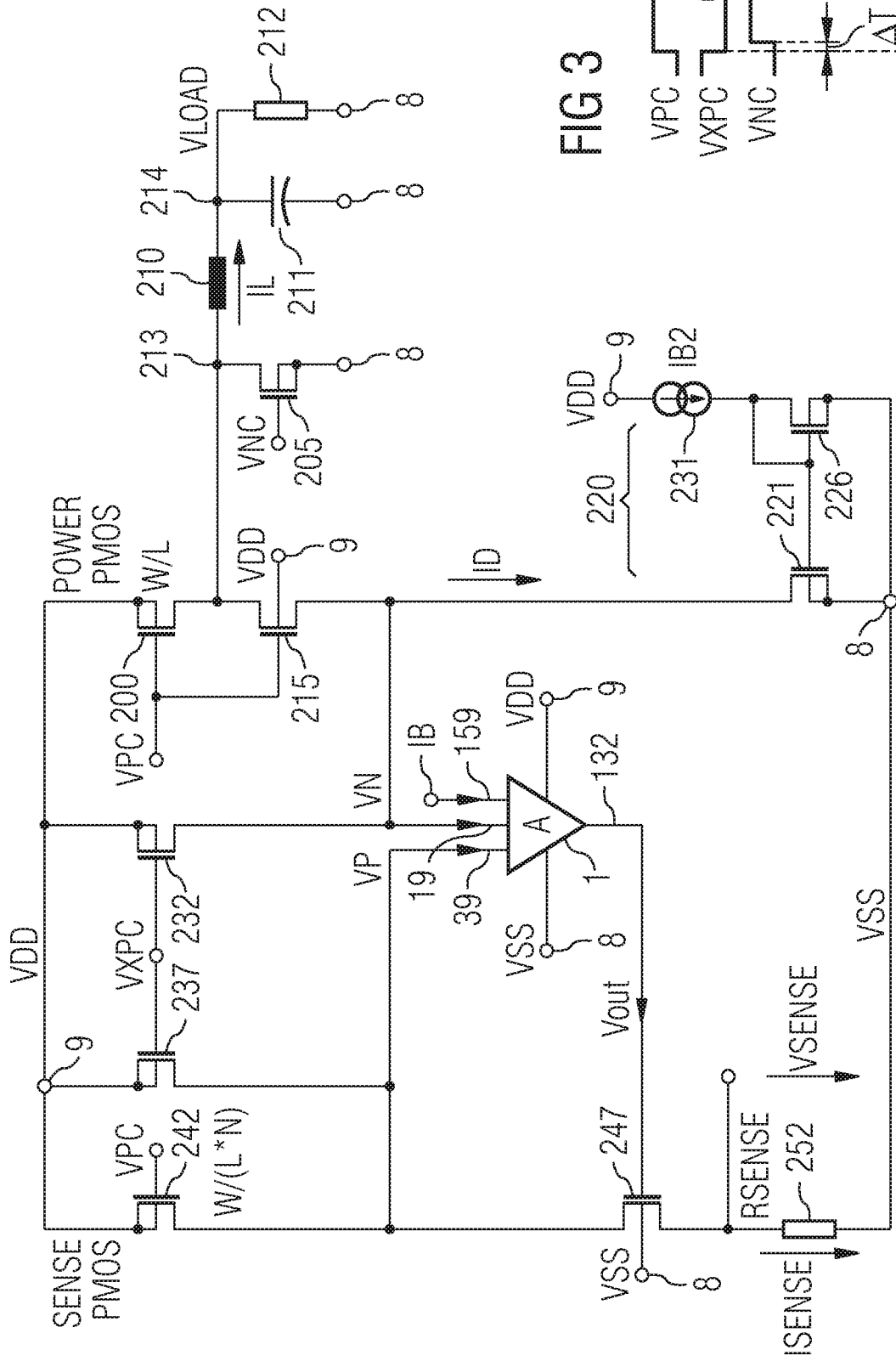
20. Method for amplification,
comprising the steps of:

- providing a first input signal (VN) to a first transistor (18),
- 5 - providing a current (I2) to the first transistor (18) using a first bias transistor (13),
- clamping a first node (12) between the first transistor (18) and the first bias transistor (13) using a first field-effect transistor (51) by supplying a first node
- 10 voltage (V1) which is provided at the first node (12) to a control terminal of the first field-effect transistor (51) which couples a control terminal of the first bias transistor (13) to a first power supply terminal (9).

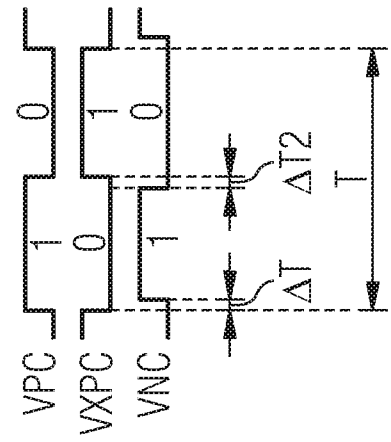
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INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2007/057685

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03F3/45

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 963 085 A (SAUER DONALD R [US]) 5 October 1999 (1999-10-05) column 5, line 44 - column 9, line 54; figure 3	1-20
A	US 6 525 607 B1 (LIU JONATHAN H [US]) 25 February 2003 (2003-02-25) column 1, line 66 - column 8, line 41; figure 1	1-20
A	US 5 973 561 A (HEATON DALE A [US]) 26 October 1999 (1999-10-26) column 4, line 3 - line 17; figure 4	1-20
A	US 2006/017504 A1 (DEVAL PHILIPPE [CH] ET AL) 26 January 2006 (2006-01-26) paragraph [0016] - paragraph [0019]; figure 1	1-20
	-/--	

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search

16 November 2007

Date of mailing of the international search report

28/11/2007

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INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2007/057685

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CHI YAT LEUNG, PHILIP K. T. MOK, KA NANG LEUNG, MANSUN CHAN: "An Integrated CMOS Current-Sensing Circuit for Low-Voltage Current-Mode Buck Regulator" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS - II: EXPRESS BRIEFS, vol. 52, no. 7, July 2005 (2005-07), pages 394-397, XP002411488 cited in the application the whole document -----	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2007/057685

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US 5963085	A	05-10-1999	NONE	
US 6525607	B1	25-02-2003	NONE	
US 5973561	A	26-10-1999	NONE	
US 2006017504	A1	26-01-2006	NONE	