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(54) **Title:** METHODS OF FORMING SELF-ALIGNED VIAS AND AIR GAPS

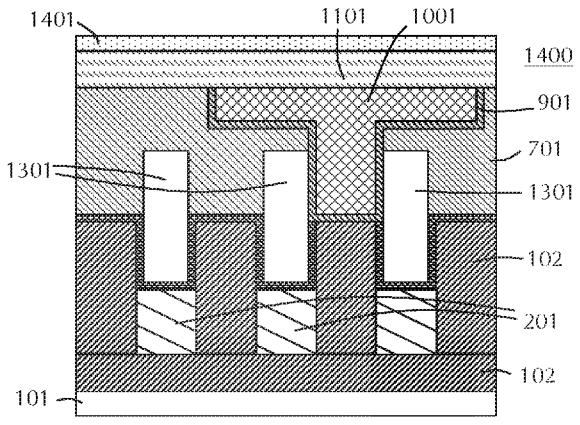


FIG. 14A

(57) **Abstract:** A first metallization layer comprises a set of first conductive lines that extend along a first direction on a first dielectric layer on a substrate. Pillars are formed on recessed first dielectric layers and a second dielectric layer covers the pillars. A dual damascene etch provides a contact hole through the second dielectric layer and an etch removes the pillars to form air gaps.

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METHODS OF FORMING SELF-ALIGNED VIAS AND AIR GAPS

TECHNICAL FIELD

[0001] The present disclosure relates generally to methods of depositing and etching thin films. In particular, the disclosure relates to processes for forming self-aligned vias and air gaps and devices containing same.

BACKGROUND

[0002] The semiconductor industry is rapidly developing chips with smaller and smaller transistor dimensions to gain more functionality per unit area. As the dimensions of devices continue to shrink, so does the gap/space between the devices, increasing the difficulty to physically isolate the devices from one another. Filling in the high aspect ratio trenches/spaces/gaps between devices which are often irregularly shaped with high-quality dielectric materials is becoming an increasing challenge to implementation with existing methods including gapfill, hardmasks and spacer applications.

[0003] Resistance-Capacitance (RC) delay is a challenging aspect of back end of line (BEOL) device production. The RC delay continues to increase with metal pitch scaling, metal line length increasing and metal line thickness decreasing. Reducing metal line resistance or dielectric capacitance in the back end of line is a priority of engineers working on BEOL. Low dielectric constant (k) materials are the main materials besides metals in the BEOL, which account for the capacitance that needs to be reduced. Reducing k has been a trend in the past decades. IBM introduced the air-gap technology around 10 years ago. However, it has not penetrated in the whole industry because of the process/design/integration complexity.

[0004] Another challenging aspect in the current semiconductor manufacture is edge placement error (EPE) appearing in the patterning steps. When patterning multiple layers, layer-to-layer connection or alignment becomes more and more difficult with smaller features. On BEOL, big EPE could cause both the resistance of interconnect and parasitic capacitance to increase which will increase the RC delay. In the worst cases, the EPE can result in the misalignment of two metal layers and device failure.

[0005] Therefore, there is a need in the art for methods for back end of line device production with decreased RC delay and/or decreased edge placement error.

SUMMARY

[0006] A method to provide self-aligned air gaps, the method comprising: recessing first conductive lines on a first dielectric layer on a substrate, the first conducting lines extending along a first direction on the first dielectric layer; forming pillars on the recessed first conductive lines; depositing a second dielectric layer between the pillars; etching the second dielectric layer to form a contact hole in the second dielectric layer between adjacent pillars; depositing a metal film in the contact hole; removing the second dielectric layer to expose the pillars; removing the pillars to form air gaps; and depositing a cap layer to enclose the air gaps.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0008] FIG. 1A illustrates a top view and a cross-sectional view of an electronic device structure to provide a fully self-aligned via according to some embodiments;

[0009] FIG. 1B is a perspective view of the electronic device structure depicted in FIG. 1A;

[0010] FIG. 2A is a side cross-sectional view of the electronic device structure after the conductive lines are recessed according to some embodiments;

[0011] FIG. 2B is a top view of the electronic device structure of FIG. 2A;

[0012] FIG. 3 is a side cross-sectional view of the electronic device structure after a liner is deposited on the recessed conductive lines according to some embodiments;

[0013] FIG. 4 is a side cross-sectional view of the electronic device structure after a seed gapfill layer is deposited on the liner according to some embodiments;

[0014] FIG. 5A is a side cross-sectional view of the electronic device structure after portions of the seed gapfill layer are removed to expose top portions of the insulating layer according to some embodiments;

[0015] FIG. 5B is a perspective view of the electronic device structure shown in FIG. 5A;

[0016] FIG. 6A is a side cross-sectional view of the electronic device structure after self-aligned selective growth pillars are formed according to some embodiments;

[0017] FIG. 6B is a perspective view of the electronic device structure shown in FIG. 6A;

[0018] FIG. 7A is a side cross-sectional view of the electronic device structure after an insulating layer is deposited to overfill the gaps between the pillars according to some embodiments;

[0019] FIG. 7B is a perspective view of the electronic device structure shown in FIG. 7A;

[0020] FIG. 8A is a side cross-sectional view of the electronic device structure after a dual damascene etch according to some embodiments;

[0021] FIG. 8B is a top view of the electronic device structure shown in FIG. 8A;

[0022] FIG. 9A is a side cross-sectional view of the electronic device structure after formation of a liner in the etched structure according to some embodiments;

[0023] FIG. 9B is a top view of the electronic device structure shown in FIG. 9A;

[0024] FIG. 10A is a side cross-sectional view of the electronic device structure after gapfill of the etched structure in accordance with one or more embodiment;

[0025] FIG. 10B is a top view of the electronic device structure shown in FIG. 10A;

[0026] FIG. 11A is a side cross-sectional view of the electronic device structure after masking in accordance with one or more embodiment;

[0027] FIG. 11B is a top view of the electronic device structure shown in FIG. 11A;

[0028] FIG. 12A is a side cross-sectional view of the electronic device structure after etching the dielectric and exposing the pillars in accordance with one or more embodiment;

[0029] FIG. 12B is a top view of the electronic device structure shown in FIG. 12A;

[0030] FIG. 13A is a side cross-sectional view of the electronic device structure after removal of the pillars in accordance with one or more embodiment;

[0031] FIG. 13B is a top view of the electronic device structure shown in FIG. 13A;

[0032] FIG. 14A is a side cross-sectional view of the electronic device structure after blanket deposition in accordance with one or more embodiment;

[0033] FIG. 14B is a top view of the electronic device structure shown in FIG. 14A; and

[0034] FIG. 15 shows a schematic of a processing chamber to form the electronic device structure in accordance with one or more embodiment of the disclosure.

[0035] In the appended figures, similar components and/or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a dash and a second label that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the second reference label.

DETAILED DESCRIPTION

[0036] Before describing several exemplary embodiments of the invention, it is to be understood that the invention is not limited to the details of construction or process steps set forth in the following description. The invention is capable of other embodiments and of being practiced or being carried out in various ways.

[0037] A "substrate" as used herein, refers to any substrate or material surface formed on a substrate upon which film processing is performed during a fabrication process. For example, a substrate surface on which processing can be performed include materials such as silicon, silicon oxide, strained silicon, silicon on insulator (SOI), carbon doped silicon oxides, amorphous silicon, doped silicon, germanium,

gallium arsenide, glass, sapphire, and any other materials such as metals, metal nitrides, metal alloys, and other conductive materials, depending on the application. Substrates include, without limitation, semiconductor wafers. Substrates may be exposed to a pretreatment process to polish, etch, reduce, oxidize, hydroxylate, anneal, UV cure, *e*-beam cure and/or bake the substrate surface. In addition to film processing directly on the surface of the substrate itself, in the present invention, any of the film processing steps disclosed may also be performed on an underlayer formed on the substrate as disclosed in more detail below, and the term "substrate surface" is intended to include such underlayer as the context indicates. Thus for example, where a film/layer or partial film/layer has been deposited onto a substrate surface, the exposed surface of the newly deposited film/layer becomes the substrate surface.

[0038] One or more embodiments of the disclosure are directed to methods and apparatus to provide self-aligned vias and air gaps. The various aspects of the disclosure are described with respect to a detailed process illustrated in the Figures.

[0039] FIG. 1A illustrates a top view 100 and a cross-sectional view 110 of an electronic device structure to provide a fully self-aligned via or air gap according to some embodiments. The cross-sectional view 110 is along an axis A-A', as depicted in FIG. 1A. FIG. 1B is a perspective view 120 of the electronic device structure depicted in FIG. 1A. A lower metallization layer (Mx) comprises a set of conductive lines 104 that extend along an X axis (direction) 121 on an insulating layer 102 on a substrate 101, as shown in FIGS. 1A and 1B. As shown in FIG. 1B, X direction 121 crosses a Y axis (direction) 122 at an angle 123. In one or more embodiments, angle 123 is about 90 degrees. In some embodiments, angle 123 is an angle that is other than a 90 degrees angle. The insulating layer 102 comprises trenches 104. The conductive lines 103 are deposited in trenches 104.

[0040] In some embodiments, the substrate 101 comprises a semiconductor material, e.g., silicon (Si), carbon (C), germanium (Ge), silicon germanium (SiGe), gallium arsenide (GaAs), InP, GaAs, InGaAs, InAlAs, other semiconductor material, or any combination thereof. In some embodiments, substrate 101 is a semiconductor-on-isolator (SOI) substrate including a bulk lower substrate, a middle insulation layer, and

a top monocrystalline layer. The top monocrystalline layer may comprise any material listed above, e.g., silicon. In various embodiments, the substrate 101 can be, for example, an organic, a ceramic, a glass, or a semiconductor substrate. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which passive and active electronic devices (e.g., transistors, memories, capacitors, inductors, resistors, switches, integrated circuits, amplifiers, optoelectronic devices, or any other electronic devices) may be built falls within the spirit and scope of the present disclosure.

[0041] In some embodiments, substrate 101 includes one or more metallization interconnect layers for integrated circuits. In some embodiments, the substrate 101 includes interconnects, for example, vias, configured to connect the metallization layers. In some embodiments, the substrate 101 includes electronic devices, e.g., transistors, memories, capacitors, resistors, optoelectronic devices, switches, and any other active and passive electronic devices that are separated by an electrically insulating layer. For example, an interlayer dielectric, a trench insulation layer or any other insulating layer known to one of ordinary skill in the art of the electronic device manufacturing. In some embodiments, the substrate includes one or more buffer layers to accommodate for a lattice mismatch between the substrate 101 and one or more layers above substrate 101 and to confine lattice dislocations and defects.

[0042] Insulating layer 102 can be any material suitable to insulate adjacent devices and prevent leakage. In some embodiments, electrically insulating layer 102 is an oxide layer, e.g., silicon dioxide, or any other electrically insulating layer determined by an electronic device design. In some embodiments, insulating layer 102 comprises an interlayer dielectric (ILD). In some embodiments, insulating layer 102 is a low-k dielectric that includes, but is not limited to, materials such as, e.g., silicon dioxide, silicon oxide, carbon doped oxide ("CDO"), e.g., carbon doped silicon dioxide, porous silicon dioxide, silicon nitride or any combination thereof.

[0043] In some embodiments, insulating layer 102 includes a dielectric material having k value less than 5. In some embodiments, insulating layer 102 includes a dielectric material having k-value less than 2. In some embodiments, insulating layer 102 includes a nitride, oxide, a polymer, phosphosilicate glass, Fluorosilicate (SiOF)

glass, organosilicate glass (SiOCH), other electrically insulating layer determined by an electronic device design, or any combination thereof. In some embodiments, insulating layer 102 may include polyimide, epoxy, photodefinable materials, such as benzocyclobutene (BCB), and WPR-series materials, or spin-on-glass.

[0044] In some embodiments, insulating layer 102 is a low-k interlayer dielectric to isolate one metal line from other metal lines on substrate 101. In some embodiments, the thickness of the layer 102 is in an approximate range from about 10 nanometers (nm) to about 2 microns (μm).

[0045] In some embodiments, insulating layer 102 is deposited using one of deposition techniques, such as but not limited to a chemical vapor deposition ("CVD"), a physical vapor deposition ("PVD"), molecular beam epitaxy ("MBE"), metalorganic chemical vapor deposition ("MOCVD"), atomic layer deposition ("ALO"), spin~on, or other insulating deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

[0046] In some embodiments, the lower metallization layer Mx comprising metal lines 103 is a part of a back end metallization of the electronic device. In some embodiments, the insulating layer 102 is patterned and etched using a hard mask to form trenches 104 using one or more patterning and etching techniques known to one of ordinary skill in the art of microelectronic device manufacturing. In some embodiments, the size of trenches in the insulating layer 104 is determined by the size of conductive lines formed later on in a process.

[0047] In some embodiments, forming the conductive lines 103 involves filling the trenches 104 with a layer of conductive material. In some embodiments, a base layer (not shown) is first deposited on the internal sidewalls and bottom of the trenches 104, and then the conductive layer is deposited on the base layer. In some embodiments, the base layer includes a conductive seed layer (not shown) deposited on a conductive barrier layer (not shown). The seed layer can include copper, and the conductive barrier layer can include aluminum, titanium, tantalum, tantalum nitride, and the like metals. The conductive barrier layer can be used to prevent diffusion of the conductive material from the seed layer, e.g., copper, into the insulating layer 102.

Additionally, the conductive barrier layer can be used to provide adhesion for the seed layer (e.g., copper).

[0048] In some embodiments, to form the base layer, the conductive barrier layer is deposited onto the sidewalls and bottom of the trenches 104, and then the seed layer is deposited on the conductive barrier layer. In another embodiment, the conductive base layer includes the seed layer that is directly deposited onto the sidewalls and bottom of the trenches 104. Each of the conductive barrier layer and seed layer may be deposited using any thin film deposition technique known to one of ordinary skill in the art of semiconductor manufacturing, e.g., sputtering, blanket deposition, and the like. In one embodiment, each of the conductive barrier layer and the seed layer has the thickness in an approximate range from about 1 nm to about 100 nm. In some embodiments, the barrier layer may be a thin dielectric that has been etched to establish conductivity to the metal layer below. In some embodiments, the barrier layer may be omitted altogether and appropriate doping of the copper line may be used to make a "self-forming barrier".

[0049] In some embodiments, the conductive layer e.g., copper, is deposited onto the seed layer of base layer of copper, by an electroplating process. In some embodiments, the conductive layer is deposited into the trenches 104 using a damascene process known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, the conductive layer is deposited onto the seed layer in the trenches 104 using a selective deposition technique, such as but not limited to electroplating, electroless, a CVD, PVD, MBE, MOCVD, ALO, spin-on, or other deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

[0050] In some embodiments, the choice of a material for conductive layer for the conductive lines 103 determined the choice of a material for the seed layer. For example, if the material for the conductive lines 103 includes copper, the material for the seed layer also includes copper. In some embodiments, the conductive lines 103 include a metal, for example, copper (Cu), ruthenium (Ru), nickel (Ni), cobalt (Co), chromium (Cr), iron (Fe), manganese (Mn), titanium (Ti), aluminum (Al), hafnium (Hi), tantalum (Ta), tungsten (W), Vanadium (V), Molybdenum (Mo), palladium (Pd), gold

(Au), silver (Au), platinum Pl, indium (In), tin (Sn), lead (Pb), antimony (Sb), bismuth (Bi), zinc (Zn), cadmium (Cd), or any combination thereof.

[0051] In alternative embodiments, examples of the conductive materials that may be used for the conductive lines 103 of the metallization layer Mx are, but not limited to, metals, e.g., copper, tantalum, tungsten, ruthenium, titanium, hafnium, zirconium, aluminum, silver, tin, lead, metal alloys, metal carbides, e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, aluminum carbide, other conductive materials, or any combination thereof.

[0052] In some embodiments, portions of the conductive layer and the base layer are removed to even out top portions of the conductive lines 103 with top portions of the insulating layer 102 using a chemical-mechanical polishing ("CMP") technique known to one of ordinary skill in the art of microelectronic device manufacturing.

[0053] In one non-limiting example, the thickness of the conductive lines 103 is in an approximate range from about 15 nm to about 1000 nm. In one non-limiting example, the thickness of the conductive lines 103 is from about 20 nm to about 200 nm. In one non-limiting example, the width of the conductive lines 103 is in an approximate range from about 5 nm to about 500 nm. In one non-limiting example, the spacing (pitch) between the conductive lines 103 is from about 2 nm lo about 500 nm. In more specific non-limiting example, the spacing (pitch) between the conductive lines 103 is from about 5 nm to about 50 nm.

[0054] In some embodiments, the lower metallization layer Mx is configured to connect to other metallization layers (not shown). In some embodiments, the metallization layer Mx is configured to provide electrical contact lo electronic devices, e.g., transistors, memories, capacitors, resistors, optoelectronic devices, switches, and any other active and passive electronic devices that are separated by an electrically insulating layer, for example, an interlayer dielectric, a trench insulation layer, or any other insulating layer known to one of ordinary skill in the art of electronic device manufacturing.

[0055] FIG. 2A is a view 200 similar to view 110 of FIG. 1A, after the conductive lines 103 are recessed according to some embodiments. FIG. 2B is a view 210 similar to FIG. 1B, after the conductive lines 103 are recessed according to some

embodiments. The conductive lines 103 are recessed to a predetermined depth to form recessed conductive lines 201. As shown in FIGS. 2A and 2B, trenches 202 are formed in the insulating layer 102. Each trench 202 has sidewalls 204 that are portions of insulating layer 102 and a bottom that is a top surface 203 of the recessed conductive line 201.

[0056] In some embodiments, the depth of the trenches 202 is from about 10 nm to about 500 nm. In some embodiments, the depth of the trenches 202 is from about 10% to about 100% of the thicknesses of the conductive lines. In some embodiments, the conductive lines 103 are recessed using one or more of wet etching, dry etching, or a combination of techniques known to one of ordinary skill in the art of electronic device manufacturing.

[0057] FIG. 3 is a view 300 similar to FIG. 2A, after a liner 301 is deposited on the recessed conductive lines 201 according to some embodiments. Liner 301 is deposited on the bottom and sidewalls of the trenches 202, as shown in FIG. 3.

[0058] In some embodiments, liner 301 is deposited to protect the conductive lines 201 from changing the properties later on in a process (e.g., during tungsten deposition, or other processes). In some embodiments, liner 301 is a conductive liner. In another embodiment, liner 301 is a non-conductive liner. In some embodiments, when liner 301 is a non-conductive liner, the liner 301 is removed later on in a process, as described in further detail below. In some embodiments, liner 301 includes titanium nitride (TiN), titanium (Ti), tantalum (Ta), tantalum nitride (TaN), or any combination thereof. In another embodiment, liner 301 is an oxide, e.g., aluminum oxide (AlO), titanium oxide (TiO_2). In yet another embodiment, liner 301 is a nitride, e.g., silicon nitride (SiN). In an embodiment, the liner 301 is deposited to the thickness from about 0.5 nm to about 10 nm.

[0059] In some embodiments, the liner 301 is deposited using an atomic layer deposition (ALD) technique. In some embodiments, the liner 301 is deposited using one of deposition techniques, such as but not limited to a CVD, PVD, MBE, MOCVD, spin-on, or other liner deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

[0060] FIG. 4 is a view 400 similar to FIG. 3, after a seed gapfill layer 401 is deposited on the liner 301 according to some embodiments. In some embodiments, seed gapfill layer 401 is a self-aligned selective growth seed film. As shown in FIG. 4, seed gapfill layer 401 is deposited on liner 301 on the top surface 203 of the recessed conductive lines 201, the sidewalls 204 of the trenches 202 and top portions of the insulating layer 102. In some embodiments, seed gapfill layer 401 is a tungsten (W) layer, or other seed gapfill layer to provide selective growth pillars. In some embodiments, seed gapfill layer 401 is a metal film or a metal containing film. Suitable metal films include, but are not limited to, films including one or more of Co, Mo, W, Ta, Ti, Ru, rhodium (Rh), Cu, Fe, Mn, V, Niobium (Nb), hafnium (Hf), Zirconium (Zr), Yttrium (Y), Al, Sn, Cr, Lanthanum (La), or any combination thereof. In some embodiments, seed gapfill layer 401 comprises is a tungsten (W) seed gapfill layer.

[0061] In some embodiments, the seed gapfill layer 401 is deposited using one of deposition techniques, such as but not limited to an ALD, a CVD, PVD, MBE, MOCVD, spin-on, or other liner deposition techniques known lo one of ordinary skill in the art of microelectronic device manufacturing.

[0062] FIG. 5A is a view 500 similar to FIG. 4, after portions of the seed gapfill layer 401 are removed to expose top portions of the insulating layer 102 according to one embodiment. FIG. 5B is a perspective view of the electronic device structure shown in FIG. 5A. In some embodiments, the portions of the seed gapfill layer 401 are removed using one of the chemical-mechanical polishing (CMP) techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

[0063] FIG. 6A is a view 600 similar to FIG. 5A, and FIG. 6B is a view 610 similar to FIG. 5B, after self-aligned selective growth pillars 601 are formed using the seed gap fill layer 401 on the liner 301 on the recessed conductive lines 201 according to one or more embodiment. As shown in FIGS. 6A and 6B, an array of the self-aligned selective growth pillars 601 has the same pattern as the set of the conductive lines 201. As shown in FIGS. 6A and 6B, the pillars 601 extend substantially orthogonally from the top surfaces of the conductive lines 201. As shown in FIGS. 6A and 6B, the pillars 601 extend along the same direction as the conductive lines 201. As shown in FIGS. 6A and 6B, the pillars 601 are separated by gaps 603.

[0064] In some embodiments, the pillars 601 are selectively grown from the seed gapfill layer 401 on portions of the liner 301 on the conductive lines 201. The pillars 601 are not grown on portions of the liner 301 on the insulating layer 102, as shown in FIGS. 6A and 6B. In some embodiments, portions of the seed gapfill layer 401 above the conductive lines 201 are expanded for example, by oxidation, nitridation, or other process to grow pillars 601. In some embodiments, the seed gapfill layer 401 is oxidized by exposure to an oxidizing agent or oxidizing conditions to transform the metal or metal containing seed gapfill layer 401 to metal oxide pillars 601. In some embodiments, pillars 601 include an oxide of one or more metals listed above. In more specific embodiment, pillars 601 include tungsten oxide (e.g., WO, WO_3 and other tungsten oxide).

[0065] The oxidizing agent can be any suitable oxidizing agent including, but not limited to, O_2, O_3, N_2O, H_2O, H_2O_2, CO, CO_2, NH_3, N_2/Ar, N_2/He, N_2/Ar/He or any combination thereof. In some embodiments, the oxidizing conditions comprise a thermal oxidation, plasma enhanced oxidation, remote plasma oxidation, microwave and radio-frequency oxidation (e.g., inductively coupled plasma (ICP), capacitively coupled plasma (CCP)).

[0066] In some embodiments, the pillars 601 are formed by oxidation of the seed gapfill layer at any suitable temperature depending on, for example, the composition of the seed gapfill layer and the oxidizing agent. In some embodiments, the oxidation occurs at a temperature in an approximate range of about 25 degrees C to about 800 degrees C. In some embodiments, the oxidation occurs at a temperature greater than or equal to about 150 ºC. In some embodiments, the height 602 of the pillars 601 is in an approximate range from about 5 angstroms (A.) to about 10 microns (μm).

[0067] FIG. 7A is a view 700 similar to FIG. 6A, and FIG. 7B is a view 710 similar to FIG. 6B, after an insulating layer 701 is deposited to overfill the gaps 603 between the pillars 601 according to some embodiments. As shown in FIGS. 7A and 7B, insulating layer 701 is deposited on the opposing sidewalls 702 and top portions 703 of the pillars 601 and through the gaps 603 on the portions of the insulating layer 102 and liner 301 between the pillars 601.

[0068] In some embodiments, insulating layer 701 is a low-k gapfill layer. In one embodiment, insulating layer 701 is a flowable silicon oxide (FSiOx) layer. In some embodiments, insulating layer 701 is an oxide layer, e.g., silicon dioxide, or any other electrically insulating layer determined by an electronic device design. In some embodiments, insulating layer 701 is an interlayer dielectric (ILD). In some embodiments, insulating layer 701 is a low-k dielectric that includes, but is not limited to, materials such as, e.g., silicon dioxide, silicon oxide, a carbon based material, e.g., a porous carbon film, carbon doped oxide ("CDO"), e.g., carbon doped silicon dioxide, porous silicon dioxide, porous silicon oxide carbide hydride (SiOCH), silicon nitride, or any combination thereof. In some embodiments, insulating layer 701 is a dielectric material having k-value less than 3. In some embodiments, insulating layer 701 is a dielectric material having k-value in an approximate range from about 2.2 to about 2.7. In some embodiments, insulating layer 701 includes a dielectric material having k-value less than 2. In some embodiments, insulating layer 701 represents one of the insulating layers described above with respect to insulating layer 102.

[0069] In some embodiments, insulating layer 701 is a low-k interlayer dielectric to isolate one metal line from other metal lines. In some embodiments, insulating layer 701 is deposited using one of deposition techniques, such as but not limited to a CVD, spin-on, an ALD, PVD, MBE, MOCVD, or other low-k insulating layer deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

[0070] FIG. 8A is a view 800 similar to FIG. 7A, and FIG. 8B is a view 810 similar to FIG. 7B, after an insulating layer 701 is deposited a dual damascene etch 801 is performed in the insulating layer 701. The dual damascene etch can be performed by any suitable method known to those skilled in the art. Briefly, a mask (not shown) is applied or positioned adjacent insulting layer 701and the etch 801 is performed through the mask. The etch 801 extends through insulating layer 701, extending between two adjacent pillars 601. The sides 802 of the etch 801 can extend up to a side of the pillar 601. The etch 801 removes liner 301 between the adjacent pillars 601 to expose insulating layer 102. A top view 810 shows a rectangular etch 801 in insulating layer 701 exposing the insulating layer 102 with liner 301 on either side of

the insulating layer 102. The opening between the adjacent pillars 601 is referred to as a contact hole.

[0071] FIG. 9A is a view 900 similar to FIG. 8A, and FIG. 9B is a view 910 similar to FIG. 8B, after the dual damascene etch 801 a conformal liner 901 is formed in the opening formed by the etch 801.

[0072] In some embodiments, liner 901 is deposited to protect the dielectric 701, pillar 601 and/or dielectric 301 from later processes (e.g., during tungsten deposition, or other processes). In some embodiments, liner 901 is a conductive liner. In another embodiment, liner 901 is a non-conductive liner. In some embodiments, when liner 901 is a non-conductive liner, the liner 901 can be removed later on in a process, as described in further detail below. In some embodiments, liner 901 includes titanium nitride (TiN), titanium (Ti), tantalum (Ta), tantalum nitride (TaN), or any combination thereof. In another embodiment, liner 901 is an oxide, e.g., aluminum oxide (AlO), titanium oxide (TiO_2). In yet another embodiment, liner 901 is a nitride, e.g., silicon nitride (SiN). In an embodiment, the liner 901 is deposited to the thickness from about 0.5 nm to about 10 nm.

[0073] In some embodiments, the liner 901 is deposited using an atomic layer deposition (ALD) technique. In some embodiments, the liner 901 is deposited using one of deposition techniques, such as but not limited to a CVD, PVD, MBE, MOCVD, spin-on, or other liner deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

[0074] Liner 901 forms conformally on dielectric 701 and dielectric 102. As used herein, the term "conformal", or "conformally", refers to a layer that adheres to and uniformly covers exposed surfaces with a thickness having a variation of less than 1% relative to the average thickness of the film. For example, a 1,000 Å thick film would have less than 10 Å variations in thickness. This thickness and variation includes edges, corners, sides, and the bottom of recesses. For example, a conformal layer deposited by ALD in various embodiments of the disclosure would provide coverage over the deposited region of essentially uniform thickness on complex surfaces.

[0075] In some embodiments, the liner 901 is a continuous film. As used herein, the term "continuous" refers to a layer that covers an entire exposed surface without

gaps or bare spots that reveal material underlying the deposited layer. A continuous layer may have gaps or bare spots with a surface area less than about 1% of the total surface area of the film.

[0076] FIG. 10A is a view 1000 similar to FIG. 9A, and FIG. 10B is a view 1010 similar to FIG. 9B, after the conformal liner 901 is deposited, a metal 1001 (also referred to as M2) is deposited in the opening formed by etch 801 lined with liner 901. FIG. 10 shows the metal 1001 even with the top of the dielectric 701. The even top can be formed by depositing the gapfill metal 1001 to provide a sufficient amount of overburden on the surface followed by a chemical mechanical planarization process to form an even surface.

[0077] The metal 1001 can be any suitable metal. In some embodiments, the film 130 is a metal film or a metal containing film. Suitable metal films include, but are not limited to, films including one or more of Co, Mo, W, Ta, Ti, Ru, Rh, Cu, Fe, Mn, V, Nb, Hf, Zr, Y, Al, Sn, Cr and/or La. In some embodiments, the metal film comprises tungsten. In another embodiment, the metal 1001 is deposited using an atomic layer deposition (ALD) technique. In some embodiments, the metal 1001 is deposited using one of deposition techniques, such as but not limited to a CVD, PVD, MBE, MOCVD, spin-on, or other liner deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

[0078] FIG. 11A is a view 1100 similar to FIG. 10A, and FIG. 11B is a view 1110 similar to FIG. 10B. After deposition of the M2 metal 1001, a mask 1101 is applied to cover the via formed by metal 1001. The top view of FIG. 11B shows the metal 1001 covered and protected by the mask 1101. The mask can be any suitable mask that can protect the metal 1001 for subsequent processes.

[0079] FIGS. 12A and 12B illustrates the result of etching after mask 1101 has been applied. The side view 1101 in FIG. 12A appears the same as FIG. 11A because the changes due to etching occur in a different plane that that illustrated. FIG. 12B shows a top view 1110 with the dielectric 701 and pillar 601 exposed.

[0080] FIGS. 13A and 13B show side view 1300 and top view 1310 after removal of the pillars 601 to leave air gaps 1301. Removal of the pillars 601 can be done by an isotropic etch that can etch sideways to remove material from beneath the mask

1101. The etching or removal process can be selective for the pillar 601 material relative to the liner 301, liner 901 and/or dielectric 701. In some embodiments, etching removes substantially all of the pillar 601 leaving air gap 1301 having substantially the same shape and size of the pillar 601. As used in this regard, the term "all of the pillar" means that greater than or equal to about 90%, 95%, 98% or 99% of the pillar (by volume) is removed.

[0081] Etching of the pillars 601 can be done by any suitable technique. In some embodiments, etching the pillars 601 comprises exposing the pillars 601 to a metal halide compound. In some embodiments, the metal halide compound has a different metal than the pillars 601.

[0082] In some embodiments, etching the pillars 601 comprises exposure to a metal-and-halogen-containing precursor (e.g. WCl_6), also referred to as a metal halide precursor. The metal halide precursor can react with the pillars 601.

[0083] In some embodiments, exposure to the metal halide precursor causes an exothermic reaction with the pillar material and no plasma is present in the substrate processing region. No plasma excites the metal-halide precursor prior to entering the substrate processing region according to one or more embodiments.

[0084] In an exemplary non-limiting process, the pillars comprise tungsten and grown by reaction with oxygen to form the tungsten oxide pillars, which may take the form of WO_3. Exposure of WO_3 to WCl_6 (or possibly WCl_5) forms volatile $WOCl_4$ and/or WO_2Cl_2 which leaves the surface until all tungsten oxide is removed. The reaction can spontaneously stop once the tungsten oxide portion (or metal oxide portion in general) is removed. The process can be repeated an integral number of cycles. Each cycle may remove a selectable amount of the original tungsten film (e.g. 1 or 2 monolayers).

[0085] In some embodiments, the metal halide precursor includes two or more or only two different elements including a metal element and a halogen element. The metal halide precursor may include only a single atom of the metal element but multiple atoms of the same halogen element (as is the case for WCl_6 and WCl_5). The metal element of the metal halide may include one or more of titanium, hafnium, zirconium, vanadium, niobium, tantalum, chromium, molybdenum, tungsten,

manganese, rhenium, technetium, iron, aluminum and gallium in embodiments. In some embodiments, the metal element of the metal halide has an atomic number of 22, 23, 24, 40, 41, 42, 72, 73 or 74. In one or more embodiments, the metal element comprises an element of group 4, group 5 or group 6 of the periodic table or may be transition metals. The halogen element may be one of F and Cl according to one or more embodiments. The halogen element may be one or more of F, Cl, Br and/or I. In some embodiments, the metal-and-halogen-containing precursor fluorine-free. Some examples of suitable metal halide precursors include, but are not limited to, vanadium pentahalides, tantalum pentahalides, chromium hexahalides, molybdenum pentahalides, molybdenum hexahalides, niobium pentahalides, tungsten pentahalides, tungsten hexahalides, and manganese tetrahalides. In some embodiments, the metal halide precursors include, but are not limited to, vanadium halides, tantalum halides, chromium halides, molybdenum halides, niobium halides, tungsten halides and/or manganese halides, where the oxidation state of the metal element can be any suitable oxidation state.

[0086] The etch processes of some embodiments has a selectivity greater than or equal to about 10:1, greater than or equal to about 15:1, greater than or equal to about 20:1 or greater than or equal to about 25:1.

[0087] In some embodiments, there is little or no local plasma used in the etch process to make etch processes more selective, delicate and isotropic. The term "plasma-free" will be used herein to describe the substrate processing region during application of no or essentially no plasma power to the substrate processing region. The etchants (the metal-and-halogen-containing precursor) described possess energetically favorable etch reaction pathways which enable the substrate processing region to be plasma-free during operations of etching metal-containing materials herein. Stated another way, the electron temperature in the substrate processing region may be less than 0.5 eV, less than 0.45 eV, less than 0.4 eV, or less than 0.35 eV according to one or more embodiments. Moreover, the metal-and-halogen-containing precursor may have not been excited in any remote plasma prior to entering the substrate processing region in embodiments. For example, if a remote plasma region or a separate chamber region is present and used to conduct the

halogen-containing precursor toward the substrate processing region, the separate chamber region or remote plasma region may be plasma-free as defined herein.

[0088] FIGS. 14A and 14B illustrate a side view 1400 and top view 1410 after blanket deposition of film 1401. Film 1401 can be any suitable material that does not fill the air gaps 1301 formed from the pillars. In some embodiments, the film 1401 is deposited by a plasma enhanced process. In some embodiments, the film 1401 is a non-conformal film. In some embodiments, the film 1401 comprises an insulating material.

[0089] FIG. 15 shows a block diagram of a plasma system to perform at least some of the operations lo provide a fully self-aligned via according to one embodiment. As shown in FIG. 15, system 1800 has a processing chamber 1801. A movable pedestal 1802 to hold an electronic device structure 1803 is placed in processing chamber 1801. Pedestal 1802 comprises an electrostatic chuck ("ESC"), a DC electrode embedded into the ESC, and a cooling/heating base. In an embodiment, pedestal 1802 acts as a moving cathode. In an embodiment, the ESC comprises an Al_2O_3 material, Y_2O_3, or other ceramic materials known to one of ordinary skill of electronic device manufacturing. A DC power supply 1804 is connected to the DC electrode of the pedestal 1802.

[0090] As shown in FIG. 15, an electronic device structure 1803 is loaded through an opening 1808 and placed on the pedestal 1802. The electronic device structure 1803 represents one of the electronic device structures described above. System 1800 comprises an inlet to input one or more process gases 1812 through a mass flow controller 1811 to a plasma source 1813. A plasma source 1813 comprising a showerhead 1814 is coupled to the processing chamber 1801 to receive one or more gases 1812 to generate plasma. Plasma source 1813 is coupled to a RF source power 1810. Plasma source 1813 through showerhead 1814 generates a plasma 1815 in processing chamber 1801 from one or more process gases 1812 using a high frequency electric field. Plasma 1815 comprises plasma particles, such as ions, electrons, radicals or any combination thereof. In an embodiment, power source 1810 supplies power from about 50W to about 3000W at a frequency from about 400kHz to about 162MHz to generate plasma 1815.

[0091] A plasma bias power 1805 is coupled lo the pedestal 1802 (e.g., cathode) via a RF match 1807 to energize the plasma. In an embodiment. the plasma bias power 1805 provides a bias power that is not greater than I000 W at a frequency between about 2 MHz to 60 MHz. and in a particular embodiment at about 13MHz. A plasma bias power 1806 may also be provided. for example to provide another bias power that is not greater than 1000 W at a frequency from about 400kHz to about 60 MHz, and in a particular embodiment, at about 60 MHz. Plasma bias power 1806 and bias power 1805 are connected lo RF match 1807 to provide a dual frequency bias power. In an embodiment. a total bias power applied lo the pedestal 1802 is from about 10 W to about 3000W.

[0092] As shown in FIG. 15, a pressure control system 1809 provides a pressure to processing chamber 1801. As shown in FIG. 15, chamber 1801 has one or more exhaust outlets 1816 lo evacuate volatile products produced during processing in the chamber. In an embodiment, the plasma system 1800 is an inductively coupled plasma (ICP) system. In an embodiment. the plasma system 180 is a capacitively coupled plasma (CCP) system.

[0093] A control system 1817 is coupled to the chamber 1801. The control system 1817 comprises a processor 1818. a temperature controller 1819 coupled to the processor 1818, a memory 1820 coupled to the processor 1818. and input/output devices 1821 coupled to the processor 1818 to form fully self-aligned via as described herein.

[0094] In one embodiment, the processor 1018 has a configuration to control recessing first conductive lines on a first insulating layer on a substrate, the first conductive lines extending along a first direction on the first insulating layer. The processor 1018 has a configuration lo control depositing a liner on the recessed first conductive lines. The processor has a configuration to control selectively growing a seed layer on the recessed first conductive lines. The processor 1018 has a configuration to control forming pillars using the selectively grown seed layer. The processor 1018 has a configuration lo control depositing a second insulating layer between the pillars. The processor 1018 has a configuration to control removing the

pillars to form air gaps (or trenches) in the second insulating layer. The processor 1018 has a configuration to control depositing a conductive layer into the contact hole, as described above.

[0095] The control system 1817 is configured to perform at least some of the methods as described herein and may be either software or hardware or a combination of both. The plasma system 1800 may be any type of high performance processing plasma systems known in the art, such as but not limited to an etcher, a cleaner, a furnace, or any other plasma system to manufacture electronic devices.

[0096] According to one or more embodiments, the substrate is subjected to processing prior to and/or after forming the layer. This processing can be performed in the same chamber or in one or more separate processing chambers. In some embodiments, the substrate is moved from the first chamber to a separate, second chamber for further processing. The substrate can be moved directly from the first chamber to the separate processing chamber, or it can be moved from the first chamber to one or more transfer chambers, and then moved to the separate processing chamber. Accordingly, the processing apparatus may comprise multiple chambers in communication with a transfer station. An apparatus of this sort may be referred to as a "cluster tool" or "clustered system," and the like.

[0097] Generally, a cluster tool is a modular system comprising multiple chambers which perform various functions including substrate center-finding and orientation, degassing, annealing, deposition and/or etching. According to one or more embodiments, a cluster tool includes at least a first chamber and a central transfer chamber. The central transfer chamber may house a robot that can shuttle substrates between and among processing chambers and load lock chambers. The transfer chamber is typically maintained at a vacuum condition and provides an intermediate stage for shuttling substrates from one chamber to another and/or to a load lock chamber positioned at a front end of the cluster tool. Two well-known cluster tools which may be adapted for the present invention are the Centura® and the Endura®, both available from Applied Materials, Inc., of Santa Clara, Calif. However, the exact arrangement and combination of chambers may be altered for purposes of performing specific steps of a process as described herein. Other processing chambers which

may be used include, but are not limited to, cyclical layer deposition (CLD), atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), etch, pre-clean, chemical clean, thermal treatment such as RTP, plasma nitridation, degas, orientation, hydroxylation and other substrate processes. By carrying out processes in a chamber on a cluster tool, surface contamination of the substrate with atmospheric impurities can be avoided without oxidation prior to depositing a subsequent film.

[0098] According to one or more embodiments, the substrate is continuously under vacuum or "load lock" conditions, and is not exposed to ambient air when being moved from one chamber to the next. The transfer chambers are thus under vacuum and are "pumped down" under vacuum pressure. Inert gases may be present in the processing chambers or the transfer chambers. In some embodiments, an inert gas is used as a purge gas to remove some or all of the reactants. According to one or more embodiments, a purge gas is injected at the exit of the deposition chamber to prevent reactants from moving from the deposition chamber to the transfer chamber and/or additional processing chamber. Thus, the flow of inert gas forms a curtain at the exit of the chamber.

[0099] The substrate can be processed in single substrate deposition chambers, where a single substrate is loaded, processed and unloaded before another substrate is processed. The substrate can also be processed in a continuous manner, similar to a conveyer system, in which multiple substrate are individually loaded into a first part of the chamber, move through the chamber and are unloaded from a second part of the chamber. The shape of the chamber and associated conveyer system can form a straight path or curved path. Additionally, the processing chamber may be a carousel in which multiple substrates are moved about a central axis and are exposed to deposition, etch, annealing, cleaning, etc. processes throughout the carousel path.

[00100] During processing, the substrate can be heated or cooled. Such heating or cooling can be accomplished by any suitable means including, but not limited to, changing the temperature of the substrate support and flowing heated or cooled gases to the substrate surface. In some embodiments, the substrate support includes a heater/cooler which can be controlled to change the substrate temperature

conductively. In one or more embodiments, the gases (either reactive gases or inert gases) being employed are heated or cooled to locally change the substrate temperature. In some embodiments, a heater/cooler is positioned within the chamber adjacent the substrate surface to convectively change the substrate temperature.

[00101] The substrate can also be stationary or rotated during processing. A rotating substrate can be rotated continuously or in discrete steps. For example, a substrate may be rotated throughout the entire process, or the substrate can be rotated by a small amount between exposures to different reactive or purge gases. Rotating the substrate during processing (either continuously or in steps) may help produce a more uniform deposition or etch by minimizing the effect of, for example, local variability in gas flow geometries.

[00102] Reference throughout this specification to "some embodiments," "certain embodiments," "one or more embodiments" or "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in some embodiments of the invention. Thus, the appearances of the phrases such as "in one or more embodiments," "in certain embodiments," "in some embodiments" or "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, materials, or characteristics may be combined in any suitable manner in one or more embodiments.

[00103] Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It will be apparent to those skilled in the art that various modifications and variations can be made to the method and apparatus of the present invention without departing from the spirit and scope of the invention. Thus, it is intended that the present invention include modifications and variations that are within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method to provide self-aligned air gaps, the method comprising:

recessing first conductive lines on a first dielectric layer on a substrate, the first conducting lines extending along a first direction on the first dielectric layer;

forming pillars on the recessed first conductive lines;

depositing a second dielectric layer between the pillars;

etching the second dielectric layer to form a contact hole in the second dielectric layer between adjacent pillars;

depositing a metal film in the contact hole;

removing the second dielectric layer to expose the pillars;

removing the pillars to form air gaps; and

depositing a cap layer to enclose the air gaps.

2. A method to provide self-aligned air gaps, the method comprising:

recessing first conductive lines on a first dielectric layer on a substrate, the first conducting lines extending along a first direction on the first dielectric layer;

forming a conformal liner on the first conductive lines and the first dielectric layer;

selectively depositing a metal in the recessed first conductive lines;

oxidizing the metal to form pillars on the recessed first conductive lines;

depositing a second dielectric layer between the pillars;

etching the second dielectric layer with a dual damascene etch to form a contact hole in the second dielectric layer between adjacent pillars;

forming a conformal liner in the contact hole;

depositing a metal film in the contact hole on the conformal liner;

masking and removing the second dielectric layer to expose the pillars;

masking and removing the pillars to form air gaps; and

depositing a cap layer to enclose the air gaps.

3. The method of claim 1 or 2, further comprising selectively growing a seed layer on the recessed first conductive lines, the pillars being formed from the seed layer.

4. The method of claim 3, wherein the pillars are formed by oxidizing the seed layer.

5. The method of claim 4, wherein the seed layer comprises tungsten and the pillars comprise tungsten oxide.

6. The method of claim 4, further comprising forming a conformal liner on the recessed first conductive lines and the first dielectric layer, the seed layer formed on the conformal liner.

7. The method of claim 1 or 2, further comprising forming a hard mask layer on the second dielectric layer after depositing the metal film and before removing the second dielectric layer to expose the pillars.

8. The method of claim 1 or 2, further comprising forming a conformal liner on the second dielectric after forming the opening in the second dielectric layer.

9. The method of claim 1 or 2, wherein removing the pillars comprises selectively etching the pillars using a metal halide etchant.

10. The method of claim 9, wherein the pillars comprise tungsten oxide and the metal halide etchant comprises a tungsten halide.

11. The method of claim 1 or 2, wherein the second dielectric layer is a flowable film.

12. The method of claim 1 or 2, wherein depositing the metal in the contact hole comprises depositing a metal overburden and removing the overburden to form a metal film that is level with a top of the second dielectric layer.

13. A system to manufacture an electronic device, the system comprising;

a processing chamber comprising a pedestal to hold an electronic device structure comprising a first metallization layer comprising a set of first conductive lines extending along a first direction on a first dielectric layer on a substrate;

a plasma source coupled to the processing chamber to generate plasma; and

a processor coupled to the plasma source, the processor having a first configuration to control recessing the first conductive lines, a second configuration to control forming pillars on the recessed first conductive lines, a third configuration to control depositing a second dielectric between the pillars, a fourth configuration to control a dual damascene etch in the second dielectric to from a contact hole in the second dielectric layer between adjacent pillars and a fifth configuration to control removal of the pillars.

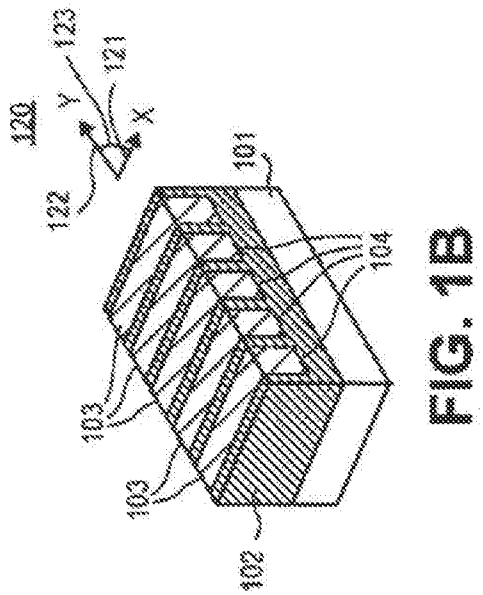


FIG. 1B

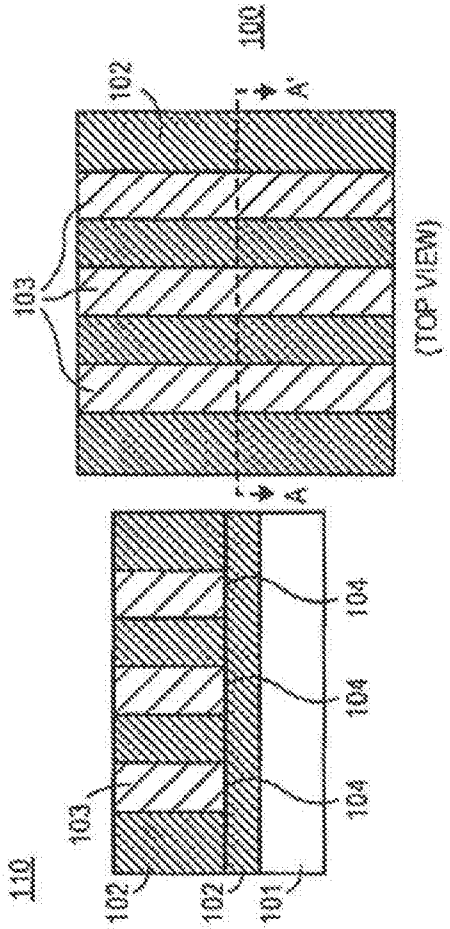


FIG. 1A

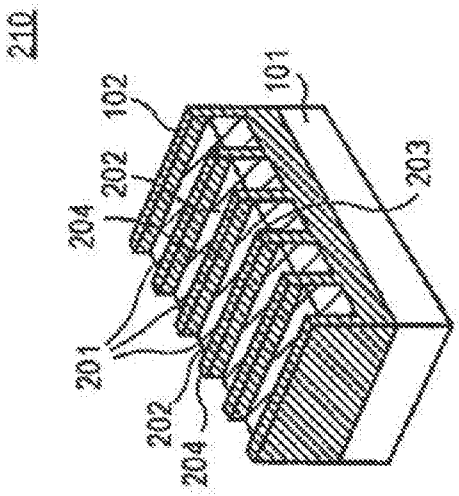


FIG. 2B

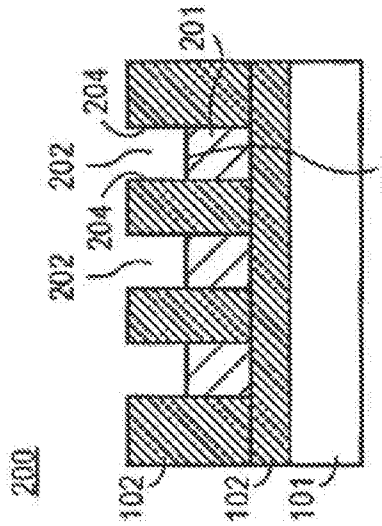


FIG. 2A

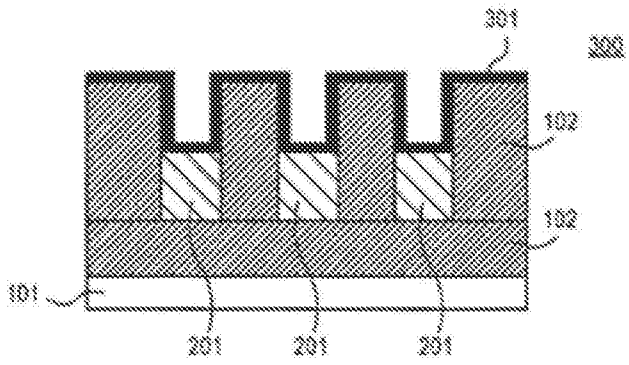


FIG. 3

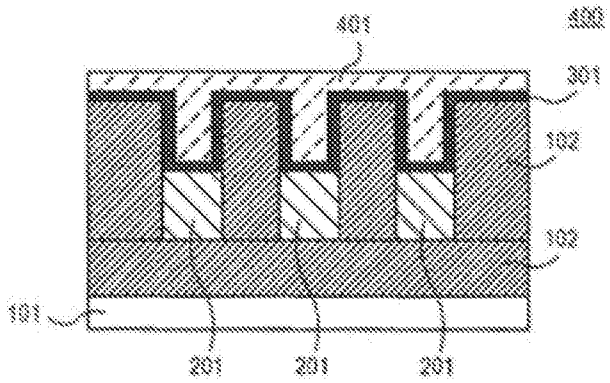


FIG. 4

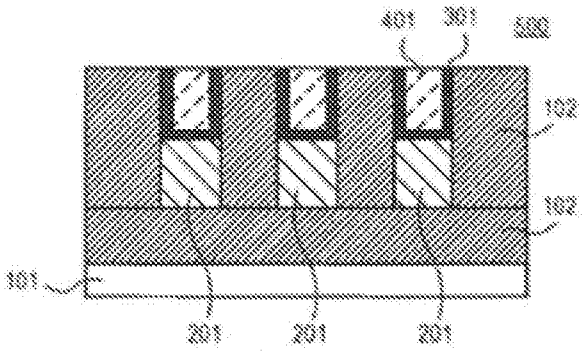


FIG. 5A

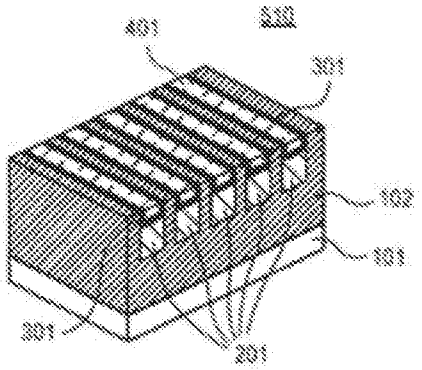


FIG. 5B

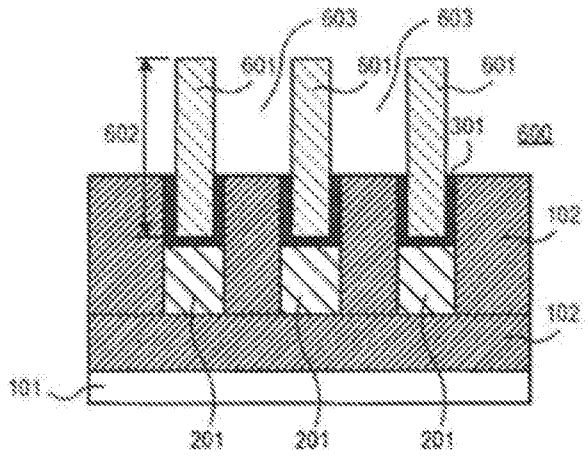


FIG. 6A

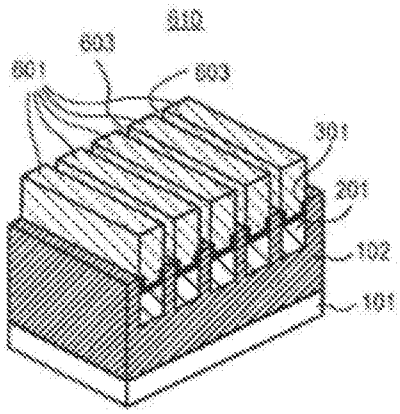


FIG. 6B

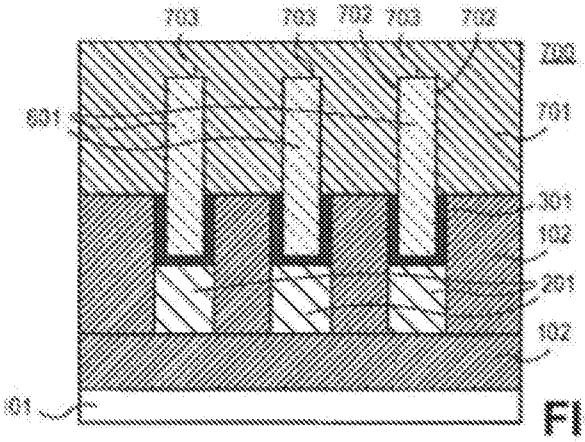


FIG. 7A

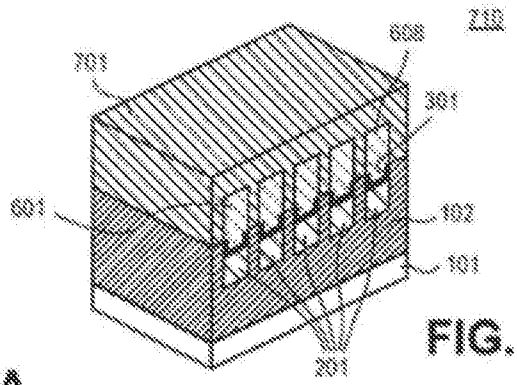


FIG. 7B

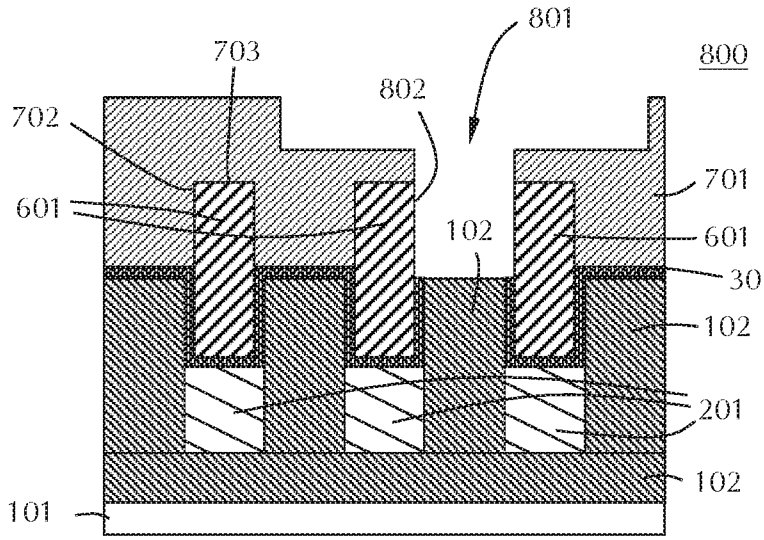


FIG. 8A

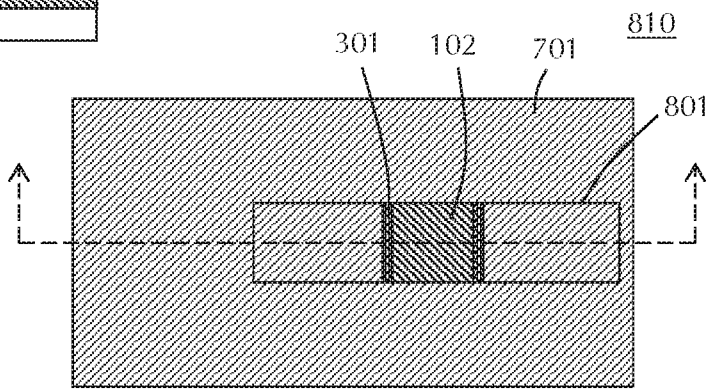


FIG. 8B

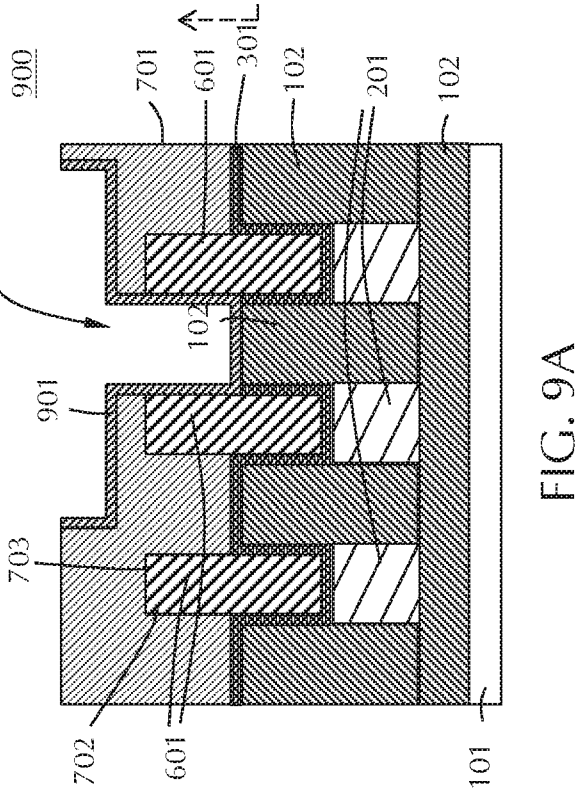


FIG. 9A

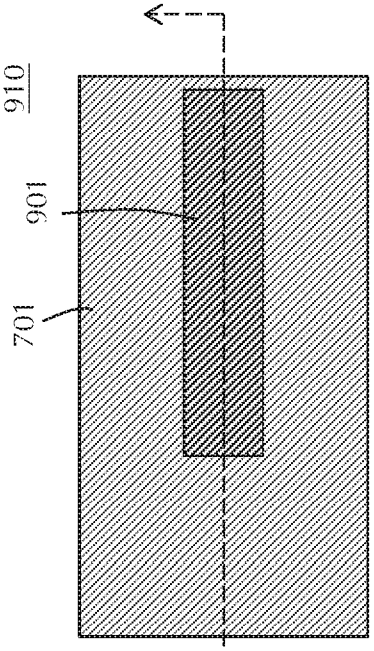


FIG. 9B

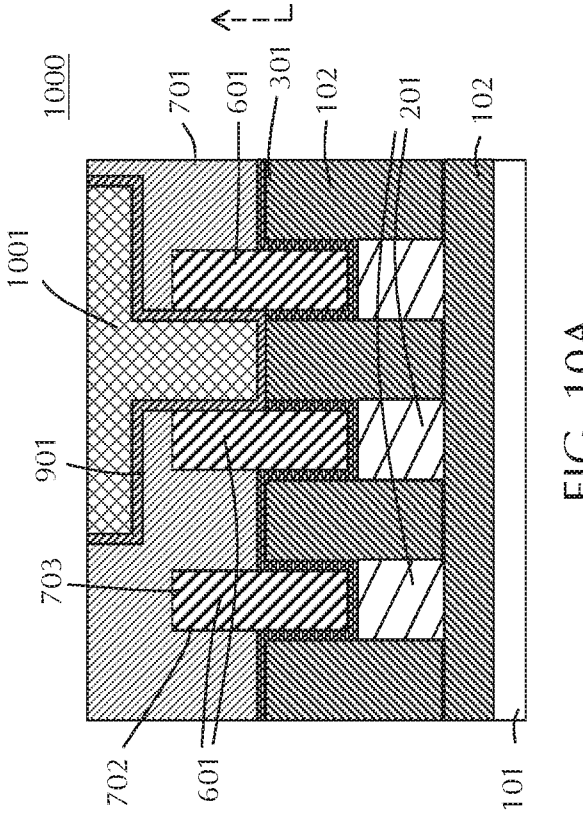


FIG. 10A

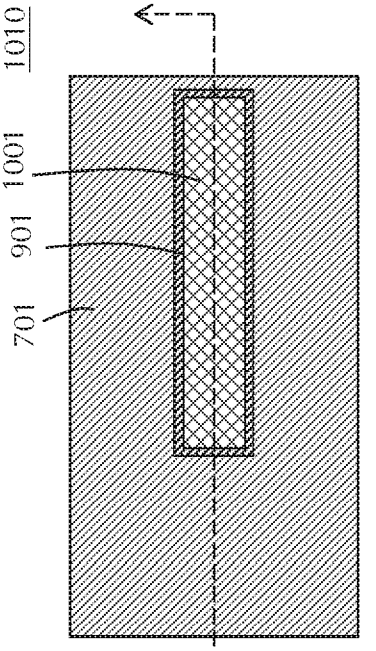


FIG. 10B

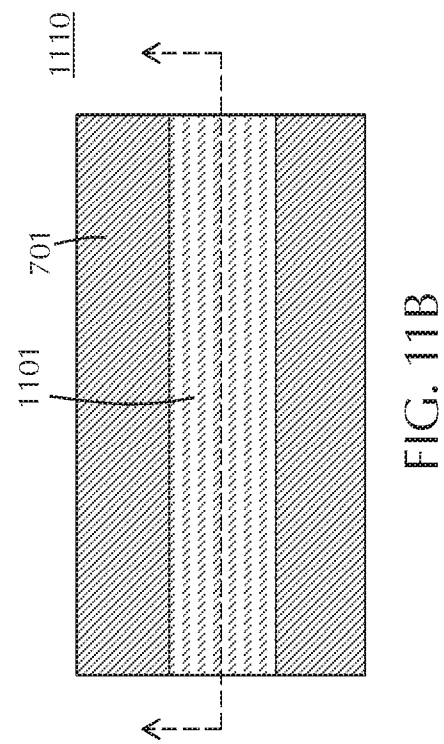


FIG. 11B

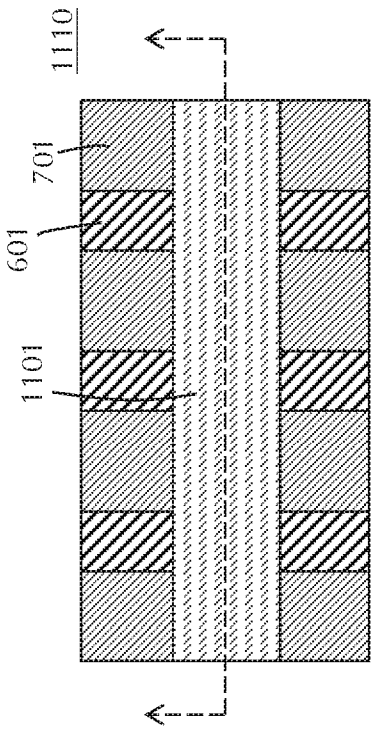


FIG. 12B

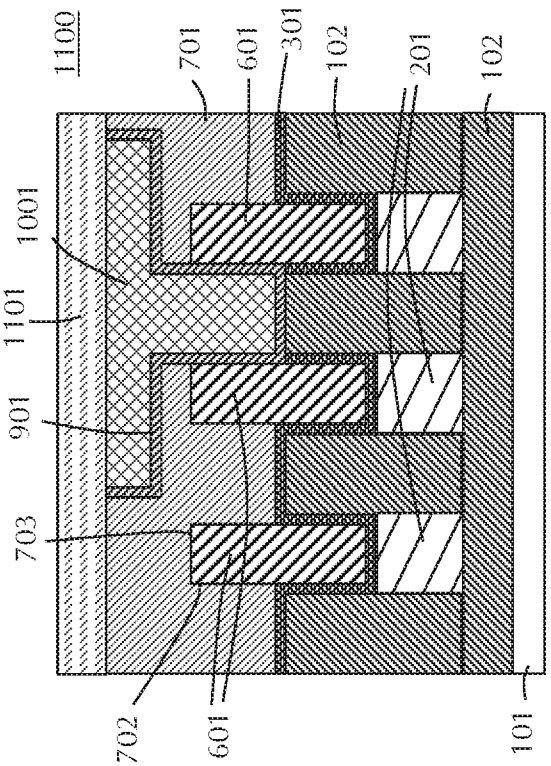


FIG. 11A

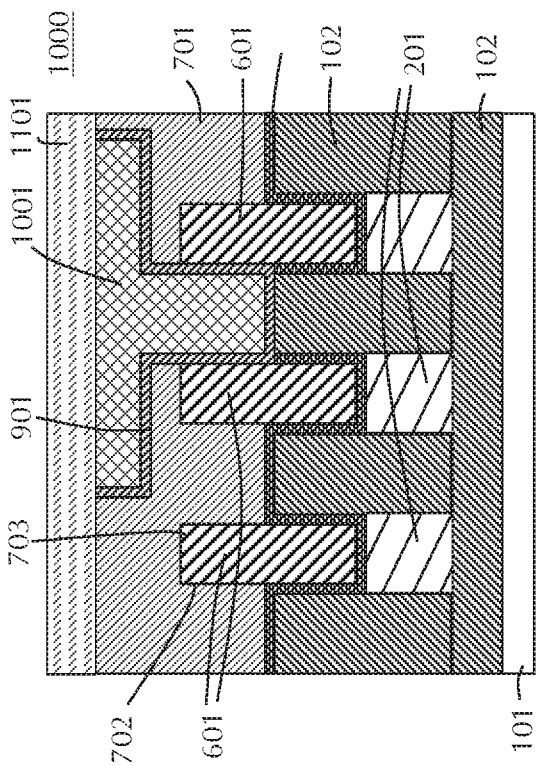


FIG. 12A

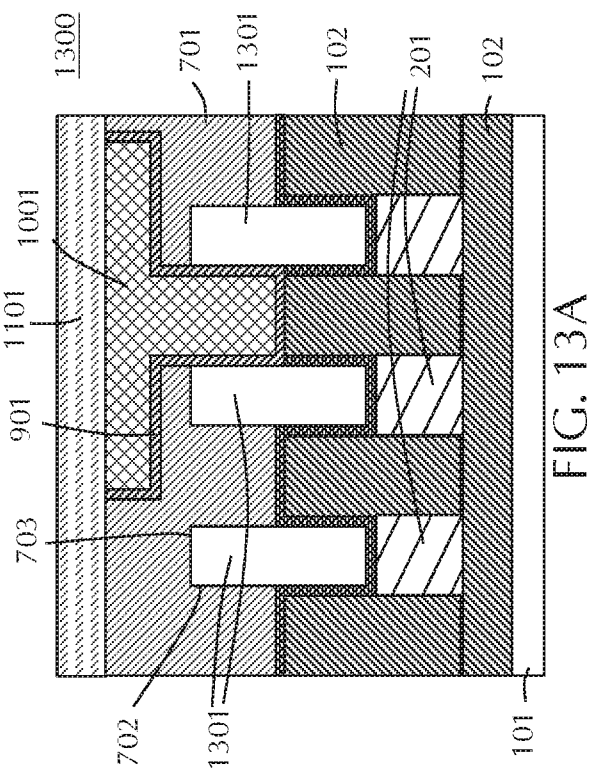


FIG. 13A

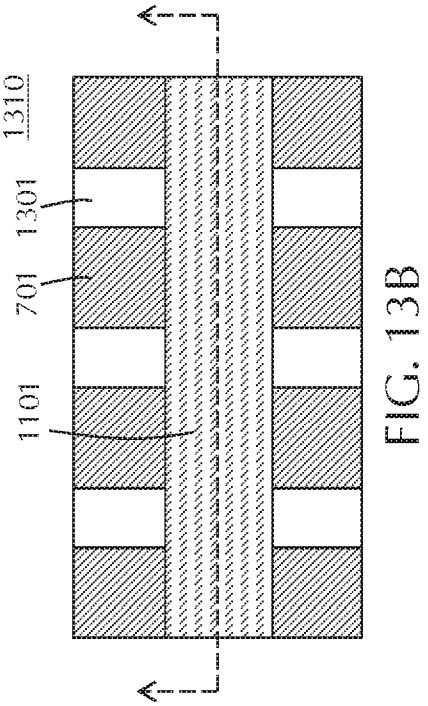


FIG. 13B

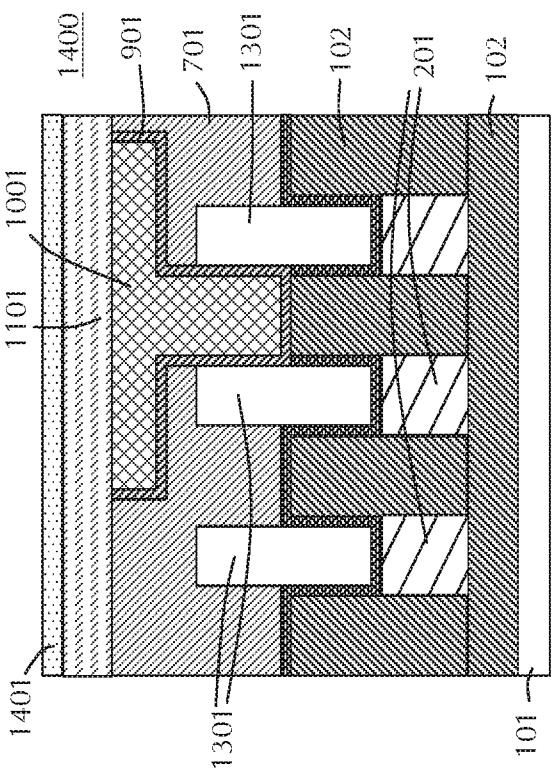


FIG. 14A

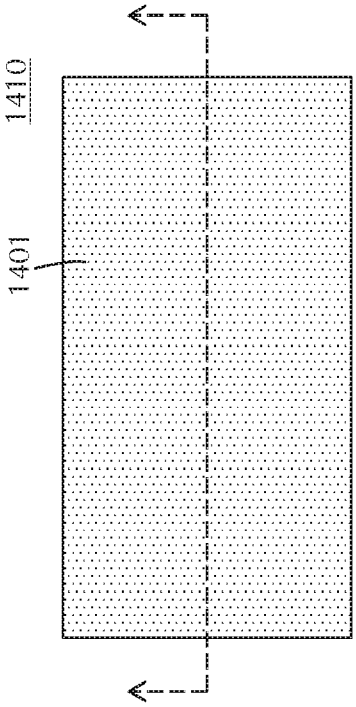


FIG. 14B

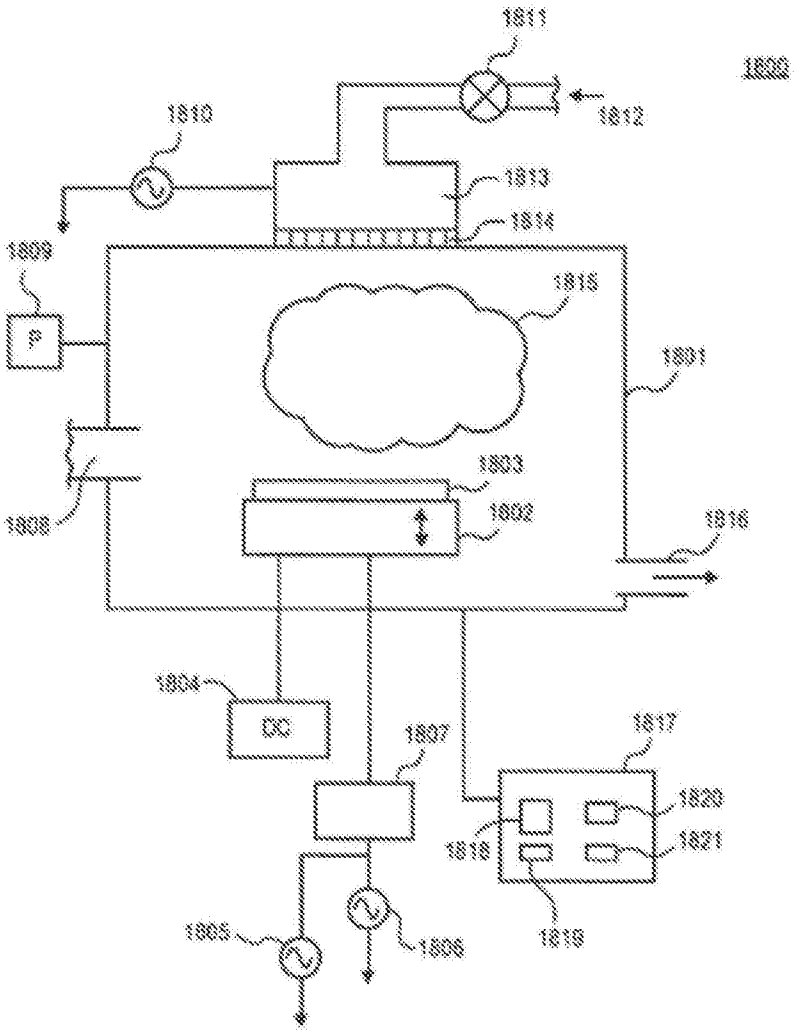

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FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/036690

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i, H01L 21/3065(2006.01)i, C23C 16/455(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; H01L 21/311; H01L 23/528; H01L 23/48; H01L 21/02; H01L 23/522; H01L 21/3065; C23C 16/455

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: self-align, air, pillar, recess, line

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2016-0056104 A1 (GLOBALFOUNDRIES INC.) 25 February 2016 See paragraphs [0045]-[0075] and figures 1-31.	1-13
A	US 2005-0167846 A1 (JUNICHI AOYAMA) 04 August 2005 See paragraphs [0037]-[0051] and figures 1-10.	1-13
A	US 2015-0170956 A1 (APPLIED MATERIALS, INC.) 18 June 2015 See paragraphs [0022]-[0067] and figures 2-8.	1-13
A	US 2010-0203725 A1 (SUK-HUN CHOI et al.) 12 August 2010 See paragraphs [0049]-[0064] and figures 1-7.	1-13
A	JP 2011-060803 A (TOSHIBA CORP.) 24 March 2011 See paragraphs [0010]-[0071] and figures 1-5.	1-13

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 September 2018 (18.09.2018)	**18 September 2018 (18.09.2018)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2018/036690

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