

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
3 February 2005 (03.02.2005)

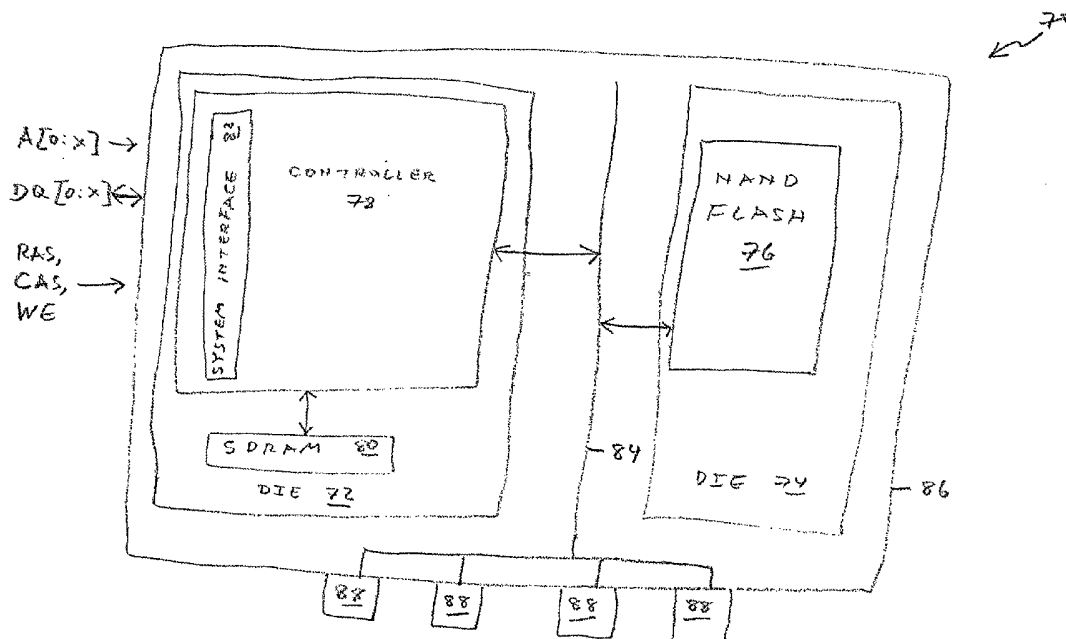
PCT

(10) International Publication Number
WO 2005/010637 A3

- (51) International Patent Classification⁷: **G06F 12/00**
- (21) International Application Number:
PCT/IL2004/000399
- (22) International Filing Date: 12 May 2004 (12.05.2004)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/492,217 31 July 2003 (31.07.2003) US
10/704,613 12 November 2003 (12.11.2003) US
- (71) Applicant (for all designated States except US): **M-SYSTEMS FLASH DISK PIONEERS LTD.** [IL/IL]; Central Park 2000, 7 Atir Yeda St., 44425 Kfar Saba (IL).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **AVRAHAM, Meir** [IL/IL]; Hasira 16, 75438 Rishon Lezion (IL). **INBAR, Dan** [IL/IL]; Derech Hahoreish 5, 56470 Yehud (IL). **PAZ, Ziv** [IL/IL]; Emek Ayalon 149, 73142 Shoham (IL).
- (74) Agent: **FRIEDMAN, Mark M.**; 7 Haomanim St., 7 Haomanim Street, 67897 Tel Aviv (IL).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: SDRAM MEMORY DEVICE WITH AN EMBEDDED NAND FLASH CONTROLLER



(57) Abstract: A memory device (86) includes two dies. A first memory (76) is fabricated on one die (74). A controller (78) of the first memory (76) is fabricated on the other die (72). Also fabricated on the other die (72) is another component, such as a second memory (80), that communicates with a host system using a plurality of signals different from the signals used by the first memory. The device includes a single interface for communicating with the host system using only the respective signals of the second component. In a most preferred embodiment, the first memory (76) is a NAND flash memory and the second memory (80) is a SDRAM.



Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(88) Date of publication of the international search report:

30 June 2005

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IL04/00399

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G06F 12/00

US CL : 711/103

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 711/103,101,104,105

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X, E	US 6,772,955 B2 (YOSHIMOTO et al) 10 August 2004 (10.08.2004), figure 1, col. 4, lines 46 - 49.	1-8,12-17,19-25,29-37,39-41
X, P	US 2003/0160102 A1 (Yoshimoto et al) 28 August 2003 (28.08.2003), figure 1, col. 4, lines 46 - 49.	1-8,12-17,19-25,29-37,39-41
X	US 6,145,069 A (Dye) 7 November 2000 (07.11.2000), figures 4,5.	1,18,21,38
X	US 6,526,462 B1 (Elabd) 25 February 2003 (25.02.2003), figure 2, col. 6, lines 2-4, col. 8, lines 8 - 10.	1, 7-11, 21, 25-28
X, E	US 6,791,877 B2 (Miura et al) 14 September 2004 (14.09.2004), figures 21, 43.	1-8,12-17,19-25,29-37,39-41
X	US 2002/0188337 A1 (Miura et al) 12 December 2002 (12.12.2002), figure 21, 43	1-8,12-17,19-25,29-37,39-41

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

18 January 2005 (18.01.2005)

Date of mailing of the international search report

27 APR 2005

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Facsimile No. (703) 305-3230

Authorized officer

Matt Kim

Telephone No. (703) 305-3900

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IL04/00399

Continuation of B. FIELDS SEARCHED Item 3:

EAST: USPAT, USPGPUB, EPO, JPO, DERWENT, IBM_TDB, Search Terms: NAND, SDRAM, IC, chip, die, semiconductor, memory controller