

12 EUROPEAN PATENT APPLICATION

21 Application number: 83103501.9

51 Int. Cl.<sup>3</sup>: H 01 L 21/38  
 H 01 L 29/08, H 01 L 29/78

22 Date of filing: 11.04.83

30 Priority: 12.04.82 US 367316

43 Date of publication of application:  
 19.10.83 Bulletin 83/42

84 Designated Contracting States:  
 CH DE FR GB LI NL SE

71 Applicant: GENERAL ELECTRIC COMPANY  
 1 River Road  
 Schenectady New York 12305(US)

72 Inventor: Baliga, Bantval Jayant  
 3 Clove Court Clifton Park  
 New York 12065(US)

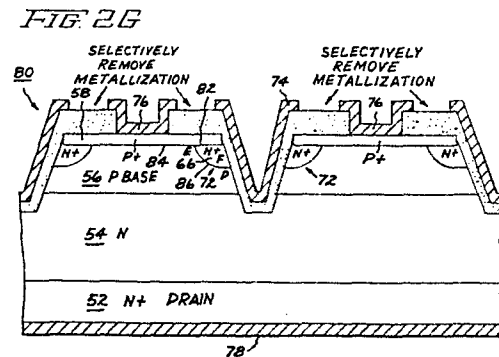
72 Inventor: Gray, Peter Vance  
 121 Acorn Drive  
 Scotia New York 12302(US)

72 Inventor: Love, Robert Paul  
 49 Hillcrest Avenue  
 Schenectady New York 12304(US)

74 Representative: Kinne, Reinhard, Dipl.-Ing. et al,  
 Patentanwaltsbüro  
 Tiedtke-Bühling-Kinne-Gruppe-Pellmann-Grams  
 Bavariaring 4  
 D-8000 München 2(DE)

54 Semiconductor device having a diffused region of reduced length and method of fabricating the same.

57 An improved semiconductor device having a diffused region of reduced length and an improved method of fabricating such a semiconductor device are disclosed. The semiconductor device may be a MOSFET or an IGR, by way of example. In a form of the method for fabricating a MOSFET, an N<sup>+</sup> SOURCE (66) is diffused into a P BASE (56) through a window of a diffusion mask. An anisotropic or directional etchant is applied to the N<sup>+</sup> SOURCE through the same window. The etchant removes most of the N<sup>+</sup> SOURCE, but allows shoulders (72) thereof to remain intact. These shoulders, which form the completed N<sup>+</sup> SOURCE regions, are of reduced length, greatly reducing the risk of turn-on of a parasitic bipolar transistor in the MOSFET. The risk of turn-on of a parasitic bipolar transistor in an IGR is similarly reduced, when the IGR is fabricated by the improved method.



SEMICONDUCTOR DEVICE HAVING A DIFFUSED REGION OF  
REDUCED LENGTH AND METHOD OF FABRICATING THE SAME

Cross-Reference to Related Application

The present application is related to commonly-owned U.S. Patent Application Serial No. 212,181, filed December 2, 1980, by B.J. Baliga, entitled "Gate Enhanced Rectifier".

5 (A gate enhanced rectifier, or "GERECT", is referred to herein as an insulated gate rectifier, or "IGR").

Summary of the Invention

Our invention relates to a semiconductor device having a diffused region of reduced length forming the SOURCE or  
10 corresponding region in a device other than a MOSFET, and to a method of fabricating the same.

Our invention is particularly useful in helping to prevent turn-on, or incipience of current conduction, in a parasitic bipolar transistor inherent in some types of semi-  
15 conductor devices, such as MOSFETs or IGRs. Turn-on of such parasitic transistor is inevitably accompanied by a partial or total loss of control of current in the semiconductor device, and may even result in complete destruction of the device.

20 To help prevent turn-on of an included parasitic bipolar transistor, a typical prior art device, for instance, a MOSFET, incorporates a "electrical short", or low resistance connection, between the adjoining SOURCE and BASE regions, which have a P-N junction between them. The purpose is to  
25 prevent such P-N junction from becoming forward biased above a threshold level that would induce turn-on of the parasitic transistor. To insure that no part of the P-N junction becomes excessively forward biased, the distance between the short

and the furthest part of the P-N junction, which corresponds generally to the length of the SOURCE, should be minimized. The SOURCE, however, has a minimum length typically in excess of about 10 micrometers, as a result of the prior art method of fabricating the MOSFET.

A prior art MOSFET is made by diffusing into its BASE a suitable type dopant, through a diffusion window, to form its SOURCE. Thereafter, an etchant is applied to the SOURCE through an etch window, to etch through <sup>an intermediate portion of</sup> the SOURCE.

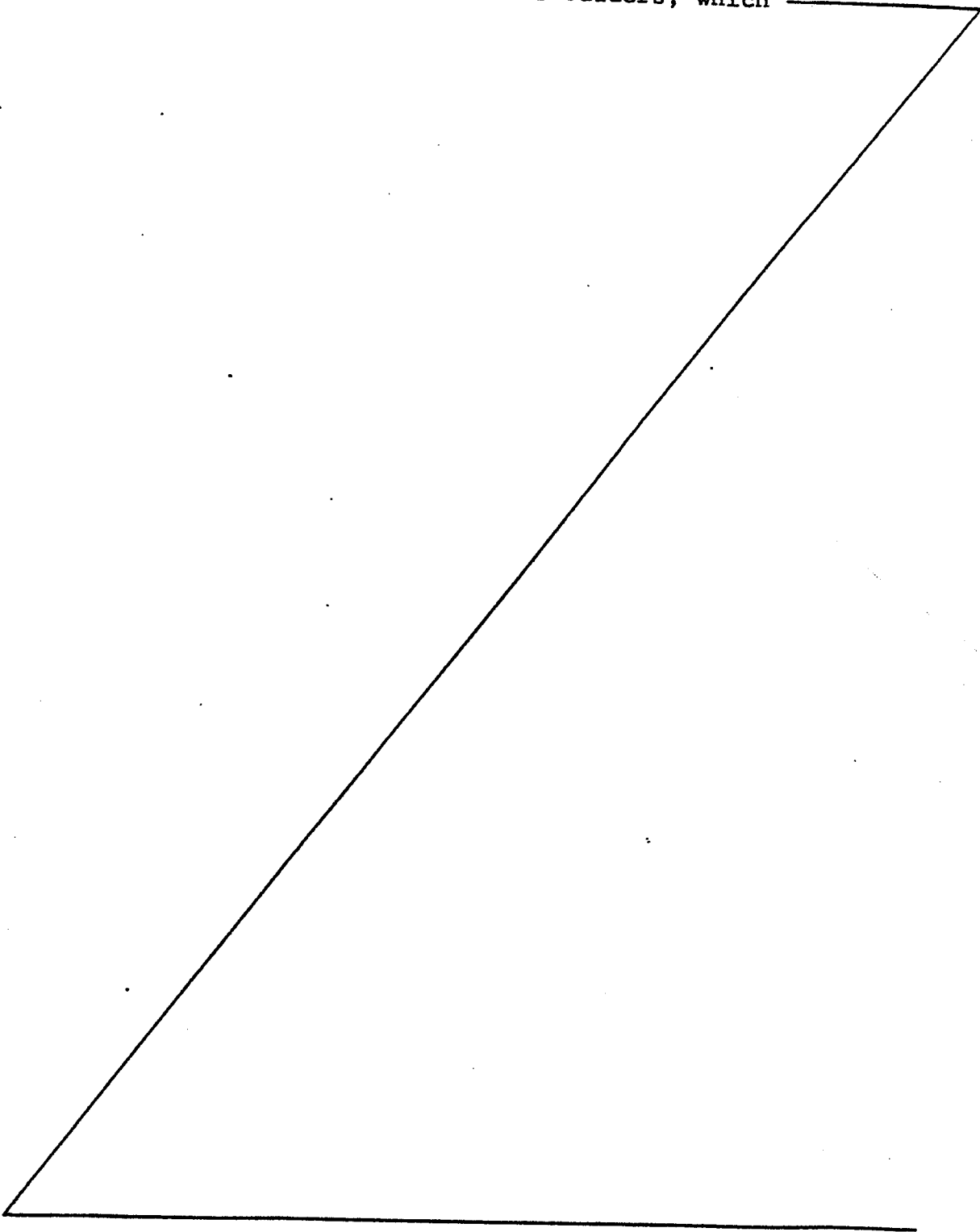
This requires aligning the etch window over the SOURCE, this alignment being a delicate procedure because the SOURCE is so small. Consequently, the SOURCE must be long enough to accommodate an alignment tolerance. It would thus be desirable to provide a semiconductor device having a diffused region (i.e., the SOURCE in a MOSFET) of reduced length.

Accordingly, it is an object of our invention to provide a semiconductor device having a diffused region of reduced length forming the SOURCE or corresponding region in a device other than a MOSFET and, in addition, a method of fabricating the same.

A further object of our invention is to provide a method of fabricating a semiconductor device not requiring a delicate alignment step for forming the SOURCE or corresponding region in a device other than a MOSFET.

Briefly stated, in carrying out one form of our invention as it applies to a MOSFET, we diffuse an N-type dopant into a P BASE, through a diffusion window, to form an N<sup>+</sup> SOURCE. We then apply an anisotropic etchant, or etchant that etches

only in a limited direction, to the  $N^+$  SOURCE through the same diffusion window. This etchant etches away most of the  $N^+$  SOURCE; however, the etchant allows shoulders of the SOURCE to remain intact. These shoulders, which



form the completed  $N^+$  SOURCE regions, are of dramatically reduced length; typically, they are each 1 micrometer long. No delicate alignment step to form the  $N^+$  SOURCE is required.

Brief Description of the Drawings

5 While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which we regard as our invention, it is believed that the invention will be better understood from the following description, taken in connection with the drawings, in which:

0 FIGURE 1A is a schematic view in cross-section of a prior art MOSFET:

FIGURES 1B and 1C are views similar to FIGURE 1A, illustrating selective prior art steps of fabricating the MOSFET of FIGURE 1A;

15 FIGURES 2A-2G are schematic views in cross-section of selected steps of fabricating a MOSFET in accordance with our invention;

20 FIGURE 3 is a view similar to FIGURE 2G, illustrating an alternative semiconductor device in accordance with our invention;

FIGURES 4A-4G are views similar to FIGURES 2A-2G, illustrating a second embodiment of <sup>a method of</sup> fabricating a MOSFET in accordance with our invention; and

25 FIGURE 5 is a view similar to FIGURE 4G, illustrating an alternative semiconductor device in accordance with our invention.

Detailed Description of the Invention

Our invention can be more fully understood by first considering the prior art in connection with FIGURES 1A-1C.

FIGURE 1A illustrates a prior art MOSFET 10 having many identical "cells", or repeated units of structure. For simplicity, explicit reference is made only to the centrally depicted cell of the MOSFET 10.

5           The MOSFET 10 is typically used to control the current level in an external circuit (not shown), which is connected between its SOURCE and drain electrodes 12 and 14. In particular, the "gate" or control electrode 16 normally determines such current level, depending upon the amplitude  
10 of a control voltage impressed on it. Normal operation of the MOSFET 10 is subject, however, to the adverse effect of turn-on of its inherent parasitic N-P-N transistor, formed from N region 18, P BASE 20, and N<sup>+</sup> SOURCE 22. If the parasitic transistor turns-on, the MOSFET 10 begins to lose  
15 control of the external circuit current level. The parasitic transistor can become so conductive that all control of the external circuit current level is lost, and the MOSFET 10 itself can be destroyed.

          The parasitic transistor will turn-on if any portion  
20 of the P-N junction 24 between P BASE 20 and N<sup>+</sup> SOURCE 22 (e.g., between locations A and C) becomes forward biased by more than about 0.7 volts (for a silicon device). To reduce this likelihood, an electrical short between P BASE 20 and N<sup>+</sup> SOURCE 22 is implemented at location B by source electrode  
25 12. As a result, the voltage drop across the P-N junction 24 at location B is held to 0 volts. This condition, however, does not hold for portions of the P-N junction 24 remote from location B. Indeed, the voltage drop between locations A and C can rise above 0.7 volts if sufficient hole current flows between

locations A and B in P BASE 20, resulting in a voltage drop from location A to B. In MOSFET 10, there are two mechanisms which can cause this type of hole current. One is known as "leakage" current, which occurs when the MOSFET 10 is in a "blocking" state, in which it does not conduct external device current; the other occurs when the MOSFET 10 is in the process of changing from its conducting state to its blocking state, and an excess of holes in P BASE 20 are caused to flow to the source electrode near location B.

10           The longer the distance A-B along P-N junction 24, the higher the voltage drop between locations A and B, and the more likely P-N junction 24 will become forward biased above 0.7 volts, with attendant turn-on of the parasitic transistor. Therefore, it would be desirable to reduce the distance A-B, for example, by reducing the length of N<sup>+</sup> SOURCE 22; that is, its horizontal dimension in FIGURE 1A.

The prior art technique of fabricating electrical shorts in the MOSFET 10, such as at location B, however, results in a lengthy N<sup>+</sup> SOURCE 22. This is because the technique includes a delicate alignment step, and the N<sup>+</sup> SOURCE 22 must be long in order to accommodate the unavoidable alignment tolerance. These particulars, as well as further drawbacks of the prior art technique, can be more easily appreciated by referring to FIGURES 1B and 1C.

25           FIGURE 1B shows a semiconductor body 28 including N<sup>+</sup> DRAIN 30, N region 18, and P BASE 20. A diffusion barrier or mask 32, such as silicon dioxide, is provided on the upper surface 33 of the body 28. The diffusion mask 32 defines diffusion window 34 (and adjacent diffusion windows). An

$N^+$  diffusion of dopant through the upper surface 33 is performed and forms the  $N^+$  SOURCE 22 (shown in phantom).

As shown in FIGURE 1C, an etch barrier or mask 38, such as silicon dioxide, is next provided on the upper surface 33. The etch mask 38 defines an etch window 40. An etchant is applied through the etch window 40 to remove semiconductor material from the body 28 to form groove 42 (shown in phantom), necessary for implementing the completed MOSFET 10 (FIG. 1). Proper construction of the  $N^+$  SOURCE 22 requires that the etch window 40 be aligned as closely as is feasible to the center of the  $N^+$  SOURCE 22. However, this alignment step is extremely delicate, since the dimensions involved are exceedingly minute (e.g., on the order of 5 microns).

Because the foregoing alignment step is delicate, precise alignment is not consistently attainable. Consequently, the etch window 40 falls at random within a minimum alignment tolerance 44. In order to accommodate the alignment tolerance 44, the completed  $N^+$  SOURCE 22 must be lengthy. This, however, increases the risk of the parasitic transistor turning on. A further drawback of having the  $N^+$  SOURCE 22 lengthy is that the individual size of each cell in the MOSFET 10 is increased. This undesirably limits the amount of current that the MOSFET 10 can carry, and reduces the manufacturing yield of operable MOSFETs. Additionally, the inclusion of the foregoing delicate alignment step further reduces the manufacturing yield of operable MOSFETs.

The details of our invention will now be described in connection with the embodiment of FIGURES 2A-2G inclusive,

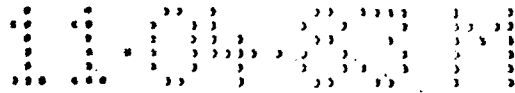
illustrating a preferred method of fabricating a MOSFET.

As shown in FIGURE 2A, we provide a semiconductor body 50, typically of silicon, and which is suitably identical to the prior art body 28 shown in FIGURE 1B. In particular, N<sup>+</sup> DRAIN 52 typically comprises a substrate layer, with N-type layer 54 epitaxially grown on N<sup>+</sup> DRAIN 52, and P BASE 56 epitaxially grown (or diffused into) the N-type layer 54. This construction is typical of "power" MOSFET, or MOSFETs designed to carry substantial levels of current. Our invention, however, can be practised with non-power devices.

FIGURE 2A additionally illustrates a processing step for implementing P<sup>+</sup> region 58 (shown in phantom). We diffuse a very shallow (i.e., a fraction of a micrometer) layer of P-type dopant, such as boron, at a high dopant concentration, into the upper surface 60 of the wafer 50. This step is known in the art as predeposition.

We then provide a thick layer (e.g., 2 micrometers) of silicon dioxide, or other suitable diffusion resistant material, to the body upper surface 60, and pattern it using photolithography (a known technique) to provide a mask 62, as shown in FIGURE 2B, which defines a window 64.

As shown in phantom in FIGURE 2B, we etch away the P<sup>+</sup> region 58 in the window 64 of the centrally depicted cell, or repeated unit of structure in the body 50, and simultaneously etch away the P<sup>+</sup> region 58 in adjacent cells. (For simplicity, the description below is explicit only as to the central cell). This etching need not be anisotropic, or directional. A suitable etching technique, for example, is planar plasma etching.



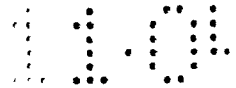
Next, as illustrated in FIGURE 2C, we diffuse an N-type dopant, such as phosphorus, through the window 64 to form  $N^+$  SOURCE 66 (shown in phantom).

During this diffusion step, the shallow  $P^+$  region 58 is "driven",  
5 or thermally diffused deeper, into the body 50 (as is apparent in the FIGURE 2D).

After the  $N^+$  SOURCE 66 is implemented, the mask 62 serves an additional purpose as an etch barrier or mask, as shown in FIGURE 2D. Through the same window 64,  
10 defined by the mask 62, we apply an etchant to etch into the semiconductor body 50. In the preferred embodiment, the etchant is dependent upon the crystal orientation of the silicon body 50, such orientation being (100). An orientation-dependent etchant, a specific type of anisotropic etchant,  
15 etches in different directions in the body 50 at different rates, and, as shown in FIGURE 2D, etches completely through the  $N^+$  SOURCE 66 and produces a V-shaped groove 68 (shown in in phantom), with or without a flat bottom 70. Such etchant does not undercut beneath the mask 62 and hence <sup>does not</sup> completely  
20 etch away the  $N^+$  SOURCE 66. This allows portions of  $N^+$  SOURCE 66 beneath the mask 62, or "shoulders" 72, to remain intact.

As shown in FIGURE 2E, we next provide an insulating layer 73 to cover the surface of the groove 68. A preferred way of implementing the layer 73 is by growing it as an oxide  
25 of the semiconductor body 50. This is accomplished by exposing the body 50 to oxygen at high temperature.

Next, as shown in FIGURE 2F, we selectively remove portions of the insulating layer 62 to provide openings 75. This is accomplished by photolithography.



We then apply metallization/entire upper surface of the structure of FIGURE 2F, and selectively remove portions of such metallization, as shown in FIGURE 2G. The remaining metallization 74 forms a gate electrode, and the remaining metallization 5 76 forms a source electrode in contact with the P<sup>+</sup> region 58. We lastly apply metallization 78 to the lower surface of the N<sup>+</sup> DRAIN 52 to form a drain electrode and implement the MOSFET 80.

In the MOSFET 80, the P<sup>+</sup> region 58 advantageously completes an electrical short between P BASE 56 and N<sup>+</sup> SOURCE 66, e.g., at location E. This electrical short has three components. One 10 component comprises the junction 82 between the P<sup>+</sup> region 58 and the N<sup>+</sup> SOURCE 66, which junction forms a "tunnel" junction, because each of the foregoing regions is heavily doped (i.e., each has a doping concentration in excess of about 10<sup>19</sup> dopant atoms 15 per cc of silicon). The tunnel junction 82 constitutes a low resistance connection between the N<sup>+</sup> SOURCE 66 and the P<sup>+</sup> region 58, at least during normal device operation. Tunnel junctions are discussed more fully, for example, in S.M.Sze, Physics of Semiconductor Devices, New York: Wiley-Interscience, 1969, Chapter 4.

20 The second component of the electrical short <sup>at</sup>/location E comprises the junction 84, between P BASE 56 and P<sup>+</sup> region 58. The junction 84 constitutes a low resistance path between the P BASE 56 and the P<sup>+</sup> region 58, because holes can freely pass from the P BASE 56 to the P<sup>+</sup> region 58. The third component of the 25 electrical short <sup>at</sup>/location E comprises the P<sup>+</sup> region 58, in the vicinity <sup>of</sup>/location E, between the tunnel junction 82 and the junction 84. This is because the region 58 is highly doped, and so constitutes a low resistance path between the junctions

82 and 84. All three of the foregoing low resistance paths collectively provide a low resistance path between the P BASE 56 and the N<sup>+</sup> SOURCE 66, thus implementing the electrical short between these regions at location E.

5           The tunnel junction 82 is also part of a low resistance path between the N<sup>+</sup> SOURCE 66 and the source electrode 76, such low resistance path also including the highly-doped P<sup>+</sup> region 58. Because the P<sup>+</sup> region 58 is highly-doped and thus conductive, the source electrode 76  
10           only needs to make contact with it at isolated locations.

          The MOSFET 80 possesses significant advantages over the prior art MOSFET 10, described above. First and foremost, the length of the N<sup>+</sup> SOURCE 66 is drastically reduced compared to the prior art. This is because all but the shoulders 72 of  
15           the N<sup>+</sup> SOURCE 66 have been etched away. Accordingly, the electrical short at location E is highly effective. This is because hole current flowing in P BASE 56, from location D to location E, produces only a low voltage drop because the distance D-E is short. Accordingly, it is unlikely that any  
20           portion of P-N junction 86 between P BASE 56 and N<sup>+</sup> SOURCE 66 (e.g., between locations D and F) can become excessively forward biased. This greatly reduces the likelihood of turn-on of the parasitic bipolar transistor in the MOSFET 80 (i.e., the transistor formed by N-region 54, P BASE 56, and N<sup>+</sup> SOURCE 66).

25           Significantly, MOSFETs made by our invention allow reduced cell size using present state of the art processing techniques. For a typical MOSFET, this size reduction amounts to about 50 percent. This dramatically increases the

manufacturing yield of operable MOSFETs, which makes them less costly. Additionally, the size reduction/<sup>increases the</sup>current-carrying capability of a 500 volt-rated MOSFET by about 30 percent, and of a 50 volt-rated MOSFET by about 100 percent. Accordingly, smaller and less costly MOSFETs made in accordance with our invention are needed in a given application, compared with MOSFETs made by the conventional methods.

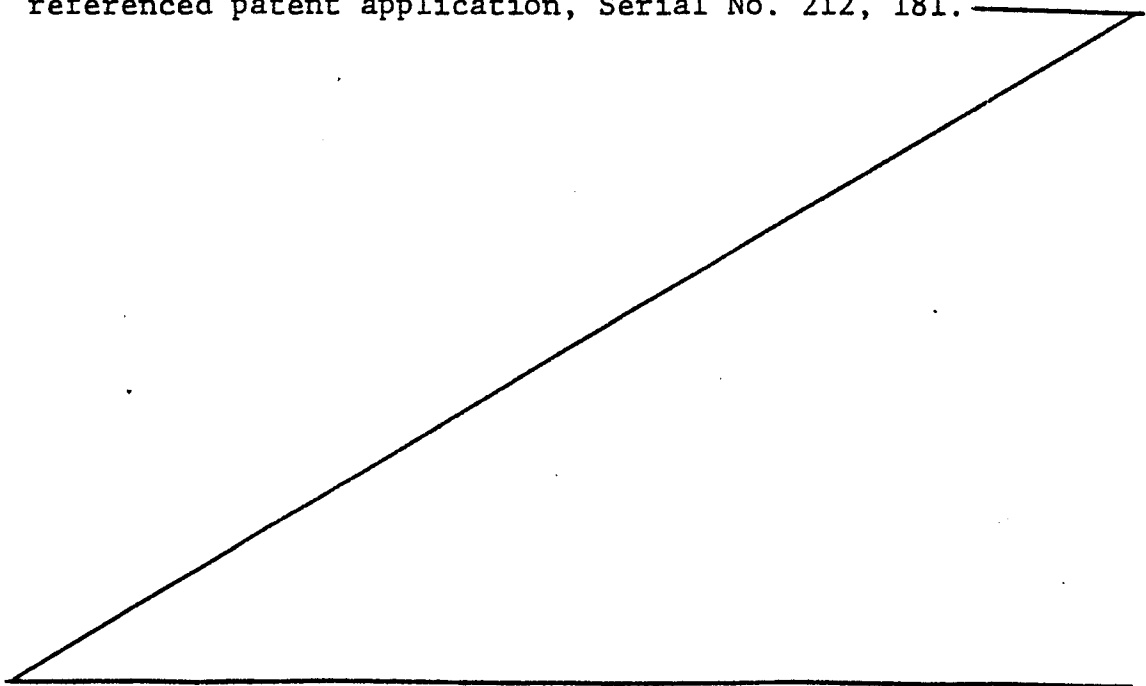
Our foregoing method of fabricating the MOSFET 80 could be modified, for example, by employing an anisotropic etchant other than the preferred orientation-dependent etchant mentioned above. However, <sup>such</sup>other suitable etchants must allow shoulders 72 of the N<sup>+</sup> SOURCE 66 to remain intact. By way of example, <sup>these</sup>other suitable etchants include a vertically collimated beam of reactive ions and a planar plasma etchant. These etchants tend to form a groove 68 (FIGURE 2D) having more of a U-shape than a V-shape. These etchants do not require the semiconductor body/<sup>to be</sup>(100) crystal oriented, as does the preferred, orientation-dependent etchant.

A further modification of our foregoing method of fabricating the MOSFET 80 (FIGURE 2G) is to form the gate electrode 74 from a conductive refractory material, rather than <sup>by</sup>metallization. Suitable refractory materials include highly-doped polysilicon, molybdenum silicide and tungsten silicide. If polysilicon were used, our foregoing method could be altered as follows, by way of example. After the insulating layer 62 of FIGURE 2E has been formed, polysilicon (not illustrated) is deposited on the upper surface of the structure shown in FIGURE 2E. The polysilicon layer is highly

doped to make it conductive, and is patterned to remove it from the desired locations for the source electrode. A layer of oxide is grown on the polysilicon by exposing it to oxygen at high temperature, openings similar to openings 5 75 (FIGURE 2F) are made, and, finally, metallization is applied to the upper surface of the modified structure to implement the source electrode.

Our invention is applicable to semiconductor devices other than MOSFETs. Another appropriate semiconductor 10 device is an insulated gate rectifier (IGR), shown in FIGURE 3. The IGR 90 includes a  $P^+$  substrate 92, in contrast with the  $N^+$  DRAIN substrate 52 of the MOSFET 80. With this substitution, the foregoing method of fabricating the present embodiment of our invention is applicable 20 to IGR 90.

Details of the structure and operation of an IGR device, such as the IGR 90, are described in the above-referenced patent application, Serial No. 212, 181.



Our invention attains advantages for the IGR 90, which are similar to the above-mentioned advantages for the MOSFET 80. In particular, the parasitic N-P-N transistor in the IGR 90, formed by N region 94, P region 96, and  $N^+$  region 97, is electrically coupled in thyristor fashion to a parasitic P-N-P transistor -- namely, the transistor formed by  $P^+$  region 92, N region 94, and P region 96. Accordingly, these parasitic transistors can "latch", or become established in a current-conducting state, if the N-P-N (or upper transistor) is allowed to turn on. Once the IGR 90 becomes latched, control of its current level by its gate 98 is totally lost. This risk of the IGR 90 becoming latched is always present when the IGR 90 is in its active or current-carrying state. Our invention greatly diminishes this risk by preventing the N-P-N transistor from becoming excessively active. This is because the distance  $H-I$  in P region 96 along P-N junction 100 is so short that P-N junction 100 (e.g., between locations  $H$  and  $J$ ) cannot become excessively forward biased. Additionally, the IGR 90 can have a reduced cell size, compared to IGRs made from prior art methods, enabling the IGR 90 to be made more economically and carry more current.

The modifications to our method of fabricating the MOSFET 80, described above, apply equally well to the IGR 90.

Our invention will now be described in connection with the embodiment of FIGURES 4A-4E, illustrating a preferred method of fabricating a MOSFET. As shown in FIGURE 4A, we provide a semiconductor body 200, typically of silicon. The body 200 typically comprises a substrate 202, constituting an  $N^+$  DRAIN, and an N region 204, typically epitaxially grown on the  $N^+$  DRAIN 202.

This construction is typical of power MOSFETs, although our invention can be practised with non-power devices.

On the upper surface 205 of the body 200, we form an insulating layer 206, suitably by growing an oxide on the body 200. Next, we form a conductive refractory material 208 (shown partially broken away) on the insulating layer 206. Where, for example, the refractory material comprises polysilicon we dope it highly to make it conductive. We then preferably form insulating layer 210 on the upper surface of the refractory material 208. With the refractory material 208 comprising polysilicon, the insulating layer 210 suitably comprises an oxide grown thereon. Finally, we form a layer 211 on the insulating layer 210, if provided, or directly on the refractory material 208. The layer 211 comprises a material, such as aluminum oxide, which is resistant to an etchant, that etches through silicon dioxide and silicon during a processing step described below.

We then pattern the layers 206, 208, 210 and 211 by conventional photolithography to produce mask 216, appearing in FIGURE 4B. The mask 216 defines a window 217 and serves as a diffusion barrier when we next make a P-type diffusion through the window 217 to form P BASE 218 (shown in phantom).

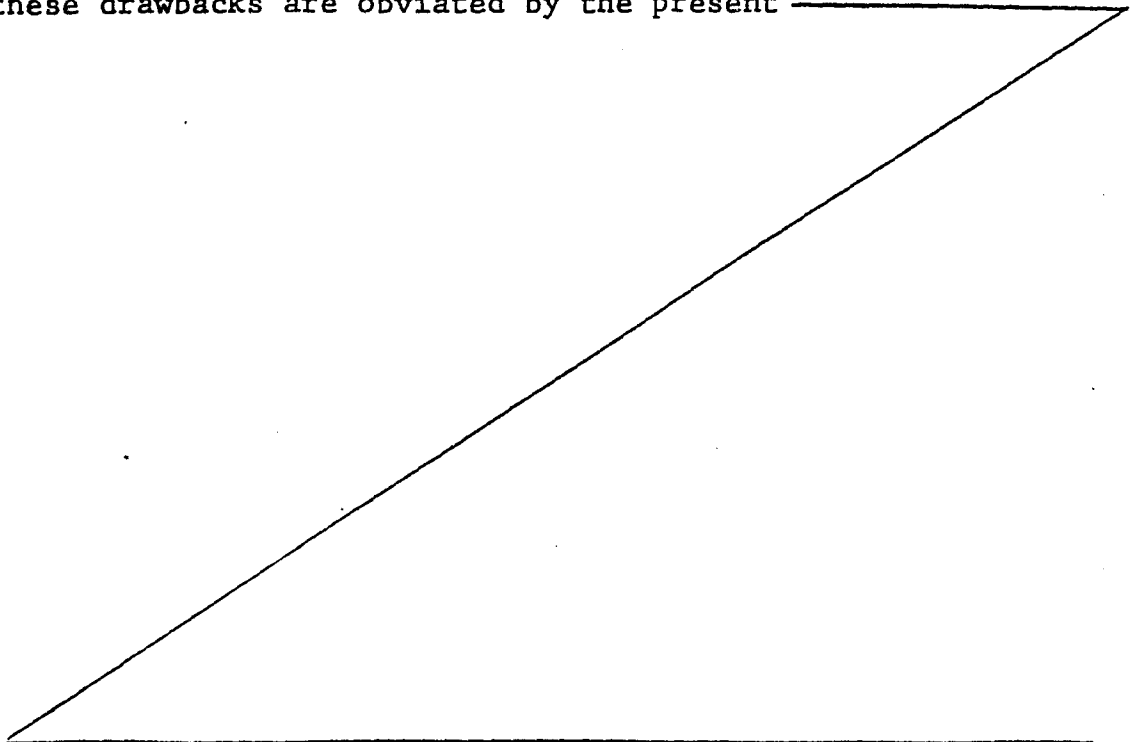
As shown in FIGURE 4C, we make an  $N^+$  diffusion through the window 217 to form  $N^+$  SOURCE 220 (shown in phantom). The  $N^+$  diffusion extends laterally beneath the refractory material 208, i.e., in region 222, approximately the same distance as it diffuses vertically downward. This diffusion occurs at high temperature in an oxidizing atmosphere. As a

result, the exposed surfaces 219 (shown in FIGURE 4B) of the refractory material 208 become oxidized so that the refractory material 208 becomes surrounded by insulating material, as shown in FIGURE 4C. Similarly, the exposed portions of the semiconductor body surface 205 (shown in FIGURE 4B) becomes oxidized to form oxide layer 221, (shown in FIGURE 4C).

As illustrated in FIGURE 4D, we next apply an anisotropic etchant (described below) to the oxide layer 221, through the same window 217 which served as the diffusion window for the  $N^+$  SOURCE 220. This etchant etches through the oxide layer 221 and at least substantially all the way through  $N^+$  SOURCE 220, but allows shoulders 223 of the  $N^+$  SOURCE 220 to remain intact. In the preferred embodiment, this etchant suitably comprises a vertically collimated beam of reactive ions or a planar plasma etchant, and forms a generally U-shaped groove 224. Alternatively, a V-shaped groove (not illustrated) could be formed by first using one of the preceding etchants to remove the oxide layer 221, and then using an orientation-dependent etchant (such as a mixture of potassium hydroxide and isopropanol, in the approximate ratio of 3 to 1) to etch into the semiconductor body 200. In this case, the body 200 would need to have a (100) crystal orientation, and an insulating layer 210 (FIGURE 4A) is necessary, because the layer 211 (at least where it comprises aluminum oxide) is removed by the orientation-dependent etchant (at least where it comprises potassium hydroxide).

We then form the MOSFET 228 as shown in FIGURE 4E by applying metallization 226 and 227 to the upper and lower surfaces, respectively, of the structure of FIGURE 4D. An electrical short in the MOSFET 228 exists at location A,  
5 where the metallization 226 electrically connects the P BASE 218 to the N<sup>+</sup> SOURCE 220.

Prior art for the MOSFET 228 (as described in detail in a discussion by B.J. Baliga, "Silicon Power Field Controlled Devices and Integrated Circuits", in Silicon  
10 Integrated Circuits: Part B, edited by D. Kahng, New York: Academic Press (1981), pages 209-228) has basically the same drawbacks of the prior art MOSFET 10, shown in FIGURE 1A and described above. These drawbacks include having a lengthy SOURCE, requiring a delicate alignment step for  
15 implementing electrical shorts, and including more processing steps to implement electrical shorts. All of these drawbacks are obviated by the present



embodiment of our invention.

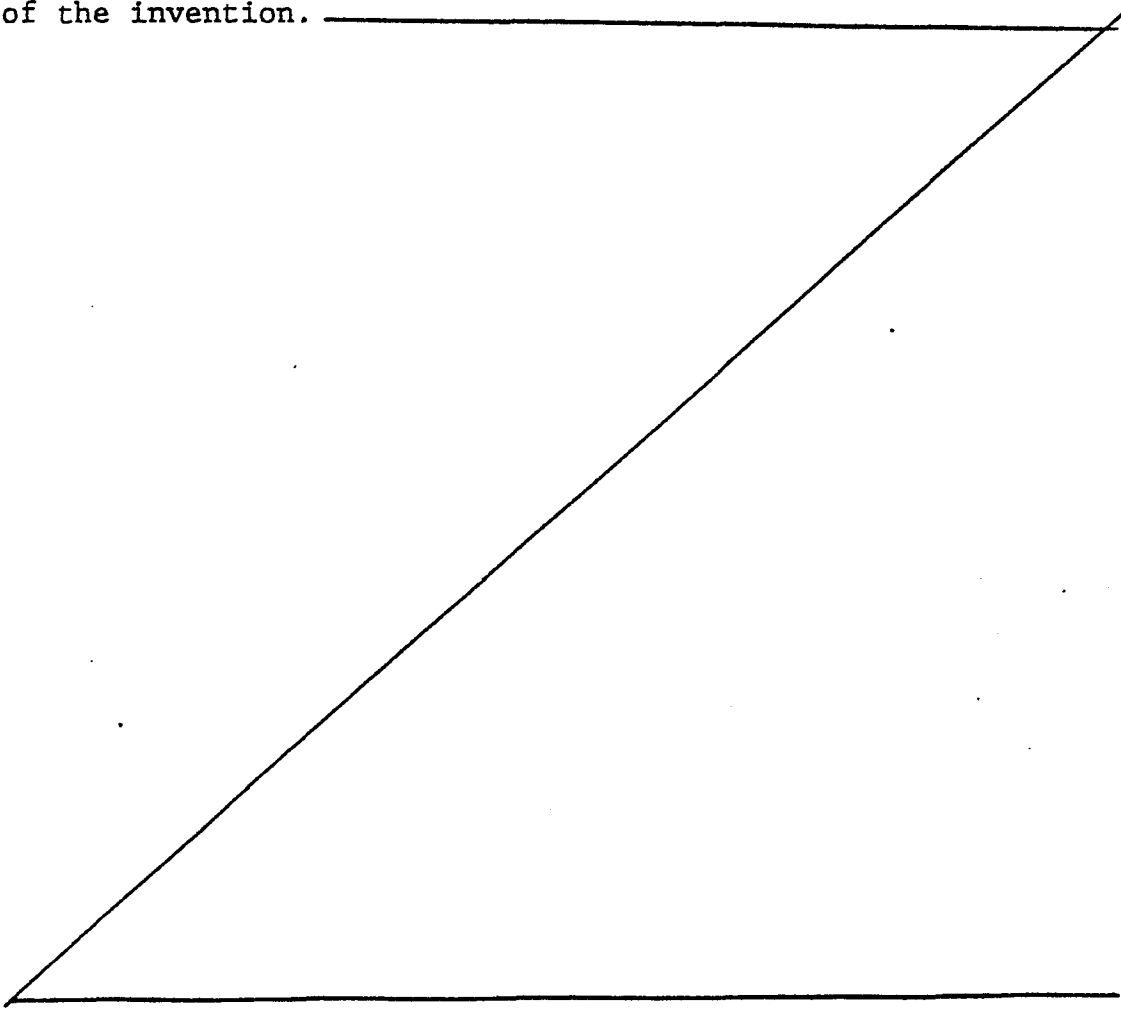
In a preferred modification of the present embodiment, we form more reliable electrical shorts by using tunnel junctions. To implement this modification, we carry out a  $P^+$  diffusion to form  $P^+$  region 230, as shown in phantom in FIGURE 4F, upon completing the etching step shown in FIGURE 4D. Both the  $P^+$  region 230 and the  $N^+$  SOURCE 220 are highly doped so that the junction 231 between them comprises a tunnel junction. An electrical short between P BASE 218 and  $N^+$  SOURCE 220 exists at location G, adjacent tunnel junction 231 (in similar fashion as with the electrical short at location E in the MOSFET 80 of FIGURE 2G). We next, implement the modified MOSFET 238<sup>as</sup> shown in FIGURE 4G by applying metallization 234 and 236 to the upper and lower surfaces, respectively, of the structure of FIGURE 4F.

The present embodiment of our invention applies to semiconductor devices other than MOSFETs. Another appropriate semiconductor device is an insulated gate rectifier (IGR) 240, as shown in FIGURE 5. The IGR 240 is similar to the MOSFET 238 (FIGURE 4G), except that the IGR 240 includes a  $P^+$  substrate 242, in contrast with the  $N^+$  DRAIN substrate 202 of the MOSFET 238. With this substitution, the foregoing/<sup>method of</sup> fabricating of the present embodiment of our invention is applicable to the IGR 240.

While the invention has been described with respect to specific embodiments, many modifications and substitutions

will be apparent to those skilled in the art. For example, complementary semiconductor devices could be made, in which P-type material is used rather than N-type material, and vice-versa. Further, a "MOSFET" is intended to describe  
5 any form of insulated gate field-effect transistor.

Additionally, the diffusion steps described herein could include the step of ion implanting -- a technique of injecting dopant atoms into a semiconductor body -- before the dopant atoms are diffused deeper into the semiconductor body. It is,  
10 therefore, to be understood that the appended claims are intended to cover these and all such modifications and substitutions as fall within the true spirit and scope of the invention.



Patent Claims

1. In a method of fabricating a semiconductor device, of the type wherein a mask (62; 216), defining a window (64; 217), is applied to a major surface (60; 205) of a semiconductor body (50; 200), and a first region (66; 220) of one dopant type (N+) is formed in a second region (56; 218) of opposite dopant type (P) in said body (50; 200) by diffusing a dopant of said one type into said body (50; 200) through said window (64; 217), with said mask (62; 216) serving as a diffusion barrier, the improvement comprising:

etching into said body (50; 200) through said window (64; 217) with said mask (62; 216) serving as an etch barrier; said etching penetrating at least substantially all the way through said first region (66; 220) but allowing shoulders (72) of said first region (66; 220) to remain intact.

2. The invention according to claim 1 wherein the step of etching into said body (50; 200) comprises etching with an anisotropic etchant.

3. The invention according to claim 2 wherein said anisotropic etchant comprises an etchant which etches in a direction dependent on the crystal orientation of said semiconductor body (50; 200).

4. The invention according to claim 1 further comprising electrically connecting said first (66; 220) and second regions (56; 218) to form electrical shorts (58; 230, 234) therebetween.

5 5. The invention according to claim 1 wherein the step of electrically connecting said first and second regions comprises diffusing a third region (230) of opposite dopant type (P) into said semiconductor body (200), said third region (230) adjoining said second region (218) and forming a tunnel junction with said first region (220).

10 6. The invention according to claim 1 wherein said semiconductor body (50; 200 ) comprises a substrate (52; 92; 202; 242) with an epitaxial layer (54, 56; 94, 96; 204; 244) thereon.

15 7. The invention according to claim 6 wherein said substrate (52; 202) comprises a DRAIN of a MOSFET of said one dopant type.

20 8. The invention according to claim 6 wherein said substrate comprises a region (92; 242) of an insulated gate rectifier of said opposite dopant type.

25 9. The invention according to claim 1 wherein said mask (216) comprises conductive refractory material (208) and an oxide (206) of said semiconductor body (200), said oxide (206) insulating said refractory material (208) from said body (200).

10. The invention according to claim 1 wherein said one dopant type comprises N-type.

30 11. The invention according to claim 10 wherein said semiconductor body (50; 200) comprises silicon.

35 12. In a semiconductor device having first (66;97;220) second (56;96;218), third (54; 94; 204; 244) and fourth (52; 92; 202; 242) successively adjoining regions, with said first, second and third regions being of alternate conductivity type; a first electrode (76; 234) electrically connected to

1 1 4 4 4 4

said first region (66; 97; 220); a second electrode (78; 236) electrically connected to said fourth region (52; 92; 202; 242) and a third electrode overlying but insulated from said second region (56; 96; 218) the improvement wherein said first region (66; 97; 220) comprises a diffused region having a length approximately equal to its diffusion depth.

13. The invention according to claim 12 wherein said first region (66; 97; 220) is electrically connected to said second region (56, 96; 218) in such a way as to form an electrical short therebetween.

14. The invention according to claim 13 further comprising a fifth region (203) conductivity type (P) opposite to that of said first region (220); said fifth region (230) adjoining said second region (218) and forming a tunnel junction with said first region (220), thereby implementing an electrical short between said first and second regions.

15. The invention according to claim 12 wherein said fourth region (52; 92; 202; 242) comprises a substrate and said third region (54; 94; 204; 244) comprises an epitaxial layer on said substrate.

16. The invention according to claim 15 wherein said substrate (52; 202) comprises a DRAIN of a MOSFET of same conductivity type (N+) as that of said first region (66; 220).

17. The invention according to claim 15 wherein said substrate (92; 242) comprises a region of an insulated gate rectifier of conductivity type opposite (P+) to that of said first region (97).

18. The invention according to claim 12 wherein said first region (66; 97; 220) is of N-type conductivity.

19. The invention according to claim 18 wherein said first, second, third and fourth regions each comprises silicon.

FIG. 1A  
(PRIOR ART)

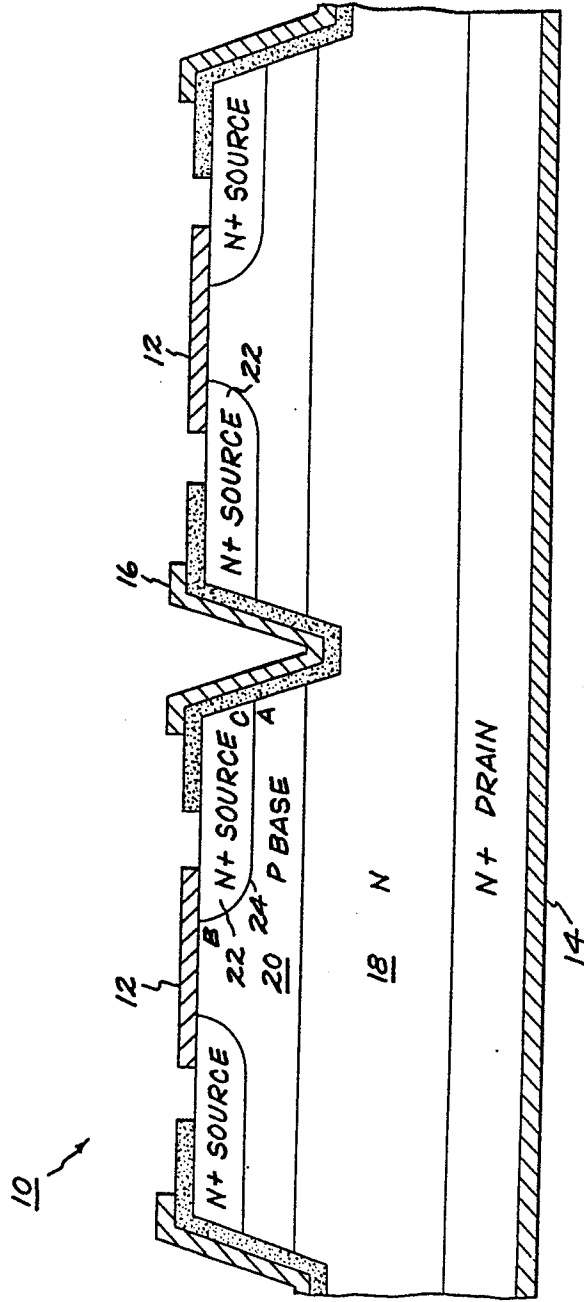


FIG. 1B  
(PRIOR ART)

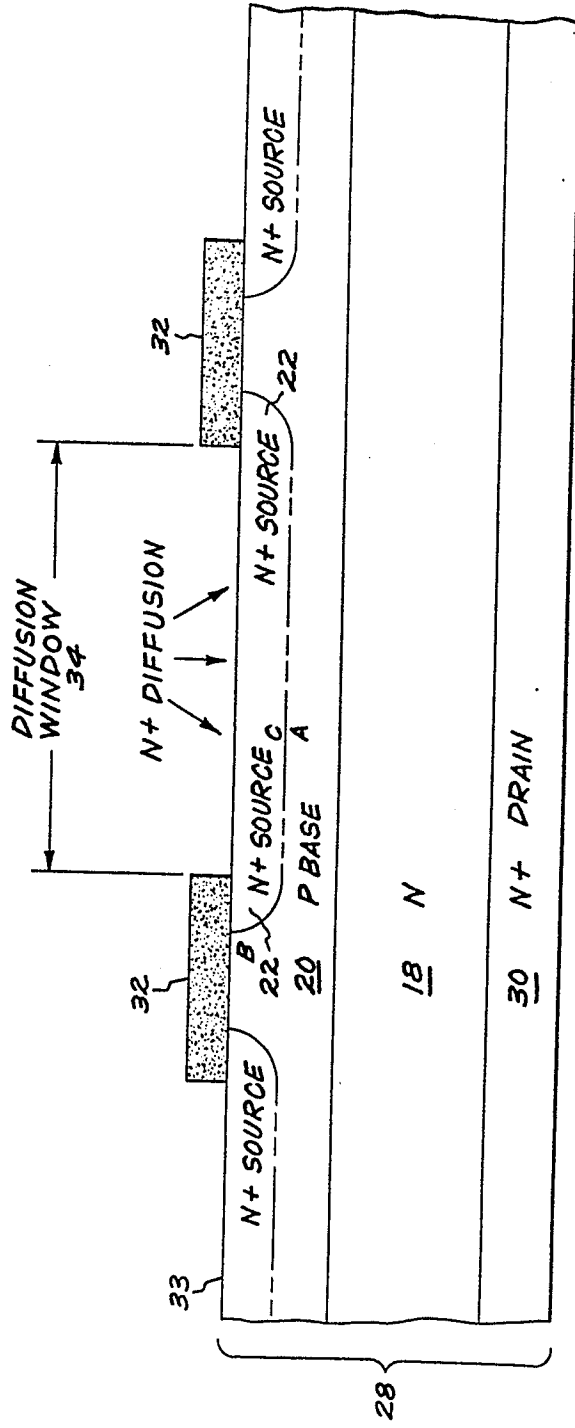


FIG. 1C  
(PRIOR ART)

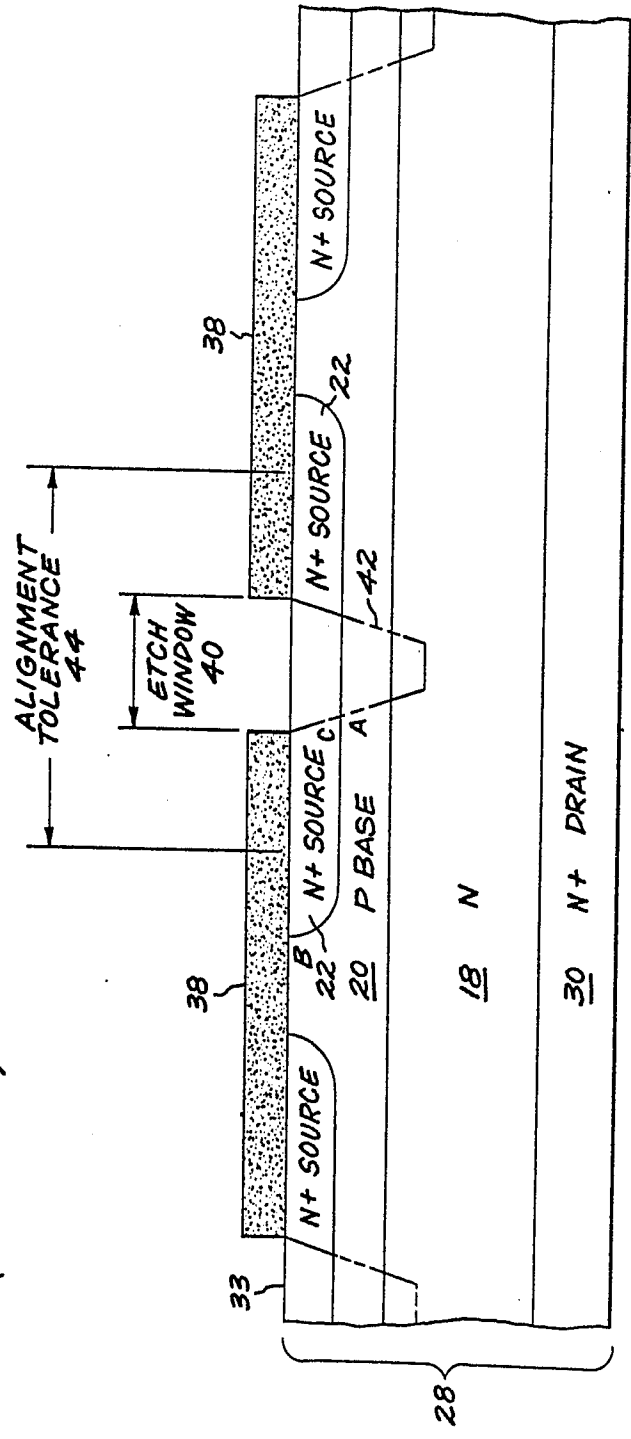


FIG. 2A

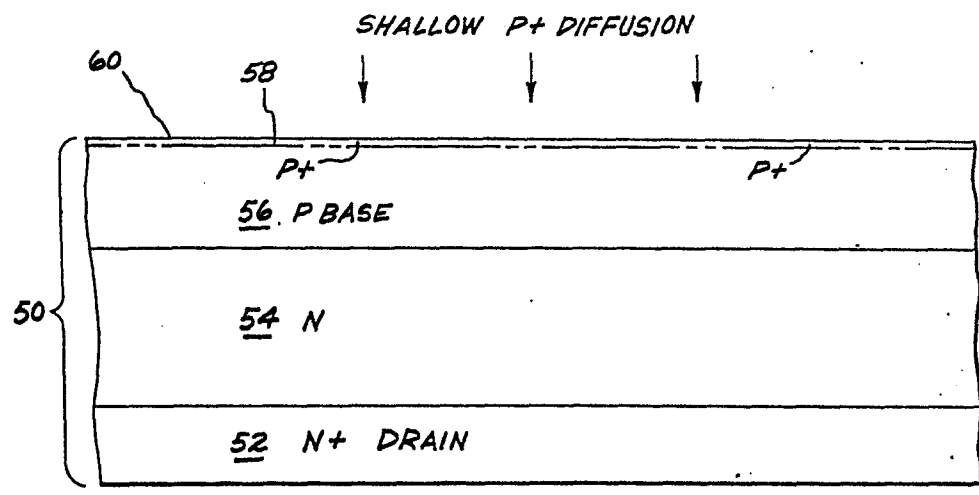


FIG. 2B

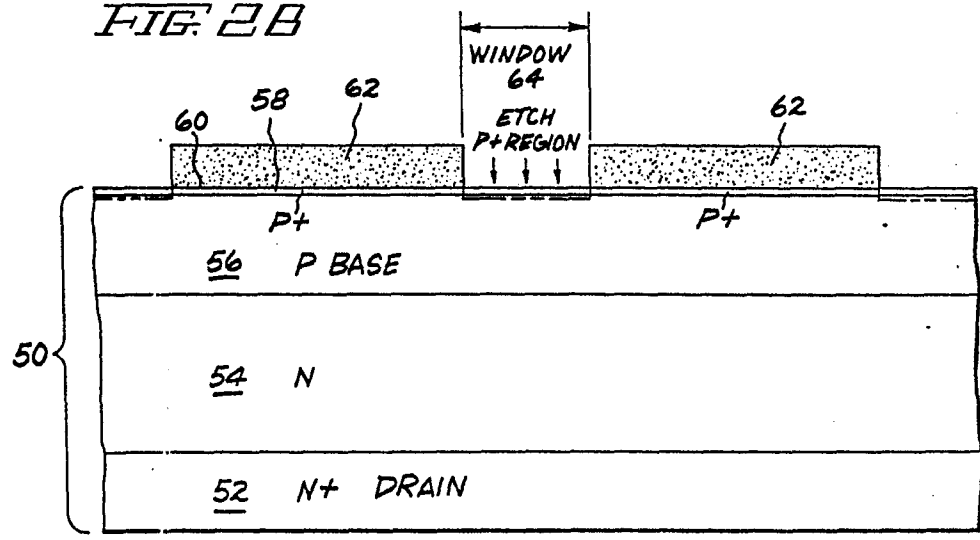


FIG. 2C

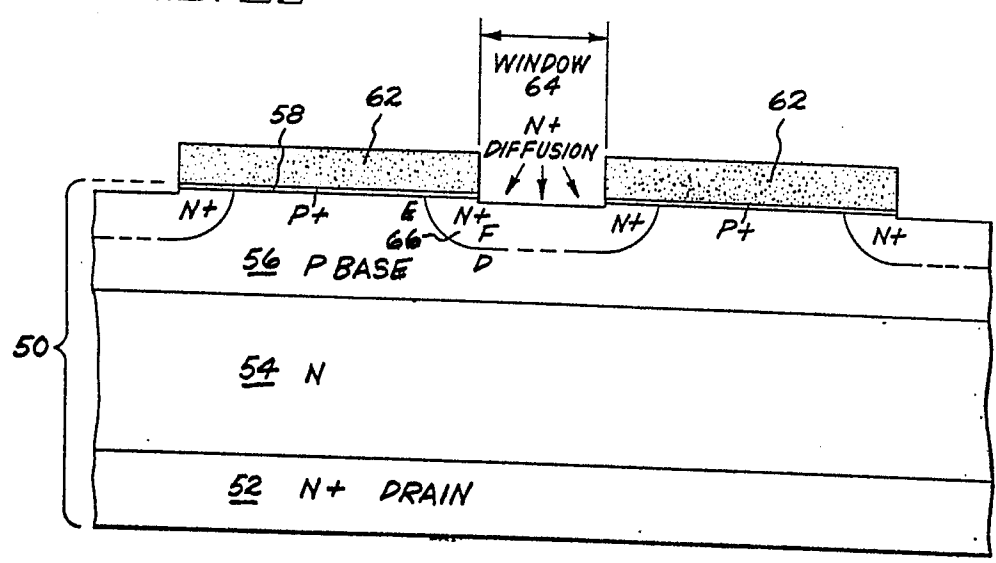


FIG. 2D

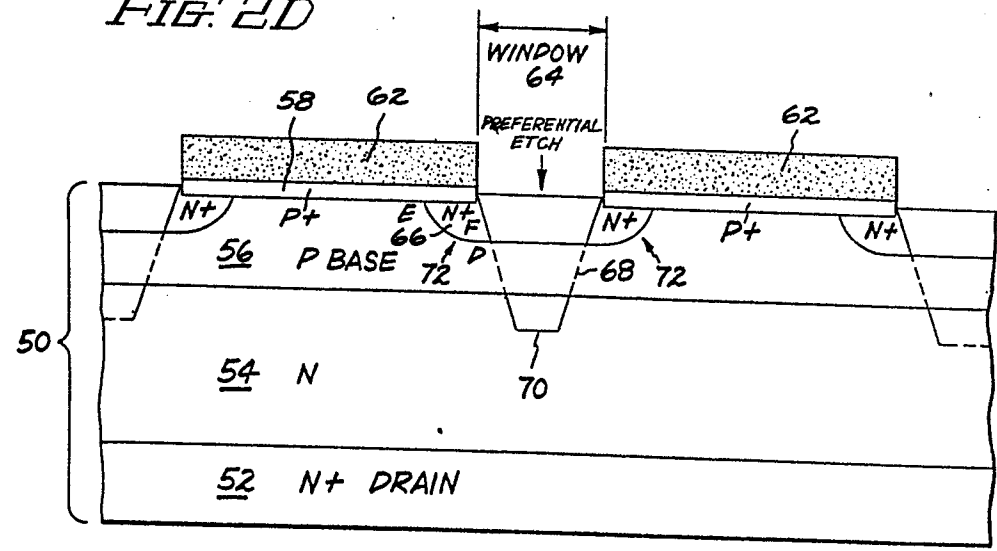


FIG. 2E

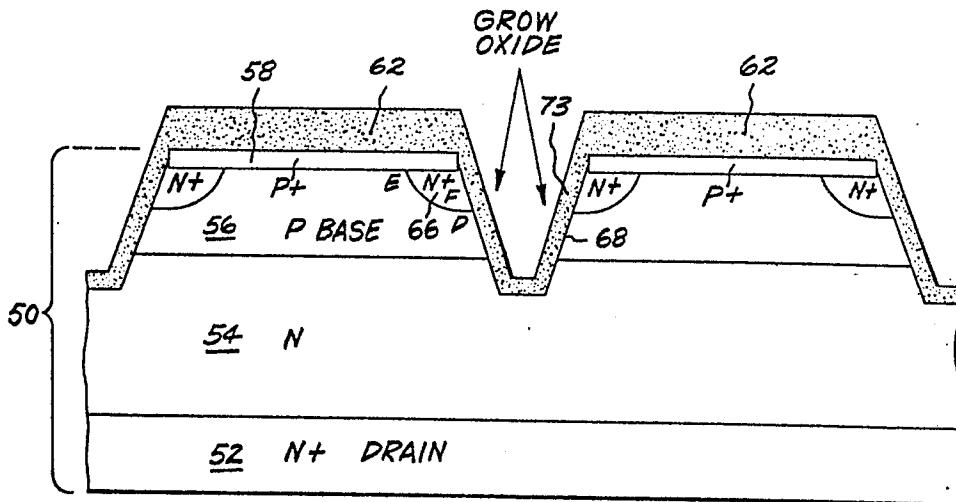


FIG. 2F

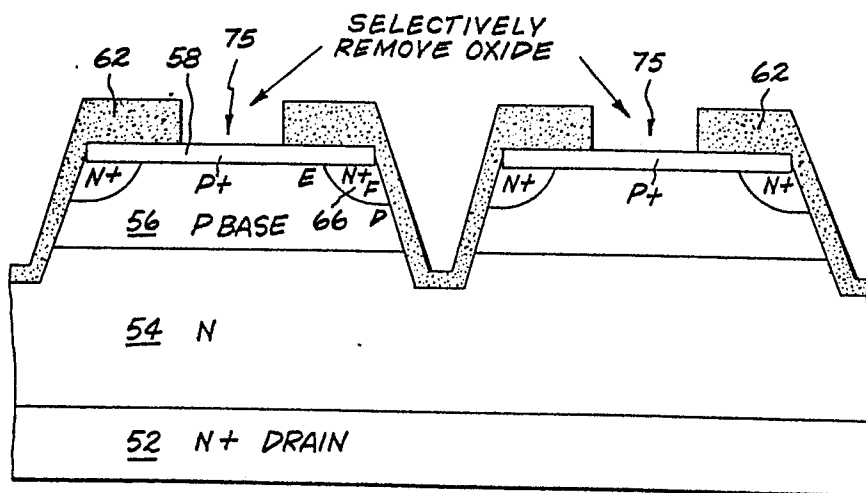


FIG. 2G

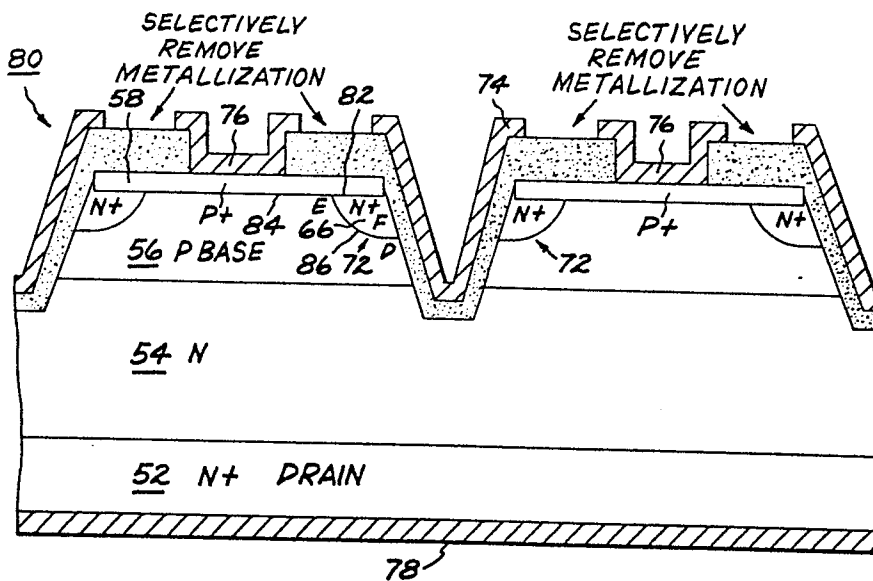


FIG. 3

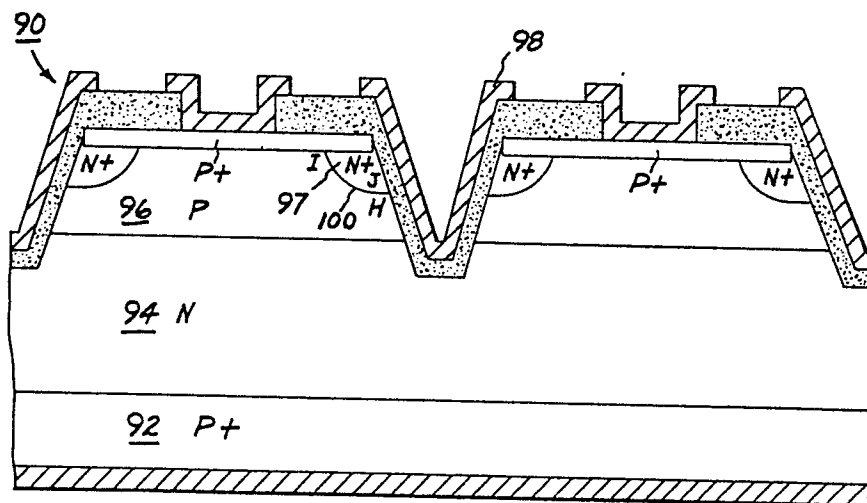


FIG. 4A

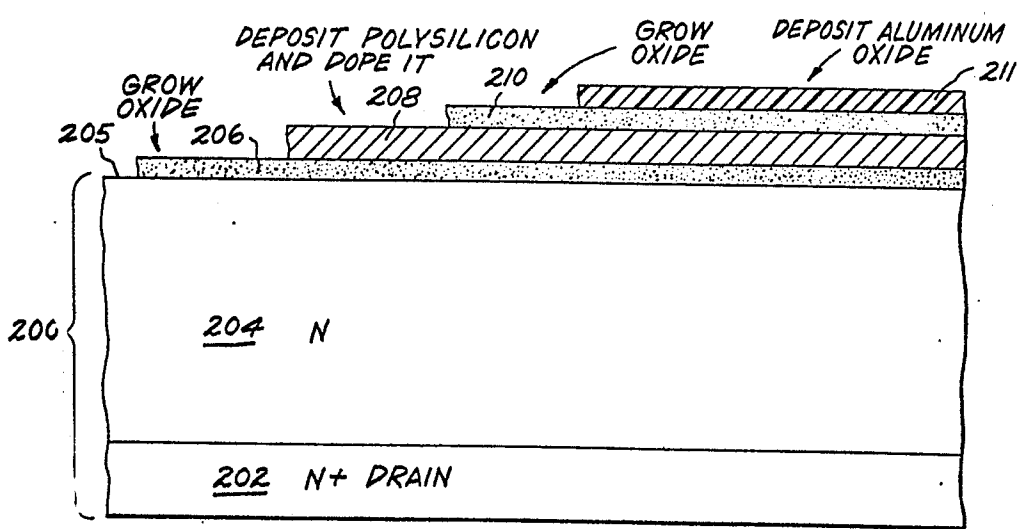


FIG. 4B

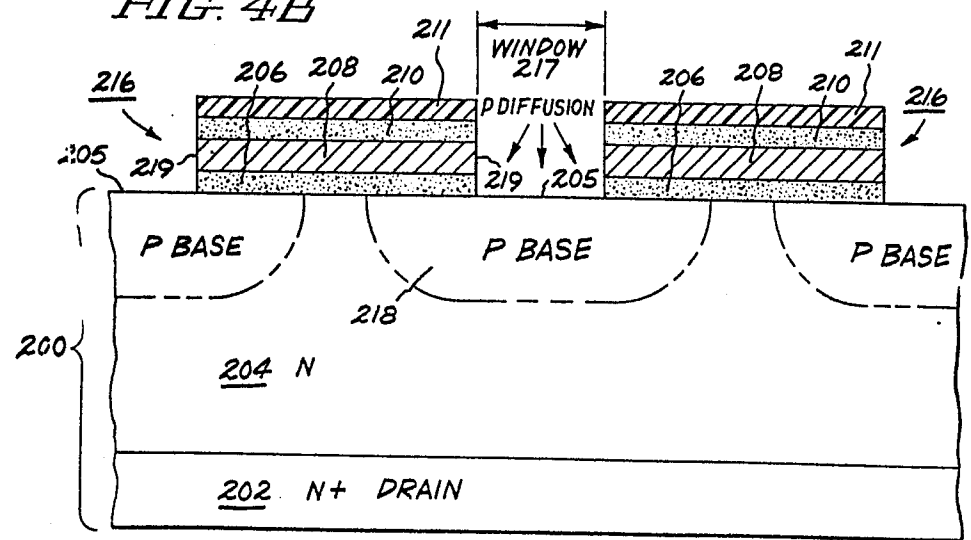


FIG. 4C

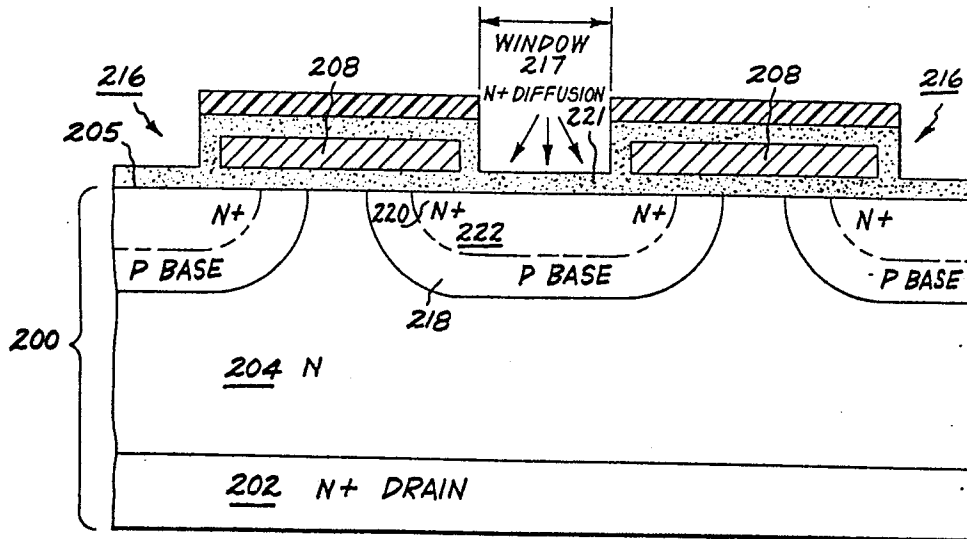


FIG. 4D

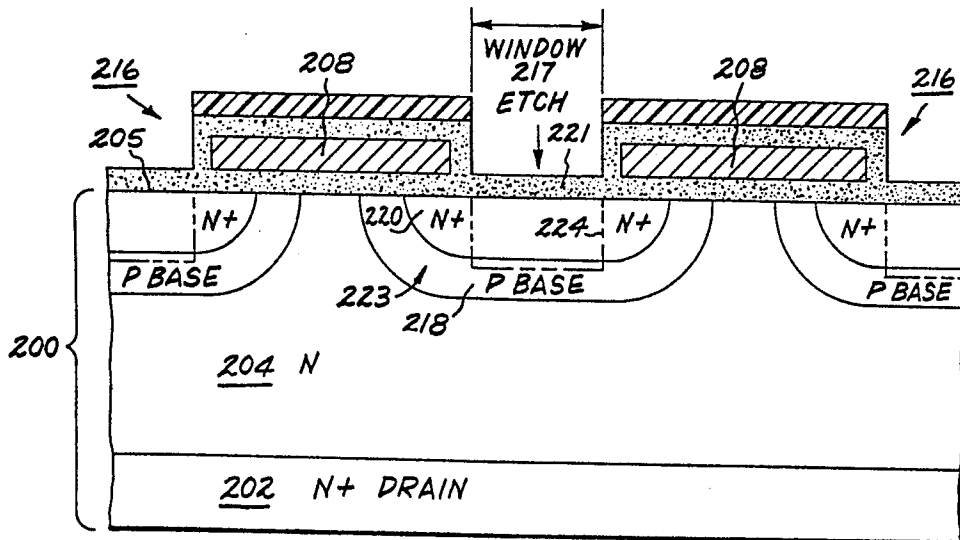


FIG. 4E

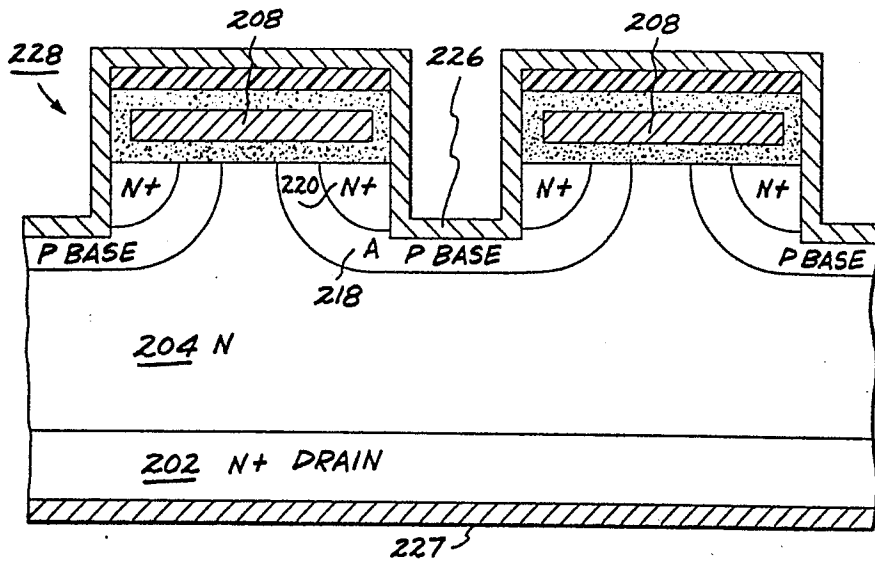


FIG. 4F

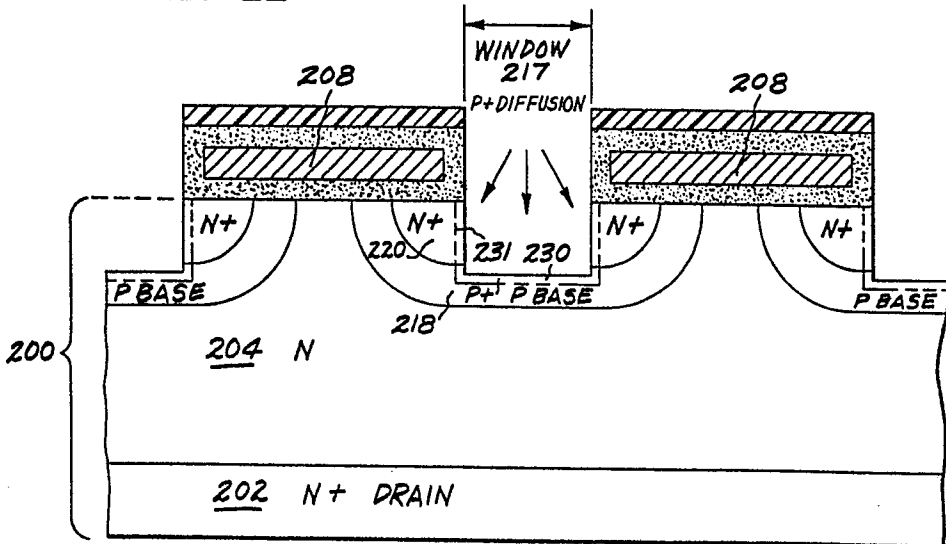


FIG. 4G

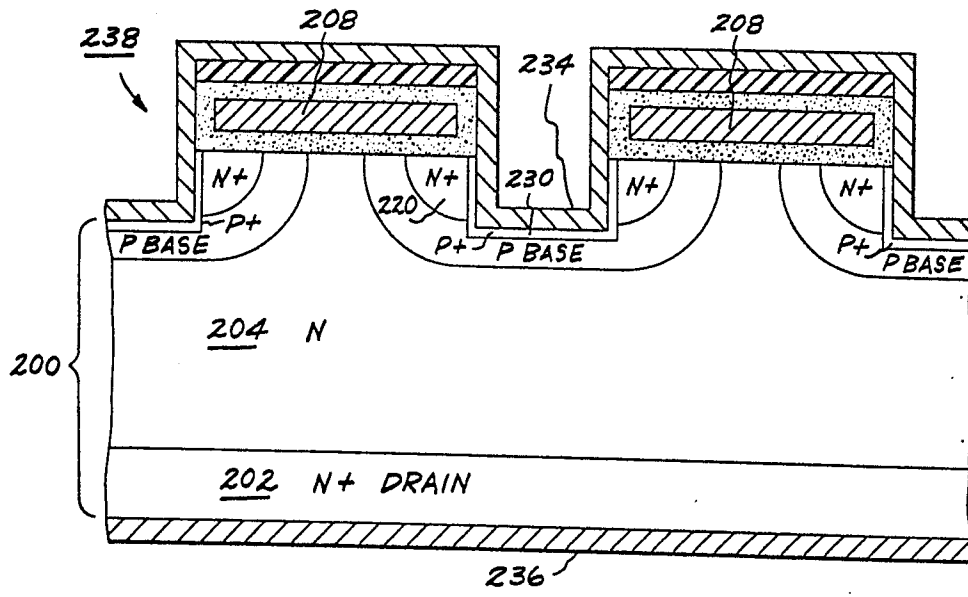


FIG. 5

