# United States Patent [19]

**Dargent**

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[45] **Sept. 25, 1973**


[54] **INTEGRATED CIRCUIT SOLID STATE WATCH**


[75] Inventor: **Bruno M. Dargent,** Lancaster, Pa.

[73] Assignee: **Hamilton Watch Company,** Lancaster, Pa.



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[21] Appl. No.: **143,492**

**Related U.S. Application Data**

[63] Continuation-in-part of Ser. No. 138,547, April 29, 1971, Pat. No. 3,714,867.

[52] **U.S. Cl.** ..... **58/50 R,** 58/4 A, 58/38, 58/57.5, 58/85.5

[51] **Int. Cl.** .... **G04b 19/30,** G04b 19/24, G04c 9/00

[58] **Field of Search** ..... 58/4 A, 23 R, 23 A, 58/50 R, 38, 85.5; 235/92 T; 350/160 R



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| 3,613,351 | 10/1971 | Walton | 58/23 BA |
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[57] **ABSTRACT**

Disclosed is a solid state electronic wristwatch with no moving parts. A crystal oscillator supplies a timing signal through a binary divider and display actuator to an electro-optical display in the form of a digital array of light-emitting diodes. The same display is used for both minutes and seconds and all displays are driven from the same decoder. The vast majority of the electrical components of the watch are incorporated in one or more large-scale integrated circuits.


**18 Claims, 9 Drawing Figures**

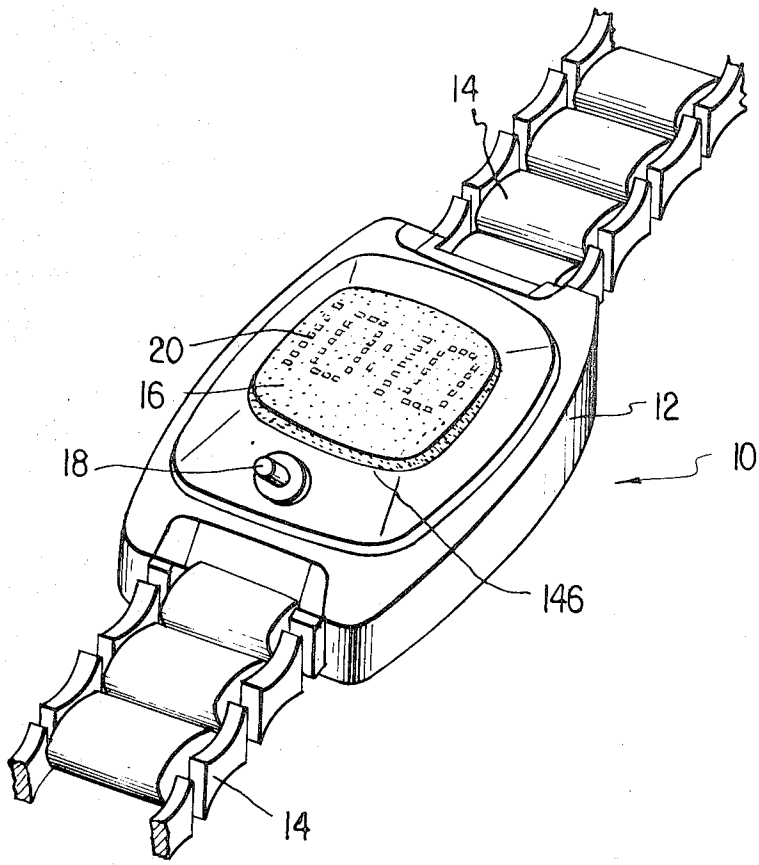
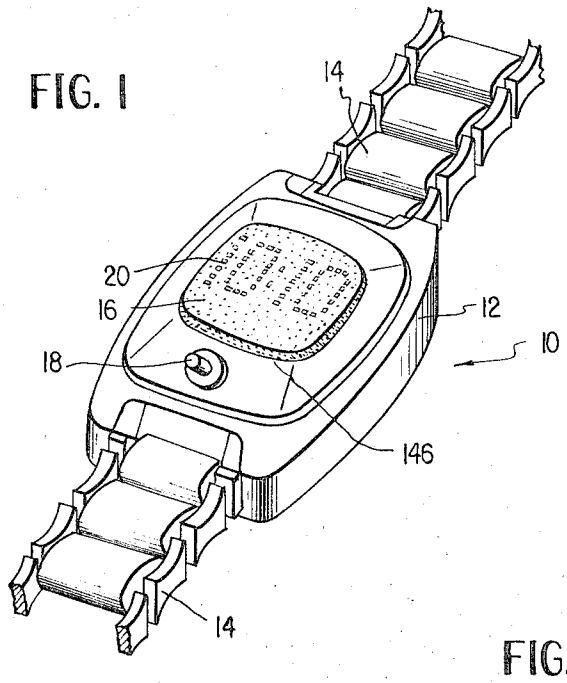


FIG. 1



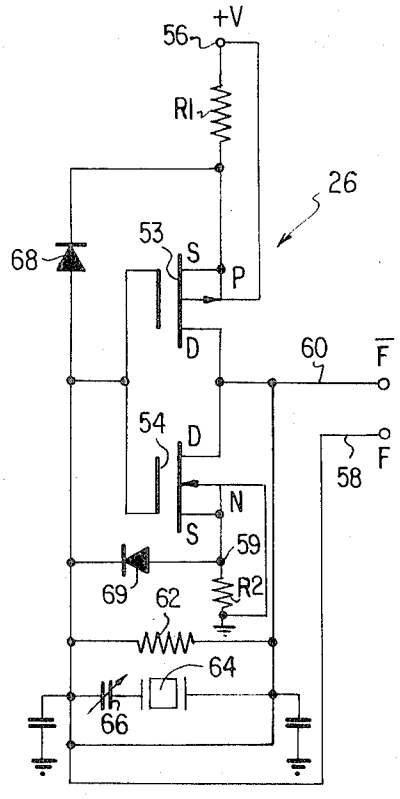
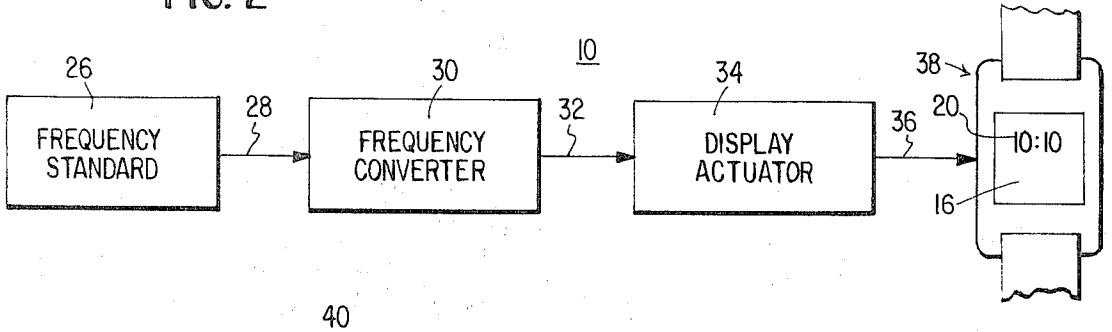




FIG. 4

FIG. 2



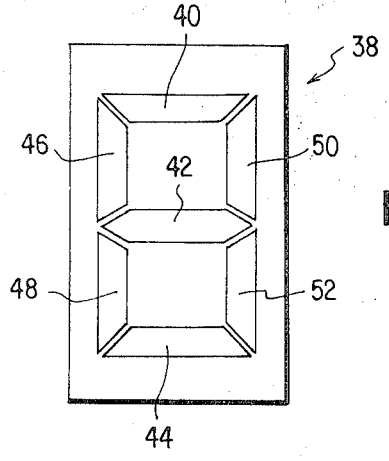




FIG. 3

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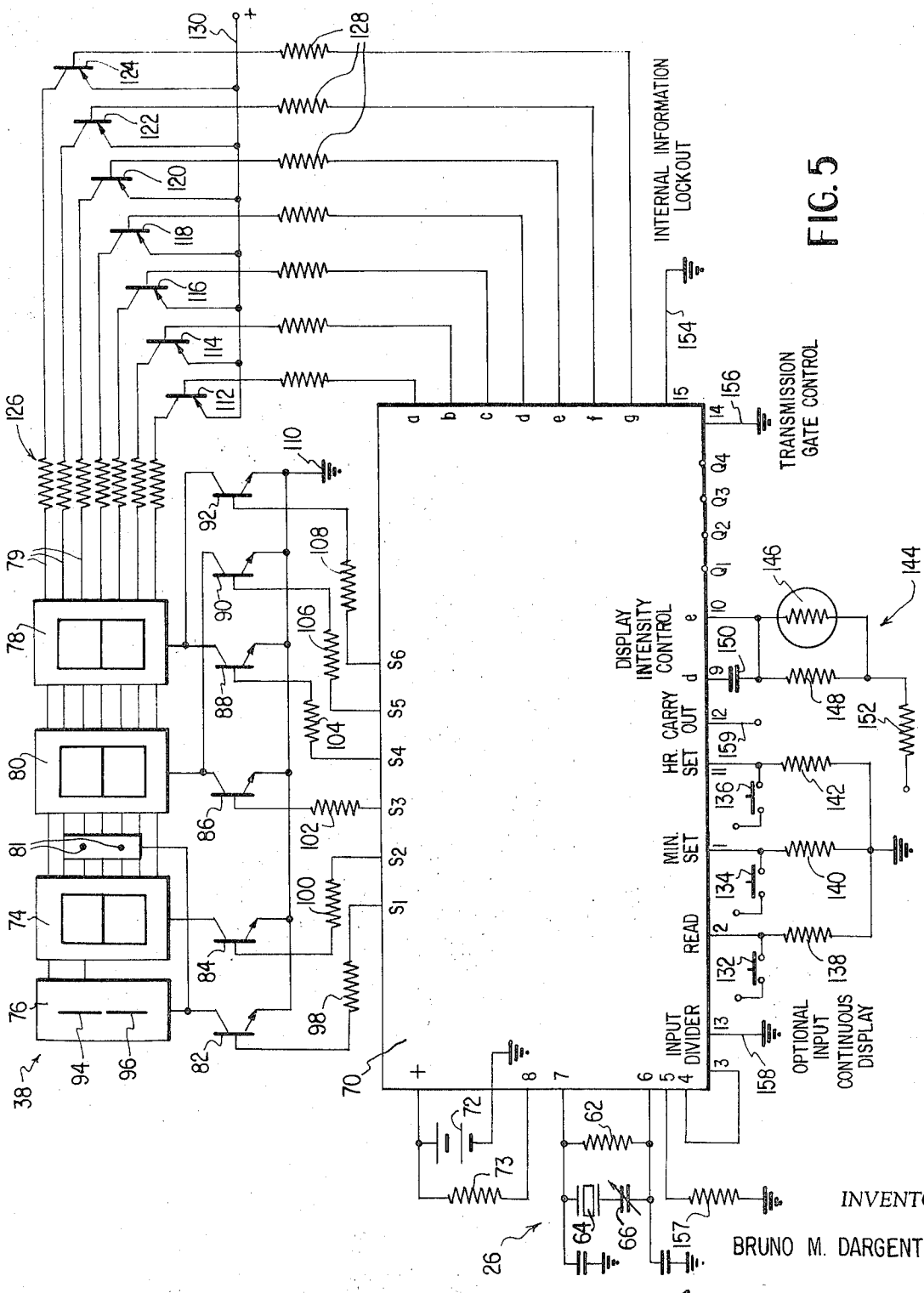


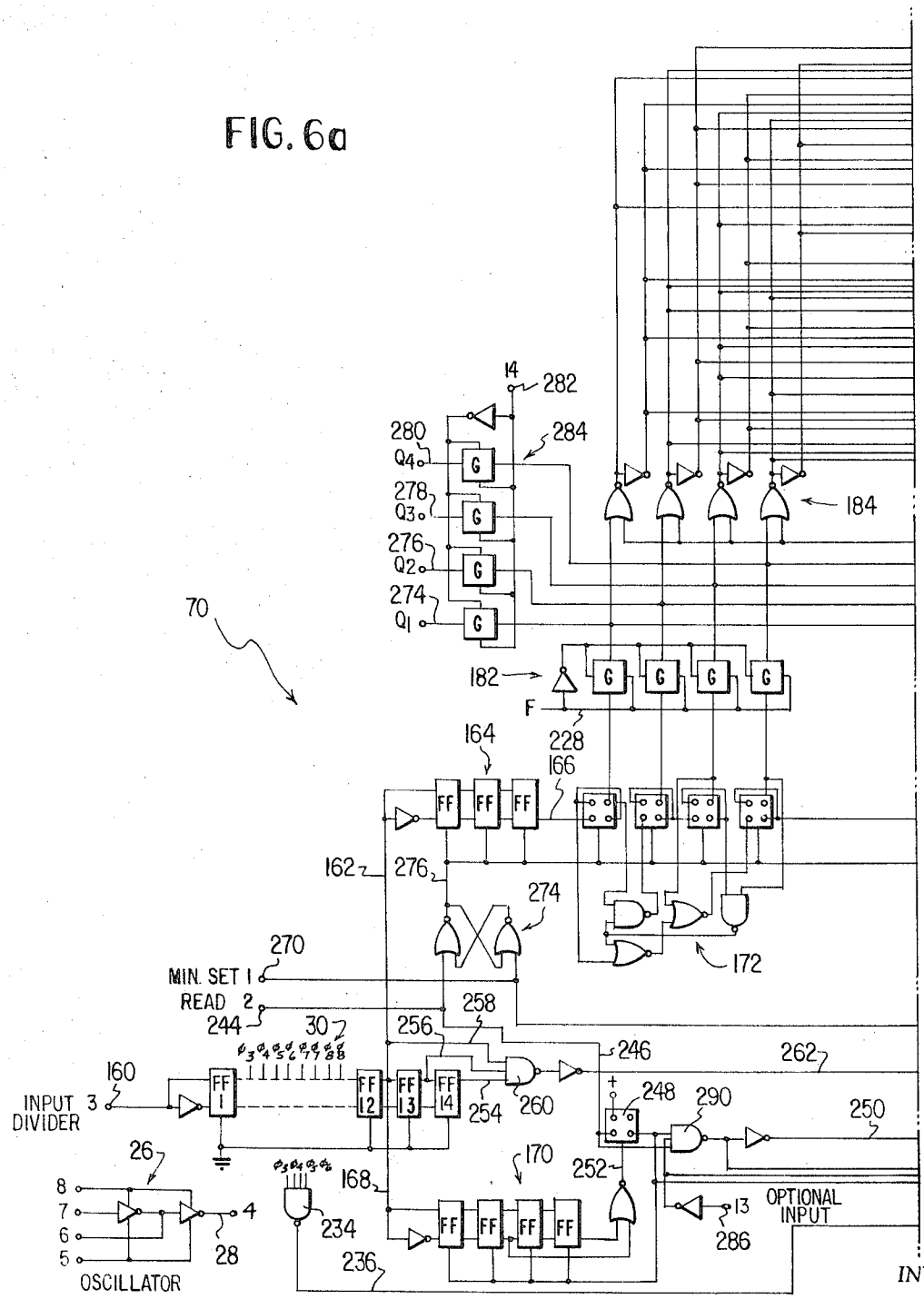

FIG. 5

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FIG. 6a



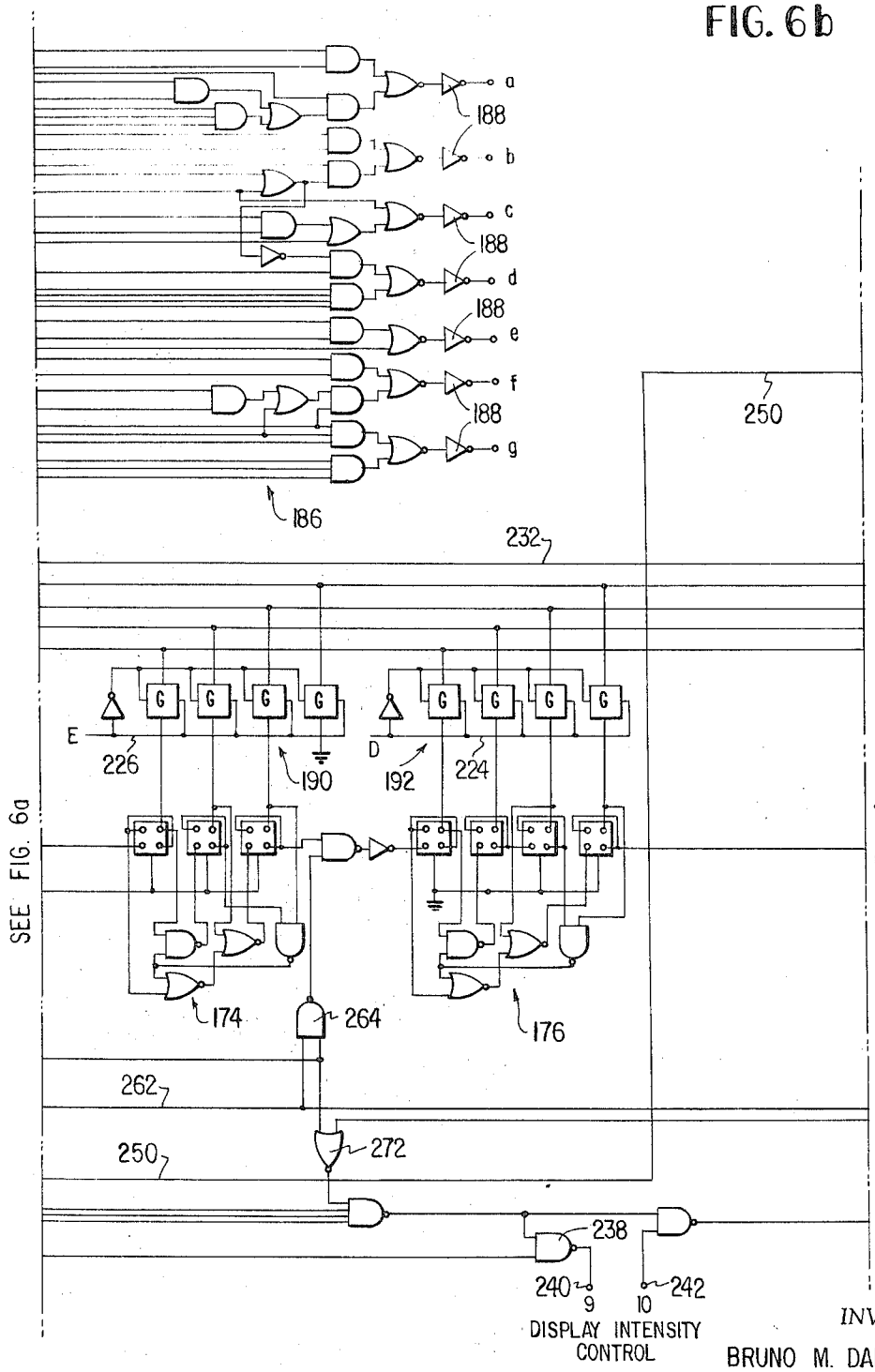

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FIG. 6b




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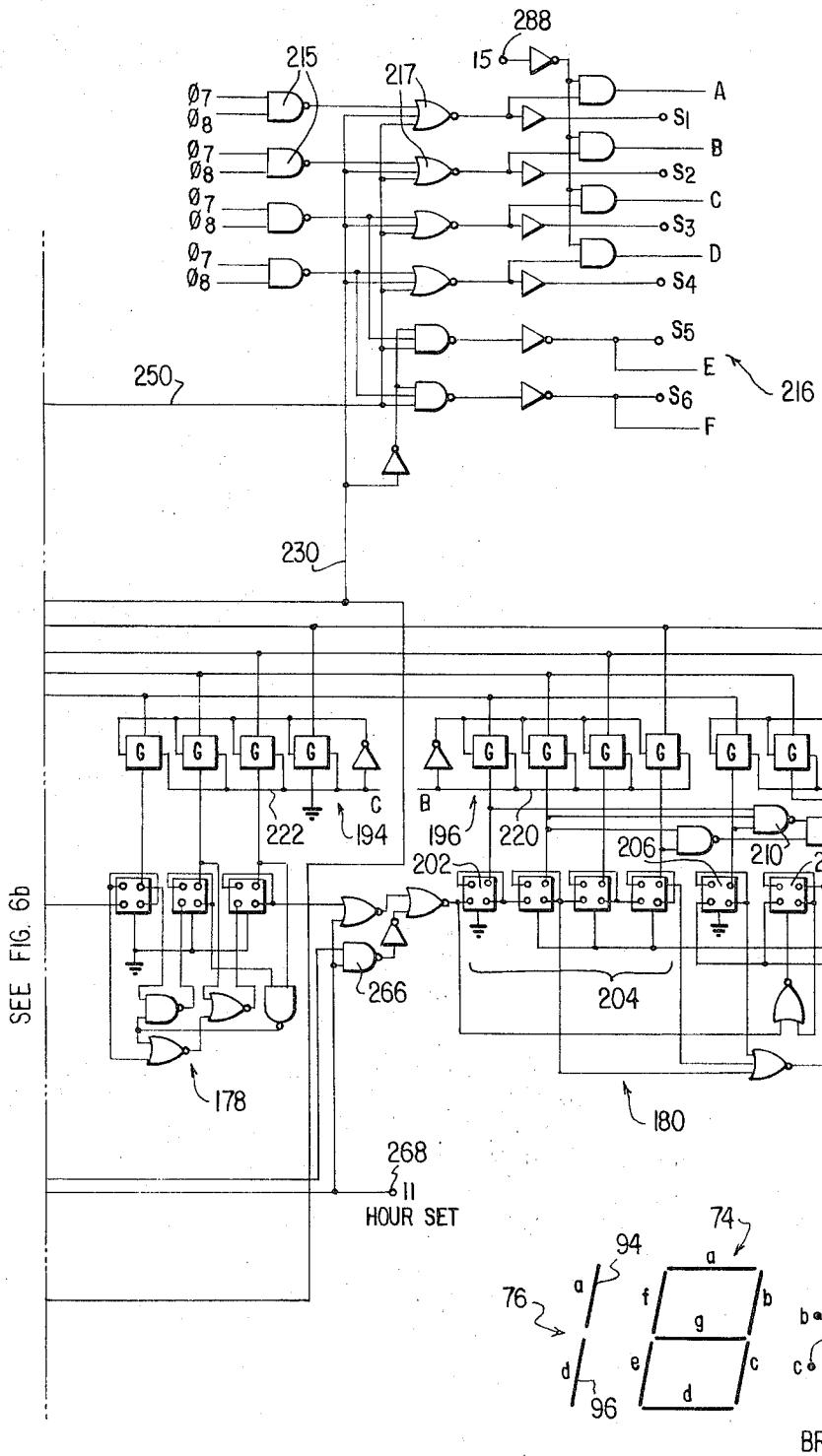



FIG. 6c




FIG. 7

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# INTEGRATED CIRCUIT SOLID STATE WATCH

This application is a continuation-in-part of copending application Ser. No. 138,547, filed Apr. 29, 1971, in the name of Bruno M. Dargent entitled "Solid State Watch Incorporating Large-Scale Integrated Circuits", now U.S. Pat. No. 3,714,867.

This invention relates to a solid state timepiece and more particularly to an electronic watch which employs no moving parts. In the present invention, a frequency standard in the form of a crystal oscillator acts through solid state electronic circuit dividers and drivers to power in timed sequence the light-emitting diodes of an electrooptic display. Low power consumption and small size and weight are achieved through the use of complementary MOS circuits to produce what is in essence a miniaturized fixed program computer. In particular, the present invention is directed to a wristwatch in which substantially all of the electrical circuitry may be constructed using large-scale integrated circuit techniques.

Battery-powered wristwatches and other small portable timekeeping devices of various types are well known and are commercially available. The first commercially successful battery-powered wristwatch was of the type shown and described in assignee's United States Reissue Patent No. RE 26,187, reissued Apr. 4, 1967, to John A. Van Horn et al for "Electric Watch." Electric watches of this type employ a balance wheel and a hairspring driven by the interaction of a current-carrying coil and a magnetic field produced by small permanent magnets.

In recent years, considerable effort has been directed toward the development of a wristwatch which does not employ an electromechanical oscillator as the master time reference. In many instances, these constructions have utilized a crystal controlled high frequency oscillator as a frequency standard in conjunction with frequency conversion circuitry to produce a drive signal at a suitable timekeeping rate. However, difficulties have been encountered in arriving at an oscillator frequency converter combination having not only the required frequency stability but also sufficiently low power dissipation and small size to be practical for use in a battery-powered wristwatch.

In order to overcome these and other problems there is disclosed in assignee's U.S. Pat. No. 3,560,998, issued Feb. 2, 1971, a high frequency oscillator type watch constructed using low power complementary MOS circuits. The oscillator/frequency converter combination of that patent is described as suitable for driving conventional watch hands over a watch dial or, alternatively, for selectively actuating the display elements of an optical display in response to the drive signal output of the converter. In assignee's U.S. Pat No. 3,576,099, issued Apr. 27, 1971, there is disclosed an improved watch construction in which the optical display is described as a plurality of light-emitting diodes which are intermittently energized to assure a minimum power consumption and an increasingly long life for the watch battery.

An improve watch construction of this general type incorporating solid state circuits and integrated circuit techniques is disclosed in assignee's copending U.S. Pat. application Ser. No. 35,196, filed May 6, 1970 U.S. Pat. No. 3,672,155. The present invention is directed to an improved watch construction of the same general type as disclosed in the above-mentioned application and patents and one which utilizes no moving parts to perform the timekeeping function. In particular, the present invention is directed to an electronic wristwatch construction in which substantially all of the electrical components are formed as large-scale integrated circuits so as to reduce both the cost and size of the watch components. Through the use of large-scale integrated circuits, it is possible to utilize standardized, mass production fabrication of the electrical components which not only substantially reduces the cost of the watch, but, because of the reduction in size, makes more space available in a conventional wristwatch case for the watch battery and other wristwatch components.



In the present invention, the wristwatch comprises a frequency standard, preferably operating at a frequency of 32,768 Hz and formed as a crystal controlled complementary MOS inverter used as an oscillator. Output signals from the frequency standard pass through a frequency converter, preferably in the form of a multi-stage binary frequency divider constructed of complementary MOS transistors. The signal is divided down in the frequency converter to produce an output of 1 Hz. The display actuator is formed by a plurality of registers, gates and a decoder which drives an electro-optical display, preferably in the form of a bar segment arrangement of light-emitting diodes. Additional functions performed by the large-scale integrated circuit involve time setting, resetting, switching, and display intensity control.

Through the use of NOR and NAND logic circuits and complementary MOS transistors, it is possible through the present invention to construct a solid state watch in which all but a very few of the electrical components may be formed using large-scale integration, commonly referred to as LSI.

The watch display preferably comprises a red colored filter which passes cold red light from a plurality of gallium arsenide phosphide light-emitting diodes which are preferably arranged in a seven bar segment array. The light-emitting diodes are energized in appropriate time relationship with an effective brightness determined by an intensity control circuit utilizing a photosensitive detector. Situated on the front of the watch adjacent the display is a pushbutton demand switch which, when depressed, instantly activates the appropriate visual display stations. Minutes and hours are programmed to display for one and one-quarter seconds with just a touch of the demand switch. Continued depression of this switch causes the minute and hour data to fade and the seconds to immediately appear. The seconds continue to count as long as the wearer depresses the demand button. Computation of the precise time is continuous and completely independent of whether or not time is displayed.

Setting is accomplished by actuating either an hour-set switch or a minute-set switch. The hour-set switch rapidly advances the hours without disturbing the timekeeping of the minutes and seconds. Actuation of the minute-set switch automatically zeros the seconds while advancing the minutes to the desired setting.

The watch of the present invention is virtually shockproof and waterproof regardless of the environment in which it is placed. The electrical components and the display may be encapsulated with a clear potting compound so that no mechanical forces or corrosive elements can attack the electronics. Since there is no con-

ventional stem for winding or setting, the small shaft sealing problem is eliminated. No maintenance or repair is normally necessary since the components are sealed and inaccessible to influences from the outside world. All solid state electrical components, including the light-emitting diode displays, have a virtually unlimited life.

Important features of the present invention include the use of an integrated circuit with a single decoder for decoding the time information to be displayed. In addition to time, the display can be used with the decoder to show day and month, as well as a.m. and p.m. of time. The display digits are individually strobed and special connections are provided to turn on the display at all times for use as a clock, for use as an alarm clock, to enter special information such as the date, month, a.m. and p.m. times. In addition, a connection is provided as a carryout from the hours register for use with a calendar circuit so that the watch circuit may be used in conjunction with other circuitry to have and show on the same display days and months.

It is therefore one object of the present invention to provide an improved electronic wristwatch.

Another object of the present invention is to provide a wristwatch which utilizes no moving parts for performing the timekeeping function.

Another object of the present invention is to provide a completely solid state electronic wristwatch in which the display is in the form of a plurality of light-emitting diodes.

Another object of the present invention is to provide an electronic watch including an illuminated display in which the light level is automatically compensated to the viewing conditions for increased eye comfort and reduced power drain.

Another object of the present invention is to provide an improved timepiece having reduced size and cost for incorporation in a conventional man's wristwatch case.

Another object of the present invention is to provide an improved solid state timepiece in which substantially all of the electrical components are formed from large-scale integrated circuits.

Another object of the present invention is to provide a simplified wristwatch construction and yet one which has increased versatility of operation so that other information can be displayed and so that the watch can be used with other external circuits.

These and further objects and advantages of the invention will be more apparent upon reference to the following specification, claims, and appended drawings, wherein:

FIG. **1** is a perspective view of a conventional sized man's wristwatch constructed in accordance with the present invention;

FIG. **2** is a simplified block diagram showing the principal components of the wristwatch of FIG. **1**;

FIG. **3** shows a seven bar segment light-emitting diode array forming a part of the display of the wristwatch of FIGS. **1** and **2**;

FIG. **4** is a diagram of an oscillator forming the time base or frequency standard of FIG. **3**;

FIG. **5** is a more detailed circuit diagram of the wristwatch of the present invention showing in block form the large-scale integrated circuit;

FIGS. **6***a*, **6***b*, and **6***c*, taken together show a detailed block diagram of the large-scale integrated circuit of FIG. **5**; and

FIG. **7** shows the arrangement of the light-emitting diode bar segments in the watch of the present invention.

Referring to the drawings, the novel watch of the present invention is generally indicated at **10** in FIG. **1**. The watch is constructed to fit into a watch case **12** of approximately the size of a conventional man's wristwatch. The case **12** is shown connected to a wristwatch bracelet **14** and includes a display window **16** through which time is displayed in digital form as indicated at **20**. The window may desirably be closed off by a red light filter to enhance the display. Mounted on the case **12** is a pushbutton demand switch **18** by means of which the display **20** may be actuated when the wearer of the wristwatch **10** desires to ascertain the time.

In normal operation, time is continuously being kept but is not displayed through the window **16**. That is, no time indication is visible through the window and this is the normal condition which prevails in order to conserve battery energy in the watch. However, even though the time is not displayed through the window **16**, it is understood that the watch **10** continuously keeps accurate time and is capable of accurately displaying this time at any instant. When the wearer desires to ascertain the correct time, he depresses the pushbutton **18** with his finger and the correct time immediately is displayed at **20** through the window **16**, which shows a light-emitting diode display giving the correct time reading of 10:10, namely, ten minutes after ten o'clock. The hours and minutes, i.e., 10:10, are displayed through the window **16** for a predetermined length of time, preferably one and one-quarter seconds, irrespective of whether or not the pushbutton **18** remains depressed. The exact time of the display is chosen to give the wearer adequate time to consult the display to determine the hour and minute of time. Should the minutes (or hours) change during the time of display, this change is immediately indicated by advancement of the minute (or hour) reading to the next number, i.e., **11**, as the watch is being read. If the pushbutton **18** remains depressed, at the end of one and one-quarter seconds the hours and minutes of the display are extinguished, i.e., they disappear, and simultaneously the seconds reading is displayed through the window **16**. The advancing seconds cycling from 0 to 59 continue to be displayed through window **16** until the pushbutton switch **18** is released.

FIG. **2** is a simplified block diagram of the principal components of the watch **10** of FIG. **1**. The watch comprises a time base or frequency standard **26**, preferably chosen to produce an electrical output signal on lead **28** at a frequency of 32,768 Hz. This relatively high frequency is supplied to a frequency converter **30** in the form of a divider which divides down the frequency from the standard **26** so that the output from the converter **30** appearing on lead **32** is at a frequency of 1 Hz. This signal is applied to the display actuator **34** which in turn drives the display **20** of the watch by way of electrical lead **36**. While only an hours and minutes display is shown, it is understood, as previously described, that the hours and minutes are first displayed for a predetermined time and if the pushbutton remains depressed, the hours and minutes are extinguished and the seconds become visible. The same display diodes are used for both minutes and seconds since these are not displayed simultaneously, thus minimizing the power drain from the watch battery. For a more de-

tailed description of the physical construction and mode of operation of the watch of the present invention, reference may be had to assignee's copending United States patent application Ser. No. 35,196, filed May 6, 1970 now U.S. Pat. No. 3,672,155, the disclosure of which is incorporated herein by reference. ,

In the preferred embodiment, the display takes the form of a seven bar segment array of light-emitting diodes, preferably formed of gallium arsenide phosphide which emit light when energized in the visible red region of the spectrum. FIG. 3 shows a single display station or numeral **38** consisting of seven light-emitting diodes **40, 42, 44, 46, 48, 50,** and **52** of elongated shape and arranged so that by lighting an appropriate combination of the bars or segments any one of the numbers 0 through 9 may be displayed. While a seven bar segment display is preferred, it is apparent that other type displays, such as a 27 dot matrix display, may be used.

FIG. 4 is a circuit diagram of the frequency standard **26** of FIG. **2.** The frequency standard is a crystal controlled oscillator comprising a complementary pair of integrated circuit enhancement transistors including a P-channel transistor **53** and an N-channel transistor **54** connected between the positive supply terminal **56** and the other or grounded side of the power supply, as indicated at **59,** to form a complementary MOS inverter. The F and $\overline{F}$ outputs for the divider **30** of FIG. **2** are developed on output leads **58** and **60** in FIG. **4.** The divider is preferably of the type shown and described in assignee's U.S. Pat. No. 3,560,998, the disclosure of which is incorporated herein by reference. Transistors **53** and **54** in FIG. **4** form an MOS integrated circuit inverter and have connected across them a bias resistor **62,** a quartz crystal **64,** and a variable tuning capacitor **66** in series with the crystal. Connected between the positive power supply terminal **56** and the transistor gate is a protective diode **68.** A $\pi$ network configuration made with two capacitors from input and output of the oscillator to ground improves stability and makes the oscillator very little circuit (CMOS) dependent.

The active element of the oscillator **26** of FIG. **4** is the complementary MOS inverter with the protective diodes **68** and **69** between the gate and source of each of the transistors **53** and **54.** This inverter can be a separate device but is preferably a part of the integrated circuit divider chain as more fully described below. The bias resistor **62** is used to bias the inverter into the linear region by making the input voltage equal to the output voltage under static conditions. Once the oscillator is under the control of the crystal, the bias resistor **62** is no longer a significant part of the circuit. A typical value for the bias resistor is about 22 megaohms. Quartz crystal **64** is of the type normally used in oscillators where the Q is high and the series resistance is low. The shunt capacitance of the crystal should be less than 10 picofarads. Tuning capacitor **66** is used to adjust the oscillator over a narrow range of frequencies. The value of this capacitor is normally between 0.5 and 5.0 picofarads. Oscillator **26** provides the two-phase output required by the first stage of the divider chain. The oscillator has two resistors $R_1$ and $R_2$ to control the current in the oscillator and make the circuit device independent. An inverter is used on the output of the oscillator as a shaping circuit in order to enter a square wave signal into the divider.

The gate protective diodes **68** and **69** are desirable because in MOS transistors it is easy to permanently damage the transistor by applying a voltage to the gate which is higher than the source or substrate voltage. A high positive or negative potential on the gate will cause arcing across the gate dielectric which will create pinholes in the dielectric and alter the transistor characteristics. By adding the diodes **68** and **69** between the gate and source of the transistors, a current path is provided when the gate voltage is higher than the source potential.

FIG. **5** is a circuit diagram of the watch **10** of the present invention with like parts bearing like reference numerals. Integrated circuit portions of the watch are illustrated by the large block **70.** This block may be formed of one or several integrated circuit chips but it is understood that all the components within block **70** (which components are illustrated in FIGS. **6***a*, **6***b*, and **6***c*) are formed by large-scale integrated circuit techniques. In addition to the integrated circuit **70** in FIG. **5,** the watch comprises a battery **72** which, by way of example only, may comprise a conventional 3 volt wristwatch battery. Connected to the positive side of the battery is a resistor **73** for a purpose more fully described below and the battery energizes the display **38** which is shown in FIG. **5** as consisting of a pair of hours stations comprising the digit station **74** and tens station **76** and a pair of combination minutes and seconds stations comprising digits station **78** and tens station **80.** In addition, the display **38** includes a pair of colon dots **81,** each formed by a single light-emitting diode. The display stations are energized from integrated circuit **70** connected to battery **72** by way of a plurality of leads **79.** The circuit is completed from the leads **79** to the anodes of the light-emitting diodes and the cathodes of the light-emitting diodes are individually connected to the other side of the power supply through strobing or switching N-P-N junction transistors **82, 84, 86, 88, 90,** and **92.** There is a separate lead **79** for the total number of bar segments in a display station. That is, with a seven bar segment display, there are seven leads **79,** each one connected to a separate bar segment of each station as more fully described below. However, all of the cathodes of each station are connected in common through the N-P-N junction transistor for that display. The two bar segments **94** and **96** for the hours tens display have their cathodes connected to transistor **82** as do the colon dots **81.** All cathodes of the hours units station **74** are connected to transistor **84.** Display stations **78** and **80** are used to display both minutes and seconds so that station **80** has the cathodes of all diodes connected to transistor **86,** referred to as the minutes transistor, and to transistor **90,** which acts as the seconds transistor. Similarly, all the diode cathodes of display station **78** are connected to a minutes transistor **88** and a seconds transistor **92.** These transistors have their bases returned to the integrated circuit **70** through current limiting resistors **98, 100, 102, 104, 106,** and **108,** the emitters of the transistors being connected in common to ground, i.e., the negative side of the power supply battery **72** as indicated at **110.**

The anodes of the bar segment diodes are energized from bipolar driver transistors illustrated in FIG. **5** as the P-N-P junction transistors **112, 114, 116, 118, 120, 122,** and **124.** Since the greatest number of bar segments at any display station is seven, there are seven driver transistors and seven leads **79.** The transistor collectors are connected to the display diodes through individual ones of current limiting resistors **126** and the

driver transistor bases are connected to the integrated circuit **70** through protective resistors **128.** The emitters of the driver transistors are connected in common as at **130** to the positive side of power supply battery **72.**

The external components of the oscillator **26** in FIG. **5** are the crystal **64,** the variable capacitor **66,** and the bias resistor **62** and $\pi$ netowrk capacitor. The of the oscillator shown in FIG. **4** are incorporated in the integrated circuit **70** of FIG. **5.** Also external to the integrated circuit is a demand or read switch **132** which is closed when the button **18** of FIG. **1** is depressed. Further manually operated switches external to the integrated circuit **70** are minute-set switch **134** and hour-set switch **136.** These switches are connected across battery **72** from the positive side of the battery to ground through respective series resistors **138, 140,** and **142.** The resistors associated with the switches are used in order to ground the corresponding inputs, otherwise the corresponding inputs would be floating and could be anything. When closed, the switches are used to switch the input voltages from ground to plus.

A feature of the watch of the present invention is that the intensity of the light emitted from the display diodes is varied in accordance with ambient light. That is, the diode light intensity is increased for greater contrast when the ambient light is bright, such as during daytime display, whereas the intensity of the light from the diodes is decreased when ambient light decreases. The automatic display intensity control circuitry is generally indicated at **144** in FIG. **5** and comprises a photosensitive resistor **146** suitably mounted on the face of the watch connected to the positive side of battery **72** and to a resistor **148** and capacitor **150.** These components are connected to the positive side of the power supply through series resistor **152.** Other external components connected to integrated circuit **70** include an internal information lockout lead **154,** a transmission gate control lead **156,** and an optional input or continuous display lead **158,** all normally grounded. A further connection to ground is through resistor **157** and the integrated circuit **70** is also provided with a carry out lead and terminal **159.**

FIGS. **6***a*, **6***b*, and **6***c* taken together show is a detailed block diagram of the integrated circuit **70** of FIG. **5.** In FIGS. **6***a*, **6***b* and **6***c*, like parts bear like reference numerals. FIG. **7** illustrates the arrangement of the light-emitting diode segments of the display.

Referring to FIGS. **6***a*, **6***b*, **6***c* and **7**, a signal having a frequency of 32,768 Hz is supplied from oscillator **26** over lead **28** to the divider input terminal **160.** The divider **30** is a **14** stage non-resettable counter forming the frequency converter **30** of FIG. **2.** The counter is formed from **14** stages of binary flip-flops in a counting chain and each stage is comprised of complementary MOS transistors as previously described. The output of the 12th stage of the divider, having a frequency of 8 Hz, is applied by way of a lead **162** to the input of a three-stage resettable counter **164** comprising three stages of MOS complementary symmetry transistor flip-flops which produce an output on lead **166** having a frequency of 1 Hz. The 8 Hz signal from the divider is also applied by way of a lead **168** to a four-stage flip-flop decade counter **170,** the output of which counter or control timer **170** controls a one and one-quarter second timing flip-flop **172.**

The 1 Hz signal on lead **166** is applied to a seconds units storing register **172** which divides by ten and whose output is in turn connected to a seconds tens register **174** which divides by six. The seconds tens register in turn has its output connected to a minutes units register **176** which again divides by ten and the output of this register is connected to a minutes tens register **178** which divides by six. The output of register **178** is in turn connected to a divide by 12 hours register, generally indicated at **180.** These registers are all comprised of binary chains of complementary MOS transistor pairs and the individual stages, except for the control terminals, are in all respects similar to the individual stages of the binary dividers **30** and **164.** For a detailed discussion of an individual stage forming a stage of either the divider **30,** divider **164,** or one of the registers **172, 174, 176, 178,** and **180,** reference may be had to assignee's U.S. Pat. No. 3,560,998.

Output signals indicative of seconds units of time are developed in register **172** and these are applied through four selection gates **182,** and through four input gates **184,** to a decoder **186.** The decoder **186** converts the 8–4–2–1 binary coded decimal signals from the register **172** into suitable drive signals for the displays which are applied to the light-emitting diodes of the display through the buffer amplifiers **188.** The individual bar segments are labeled a through *g* and the relationships of the segments and their interconnections to the outputs of the buffer amplifiers **188** is illustrated in FIG. **7.** That FIGURE shows the hours tens station **76** and the hours units station **74,** along with the colon dots **81.** While only the hours station **74** is illustrated in FIG. **7,** it is understood that the outputs of the buffer amplifiers **188** are also connected to the corresponding bar segments of the combination minutes and seconds stations **78** and **80** of FIG. **5,** each of these stations being in all respects identical to station **74.** That is, output a from buffer amplifier **188** is not only connected to the a bar segment of station **74,** but is also connected to the corresponding segment of stations **78** and **80** of FIG. **5.** The correspondingly labeled other outputs of buffer amplifiers **188** are connected to the corresponding other bar segments of each of the stations **74, 78,** and **80.** Outputs *b* and *c* are also connected to the anodes of the colon dot diodes and outputs *a* and *d* from the buffer amplifiers **188** are connected to the anodes of the two diodes **94** and **96** forming the hours display. These diodes are simultaneously on or off to display a "1" or nothing at all in correspondence with the hours tens digit of time.

Register **174** in FIG. **6***b* is similarly connected through four selection gates **190** to the input gates **184** and to the decoder **186,** the input gates **184** and decoder **186** being common to all the registers. Register **176** is connected to the input gates **184** through selection gate **192** and register **178** is similarly connected to the input gates through selection gates **194.** Finally, hours register **180** is connected to the input gates through two sets of selection gates, i.e., first set **196** and second set **200.** The integrated circuit **70** of FIG. **6** performs the functions of time base generation, time storage and information decoding, as well as the miscellaneous functions of display timing, automatic intensity control and display selection. The circuit is designed to operate 2.5 to 3.2 volts and to use 1.00 inch light-emitting diode displays. The time base generator portion of the circuit consists of external components

(crystal, resistor, and trimming capacitor), an inverter used as an oscillator and a 14-stage non-resettable counter **30**, as well as the three-stage resettable counter **164**. The 14-stage counter **30** provides the frequencies used throughout the system to perform such functions as timing, setting, resetting, switching, and display intensity control. The three-stage counter **164** is resettable because it acts as a "hold" circuit during minute setting. After the minutes have been set, this counter remains in the reset mode which keeps a signal from passing into the second storage register **172** until the read or demand button **18** of FIG. **1** has been depressed and the read switch **132** of FIG. **5** closed. This counter consists of three stages so that the error upon starting is no greater than one-eighth of a second.

The time storage portion of the circuit consists of three registers, two divide by **60** and another divide by **12**. The first divide by **60** register is resettable and is used to accumulate seconds. Both divide by **60** registers are subdivided into divide by ten and divide by six sections such that the first divide by **60** register is formed by the register sections **172** and **174** and the second divide by **60** register is formed by register sections **176** and **178**. This division is provided because the time information must be displayed as decimal numbers. The divide by 12 register **180** displays the numbers 1 through 12 and resets to 1. This is accomplished by making the first flip-flop **202** in the divide by 10 section, indicated by the bracket **204**, nonresettable. The first four flip-flops enclosed within bracket **204** constitute the divide by 10 section, the next flip-flop **206** controls the tens of hours and the last flip-flop **208** is used to insure positive resetting. At the count of 10, 8 and 2 are detected. This sets the tens of hours flip-flop **206** and triggers the resetting flip-flop **208** which resets stages 2, 4, and 8. Stage 1, i.e., flip-flop **202** is already at "0" so the units hours decodes to zero. However, at **13**, an AND gate **210** reads the tens of hours in stages **1** and **2**. This toggles the tens of hours flip-flop **206** by way of lead **212** back to zero and resets stages **2, 4,** and **8** by way of lead **214**. Stage **1**, i.e., flip-flop **202**, is not reset and therefore the number "1" is decoded. However, this happens so rapidly that the number 13 is never displayed.

It is a feature of this invention that only one decoder **186** is used in conjunction with a strobing circuit, generally indicated at **216**, by means of which the digits are individually strobed. The six strobe outputs, labeled A, B, C, D, E, and F, of the strobe circuit **216** are applied to the corresponding and similarly labeled lines **218, 220, 222, 224, 226,** and **228** of the selection gates **182, 190, 192, 194** and two sets in group **196**, such that these selection gates are enabled in accordance with the strobe outputs. A second set of strobe circuit outputs, labeled $S_1$, $S_2$, $S_3$, $S_4$, $S_5$, and $S_6$, are applied as correspondingly labeled inputs in FIG. **5** to the strobe transistors **82, 84, 86, 88, 90,** and **92**. The strobing outputs are such that the sequence of the display is as follows: (a) tens of hours and colon, (b) units of hours, (c) tens of minutes, (d) units of minutes, or (a) nothing, (b) nothing, (c) tens of seconds, (d) units of seconds if seconds are displayed, an then the cycle repeats.

It is apparent from FIG. **6** that a common decoder **186** is used for all numerals to be displayed. The high frequency output of oscillator **26** is lowered in frequency by a series of binary divider stages in divider **30**. This divider produces several output frequencies including a 8 Hz output which is fed into the register **164** to produce a 1 Hz output on lead **166**. The 1 Hz output is fed into the counting registers **172, 174, 176, 178,** and **180** where it is further divided by 10, 6, 10, 6, and 12, corresponding to the digits needed to display seconds, minutes and hours. The binary coded decimal outputs of all the dividers in the counting registers are fed into corresponding selection gates **182, 190, 192, 194,** and **196**. These gates are controlled by the strobe circuit **216** and the number passing through the input gates **184** into the decoder-driver **186** is determined by this strobe circuit.

In the operation of the system, the timer **170** controls the strobing circuit. When the demand switch is depressed, the minutes and hours are displayed for one and one-quarter seconds and if the demand switch remains depressed, the display automatically switches to seconds. Therefore, it is necessary for the strobe circuit to strobe only four numerals at any one time, although it controls all six numerals. After the strobing circuit **216** selects the register to be read, the time stored in that register (in binary coded decimal form) passes through the set of selection gates opened by the strobe circuit and through the input gates **184** which act as an interface to the decoder **186**. This decoder changes the B-C-D information into the output necessary to form intelligible numerals. The strobing circuit **216** not only chooses which counting register will be read, but also completes the anode circuit for the corresponding numeral diodes. Therefore, only one numeral can be on at any one time but because the strobing action takes place so rapidly, it appears that as many as four numerals are lighted simultaneously.

Divider **30** produces a 256 Hz output ($\phi 7$) and a 128 Hz output ($\phi 8$) which are applied to selected ones of four NAND gates **215** in strobe circuit **216**. These signals are in turn passed through four NOR gates **217** which also receive a signal by way of lead **250** from the timer control flip-flop **248**. The outputs A, B, C, D, E, and F from strobe circuit **216** are applied to the corresponding sets of selection gates **182, 190, 192, 194,** and **196** to control which numerals are to be displayed as described above. The other strobe outputs $S_1$, $S_2$, $S_3$, $S_4$, $S_5$, and $S_6$ are applied to the bases of transistors **82, 84, 86, 88, 90,** and **92** of FIG. **5** to complete the anode-cathode circuits of the display diodes. In this way, it is possible for the strobe circuit to control which information from which register will pass to the decoder **186** and this B-C-D information must pass through the input gates **184** which are provided to prevent interference between the several outputs from the selection gates as they enter the decoder. The output of the decoder-driver **186** provides power by way of driver transistors **112, 114, 116, 118, 120, 122,** and **124** in FIG. **5** to those segments or display diodes which are to be activated to display the number corresponding to the B-C-D input number.

Display intensity control is obtained by varying the duty cycle of the strobe drive signal supplied to the strobing circuit **216** by way of a lead **230**, this signal also being supplied as an ON-OFF signal by way of lead **232** to the input gates **184**. The signal on lead **232** insures that the diodes, even when on, will blink on and off but at a rate such as 64 Hz so as to give the appearance of being continuously energized. The ON-OFF signal on lead **232** and the strobe drive signal **230** is therefore a 64 Hz signal or series of short width pulses

having a repetition rate of 64 Hz in which the pulse width may be varied to vary the average duty cycle of the signal. This is accomplished by taking signals from the third, fourth, fifth and sixth stages of divider **30**, which signals are identified as $\phi 3$, $\phi 4$, $\phi 5$, and $\phi 6$, and applying them to the four inputs of a NAND gate **234**. The output from this gate on lead **236** is a series of **64** Hz pulses having a very short pulse width. These are applied through a NAND gate **238** by way of terminal **240** (labeled terminal **9**) to the display intensity control **144** of FIG. **5**. Resistor **152** in series with light sensor **146** gives increased linearity and the circuit in essence acts as a multivibrator which is triggered at a rate of 64 Hz from the divider **30** and NAND gate **234**. The length of the output pulse generated by the multivibrator **144** and applied to terminal **242** (labeled terminal **10** in FIG. **6**) is determined primarily by the fixed capacitor **150** and the light sensitive resistor **146** in FIG. **5**. These 64 Hz pulses, having a variable width and therefore a variable duty cycle in accordance with ambient light intensity, are supplied to the strobe circuit **216** by way of lead **230** and as ON-OFF or blinking signals to the input gates **184** to control the illumination duty cycle of the display diodes. The duty cycle in each digit is a maximum of 25 percent modulated by the light control network **144** to as low as 1.56 percent in the dark (6.25 percent of 25 percent). The strobing signals used for the minutes are also used for the seconds but in the preferred embodiment as illustrated, the minute display is also used for displaying seconds.

The display timer is generally indicated at **170** in FIG. **62**. This timer automatically turns off the hours and minutes after one and one-quarter seconds. A momentary depression of the read or demand button **18** produces a corresponding closure of the manual switch **132** in FIG. **5** and this completes a setting circuit, i.e., connects B+ to terminal **244** in FIG. **6**, which is connected by way of lead **246** and acts to set a timing flip-flop **248**. This flip-flop is reset only after the decade counter **170** has counted ten pulses of an 8 Hz signal applied to it over lead **168**. As long as flip-flop **248** is in the set condition, it puts the proper signal on lead **250** so that only the hours and minutes are displayed. If the read or demand button remains depressed after the decade counter **170** had completed a cycle and supplied a reset signal by way of lead **252**, the display automatically reverts to a display of seconds.

Divider **30** is a 14-stage binary device and produces a 2 Hz output on lead **254** which is combined with a 4 Hz signal on lead **256** and an 8 Hz signal on lead **258** in NAND gate **260** to produce a 2 Hz setting signal on lead **262** which has a very short pulse width. This signal is applied through NAND gate **264** to the input of minutes register **176** and through NAND gate **266** to the input of hours register **180**. Closure of the hours-set switch **136** in FIG. **5** applies B+ to terminal **268** and the short pulse width 2 Hz setting signal passes through NAND gate **266** to the hours register setting the hours display at the "fast" rate of two hours per second. Closure of minute-set switch **134** in FIG. **5** applies B+ to minute-set terminal **270** causing the 2 Hz setting signal to pass through gate **264** to the input of minute units register **176**. This is a "slow" or fine setting with the minutes advanced at two per second. A display during setting is assured by connecting hours-set terminal **268** and minutes-set terminal **270** through NOR gate **272** to the display intensity control circuit connected to terminals **240** and **242**.

Operation of the minute-set switch applies a reset impulse from minute-set terminal **270** through NOR gates **274** to lead **276** which resets counter **164** and the seconds registers **172** and **174** to zero. In this way, the seconds display is automatically zeroed when the minutes are set. Counting is resumed in the seconds registers as soon as the pushbutton **18** is depressed and the read switch **132** closed.

Decoder **186** is used to convert the 8–4–2–1 binary coded decimal codes from the registers into a seven segment display code for the display stations. It is used for the units and tens of seconds, for the units and tens of minutes, and for the units of hours. As previously described, the tens of hours are either on or off to display a "1" or nothing. The tens of hours display is connected to the a and d outputs of the decoder while the colon is connected to the *b* and *c* outputs so that a B-C-D "1" turns on the colon only and a B-C-D "0" turns on the colon and the tens of hours. The proper coded information is generated in the large-scale integration circuit **70** itself. A special feature of the decoder is that special information can be fed into it according to the following table:

TABLE

| B-C-D input | a | b | c | d | Display |
|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 1 : hours |
| | 1 | 0 | 0 | 0 | : |
| | 0 | 1 | 0 | 0 | 1 : AM |
| 0 1 1 0 | | | | | 1 : PM |
| | | | | | month |
| | 0 | 1 | 0 | 1 | : AM |
| | 0 | 1 | 1 | 1 | : PM |

That is, the display can be used with the decoder to show date and month, A.M. and P.M. being shown with one or the other dot of the colon. This special information is introduced through leads **274**, **276**, **278**, and **280**, labeled $Q_1$, $Q_2$, $Q_3$, and $Q_4$, respectively, all under the control of an input terminal **282** which is connected to the transmission gate control lead **156** in FIG. **5** and is normally grounded. Terminal **282** allows or prevents any signal to pass through the corresponding transmission gates, generally indicated at **284**. That is, if terminal **282** is grounded, the transmission gate acts as an open circuit. If terminal **282** is connected to B+, the transmission gates **284** are short circuits.

Also provided in the circuit is an optional input terminal **286** connected to the optional input lead **158** in FIG. **5** and normally grounded, as well as an internal information lockout terminal **288** coupled to the strobe circuit **216** and connected to the internal information lockout lead **154** of FIG. **5** and also normally grounded. When optional input terminal **286** is connected to a positive signal, this positive signal is applied to a NAND gate **290** so that decade timer **170** is defeated and the display hours and minutes are on all the time that a positive signal is applied to terminal **286**. When internal information lockout terminal **288** is connected to a positive signal, the strobing switch outputs $S_1$, $S_2$, $S_3$, and $S_4$ are not disturbed but the decoder is no longer able to send the B-C-D information from the registers because the control signal outputs A, B, C, and D from the strobe circuit **216** are stopped. With these circuits connected to the terminals **282**, **286**, and **288**, it is possible by using the proper combinations to (1) turn ON the display all the time for use as a clock, (2) defeat the

reading of the internal time and read any information entered at terminals **274, 276, 278,** and **280,** (3) read on terminals **274, 276, 278,** and **280** the time in the watch in B-C-D form (with the exception of the seconds at any time). When the display is ON all the time, it may be used as an alarm clock. It is also possible to (4) use this circuit with another one to have and show on the same display days and months.

Additional features of the circuit **70** include a carryout terminal **292** connected to external terminal and lead **159** in FIG. **5** to provide a carryout of the hours register for use with a calendar circuit. Also, it should be noted that + and − leads of the oscillator **26** are available so that limiting resistors can be introduced, that the output of the oscillator is available for use if desired.

It is apparent from the above that the present invention provides an improved solid state watch construction in which a vast majority, i.e., substantially all, of the electrical components are formed from a large-scale integrated circuit. The circuit is fabricated in its entirety from complementary symmetry MOS transistor and only the buffers in the circuit carry high currents so that small transistors can be used throughout substantially the entire circuit.

Important features of the invention include an electronically regulated timekeeping device characterized by sufficiently small size and low power dissipation to be practical for use in a device of wristwatch size. Through the use of large-scale integration, the circuit may be more economically manufactured and permits more space in a conventional wristwatch case for a battery, crystal and other components. While the preferred embodiment and certain especially significant operating conditions have been set forth in detail, it should be understood that various modifications are readily apparent. In the preferred embodiment, the light-emitting diodes take the form of gallium arsenide phosphide LED's of the type more fully shown and described in assignee's U.S. Pat. No 3,576,099, issued Apr. 27, 1971, the disclosure of which is incorporated herein by reference. However, it is understood that the display can assume any one of several forms. For example, the optical display may be formed using such well known devices as miniature incandescent bulbs, other types of light-emitting diodes or the well known liquid crystals, as well as lesser known devices such as ferroelectric crystals or electroluminescent displays and others. If desired, the electrical signals may be connected through a suitable electromechanical transducer or motor to drive conventional watch hands.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

What is claimed and desired to be secured by United States Letters Patent is:

**1.** A solid state wristwatch comprising a source of constant frequency electrical signals, a plurality of electrooptical display devices, said display devices being physically arranged to display at least the seconds and minutes of time in digital form, and an integrated circuit formed on a single chip entirely of complementary symmetry MOS transistors electrically coupling said source to said display devices, said single chip integrated circuit including a divider for dividing down the frequency of the signals from said source and a single decoder coupling said divided signals to said display devices, a plurality of counting registers coupled to said divider and producing binary coded decimal signals, and means coupling said binary coded decimal signals to said decoder, said means coupling said binary coded decimal signals to said decoder comprising a plurality of selection gates.

**2.** A solid state wristwatch comprising a source of constant frequency electrical signals, a plurality of electrooptical display devices, said display devices being physically arranged to display at least the minutes and hours of time in digital form, and a single chip large-scale integrated circuit formed entirely of complementary symmetry MOS transistors electrically coupling said source to said display devices, said integrated circuit including a divider for dividing down the frequency of the signals from said source and a decoder coupling said divided signals to said display devices, and a strobe circuit coupled to said display devices for energizing said display devices in sequence at a rate sufficiently high to give the appearance of continuous energization.

**3.** A solid state wristwatch comprising a source of constant frequency electrical signals, a plurality of electrooptical display devices, said display devices being physically arranged to display at least the minutes and hours of time in digital form, and a single chip integrated circuit formed entirely of complementary symmetry MOS transistors electrically coupling said source to said display devices, said integrated circuit including a divider coupled to said source for dividing down the frequency of the signals from said source, a plurality of counting registers coupled to the output of said divider and producing binary coded decimal signals, a plurality of selection gates coupled to the outputs of said registers, a decoder coupling the output of said selection gates to said display devices, and a strobing circuit coupled to said selection gates whereby said gates are activated in sequence in accordance with the output of said strobing circuit.

**4.** A wristwatch according to claim **2** wherein the same ones of said electro-optical display devices display both minutes and seconds of time.

**5.** A wristwatch according to claim **4** wherein said electro-optical display devices include means coupled to said divider and physically arranged to decimal the hours of time in physical form.

**6.** A wristwatch according to claim **5** wherein said display devices comprise a plurality of stations formed by a seven bar segment array of electro-optical devices.

**7.** A wristwatch according to claim **6** wherein said hours display includes an hours tens station comprising a pair of commonly connected colinear electro-optical bar segments.

**8.** A wristwatch according to claim **6** wherein said electro-optical display devices comprise light-emitting diodes.

**9.** A wristwatch according to claim **2** wherein said constant frequency source comprise a crystal controlled oscillator.

10. A wristwatch according to claim 2 wherein said strobe circuit forms part of said large-scale integrated circuit means.

11. A wristwatch according to claim 10 wherein said strobe circuit is coupled to said divider to receive signals having a frequency of at least 128 Hz from said divider.

12. A wristwatch according to claim 11 including a photosensor on the face of said timepiece, said photosensor being coupled between said divider and said strobe circuit whereby the duty cycle of the signal from said strobe circuit varies in accordance with the light incident on the face of said timepiece.

13. A wristwatch according to claim 3 wherein said strobing circuit has a first set of outputs coupled to said selection gates and a second set of outputs coupled to said display devices.

14. A wristwatch according to claim 3 wherein said display devices comprise four stations, two of said stations forming both a minutes and seconds display, the other two stations forming an hours display.

15. A wristwatch according to claim 3 including a plurality of electrical information inputs coupled to said decoder for introducing special information into said display from externally of said wristwatch.

16. A wristwatch according to claim 3 wherein said registers comprise a seconds register, a minutes register and an hours register, and an electrical carry output terminal coupled to said hours register to provide a carryout signal from said wristwatch.

17. A wristwatch according to claim 3 including an information lockout terminal coupled to said strobing circuit for inhibiting the output from said registers to said decoder.

18. A wristwatch according to claim 3 including an optional electrical input terminal coupled to said strobing circuit for turning the hours and minutes display devices on all the time.

* * * * *

# UNITED STATES PATENT OFFICE

# CERTIFICATE OF CORRECTION

Patent No. 3,760,584 Dated September 25, 1973

Inventor(s) Bruno M. Dargent

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 7, line 8, "netowrk" should read --network--; line 8. "The of" should read --The remaining portions of--; line 45, "show is a" should read --show a--.

Col. 8, line 65, "2.5" should read --at 2.5--.

Col. 9, line 62, "an" should read --and--.

Col. 11, line 32, "Fig. 62" should read --Fig. 6a--.

Col. 12, line 32, "0 1 1 0" should be moved along in line to fall under column "a b c d".

Col. 13, line 22-23, "transistor" should read --transistors--.

Col. 14, line 53, claim 5, "decimal" should read --display--; line 54, "physical" should read --decimal--;

Signed and sealed this 6th day of August 1974.

(SEAL)
Attest:

McCOY M. GIBSON, JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

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