



(51) International Patent Classification:

GIIC 16/34 (2006.01) *GIIC 16/08* (2006.01)

(21) International Application Number:

PCT/CN2019/123978

(22) International Filing Date:

09 December 2019 (09.12.2019)

(25) Filing Language:

English

(26) Publication Language:

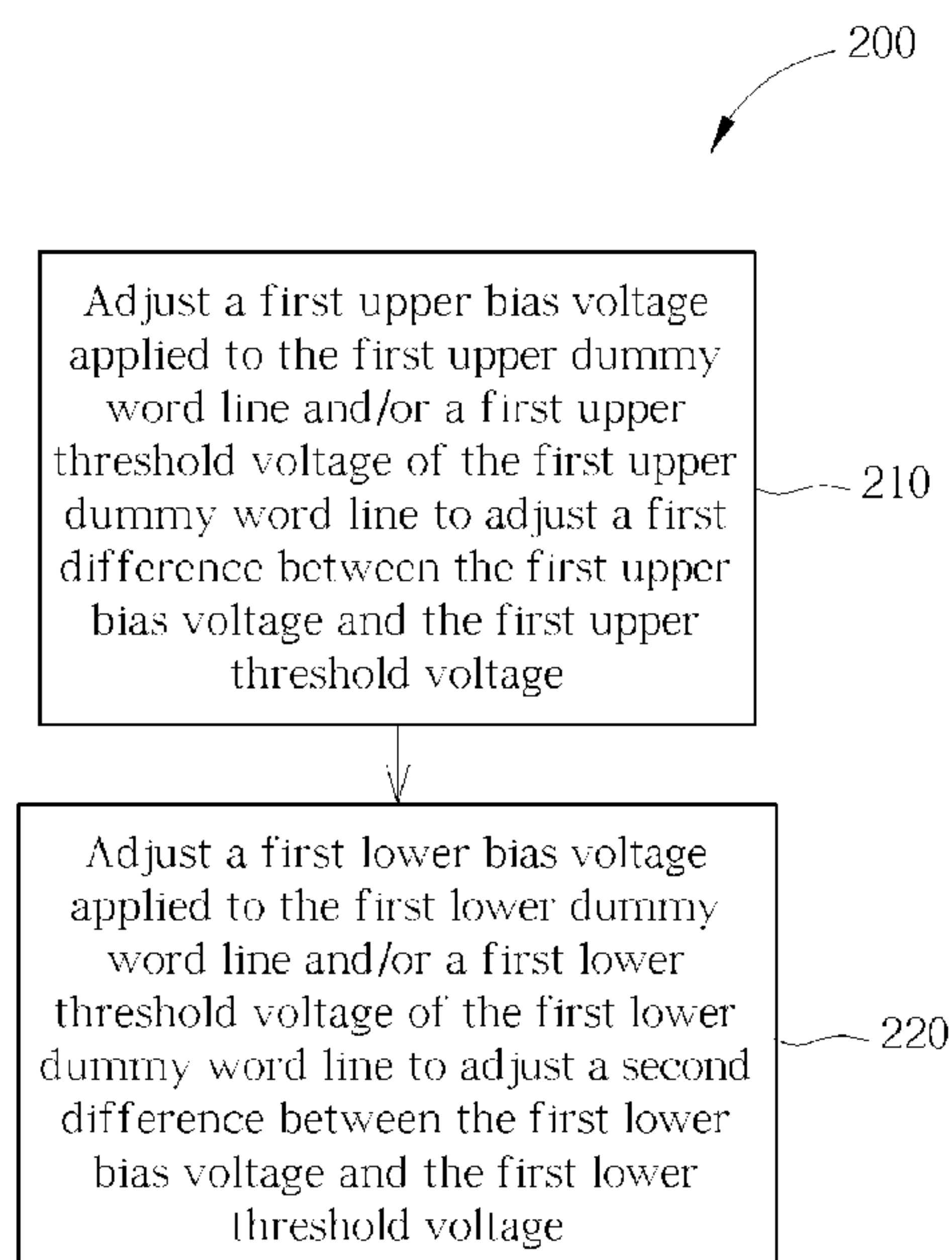
English

(71) Applicant: **YANGTZE MEMORY TECHNOLOGIES CO., LTD.** [CN/CN]; No.88 Weilai 3rd Road, East Lake High-Tech Development Zone, Wuhan, Hubei 430074 (CN).

(72) Inventors: **SONG, Yali**; Room 7018, No.18, Huaguang Road, Guandong Science, And Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **JIA, Jianquan**; Room 7018, No.18, Huaguang Road, Guandong Science, And Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **YOU, Kaikai**; Room 7018, No.18, Huaguang Road, Guandong Science, And Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **ZHANG, An**; Room 7018, No.18, Huaguang Road, Guandong Science, And Technology Industrial Park, East Lake

Development Zone, Wuhan, Hubei 430074 (CN). **ZHAO, Xiangnan**; Room 7018, No.18, Huaguang Road, Guandong Science, And Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **CUI, Ying**; Room 7018, No.18, Huaguang Road, Guandong Science, And Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **LI, Shan**; Room 7018, No.18, Huaguang Road, Guandong Science, And Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **LI, Kaiwei**; Room 7018, No.18, Huaguang Road, Guandong Science, And Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **JIN, Lei**; Room 7018, No.18, Huaguang Road, Guandong Science, And Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **HUANG, Xueqing**; Room 7018, No.18, Huaguang Road, Guandong Science, And Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **LOU, Meng**; Room 7018, No.18, Huaguang Road, Guandong Science, And Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **ZHANG, Jinlong**; Room 7018, No.18, Huaguang Road, Guandong Science, And Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN).

(54) Title: METHOD AND MEMORY USED FOR REDUCING PROGRAM DISTURBANCE BY ADJUSTING VOLTAGE OF DUMMY WORD LINE



(57) Abstract: A memory includes an upper deck and a lower deck. The upper deck includes a first upper dummy word line. The lower deck includes a first lower dummy word line. A method for reducing program disturbance of the memory includes adjusting a first upper bias voltage applied to the first upper dummy word line and/or a first upper threshold voltage of the first upper dummy word line to adjust a first difference between the first upper bias voltage and the first upper threshold voltage; and adjusting a first lower bias voltage applied to the first lower dummy word line and/or a first lower threshold voltage of the first lower dummy word line to adjust a second difference between the first lower bias voltage and the first lower threshold voltage.

FIG. 2

(74) **Agent: NTD UNIVATION INTELLECTUAL PROPERTY AGENCY LTD.;** 10th Floor, Tower C, Beijing Global Trade Center, 36 North Third Ring Road East, Dongcheng District, Beijing 100013 (CN).

(81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

METHOD AND MEMORY USED FOR REDUCING PROGRAM DISTURBANCE BY ADJUSTING VOLTAGE OF DUMMY WORD LINE

Background of the Invention

1. Field of the Invention

The disclosure is related to a method and a memory for reducing program disturbance, and more particularly, a method and a memory for reducing program disturbance by adjusting voltage of a dummy word line.

2. Description of the Prior Art

In order to increase the capacity of a memory, a memory with a three-dimensional structure has been developed. For example, a three-dimensional stack NAND flash memory can be available presently.

A three-dimensional structure of a memory can include a plurality of layers so as to store more data on a same area. This solution has been proved to be effective for increasing capacity of memory.

However, the program disturbance will become more serious when the number of layers is increased. Program disturbance will lead to a higher failure rate of programming a memory. Hence, a solution for reducing program disturbance when operating a three-dimensional memory is in need in the field.

Summary of the Invention

An embodiment discloses a method for reducing program disturbance of a memory. The memory includes an upper deck and a lower deck. The upper deck includes a first upper dummy word line. The lower deck includes a first lower dummy word line. The method includes adjusting a first upper bias voltage applied to the first upper dummy word line and/or a first upper threshold voltage of the first upper dummy word line to adjust a first difference between the first upper bias voltage and the first upper threshold voltage; and adjusting a first lower bias voltage applied to the first lower dummy word line and/or a first lower threshold voltage of the first lower dummy word line to adjust a second difference between the first lower bias voltage and the first lower threshold voltage.

Another embodiment includes a memory for reducing program disturbance. The memory includes an upper deck and a lower deck. The upper deck includes a first upper dummy word

line configured to receive a first upper bias voltage and have a first upper threshold voltage. The lower deck includes a first lower dummy word line configured to receive a first lower bias voltage and have a first lower threshold voltage. The first upper bias voltage and/or the first upper threshold voltage is adjusted to adjust a first difference between the first upper bias voltage and the first upper threshold voltage. The first lower bias voltage and/or the first lower threshold voltage is adjusted to adjust a second difference between the first lower bias voltage and the first lower threshold voltage.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

FIG.1 illustrates a memory according to an embodiment.

FIG.2 is a flowchart of a method for reducing program disturbance of the memory of FIG.1.

FIG.3 illustrates a memory according to another embodiment.

FIG.4 is a flowchart of a method for reducing program disturbance of the memory of FIG.3.

FIG.5 illustrates a memory according to another embodiment.

FIG.6 is a flowchart of a method for reducing program disturbance of the memory of FIG.5.

FIG.7 illustrates a memory according to another embodiment.

FIG.8 is a flowchart of a method for reducing program disturbance of the memory of FIG.7.

FIG.9 is a waveform of controlling the memory of FIG.7.

FIG.10 is a waveform of controlling the memory of FIG.7 according to another embodiment.

FIG.11 to FIG.14 illustrate a memory according to different embodiments.

Detailed Description

In the text, when an item A and an item B are connected with the conjunction “and/or” to be “A and/or B”, it indicates A, B or both of A and B.

FIG.1 illustrates a memory 100 according to an embodiment. The memory 100 may include an upper deck 110 and a lower deck 120. The upper deck 110 may be formed above

the lower deck 120. The memory 100 may further include a joint oxide layer 155 formed between the upper deck 110 and the lower deck 120.

As shown in FIG.1, the upper deck 110 may include a first upper dummy word line IDMY_u0, and the lower deck 120 may include a first lower dummy word line IDMY_l0.

FIG.2 is a flowchart of a method 200 for reducing program disturbance of the memory 100 of FIG.1. The method 200 includes following steps.

Step 210: adjust a first upper bias voltage V_{u0} applied to the first upper dummy word line IDMY_u0 and/or a first upper threshold voltage V_{t_u0} of the first upper dummy word line IDMY_u0 to adjust a first difference ΔV_{u0} between the first upper bias voltage V_{u0} and the first upper threshold voltage V_{t_u0} ; and

Step 220: adjust a first lower bias voltage V_{l0} applied to the first lower dummy word line IDMY_l0 and/or a first lower threshold voltage V_{t_l0} of the first lower dummy word line IDMY_l0 to adjust a second difference ΔV_{l0} between the first lower bias voltage V_{l0} and the first lower threshold voltage V_{t_l0} .

FIG.2 is merely an example, and the steps in FIG.2 may be performed in any sequence. For example, Step 220 may be performed first. The steps may be performed concurrently.

ΔV_{u0} and ΔV_{l0} in Step 210 and 220 may be expressed as the following equations:

$$\Delta V_{u0} = V_{u0} - V_{t_u0} \dots (\text{eq-1}); \text{ and}$$

$$\Delta V_{l0} = V_{l0} - V_{t_l0} \dots (\text{eq-2}).$$

As described in Step 210 and Step 220, V_{u0} and/or V_{t_u0} may be adjusted to adjust ΔV_{u0} . V_{l0} and/or V_{t_l0} may be adjusted to adjust ΔV_{l0} . By adjusting the first difference ΔV_{u0} and the second difference ΔV_{l0} as below, program disturbance may be reduced.

As shown in FIG.1, a word line WL_n may be at the first layer below the first lower dummy word line IDMY_l0. A word line $WL_{(n-1)}$ may be at the second layer below the first lower dummy word line IDMY_l0. Word lines $WL_{(n-2)}$ to WL_0 may be at layers below the layer of the word line $WL_{(n-1)}$.

A word line $WL_{(n+1)}$ may be at the first layer above the first upper dummy word line IDMY_u0. A word line $WL_{(n+2)}$ may be at the second layer above the first upper dummy word line IDMY_u0. Word lines $WL_{(n+3)}$ to WL_m may be at layers above the layer of the word line $WL_{(n+2)}$.

Regarding the adjustment of the first difference ΔV_{u0} and the second difference ΔV_{l0} , when programming a word line of the word lines $WL_{(n-1)}$ to $WL_{(n+2)}$, the first difference ΔV_{u0} may be adjusted to be higher than a threshold TH1. The second difference ΔV_{l0} may be adjusted to be higher than the threshold TH1. In other words, after the adjustment, ΔV_{u0}

$= V_{u0} - V_{t_{u0}} > TH1$, and $\Delta V_{l0} = V_{l0} - V_{t_{l0}} > TH1$. For example, the threshold TH1 may be 7 volts.

When programming a word line of the word lines WL(n+3) to WLm, the first difference ΔV_{u0} may be adjusted to be lower than a threshold TH2. The second difference ΔV_{l0} may be adjusted to be lower than the threshold TH2. In other words, after the adjustment, $\Delta V_{u0} = V_{u0} - V_{t_{u0}} < TH2$, and $\Delta V_{l0} = V_{l0} - V_{t_{l0}} < TH2$. For example, the threshold TH2 may be 7 volts.

When programming a word line of the word lines WL0 to WL(n-2), the first difference ΔV_{u0} and the second difference ΔV_{l0} may not be limited; however, according to experiments, the first difference ΔV_{u0} and the second difference ΔV_{l0} may be higher than a threshold TH3. For example, the threshold TH3 may be 3 volts.

FIG.3 illustrates the memory 100 according to another embodiment. The structure shown in FIG.3 may be similar to that shown in FIG.1. As shown in FIG.3, the lower deck 120 may further include a second lower dummy word line IDMY_{l1}.

FIG.4 is a flowchart of a method 400 for reducing program disturbance of the memory 100 of FIG.3. The method 400 may include following steps.

Step 210: adjust a first upper bias voltage V_{u0} applied to the first upper dummy word line IDMY_{u0} and/or a first upper threshold voltage $V_{t_{u0}}$ of the first upper dummy word line IDMY_{u0} to adjust a first difference ΔV_{u0} between the first upper bias voltage V_{u0} and the first upper threshold voltage $V_{t_{u0}}$;

Step 220: adjust a first lower bias voltage V_{l0} applied to the first lower dummy word line IDMY_{l0} and/or a first lower threshold voltage $V_{t_{l0}}$ of the first lower dummy word line IDMY_{l0} to adjust a second difference ΔV_{l0} between the first lower bias voltage V_{l0} and the first lower threshold voltage $V_{t_{l0}}$; and

Step 230: adjusting a second lower bias voltage V_{l1} applied to the second lower dummy word line IDMY_{l1} and/or a second lower threshold voltage $V_{t_{l1}}$ of the second lower dummy word line IDMY_{l1} to adjust a third difference ΔV_{l1} between the second lower bias voltage V_{l1} and the second lower threshold voltage $V_{t_{l1}}$.

FIG.4 is merely an example, and the steps in FIG.4 may be performed in any sequence. For example, Step 220 or Step 230 may be performed before Step 210. The steps may be performed concurrently.

ΔV_{u0} and ΔV_{l0} in Steps 210 and 220 may be expressed as the equations (eq-1) and (eq-2) above. ΔV_{l1} in Step 230 may be expressed as the following equation.

$$\Delta V_{l1} = V_{l1} - V_{t_{l1}} \dots \text{(eq-3)}.$$

As described in Step 210 to Step 230, the first difference ΔV_{u0} , the second difference ΔV_{l0} and the third difference ΔV_{l1} may be adjusted as below to reduce program disturbance.

When programming a word line of the upper deck 110, the first difference ΔV_{u0} may be adjusted to be higher than a threshold TH4, the second difference ΔV_{l0} may be adjusted to be lower than the threshold TH4, and the third difference ΔV_{l1} may be adjusted to be lower than the threshold TH4. In other words, after the adjustment, $\Delta V_{u0} = V_{u0} - V_{t_{u0}} > TH4$, $\Delta V_{l0} = V_{l0} - V_{t_{l0}} < TH4$, and $\Delta V_{l1} = V_{l1} - V_{t_{l1}} < TH4$. For example, the threshold TH4 may be 7 volts.

In addition, according to an embodiment, a condition (c-1) may also have to be met for reducing program disturbance of the memory 100 of FIG.3.

The condition (c-1) may include that a difference between the first difference ΔV_{u0} and the second difference ΔV_{l0} may be within a predetermined range, and another difference between the first difference ΔV_{u0} and the third difference ΔV_{l1} may be within the predetermined range.

The predetermined range related to the condition (c-1) may be within a level L1 and a level L2 higher than the level L1. Hence, in other words, the condition (c-1) may be expressed as $L1 < (\Delta V_{u0} - \Delta V_{l0}) < L2$, and $L1 < (\Delta V_{u0} - \Delta V_{l1}) < L2$. For example, the level L1 may be 3 volts, and the second level L2 may be 7 volts.

Regarding FIG.3, the equations and inequalities related to the first difference ΔV_{u0} , the second difference ΔV_{l0} and the third difference ΔV_{l1} mentioned above may be applied when programming a word line of the upper deck 110.

When programming a word line of the lower deck 120, the first difference ΔV_{u0} , the second difference ΔV_{l0} and the third difference ΔV_{l1} may not be limited; however, according to experiments, the differences ΔV_{u0} , ΔV_{l0} and ΔV_{l1} may be higher than a threshold such as 3 volts.

FIG.5 illustrates the memory 100 according to another embodiment. The structure shown in FIG.5 may be similar to that shown in FIG.1. As shown in FIG.5, the upper deck 110 may further include a second upper dummy word line IDMY_u1.

FIG.6 is a flowchart of a method 600 for reducing program disturbance of the memory 100 of FIG.5. The method 600 may include following steps.

Step 210: adjust a first upper bias voltage V_{u0} applied to the first upper dummy word line IDMY_u0 and/or a first upper threshold voltage $V_{t_{u0}}$ of the first upper dummy word line IDMY_u0 to adjust a first difference ΔV_{u0} between the first upper bias voltage

V_{u0} and the first upper threshold voltage $V_{t_{u0}}$;

Step 220: adjust a first lower bias voltage V_{l0} applied to the first lower dummy word line IDMY_{l0} and/or a first lower threshold voltage $V_{t_{l0}}$ of the first lower dummy word line IDMY_{l0} to adjust a second difference ΔV_{l0} between the first lower bias voltage V_{l0} and the first lower threshold voltage $V_{t_{l0}}$; and

Step 240: adjusting a second upper bias voltage V_{u1} applied to the second upper dummy word line IDMY_{u1} and/or a second upper threshold voltage $V_{t_{u1}}$ of the second upper dummy word line IDMY_{u1} to adjust a fourth difference ΔV_{u1} between the second upper bias voltage V_{u1} and the second upper threshold voltage $V_{t_{u1}}$.

FIG.6 is merely an example, and the steps in FIG.6 may be performed in any sequence. For example, Step 220 or Step 240 may be performed before Step 210. The steps may be performed concurrently.

ΔV_{u0} and ΔV_{l0} in Step 210 and 220 may be expressed as the equations (eq-1) and (eq-2) above. ΔV_{u1} in Step 240 may be expressed as the following equation.

$$\Delta V_{u1} = V_{u1} - V_{t_{u1}} \dots (\text{eq-4}).$$

As described in Step 210, Step 220 and Step 230, the first difference ΔV_{u0} , the second difference ΔV_{l0} and the fourth difference ΔV_{u1} may be adjusted as below to reduce program disturbance.

When programming a word line of the upper deck 110, the first difference ΔV_{u0} may be adjusted to be lower than a threshold TH5, the second difference ΔV_{l0} may be adjusted to be lower than the threshold TH5, and the fourth difference ΔV_{u1} may be adjusted to be higher than the threshold TH5. In other words, after the adjustment, $\Delta V_{u0} = V_{u0} - V_{t_{u0}} < \text{TH5}$, $\Delta V_{l0} = V_{l0} - V_{t_{l0}} < \text{TH5}$, and $\Delta V_{u1} = V_{u1} - V_{t_{u1}} > \text{TH5}$. For example, the threshold TH5 may be 7 volts.

In addition, according to an embodiment, a condition (c-2) may also have to be met for reducing program disturbance of the memory 100 of FIG.5.

The condition (c-2) may include that a difference between the fourth difference ΔV_{u1} and the first difference ΔV_{u0} may be within a predetermined range, and another difference between the fourth difference ΔV_{u1} and the second difference ΔV_{l0} may be within the predetermined range.

The predetermined range related to the condition (c-2) may be within a level L3 and a level L4 higher than the level L3. Hence, in other words, the condition (c-2) may be expressed as $L3 < (\Delta V_{u1} - \Delta V_{u0}) < L4$, and $L3 < (\Delta V_{u1} - \Delta V_{l0}) < L4$. For example, the level L3 may be 3 volts, and the level L4 may be 7 volts.

Regarding FIG.5, the equations and inequalities related to the differences ΔV_{u0} , ΔV_{l0} and ΔV_{u1} mentioned above may be applied when programming a word line of the upper deck 110.

When programming a word line of the lower deck 120, the differences ΔV_{u0} , ΔV_{l0} and ΔV_{u1} may not be limited; however, according to experiments, the differences ΔV_{u0} , ΔV_{l0} and ΔV_{u1} may be higher than a threshold such as 3 volts.

FIG.7 illustrates the memory 100 according to another embodiment. The structure shown in FIG.7 may be similar to that shown in FIG.1. Compared with FIG.1, in FIG.7, the upper deck 110 may further include the second upper dummy word line IDMY_u1, and the lower deck 120 may further include the second lower dummy word line IDMY_l1.

FIG.8 is a flowchart of a method 800 for reducing program disturbance of the memory 100 of FIG.7. The method 800 may include following steps.

Step 210: adjust a first upper bias voltage V_{u0} applied to the first upper dummy word line IDMY_u0 and/or a first upper threshold voltage V_{t_u0} of the first upper dummy word line IDMY_u0 to adjust a first difference ΔV_{u0} between the first upper bias voltage V_{u0} and the first upper threshold voltage V_{t_u0} ;

Step 220: adjust a first lower bias voltage V_{l0} applied to the first lower dummy word line IDMY_l0 and/or a first lower threshold voltage V_{t_l0} of the first lower dummy word line IDMY_l0 to adjust a second difference ΔV_{l0} between the first lower bias voltage V_{l0} and the first lower threshold voltage V_{t_l0} ;

Step 230: adjusting a second lower bias voltage V_{l1} applied to the second lower dummy word line IDMY_l1 and/or a second lower threshold voltage V_{t_l1} of the second lower dummy word line IDMY_l1 to adjust a third difference ΔV_{l1} between the second lower bias voltage V_{l1} and the second lower threshold voltage V_{t_l1} ; and

Step 240: adjusting a second upper bias voltage V_{u1} applied to the second upper dummy word line IDMY_u1 and/or a second upper threshold voltage V_{t_u1} of the second upper dummy word line IDMY_u1 to adjust a fourth difference ΔV_{u1} between the second upper bias voltage V_{u1} and the second upper threshold voltage V_{t_u1} .

FIG.8 is merely an example, and the steps in FIG.8 may be performed in any sequence. For example, Step 220, Step 230 or Step 240 may be performed before Step 210. The steps may be performed concurrently.

ΔV_{u0} , ΔV_{l0} , ΔV_{l1} and ΔV_{u1} in Step 210 to Step 240 may be expressed as the equations (eq-1) to (eq-4) described above.

As described in Step 210 to Step 240, the first difference ΔV_{u0} , the second difference

ΔV_{10} , the third difference ΔV_{11} and the fourth difference ΔV_{u1} may be adjusted as below to reduce program disturbance.

When programming a word line of the upper deck 110, the first difference ΔV_{u0} may be adjusted to be lower than a threshold TH11. The second difference ΔV_{10} may be adjusted to be lower than a second threshold TH12. The third difference ΔV_{11} may be adjusted to be lower than the first threshold TH11. The fourth difference ΔV_{u1} may be adjusted to be higher than the second threshold TH12. In other words, after the adjustment, $\Delta V_{u0} = V_{u0} - V_{t_{u0}} < TH11$, $\Delta V_{10} = V_{10} - V_{t_{10}} < TH12$, $\Delta V_{11} = V_{11} - V_{t_{11}} < TH11$, and $\Delta V_{u1} = V_{u1} - V_{t_{u1}} > TH12$. For example, the first threshold TH11 may be 11 volts, and the second threshold TH12 may be 7 volts.

In addition, according to an embodiment, one of a condition (c-3) and a condition (c-4) may also have to be met for reducing program disturbance of the memory 100 of FIG.7.

The condition (c-3) may include that a difference between the fourth difference ΔV_{u1} and the first difference ΔV_{u0} may be within a predetermined range, and another difference between the fourth difference ΔV_{u1} and the second difference ΔV_{10} may be within the predetermined range.

The predetermined range related to the condition (c-3) may be within a level L5 and a level L6 higher than the level L5. Hence, in other words, the condition (c-3) may be expressed as $L5 < (\Delta V_{u1} - \Delta V_{u0}) < L6$, and $L5 < (\Delta V_{u1} - \Delta V_{10}) < L6$. For example, the level L5 may be 3 volts, and the level L6 may be 7 volts.

The condition (c-4) may include that a difference between the fourth difference ΔV_{u1} and the second difference ΔV_{10} may be within a predetermined range, and another difference between the fourth difference ΔV_{u1} and the third difference ΔV_{11} may be within the predetermined range.

The predetermined range related to the condition (c-4) may be within a level L7 and a level L8 higher than the level L7. Hence, in other words, the condition (c-4) may be expressed as $L7 < (\Delta V_{u1} - \Delta V_{10}) < L8$, and $L7 < (\Delta V_{u1} - \Delta V_{11}) < L8$. For example, the level L7 may be 3 volts, and the level L8 may be 7 volts.

Regarding FIG.7, the equations and inequalities related to the differences ΔV_{u0} , ΔV_{10} , ΔV_{11} and ΔV_{u1} mentioned above may be applied when programming a word line of the upper deck 110.

When programming a word line of the lower deck 120, the differences ΔV_{u0} , ΔV_{10} , ΔV_{11} and ΔV_{u1} may not be limited; however, according to experiments, the differences ΔV_{u0} , ΔV_{10} , ΔV_{11} and ΔV_{u1} may be higher than a threshold such as 3 volts.

FIG.9 is a waveform of controlling the memory 100 of FIG.7. According to an embodiment, the memory 100 may further include a top select gate electrode (denoted as TSG), a select word line (denoted as Sel_WL), an unselect word line (denoted as Unsel_WL), a dummy word line (denoted as Dummy_WL), a select bit line (denoted as Sel_BL) and a bottom select gate electrode (denoted as BSG) used for controlling both of the upper deck 110 and the lower deck 120.

As shown in FIG.9, before a program operation, a pre-pulse operation may be performed. The pre-pulse operation may be performed to avoid failure of the program operation.

As shown in FIG.9, before the pre-pulse operation, 0 volts may be applied to the select word line (Sel_WL), the dummy word line (Dummy_WL), the select bit line (Sel_BL) and the bottom select gate electrode (BSG). The first upper bias voltage V_{u0} , the first lower bias voltage V_{l0} , the second lower bias voltage V_{l1} and the second upper bias voltage V_{u1} may be set as 0 volts.

The first upper bias voltage V_{u0} , the first lower bias voltage V_{l0} , the second lower bias voltage V_{l1} and the second upper bias voltage V_{u1} may be set to a pre-pulse level V_p during the pre-pulse operation. Then, the first upper bias voltage V_{u0} , the first lower bias voltage V_{l0} , the second lower bias voltage V_{l1} and the second upper bias voltage V_{u1} may be set to a program level V_{pass} during the program operation.

During the program operation, a voltage of the program level V_{pass} may be applied to the unselect word line (Unsel_WL) and the dummy word line (Dummy_WL). A voltage applied to the select word line (Sel_WL) may be increased to a level V_{pgm} .

As shown in FIG.9, during the program operation, 0 volts may be applied to the top select gate electrode (TSG) and the bottom select gate electrode (BSG). After the program operation, the select word line (Sel_WL), the unselect word line (Unsel_WL), the dummy word line (Dummy_WL), the select bit line (Sel_BL) and the bias voltages V_{u0} , V_{l0} , V_{l1} and V_{u1} may be set as floating.

In FIG.9, the pre-pulse level V_p may be higher than a maximum allowable level V_{t_max} of the first upper threshold voltage V_{t_u0} , the first lower threshold voltage V_{t_l0} , the second lower threshold voltage V_{t_l1} and the second upper threshold voltage V_{t_u1} .

As FIG.9, the bias voltages V_{u0} , V_{l0} , V_{l1} and V_{u1} may be supplied by the same voltage source to reduce the number of voltage sources.

FIG.10 is a waveform of controlling the memory 100 of FIG.7 according to another embodiment. FIG.10 may be similar to FIG.9. The similarities of FIG.10 and FIG.9 are not described repeatedly.

As FIG.9, in FIG.10, a pre-pulse operation may be performed before a program operation.

During the pre-pulse operation, the first upper bias voltage V_{u0} , the first lower bias voltage V_{l0} , the second lower bias voltage V_{l1} , and the second upper bias voltage V_{u1} may be set to a first pre-pulse level V_{p1} , a second pre-pulse level V_{p2} , a third pre-pulse level V_{p3} and a fourth pre-pulse level V_{p4} respectively.

During the program operation, the first upper bias voltage V_{u0} , the first lower bias voltage V_{l0} , the second lower bias voltage V_{l1} , and the second upper bias voltage V_{u1} may be set to a first program level V_{pass1} , a second program level V_{pass2} , a third program level V_{pass3} and a fourth program level V_{pass4} respectively.

In FIG.10, each of the first pre-pulse level V_{p1} , the second pre-pulse level V_{p2} , the third pre-pulse level V_{p3} and the fourth pre-pulse level V_{p4} may be higher than a maximum allowable level V_{t_max} of the first upper threshold voltage V_{t_u0} , the first lower threshold voltage V_{t_l0} , the second lower threshold voltage V_{t_l1} and the second upper threshold voltage V_{t_u1} .

In FIG.10, the bias voltages V_{u0} , V_{l0} , V_{l1} and V_{u1} may be supplied separately for better controllability and flexibility.

The waveforms in FIG.9 and FIG.10 may be applied when programming a word line of the lower deck 120. When programming a word line of the upper deck 110, the bias voltages V_{u0} , V_{l0} , V_{l1} and V_{u1} may be 0 volts during the pre-pulse operation.

FIG.11 to FIG. 14 illustrate a memory 1100 according to different embodiments. Like the memory 100 described above, the memory 1100 may include an upper deck 110 and a lower deck 120. However, the memory 1100 may not include the joint oxide layer 155 shown in FIG.1. Compared with the memory 100, program disturbance may be more severe when programming the memory 1100.

FIG.11 to FIG.14 may be similar to FIG.1, FIG.3, FIG.5 and FIG.7 respectively.

The equations and inequalities corresponding to FIG.1, FIG.3, FIG.5 and FIG.7 described above may be respectively applied to the cases of FIG.11 to FIG.14 for reducing program disturbance. The equations and inequalities are not described repeatedly.

In summary, by adjusting the bias voltage(s) and the threshold voltage(s) related to dummy word lines (e.g. IDMY_u0, IDMY_l0, IDMY_l1 and IDMY_u1 mentioned above) in a three-dimensional memory, program disturbance may be reduced. According to embodiments, program disturbance occurred when programming a word line of an upper deck may be better reduced. Hence, the problem in the field may be reduced.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Claims**What is claimed is:**

1. A method for reducing program disturbance of a memory, the memory comprising an upper deck and a lower deck, the upper deck being formed above the lower deck, the upper deck comprising a first upper dummy word line, the lower deck comprising a first lower dummy word line, the method comprising:
adjusting a first upper bias voltage applied to the first upper dummy word line and/or a first upper threshold voltage of the first upper dummy word line to adjust a first difference between the first upper bias voltage and the first upper threshold voltage;
and
adjusting a first lower bias voltage applied to the first lower dummy word line and/or a first lower threshold voltage of the first lower dummy word line to adjust a second difference between the first lower bias voltage and the first lower threshold voltage.
2. The method of claim 1, wherein:
the first difference is adjusted to be lower than a threshold; and
the second difference is adjusted to be lower than the threshold.
3. The method of claim 1, wherein:
the first difference is adjusted to be higher than a threshold; and
the second difference is adjusted to be higher than the threshold.
4. The method of claim 1, wherein the lower deck further comprises a second lower dummy word line, and the method further comprising:
adjusting a second lower bias voltage applied to the second lower dummy word line and/or a second lower threshold voltage of the second lower dummy word line to adjust a third difference between the second lower bias voltage and the second lower threshold voltage.
5. The method of claim 4, wherein:
the first difference is adjusted to be higher than a threshold;
the second difference is adjusted to be lower than the threshold; and
the third difference is adjusted to be lower than the threshold.

6. The method of claim 4, wherein a difference between the first difference and the second difference is within a predetermined range, and another difference between the first difference and the third difference is within the predetermined range.
7. The method of claim 1, wherein the upper deck further comprises a second upper dummy word line, and the method further comprising:
adjusting a second upper bias voltage applied to the second upper dummy word line and/or a second upper threshold voltage of the second upper dummy word line to adjust a fourth difference between the second upper bias voltage and the second upper threshold voltage.
8. The method of claim 7, wherein:
the first difference is adjusted to be lower than a threshold;
the second difference is adjusted to be lower than the threshold; and
the fourth difference is adjusted to be higher than the threshold.
9. The method of claim 8, wherein a difference between the fourth difference and the first difference is within a predetermined range, and another difference between the fourth difference and the second difference is within the predetermined range.
10. The method of claim 1, wherein the upper deck further comprises a second upper dummy word line, the lower deck further comprises a second lower dummy word line, and the method further comprising:
adjusting a second lower bias voltage applied to the second lower dummy word line and/or a second lower threshold voltage of the second lower dummy word line to adjust a third difference between the second lower bias voltage and the second lower threshold voltage; and
adjusting a second upper bias voltage applied to the second upper dummy word line and/or a second upper threshold voltage of the second upper dummy word line to adjust a fourth difference between the second upper bias voltage and the second upper threshold voltage.
11. The method of claim 10, wherein:
the first difference is adjusted to be lower than a first threshold;

the second difference is adjusted to be lower than a second threshold;
the third difference is adjusted to be lower than the first threshold; and
the fourth difference is adjusted to be higher than the second threshold.

12. The method of claim 10, wherein a difference between the fourth difference and the first difference is within a predetermined range, and another difference between the fourth difference and the second difference is within the predetermined range.
13. The method of claim 10, wherein a difference between the fourth difference and the second difference is within a predetermined range, and another difference between the fourth difference and the third difference is within the predetermined range.
14. The method of claim 10, further comprising:
setting the first upper bias voltage, the first lower bias voltage, the second lower bias voltage and the second upper bias voltage to a pre-pulse level during a pre-pulse operation; and
setting the first upper bias voltage, the first lower bias voltage, the second lower bias voltage and the second upper bias voltage to a program level during a program operation;
wherein and the pre-pulse level is higher than a maximum allowable level of the first upper threshold voltage, the first lower threshold voltage, the second lower threshold voltage and the second upper threshold voltage.
15. The method of claim 10, further comprising:
setting the first upper bias voltage, the first lower bias voltage, the second lower bias voltage, and the second upper bias voltage to a first pre-pulse level, a second pre-pulse level, a third pre-pulse level and a fourth pre-pulse level respectively during a pre-pulse operation; and
setting the first upper bias voltage, the first lower bias voltage, the second lower bias voltage, and the second upper bias voltage to a first program level, a second program level, a third program level and a fourth program level respectively during a program operation;
wherein each of the first pre-pulse level, the second pre-pulse level, the third pre-pulse

level and the fourth pre-pulse level is higher than a maximum allowable level of the first upper threshold voltage, the first lower threshold voltage, the second lower threshold voltage and the second upper threshold voltage.

16. A memory for reducing program disturbance, comprising:
 - an upper deck comprising a first upper dummy word line configured to receive a first upper bias voltage and have a first upper threshold voltage; and
 - an lower deck comprising a first lower dummy word line configured to receive a first lower bias voltage and have a first lower threshold voltage;wherein the upper deck is formed above the lower deck, the first upper bias voltage and/or the first upper threshold voltage is adjusted to adjust a first difference between the first upper bias voltage and the first upper threshold voltage, and the first lower bias voltage and/or the first lower threshold voltage is adjusted to adjust a second difference between the first lower bias voltage and the first lower threshold voltage.
17. The memory of claim 16, wherein the lower deck further comprises a second lower dummy word line configured to receive a second lower bias voltage and have a second lower threshold voltage, and the second lower bias voltage and/or the second lower threshold voltage is adjusted to adjust a third difference between the second lower bias voltage and the second lower threshold voltage.
18. The memory of claim 16, wherein the upper deck further comprises a second upper dummy word line configured to receive a second upper bias voltage and have a second upper threshold voltage, and the second upper bias voltage and/or the second upper threshold voltage is adjusted to adjust a fourth difference between the second upper bias voltage and the second upper threshold voltage.
19. The memory of claim 16, further comprising a joint oxide layer formed between the upper deck and the lower deck.
20. The memory of claim 16, further comprising a select top gate electrode, a select word line, an unselect word line, a dummy word line, a select bit line and a bottom select gate electrode.

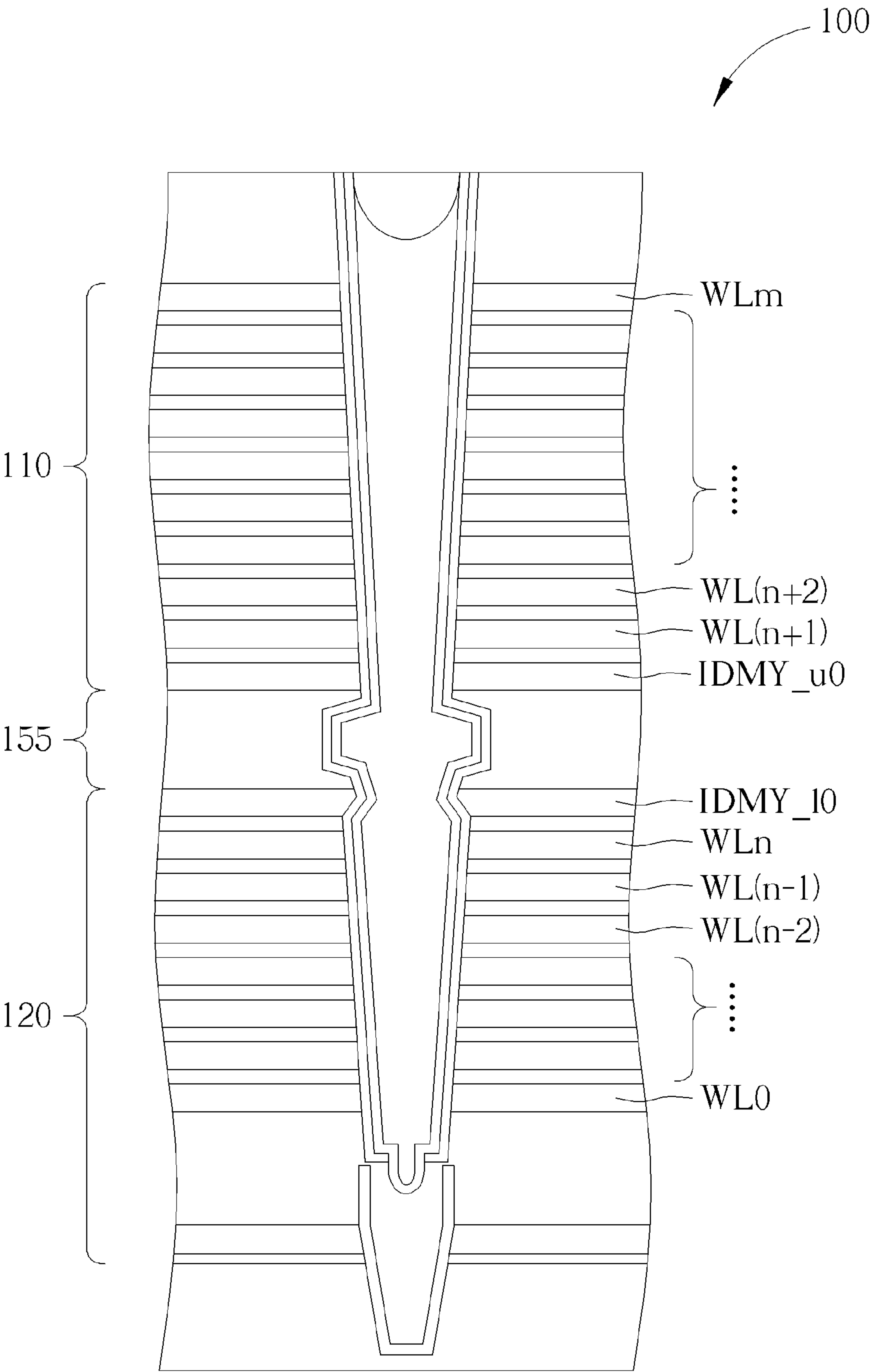


FIG. 1

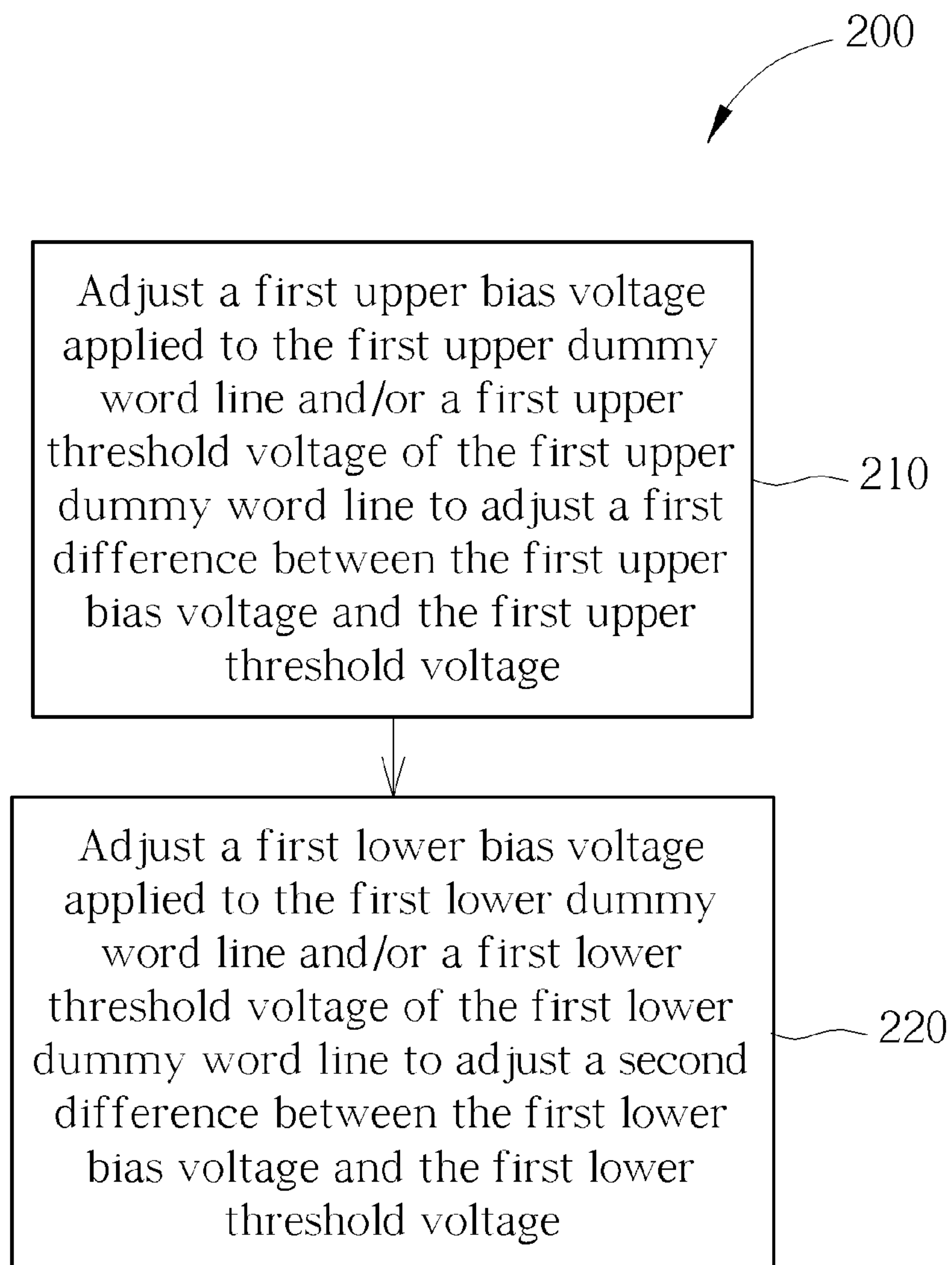


FIG. 2

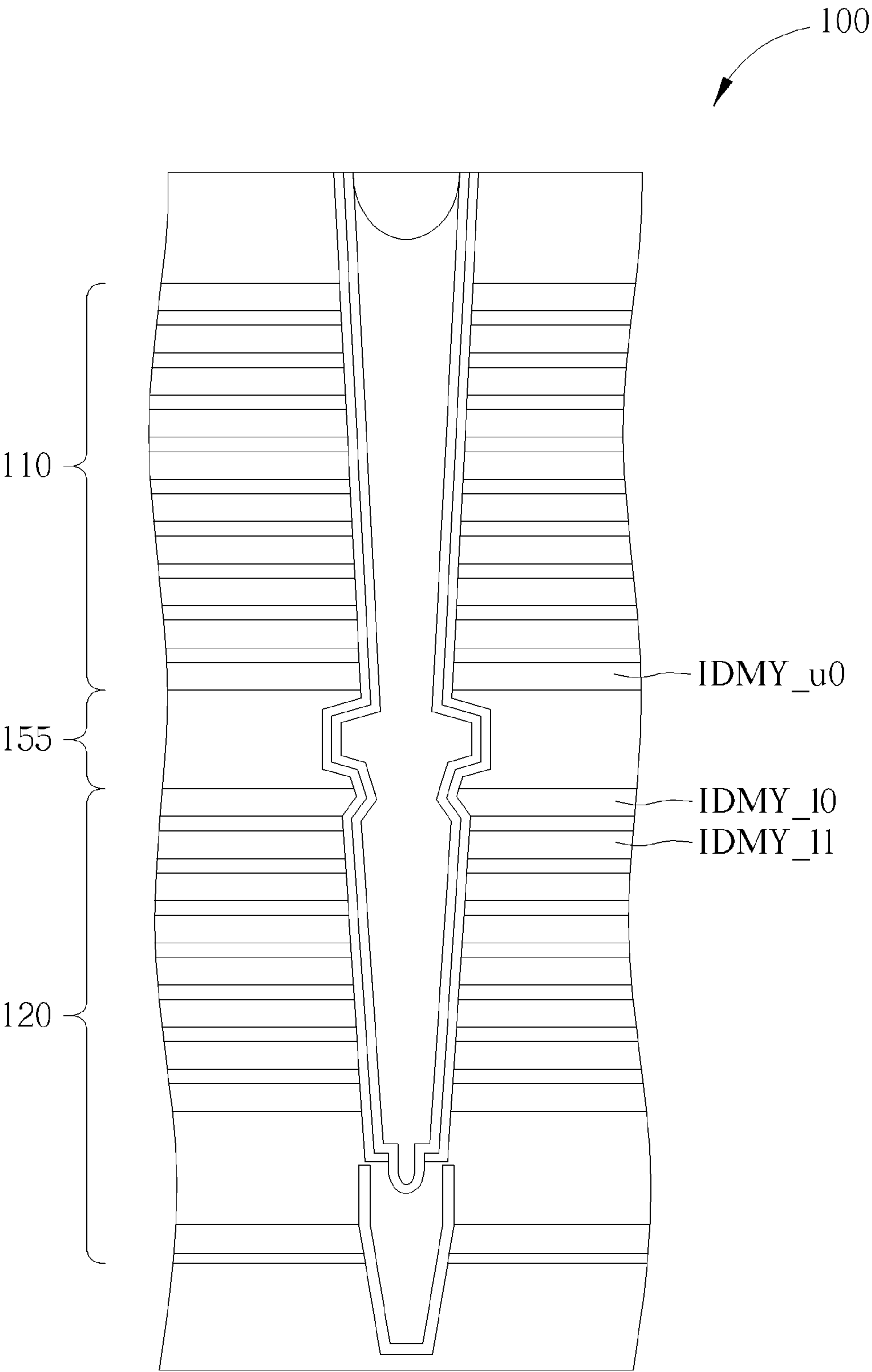


FIG. 3

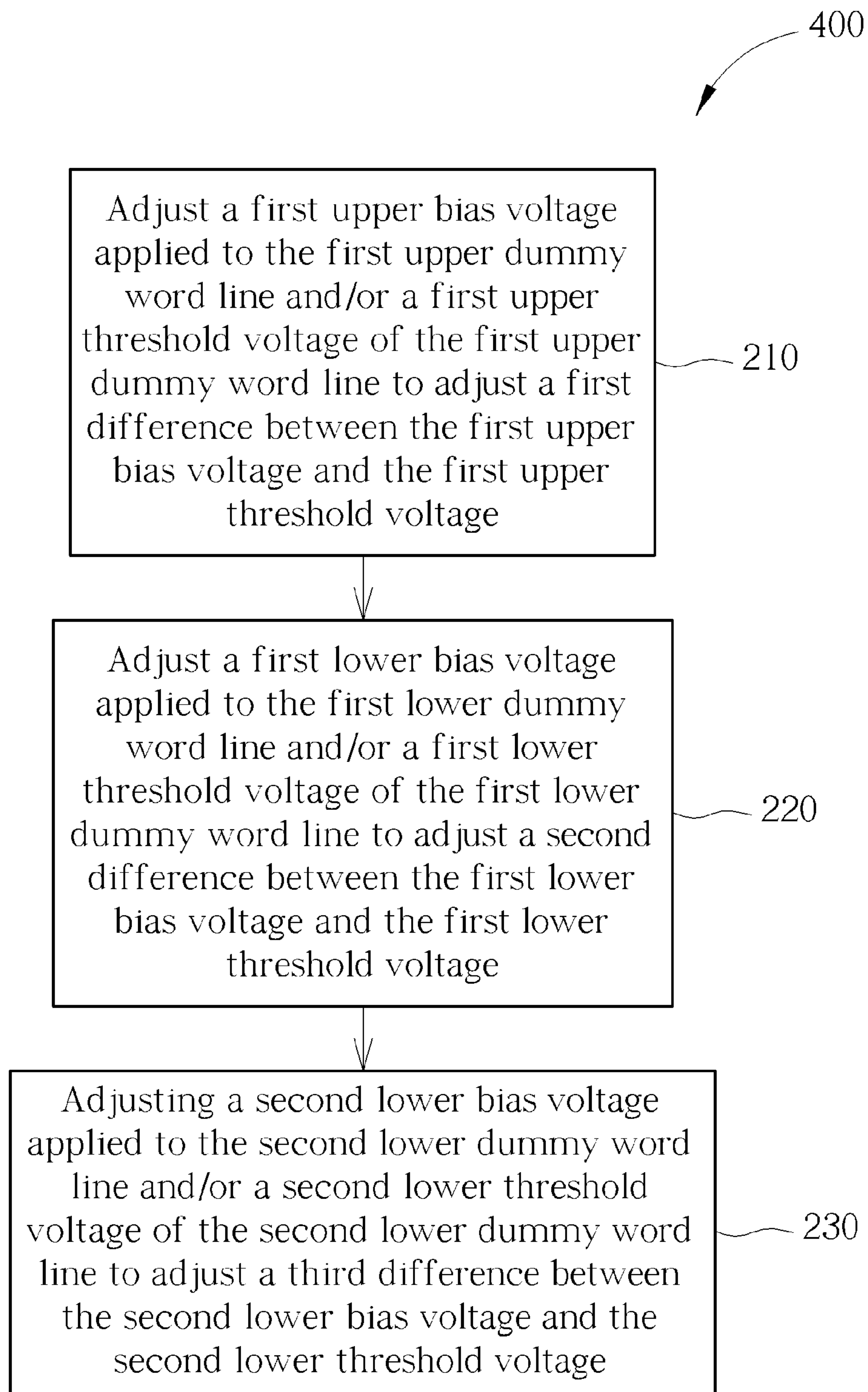


FIG. 4

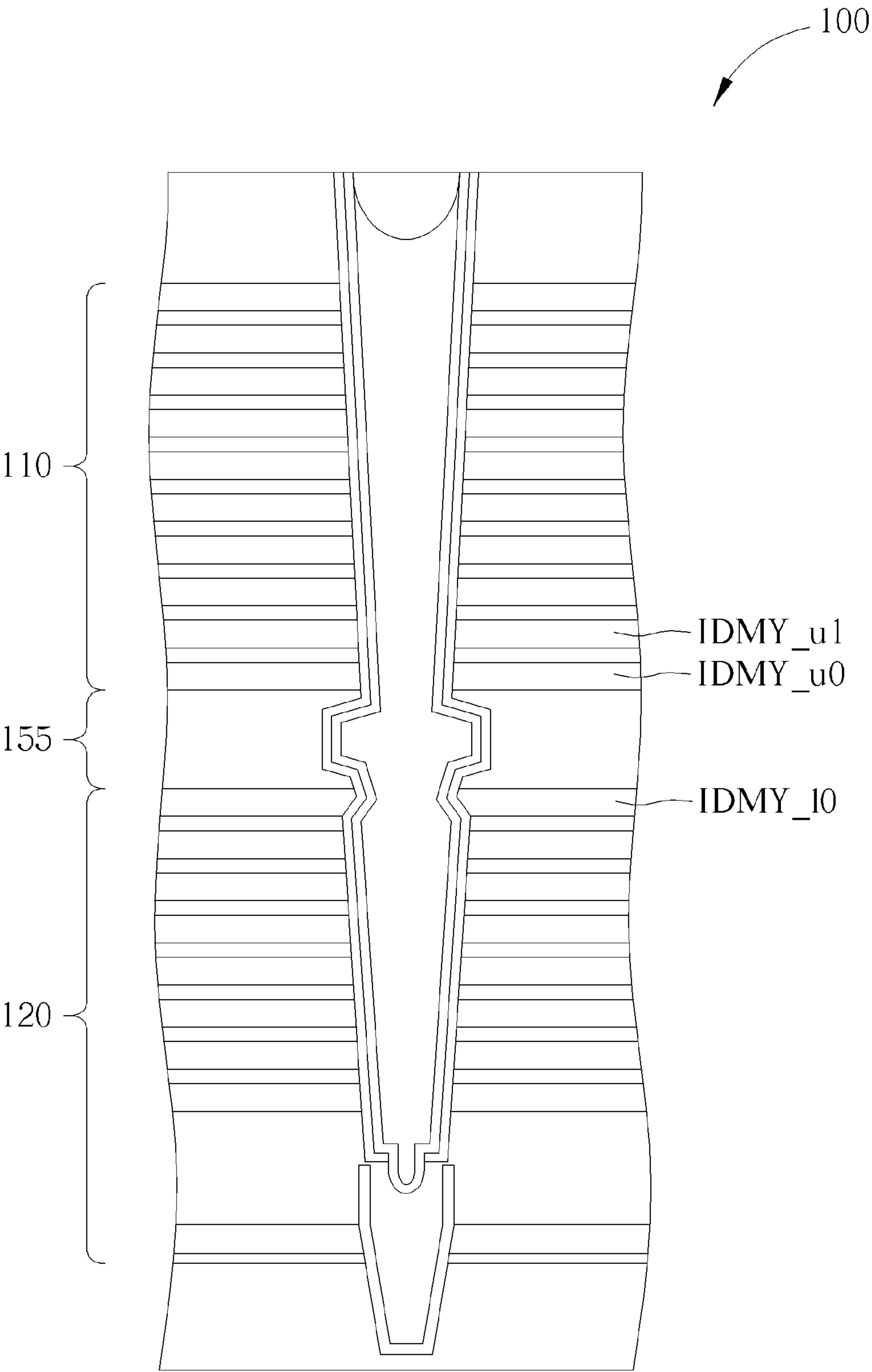


FIG. 5

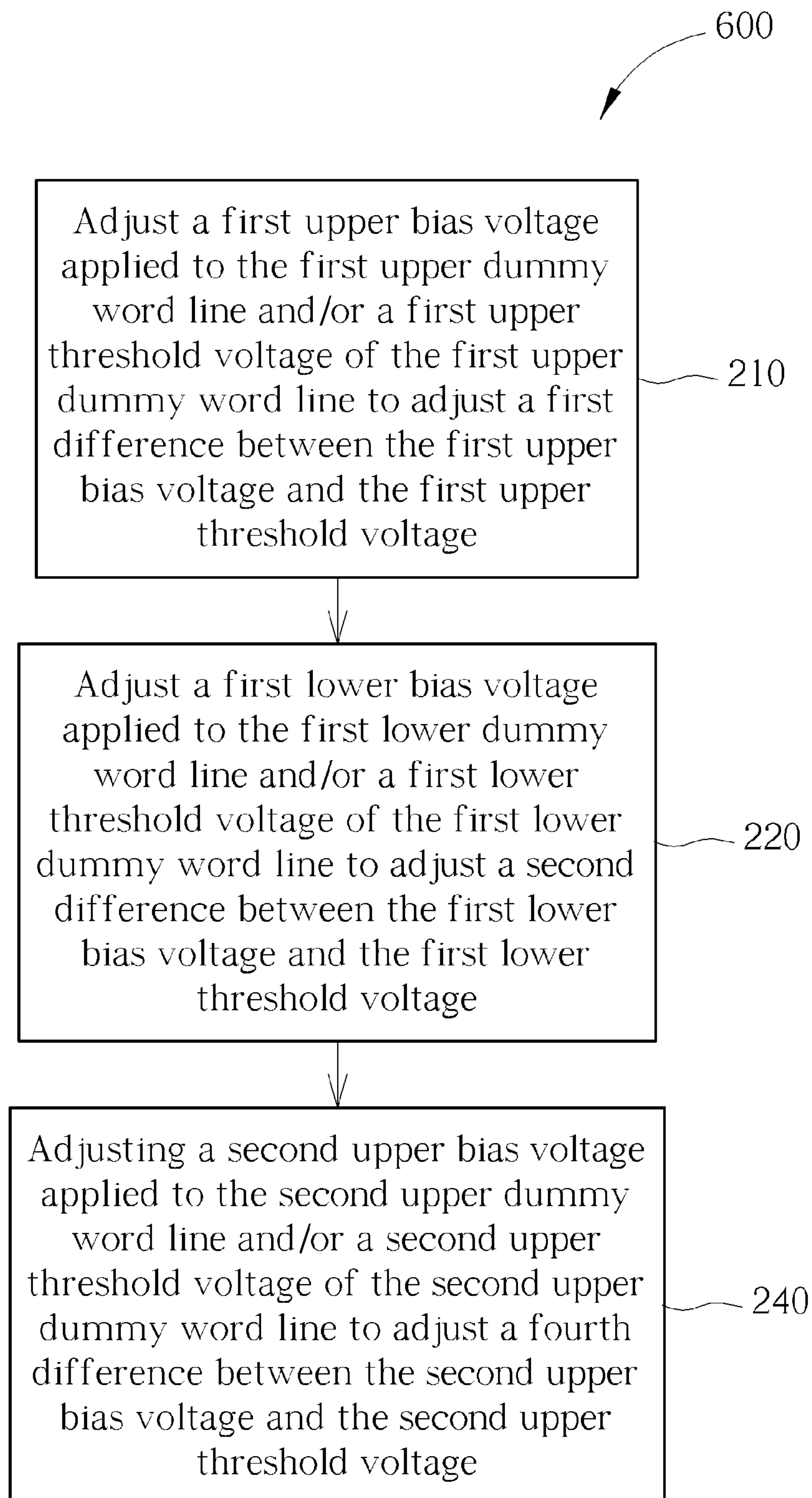


FIG. 6

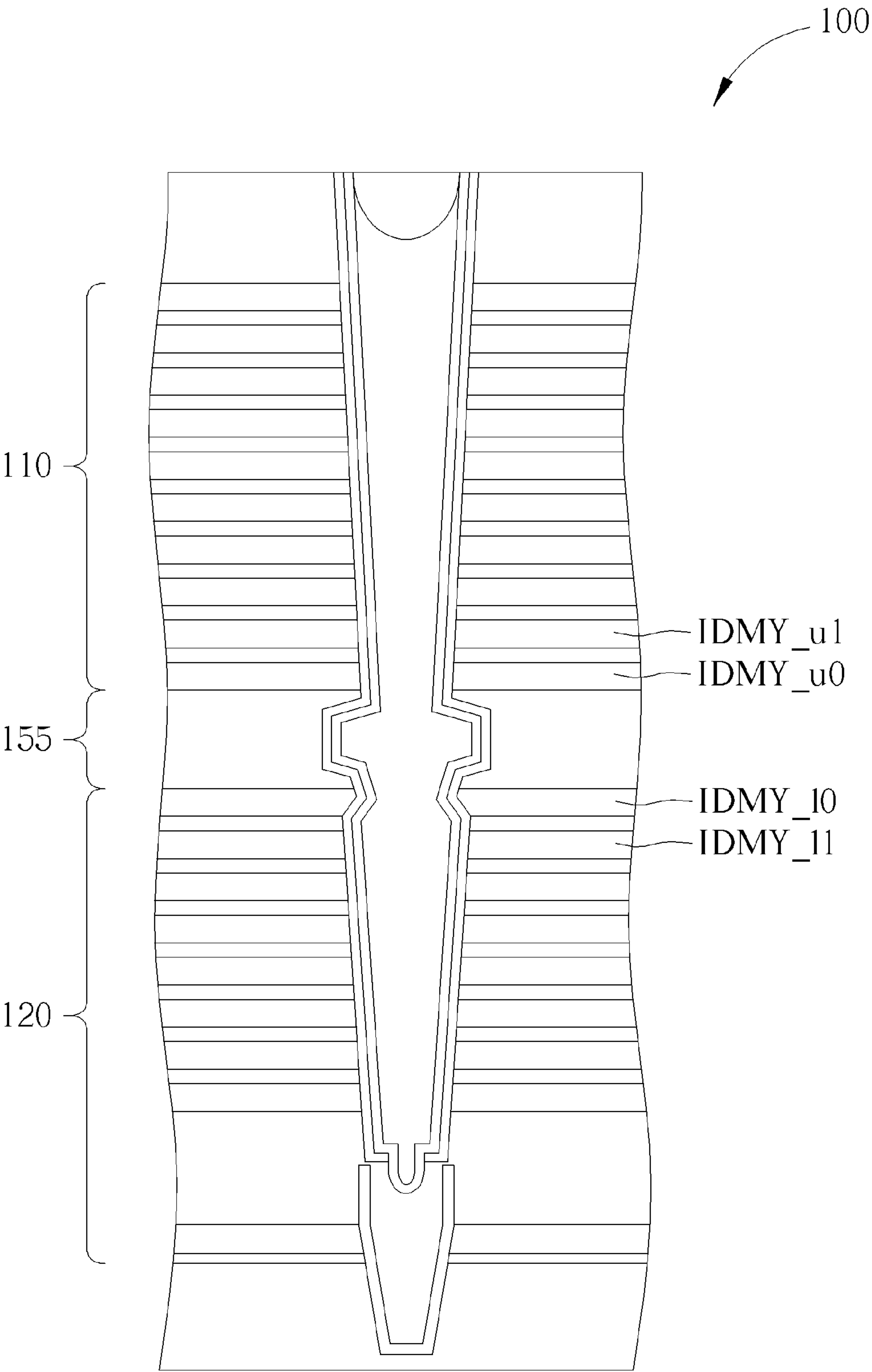


FIG. 7

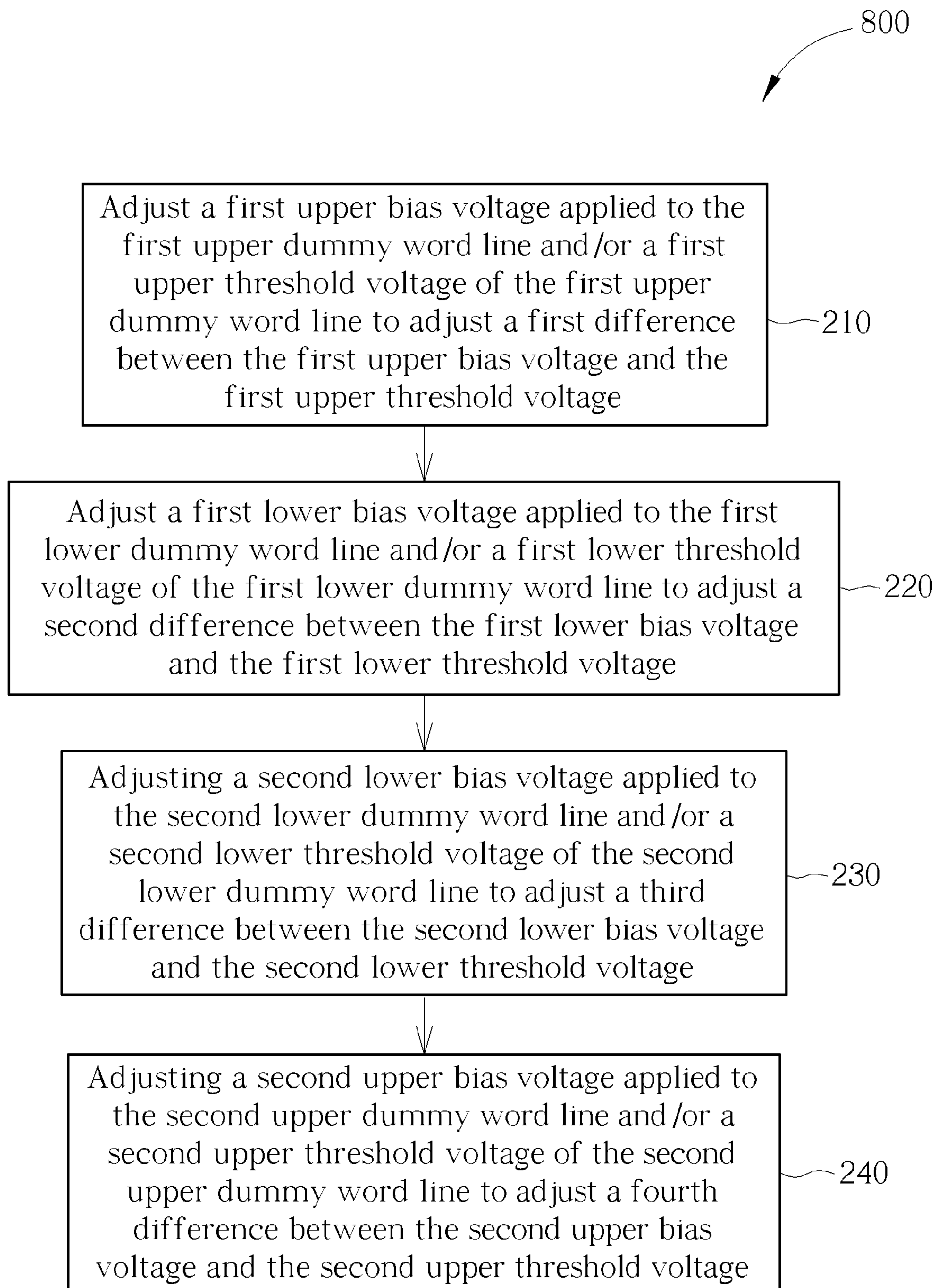


FIG. 8

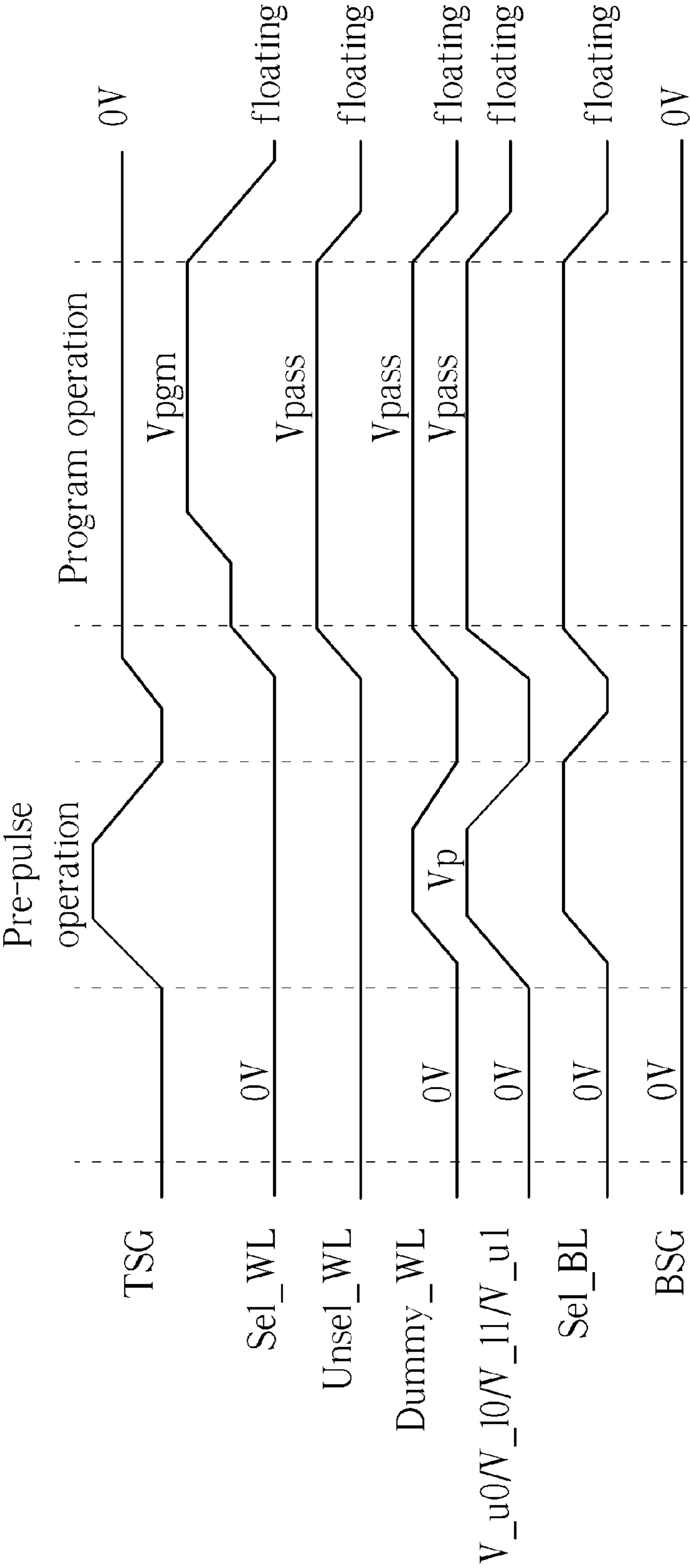


FIG. 9

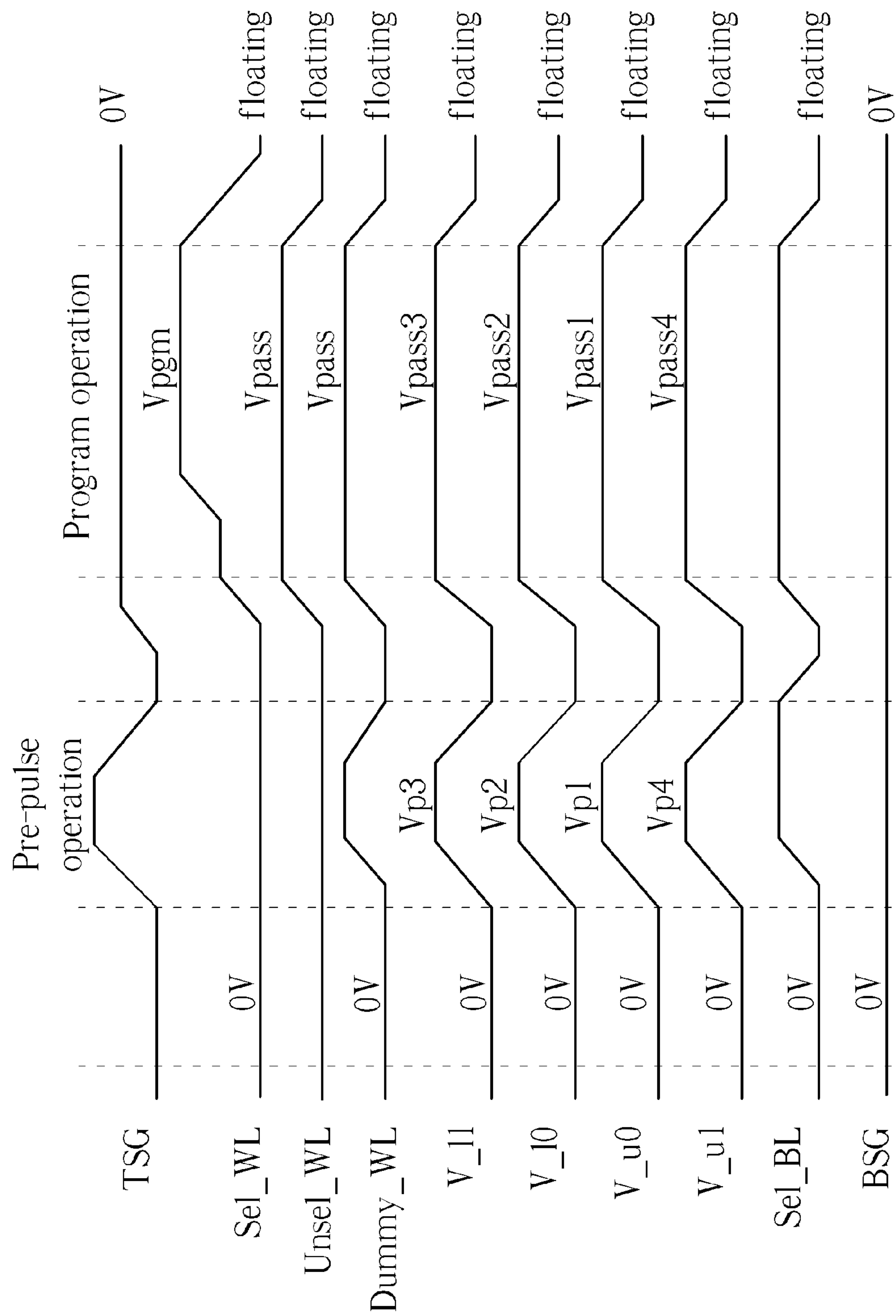


FIG. 10

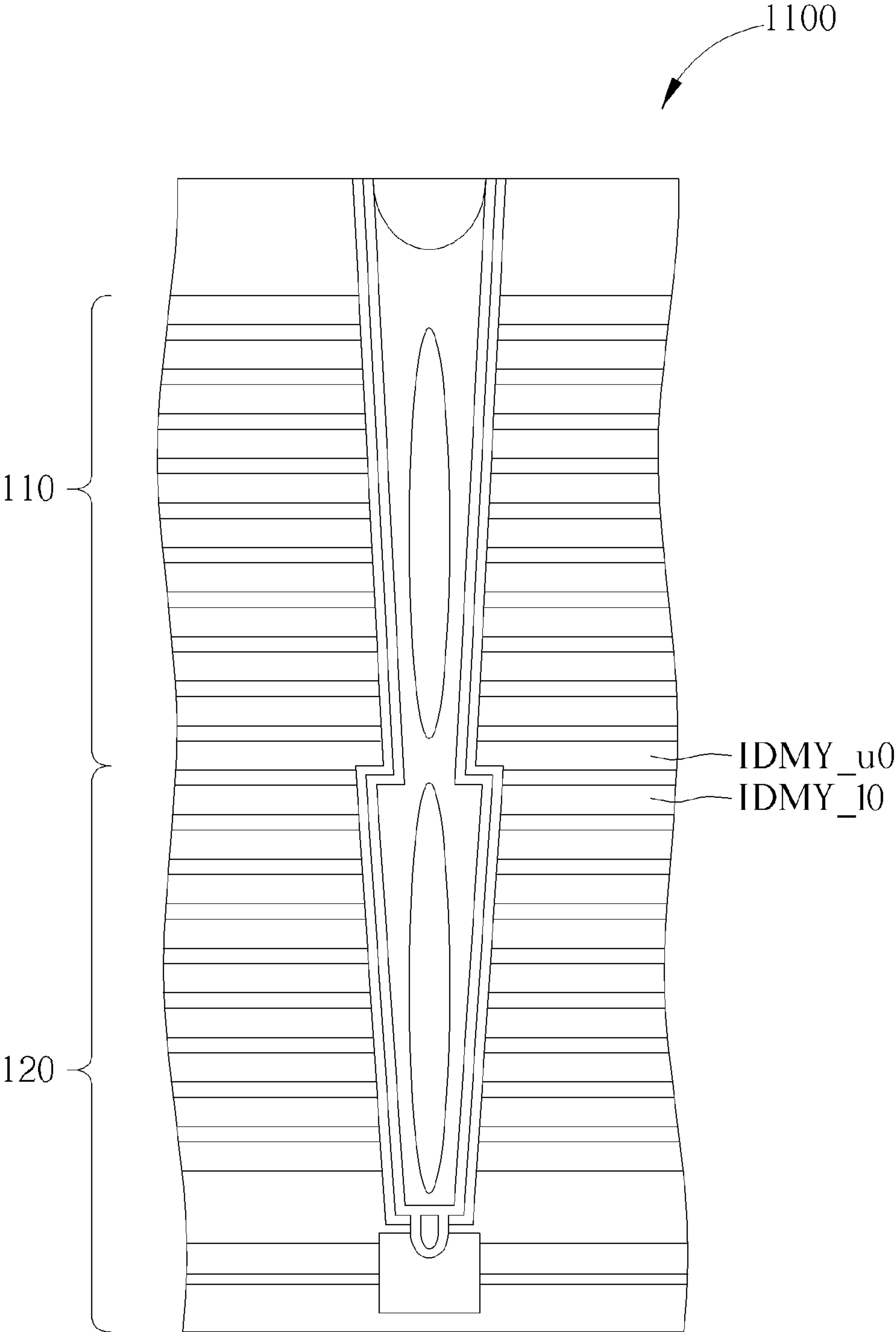


FIG. 11

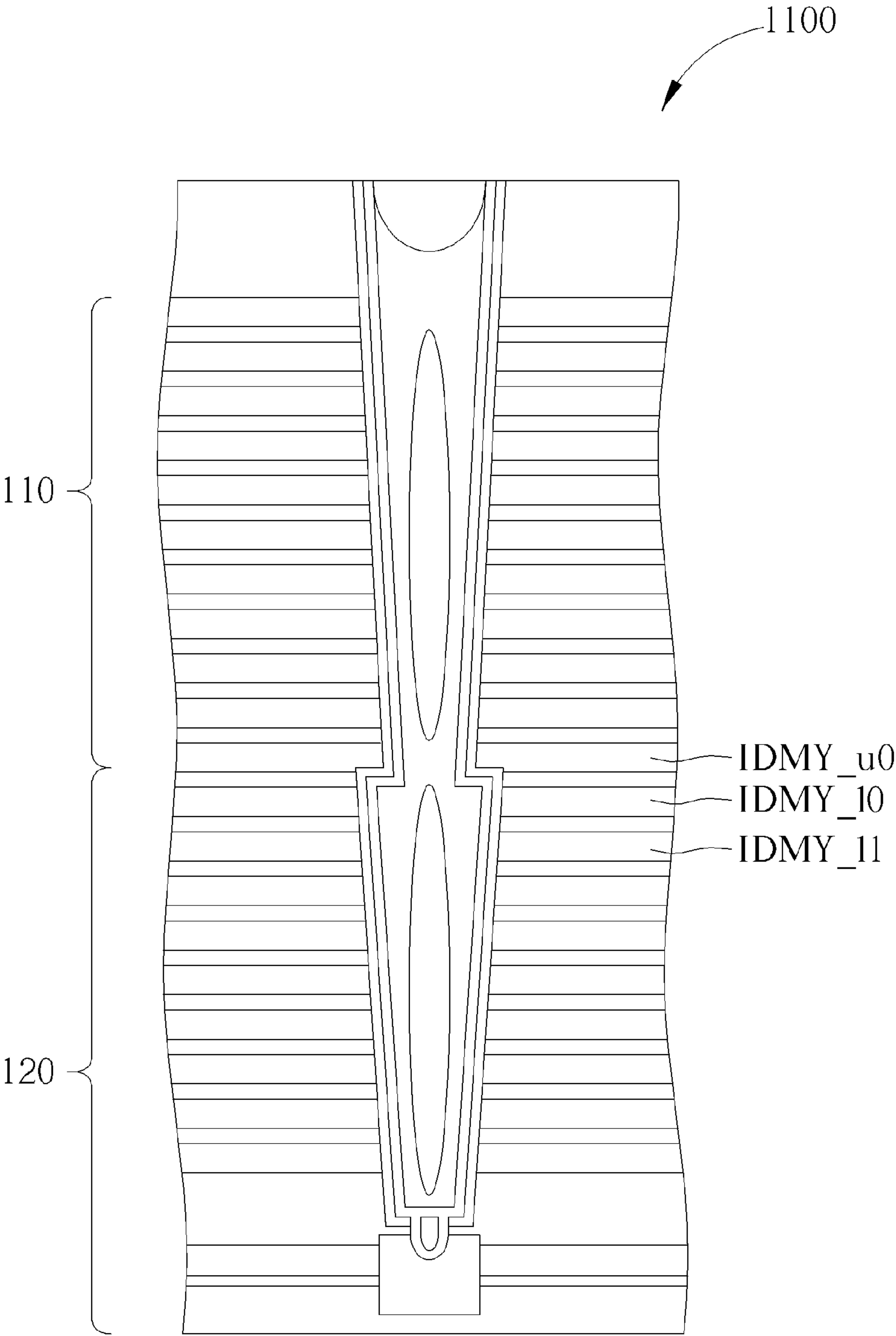


FIG. 12

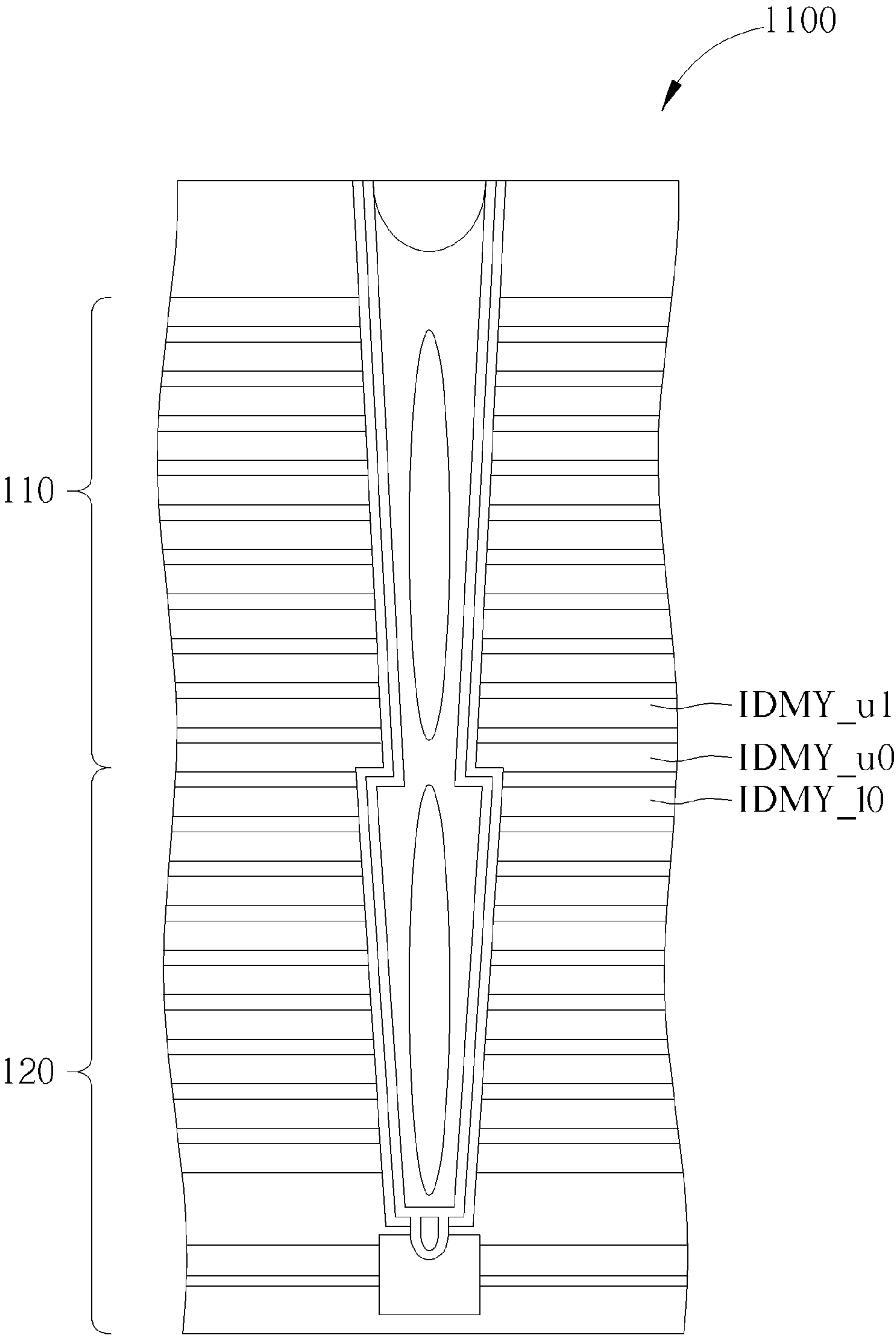


FIG. 13

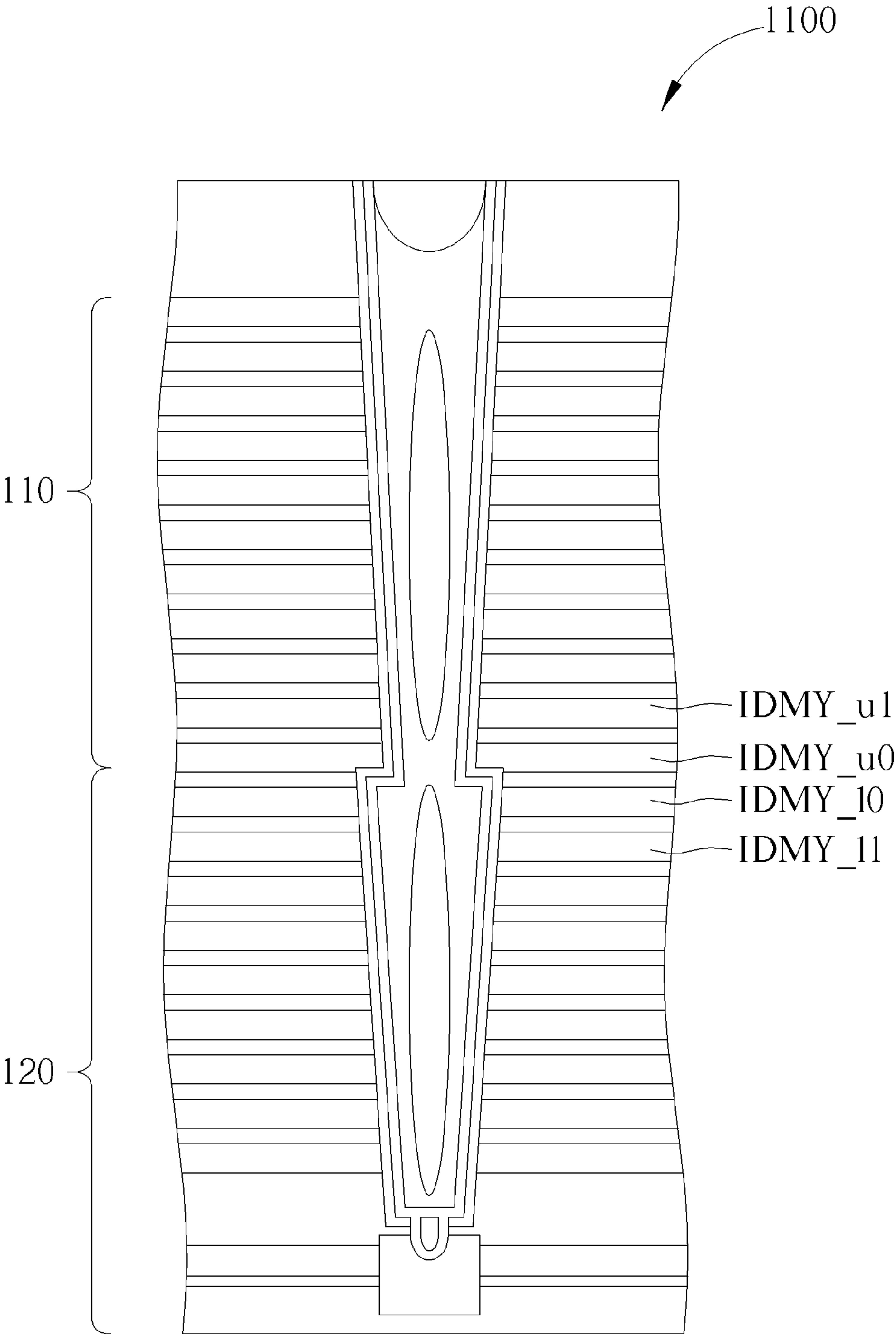


FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/123978

A. CLASSIFICATION OF SUBJECT MATTER

G11C 16/34(2006.01)i; G11C 16/08(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C

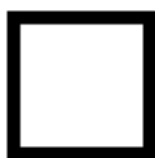
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, WPI, EPODOC: memory, 3D, three 1w dimensional, disturb, interference, program+, dummy, line, word, gate, bias, erase, voltage, writ+, threshold, difference

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2018358102 A1 (SANDISK TECHNOLOGIES LLC) 13 December 2018 (2018-12-13) description, paragraphs [0095]-[0099], [0121]-[0146], and figures 3A, 7A-9	1-20
A	WO 2017069869 A1 (SANDISK TECHNOLOGIES LLC) 27 April 2017 (2017-04-27) the whole document	1-20
A	US 2011222339 A1 (KIM, Sung-Hoon et al.) 15 September 2011 (2011-09-15) the whole document	1-20
A	US 2019279726 A1 (MACRONIX INTERNATIONAL CO., LTD.) 12 September 2019 (2019-09-12) the whole document	1-20
A	US 2017330631 A1 (SANDISK TECHNOLOGIES INC.) 16 November 2017 (2017-11-16) the whole document	1-20
A	CN 110211625 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 06 September 2019 (2019-09-06) the whole document	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“A” document defining the general state of the art which is not considered to be of particular relevance	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“E” earlier application or patent but published on or after the international filing date	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	“&” document member of the same patent family
“O” document referring to an oral disclosure, use, exhibition or other means	
“P” document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

19 August 2020

Date of mailing of the international search report

28 August 2020

Name and mailing address of the ISA/CN

National Intellectual Property Administration, PRC
6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing
100088
China

Authorized officer

LIU,Xuelian

Facsimile No. (86-10)62019451

Telephone No. (86-10)53961471

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2019/123978

Patent document cited in search report				Publication date (day/month/year)		Patent family member(s)		Publication date (day/month/year)	
US	2018358102	A1	13 December 2018	US	10297330	B2	21 May 2019		
				WO	2018226280	A1	13 December 2018		
WO	2017069869	A1	27 April 2017	CN	108028070	A	11 May 2018		
				JP	6531220	B2	12 June 2019		
				US	9460805	B1	04 October 2016		
				EP	3332407	A1	13 June 2018		
				JP	2018536959	A	13 December 2018		
US	2011222339	A1	15 September 2011	KR	20110102735	A	19 September 2011		
				US	8488386	B2	16 July 2013		
US	2019279726	A1	12 September 2019	US	10636496	B2	28 April 2020		
US	2017330631	A1	16 November 2017	WO	2017196424	A1	16 November 2017		
				US	9852803	B2	26 December 2017		
CN	110211625	A	06 September 2019	None					