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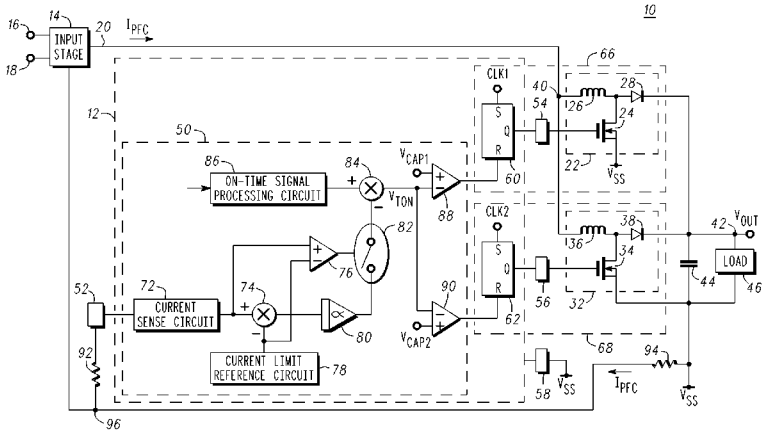
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(54) **Title**: METHOD FOR PROVIDING OVER CURRENT PROTECTION AND CIRCUIT

Fig. 1



(57) **Abstract**: A method and circuit for protecting against an over current condition. A conduction time of one or more transistors is reduced during the over current condition. The conduction time is reduced in an amount that is an increasing function of the amount of the over current. The conduction time may be reduced proportionally to the excess current.

WO 2010/126491 A1

METHOD FOR PROVIDING OVER CURRENT PROTECTION AND CIRCUIT

TECHNICAL FIELD

[0001] The present invention relates, in general, to power supplies and, more particularly, to interleaved power factor correction stages in power supplies.

BACKGROUND

[0002] Voltage regulators that provide AC/DC rectification typically include a full wave voltage rectifier stage, such as, for example, a diode bridge, a main Switch Mode Power Supply (SMPS) stage, and a Power Factor Correction (PFC) stage inserted between the line and the main SMPS. The SMPS provides regulation of an output waveform and the PFC stage draws a sinusoidal current from the line and provides Direct Current (DC) voltage to the main SMPS. Depending on the desired output power, the PFC stage may include a large inductor. However, large inductors are unsuitable for use in systems such as, for example, Liquid Crystal Display (LCD) television power supplies, in which it is desirable to use components having low profiles. To decrease the size of the magnetic components of a PFC stage and thereby lower their profile, manufacturers split the PFC stage into smaller parallel sub-stages that operate out of phase from each other. When the PFC stage is split into two parallel sub-stages they operate 180 degrees out of phase from each other. This configuration is referred to as being an interleaved PFC. Generally, the two PFC sub-stages operate in Critical Conduction Mode (CRM). Because the two PFC sub-stages are out-of-phase from each other, the total input current has the shape of a continuous conduction mode PFC which results in a lower input/output Root Mean Square (RMS) current and easier Electromagnetic Interference (EMI) filtering of the power supply.

[0003] In SMPS stages it is important to protect transistors such as power Metal Oxide Semiconductor Field Effect Transistors (MOSFETS) from over current conditions. This may be accomplished by comparing the current flowing through the power MOSFETS with a reference current. If the current is too high, the MOSFETS are turned

off. For an interleaved PFC stage, there are two current branches operating independently with a 180 degree phase shift, where each current branch is driven by a MOSFET. If there are two input/output pins, each current branch is associated with a corresponding input/output pin. If a current is too high in a current branch, the controller of the PFC turns off the MOSFET associated with that current branch. If there is a single current sense input/output pin, the current sensed is the total current flowing through both power MOSFETS. When the total current exceeds the reference limit, both MOSFETS are turned off at the same time. Because the two MOSFETs operate out of phase, the current may not be equally distributed between them at the moment the over current is detected. For example, one MOSFET may be conducting most of the current whereas the other MOSFET conducts almost zero current. Thus, during an over current event, one phase delivers all the power while the other phase provides almost none of the power. A disadvantage of this is that it leads to inefficient operation of the power supply, e.g., the power supply may have a longer startup time or poor current conduction.

[0004] Accordingly, it would be advantageous to have a circuit and method for protecting the MOSFETS from an over current event. It would of further advantage for the circuit and method to improve the current sharing of the PFC branches during an over current event.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present invention will be better understood from a reading of the following detailed description, taken in conjunction with the accompanying drawing figures, in which like reference characters designate like elements and in which:

[0006] FIG. 1 is a schematic diagram of a power factor correction circuit having an over current protection stage in accordance with an embodiment of the present invention; and

[0007] FIG. 2 is a schematic diagram of the over current protection stage of FIG.1 in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0008] FIG. 1 is a schematic diagram of a portion of a Switch Mode Power Supply (SMPS) 10 that includes a Power Factor Correction (PFC) controller or PFC control circuit 12 connected to an input stage 14 and to output drive stages 22 and 32. PFC controller 12 is also referred to as a PFC control circuit and output drive stages 22 and 32 are also referred to as drive stages or drive circuits. Input stage 14 has inputs 16 and 18 coupled for receiving an Alternating Current (AC) signal from an AC line and an output 20 coupled for transmitting a rectified input signal to output drive stages 22 and 32. Output drive stage 22 is comprised of a circuit element 24, an inductor 26, and a diode 28 and output drive stage 32 is comprised of a circuit element 34, an inductor 36, and a diode 38. By way of example, circuit elements 24 and 34 are field effect transistors such as, for example, MOSFETS and power Field Effect transistors (FETS). The drain of MOSFET 24 is commonly connected to a terminal of inductor 26 and to the anode of diode 28 and the drain of MOSFET 34 is commonly connected to a terminal of inductor 36 and to the anode of diode 38. The other terminal of inductor 26 and the other terminal of inductor 36 are commonly connected together to form a node 40, which node 40 is connected to output 20 of input stage 14. The cathodes of diodes 28 and 38 are commonly connected to form an output node 42. An output signal V_{OUT} is generated at output node 42. The sources of MOSFETS 24 and 34 are coupled for receiving a source of operating potential such as, for example V_{SS}. A capacitor 44 and a load 46 are coupled between output node 42 and source of operating potential V_{SS}. By way of example operating potential V_{SS} is ground potential.

[0009] PFC controller 12 is comprised of an over current protection circuit 50 coupled to Pulse Width Modulator (PWM) latches 60 and 62 and has input/output nodes 52, 54, 56, and 58. Input/output nodes 52, 54, 56, and 58 may be input/output pins and therefore may be referred to as input/output pins. PWM latches 60 and 62 each have a set input (S), a reset input (R), and an output (Q). Set input S of PWM latch 60 is coupled for receiving a clock signal CLK1 and output Q is coupled to the gate of MOSFET 24 through input/output node 54. Set input S of PWM latch 62 is coupled for receiving a clock signal CLK2 and output Q is coupled to the gate of MOSFET 34 through

input/output node 56. Input/output node 58 is coupled for receiving a source of operating potential such as, for example, V_{SS}. PWM latch 60 and output drive stage 22 cooperate to form a PFC stage 66 and PWM latch 62 and output drive stage 32 cooperate to form a PFC stage 68. Preferably, PFC stages 66 and 68 are interleaved. For the sake of clarity, outputs Q of latches 60 and 62 are shown as being directly connected to the gates of MOSFETS 24 and 34, respectively. However, it should be understood that latches 60 and 62 may not be directly connected to MOSFETS 24 and 34, respectively, but that intermediate stages or buffers may be included. Preferably, the intermediate stages or buffers have a current capability that allow efficiently turning on and turning off MOSFETS 24 and 34. Additional circuit elements such as, for example, resistors may be further included to control the switching speeds of MOSFETS 24 and 34.

[00010] Over current protection circuit 50 is comprised of a current sense circuit 72 having an input connected to input/output node 52 and an output commonly connected to a summing input of a summer 74 and to a non-inverting input of a comparator 76. A current limit reference 78 has an output commonly connected to a subtracting input of summer 74 and to an inverting input of comparator 76. An output of summer 74 is connected to an input of a current gain stage 80 having a gain α. By way of example, α is 0.5. The output of current gain stage 80 is connected to a current conduction terminal of a switch 82 and the output of comparator 76 is connected to a control terminal of switch 82. The other current conduction terminal of switch 82 is connected to a subtracting input of summer 84. An output of on-time signal processing circuit 86 is connected to a summing input of summer 84. An output of summer 84 is commonly connected to the inverting inputs of PWM comparators 88 and 90. The non-inverting input of PWM comparator 88 is coupled for receiving a capacitance voltage V_{CAP1} and the non-inverting input of PWM comparator 90 is coupled for receiving a capacitance voltage V_{CAP2}.

[00011] SMPS 10 further includes an over current protection resistor 92 having a terminal commonly connected to input/output node 52 and to a terminal of a current sense resistor 94 to form a node 96. The other terminal of current sense resistor 94 is coupled for receiving a source of operating potential such as, for example, V_{SS}.

[00012] Referring now to FIG. 2, a schematic diagram of PFC control circuit 12 illustrated in FIG. 1 is shown. As discussed above, PFC control circuit 12 is comprised

of over current protection circuit 50, which includes current sense circuit 72 and current limit reference 78. In accordance with an embodiment of the present invention, current sense circuit 72 is comprised of an operational amplifier 102 having a non-inverting input coupled for receiving a reference voltage V_{SS} and an inverting input connected to input/output node 52. An output of operational amplifier 102 is connected to a base terminal of a bipolar junction transistor 104. The emitter of bipolar junction transistor 104 is coupled for receiving a source of operating potential such as, for example, V_{SS}. A clamp circuit 106 is connected to input/output node 52. A current mirror 110 has a terminal 112 connected to input/output node 52, an input connected to the collector of bipolar junction transistor 104, and an output connected to current limit reference circuit 78 (shown as current source 134 in FIG. 2). By way of example, current mirror 110 is comprised of PNP bipolar junction transistors 114 and 116 wherein the bases of bipolar junction transistors 114 and 116 are commonly connected together and the emitters of bipolar junction transistors 114 and 116 are commonly connected together and for receiving a source of operating potential V_{CC}. The emitter and base of bipolar junction transistor 114 are coupled together through a resistor 118. The commonly connected bases of bipolar junction transistors 114 and 116 are connected to the drain of NPN bipolar junction transistor 104. The collector of bipolar junction transistor 116 serves as an output 117 of current mirror 110. It should be noted that the circuit configuration shown and described for current sense circuit 72 is an example that is included merely for the sake of clarity. Alternative examples of circuit configurations include circuits that measure the current that forces a virtual zero voltage at input/output node 52 and mirror this current to node 135.

[00013] Over current protection circuit 50 further includes an operational amplifier 120 having a capacitor 122 coupled between the output of operational amplifier 120 and its inverting input. A resistor 124 is connected between the inverting input of operational amplifier 120 and its output, i.e., node 126. Thus operational amplifier 120 is configured as a follower. A terminal of capacitor 122 is connected to the inverting input of operational amplifier 120 and the other terminal of capacitor 122 is connected to the inverting inputs of PWM comparators 88 and 90 and to the output of operational amplifier 120 forming a node 126. Control signal V_{TON} appears at node 126. A non-

inverting input of operational amplifier 120 is coupled for receiving a voltage V_{REGUL}. It should be noted that voltage V_{REGUL} is a regulation signal resulting from the amplification of the error between the actual voltage appearing at output node 42 and its desired value for regulation as provided by a regulation block (not shown). Thus, control signal V_{TON} is generated from voltage V_{REGUL} which serves as an error correction signal. A current source 130 is coupled to the inverting input of operational amplifier 120 through switch 82 and transmits a current substantially equal to the product of a gain factor α and the difference between currents I_{CS} and I_{ILIM1}, i.e., $\alpha*(I_{CS} - I_{ILIM1})$. An input of a current comparator 132 is commonly connected to output 117 of current mirror 110 and to a current source 134 to form a node 135. Current source 134 sinks a current I_{ILIM1} and is referred to as a current sink. An output of current comparator 132 is connected to a control terminal of switch 82. The output of current mirror 110 that is commonly connected to the input of current comparator 132 and to current source 134 sources a current I_{CS}.

[00014] In operation and referring to FIG. 1, an AC signal is received at inputs 16 and 18 of input stage 14, which generates an output current I_{PFC} at output 20. Current I_{PFC} flows through output drive stages 22 and 32 and is returned through resistor 94. Resistor 94 generates a negative current sense voltage V_{CS} which is proportional to current I_{PFC}. PFC control circuit 12 monitors voltage V_{CS} to detect when current I_{PFC} exceeds a predetermined level. Current sense circuit 72 generates a current I_{CS} that is substantially equal to the product of current I_{PFC} and the ratio of the resistor values for resistors 94 and 92, i.e., $I_{CS}=I_{PFC}*(R_{94}/R_{92})$, where R_{94} is the resistance value of resistor 94 and R_{92} is the resistance value of resistor 92. Current I_{CS} is transmitted to the inverting input of comparator 76 and to the summing input of summer 74. The conduction times of MOSFETS 24 and 34 of output drive stages 22 and 32, respectively, are controlled by a control signal V_{TON} appearing at the inverting inputs of PWM comparators 88 and 90. Control signal V_{TON} is further described below.

[00015] Current limit reference circuit 78 sinks a current I_{ILIM1} from summer 74, i.e., a negative current I_{ILIM1} appears at the subtracting input of summer 74. Current I_{ILIM1} is a maximum desired current flowing in SMPS 10 and may be identified as current I_{ILIM1} or current I_{REF}. In addition, current I_{ILIM1} is transmitted to the inverting input of

comparator 76. In response to currents I_{CS} and I_{ILIM1} appearing at its inputs, comparator 76 generates a control voltage that controls the state of switch 82. If current I_{CS} is less than current I_{ILIM1}, switch 82 is open and if current I_{CS} is greater than current I_{ILIM1}, switch 82 is closed. When switch 82 is open, the current amplified by amplifier 80 does not flow. When switch 82 is closed, the current generated by amplifier 80 is transmitted to the subtracting input of summer 84. Amplifier 80 generates a current substantially equal to the product of a gain factor α and the difference between currents I_{CS} and I_{ILIM1}. Thus, amplifier 80 generates a current $I_{SHIFT} = \alpha*(I_{CS}-I_{ILIM1})$. It should be noted that the configuration of the circuitry for generating current I_{SHIFT} is not a limitation of the present invention. For example, switch 82 and current comparators 76 and 132 (shown in FIGS. 1 and 2, respectively) may be omitted from embodiments in which gain stage 80 or current source 130 generate current I_{SHIFT} when current I_{CS} is greater than current I_{ILIM1}. Thus, other embodiments of PFC control circuits 12 may include current comparators, switches, current gain stages, or combinations thereof that inject a current I_{SHIFT} when current I_{CS} is greater than current I_{ILIM1}. It should be further noted that current I_{SHIFT} is not limited to being a current that is the product of a gain factor, e.g., α, and the difference between currents I_{CS} and I_{ILIM1}. Current I_{SHIFT} may be generated such that it is an increasing function of the amount by which current I_{CS} exceeds current I_{ILIM1}. For example, current I_{SHIFT} may be the product of gain factor α and the square of the difference between currents I_{CS} and I_{ILIM1}, i.e., $I_{SHIFT} = \alpha*(I_{CS}-I_{ILIM1})^2$.

[00016] On-time signal processing circuit 86 generates a control voltage or control signal V_{TON} which appears at the input of summer 84. If switch 82 is open, control voltage V_{TON} is input into the inverting inputs of PWM comparators 88 and 90. A sawtooth voltage signal V_{CAP1} from a timing capacitor (not shown) is input into the non-inverting input of PWM comparator 88, which generates an input signal at reset input R of PWM latch 60. Likewise, a sawtooth voltage signal V_{CAP2} from a timing capacitor (not shown) is input into the non-inverting input of PWM comparator 90, which generates an input signal at reset input R of PWM latch 62. Clock signals CLK1 and CLK2 are input at set inputs S of PWM latches 60 and 62, respectively. PFC control circuit 12 generates control signals that control the conduction times of MOSFETS 24 and 34. In response to

the output signals from latches 60 and 62, MOSFETS 24 and 34 generate an output signal V_{OUT} at output node 42.

[00017] If current I_{CS} is greater than reference current I_{REF}, an over current condition exists. As discussed above, under this condition switch 82 is closed and amplifier 80 injects current I_{SHIFT} into summer 84, which then shifts the value of voltage V_{TON}. When current I_{CS} is greater than current I_{ILIM1}, output current I_{SHIFT} and on-time signal processing circuit 86 cooperate to lower control voltage V_{TON}. As discussed above, sawtooth voltage signals V_{CAP1} and V_{CAP2} from timing capacitors (not shown) are input into the non-inverting inputs of PWM comparators 88 and 90, which generate signals for PWM latches 60 and 62, respectively. PFC control circuit 12 generates control signals that control the conduction times of MOSFETS 24 and 34. Because, control voltage V_{TON} controls the output voltage levels of PWM comparators 88 and 90, it controls the output signals of PWM latches 60 and 62 and thereby the conduction times of MOSFETS 24 and 34.

[00018] FIG. 2 illustrates an embodiment of PFC controller 12 in which operational amplifier 102 uses NPN bipolar junction transistor 104 to source a current that maintains the voltage at input/output node 52 in the range of voltage V_{SS}. Resistor 92 is inserted between input/output node 52 to adjust the current I_{CS} flowing through input terminal 112. A current I_{CS} flowing through input/output node 52 is mirrored to output 117 of current mirror 110 and flows toward node 135. Current I_{CS} is compared to a reference or threshold current I_{ILIM1}. In addition, current source 134 sinks a current I_{ILIM1} from node 135. As discussed above, current I_{ILIM1} is a maximum desired current flowing in SMPS 10 and may be identified as current I_{ILIM1} or current I_{REF}. If current I_{CS} is less than reference current I_{ILIM1}, current comparator 132 generates a logic low voltage that opens switch 82 or maintains switch 82 in an open position if it was already at a logic low voltage level. Current comparator 132 compares current I_{CS} with current I_{ILIM1} and generates a control signal that opens or closes switch 82. Current comparator 132 is analogous to comparator 76 of FIG. 1. Because an over current condition is not occurring, operational amplifier 120 generates a control signal V_{TON} that is at a nominal value. Control signal V_{TON} is input into the inverting inputs of PWM comparators 88 and 90. Sawtooth voltage signals V_{CAP1} and V_{CAP2} from timing capacitors (not shown) are

input into the non-inverting inputs of PWM comparators 88 and 90, which comparators 88 and 90 generate an input signals for reset inputs R of PWM latches 60 and 62. Clock signals CLK1 and CLK2 are input to set inputs S of PWM latches 60 and 62, respectively. PWM latches 60 and 62 transmit control signals that control the conduction times of MOSFETS 32 and 34. In response to the output signals from latches 60 and 62, MOSFETS 24 and 34 generate an output signal V_{OUT} at output node 42.

[00019] If current I_{CS} is greater than reference current I_{REF}, an over current condition exists. In response to the over current condition, current comparator 132 generates a logic high voltage at its output, which closes switch 82. By closing switch 82, a current I_{SHIFT} from current source 130 is injected into the inverting input terminal of operational amplifier 120. The current from current source 130 has a value substantially equal to the product of the gain factor α and the difference between current I_{CS} and a reference current I_{ILIM1}. Operational amplifier 120 strives to maintain input voltage V_{IN+} appearing at the non-inverting input of operational amplifier 120 equal to input voltage V_{IN-} appearing at the inverting input of operational amplifier 120. Accordingly, operational amplifier 120 reduces or lowers the voltage at the output of operational amplifier 120, i.e., it reduces voltage V_{TON}. As discussed above, sawtooth voltage signals V_{CAP1} and V_{CAP2} from timing capacitors (not shown) are input into the non-inverting inputs of PWM comparators 88 and 90, which generate signals for PWM latches 60 and 62. Clock signals CLK1 and CLK2 are input to set inputs S of PWM latches 60 and 62. PFC control circuit 12 generates control signals that control the conduction times of MOSFETS 24 and 34. Because control voltage V_{TON} controls the output voltage level of PWM comparators 88 and 90, it controls the output of PWM latches 60 and 62 and thus the conduction times of MOSFETS 24 and 34.

[00020] By now it should be appreciated that an over current protection circuit and a method for protecting an SMPS from an over current have been provided. In accordance with an embodiment, over current protection is provided by changing the conduction times of MOSFETS present in the PFC stage, rather than turning off these transistors. A control voltage or control signal V_{TON} is reduced in a proportion that depends on the excess current flowing in the SMPS. Thus, control signal V_{TON} is changed in accordance with the current flowing in the switch mode power supply. Control voltage

V_{TON} is transmitted to the PWM comparators to control the PWM latches. The output signals from the PWM latches are then used to control the conduction times of the MOSFETS of current drive stages 22 and 32.

[00021] Although specific embodiments have been disclosed herein, it is not intended that the invention be limited to the disclosed embodiments. Those skilled in the art will recognize that modifications and variations can be made without departing from the spirit of the invention. For example, rather than changing the control signal V_{TON}, the ramp signals can be varied in response to an over current protection signal, i.e., a signal from current comparator 132. It is intended that the invention encompass all such modifications and variations as fall within the scope of the appended claims.

CLAIMS

What is claimed is:

1. A method for protecting against an over current condition, comprising changing a conduction time of a circuit element of a plurality of circuit elements in response to a first current exceeding a second current, wherein the conduction time is reduced proportionally in an amount that is an increasing function of the amount by which the first current exceeds the second current.

2. The method of claim 1, further including comparing the first current to the second current.

3. The method of claim 2, wherein changing the conduction time includes reducing the conduction time of the circuit element of the plurality of circuit elements.

4. The method of claim 3, wherein reducing the conduction time of the circuit element comprises varying a control signal of the circuit element.

5. The method of claim 3, wherein reducing the conduction time of the circuit element comprises varying a ramp signal of the circuit element.

6. The method of claim 1, further including amplifying a difference between the first current and the second current.

7. The method of claim 1, further including amplifying a square of the difference between the first current and the second current.

8. The method of claim 7, wherein changing the conduction time of the circuit element comprises changing the conduction time of at least one transistor of a plurality of transistors.

9. The method of claim 1, wherein changing the conduction time of the circuit element comprises:

providing a first input signal at a non-inverting input of an operational amplifier;

providing a second input signal at an inverting input of the operational amplifier, the operational amplifier configured as a follower; and

injecting a current into the inverting input to reduce an output voltage appearing at the output of the operational amplifier.

10. A method for protecting a circuit from an over current condition comprising changing a conduction time of at least one transistor in response to an over current, wherein the conduction time is changed in an amount that is an increasing function of the amount of the over current.

11. The method of claim 10, further including determining an over current by comparing a first current to a second current.

12. The method of claim 11, wherein the over current is a difference between the first current and the second current.

13. The method of claim 12, wherein the first current is a mirrored current and the second current is a reference current.

14. The method of claim 10, further including multiplying the over current by a gain factor.

15. The method of claim 10, wherein changing the conduction time of the at least one transistor comprises reducing the conduction time.

16. The method of claim 15, wherein reducing the conduction time includes injecting current into a follower.

17. The method of claim 10, wherein changing the conduction time includes comparing a ramp signal with a control signal.

18. The method of claim 10, wherein changing the conduction time includes reducing the on-time of the at least one transistor by changing the ramp signal or the control signal.

19. An over current protection circuit of a power factor correction circuit, comprising:

a pulse width modulation comparator having an inverting input, a non-inverting input, and an output;

a summer having at least first and second inputs and an output, the output connected to the inverting input of the pulse width modulation comparator;

an on-time signal processing circuit having an output coupled to the first input of the summer;

a current injection circuit coupled to the second input of the summer; and

a pulse width modulation latch having a set input coupled to the output of the pulse width modulation comparator.

20. The over current protection circuit of claim 19, wherein the on-time signal processing circuit comprises:

an operational amplifier having an inverting input, a non-inverting input, and an output;

a capacitor coupled between the inverting input and the output of the operational amplifier;

a switch having first and second current conducting terminals and a control terminal, the first current conducting terminal coupled to the inverting input of the operational amplifier;

a first current source coupled to the second current conducting terminal of the switch;

a current comparator having an input and an output, the output coupled to the control terminal of the switch;

a second current source coupled to the input of the current comparator; and

a current sink coupled to the input of the current comparator.

Fig. 1

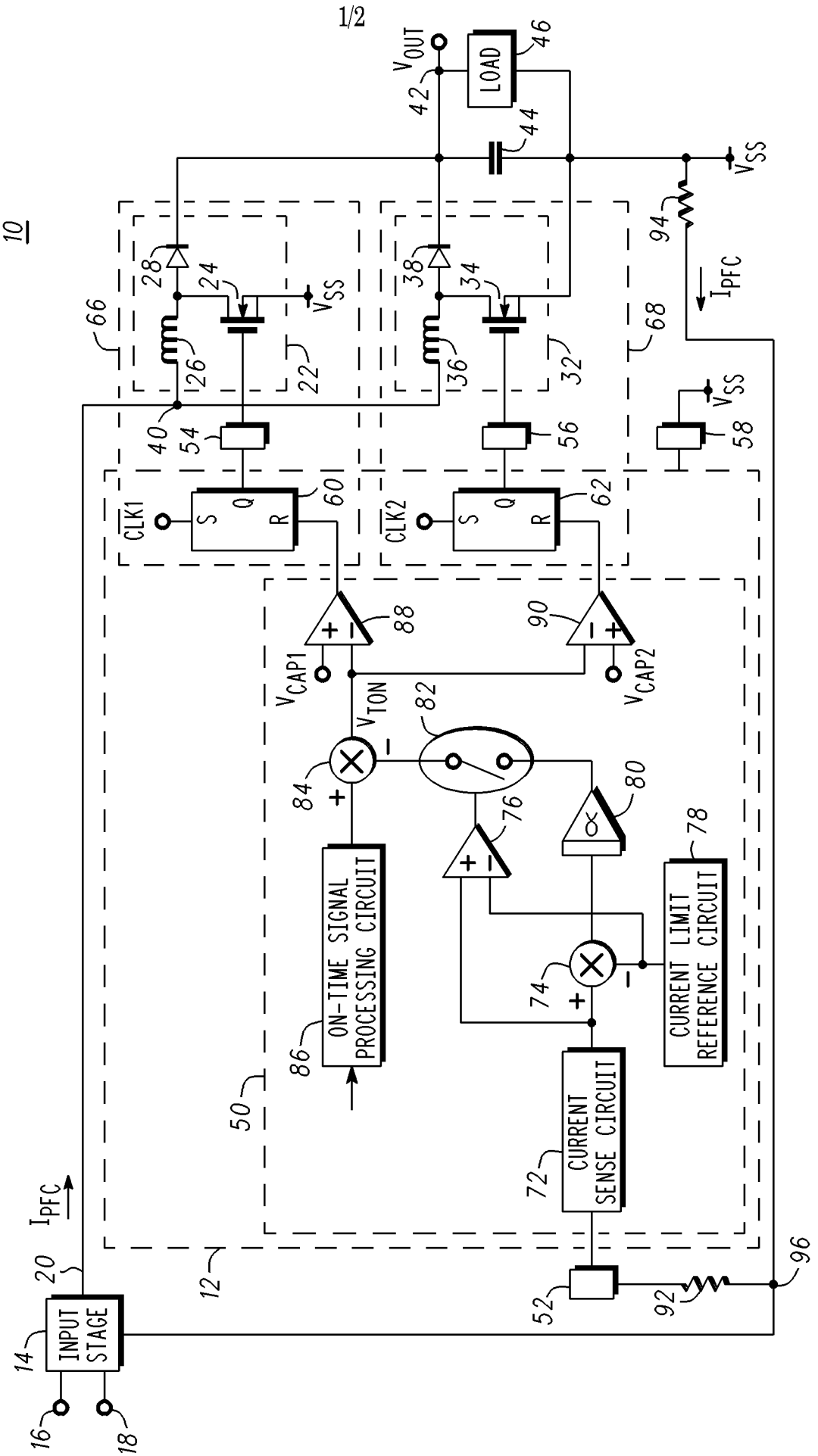
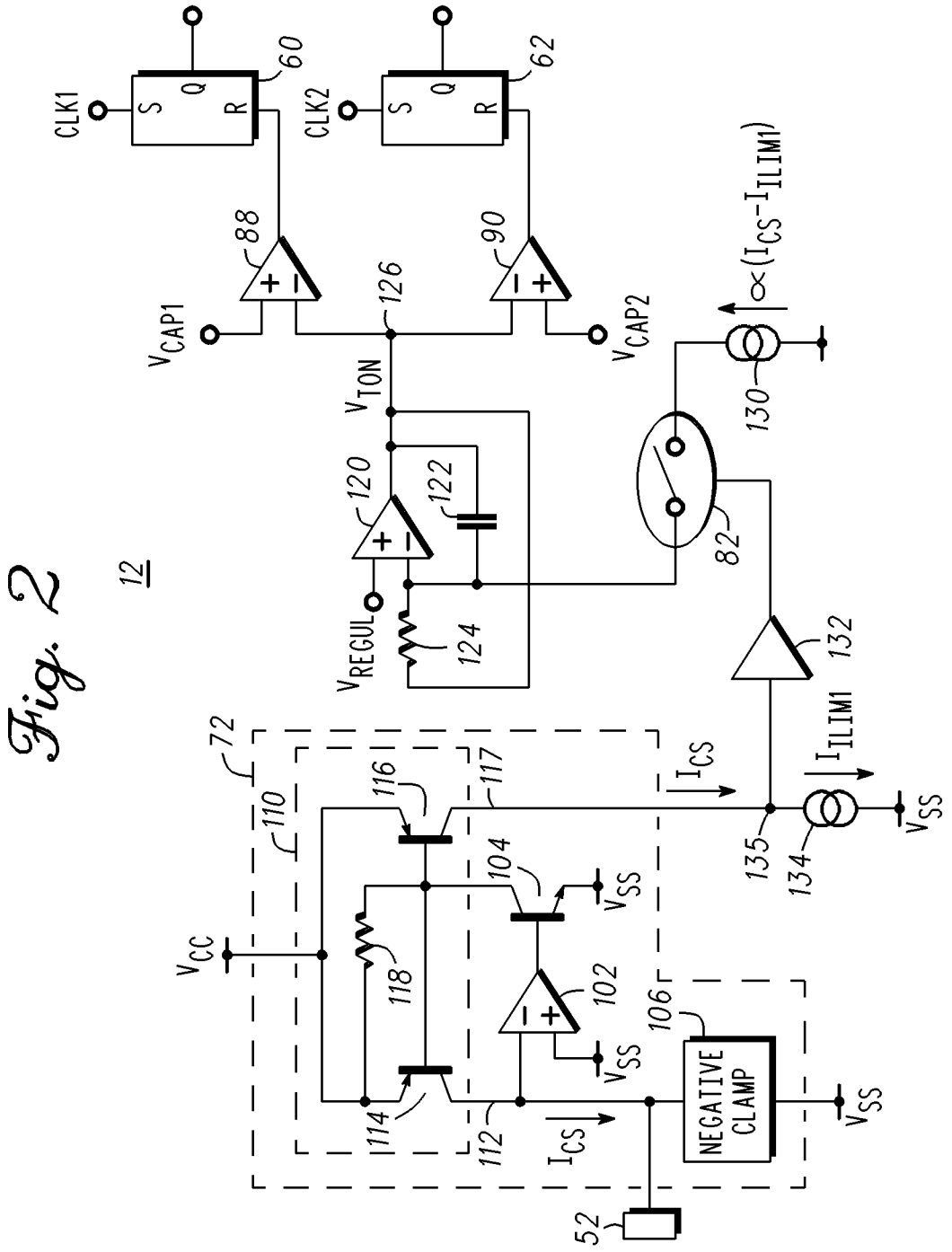

10
V_{OUT}
42
LOAD
46
44
V_{SS}
94
I_{PFC}
28
24
38
34
66
68
26
22
36
32
40
54
56
58
CLK1
CLK2
S
R
Q
60
62
88
90
V_{CAP1}
V_{CAP2}
V_{TON}
82
84
80
76
78
ON-TIME SIGNAL PROCESSING CIRCUIT
CURRENT LIMIT REFERENCE CIRCUIT
CURRENT SENSE CIRCUIT
74
72
86
50
12
52
92
96
20
14
INPUT STAGE
16
18

Fig. 2


12
CLK1
CLK2
S
Q
R
60
62
88
90
126
V_{CAP1}
V_{CAP2}
V_{TON}
120
122
124
V_{REGUL}
$\propto(I_{CS}-I_{ILIM1})$
130
82
132
I_{ILIM1}
72
110
116
117
I_{CS}
104
V_{SS}
135
134
V_{CC}
118
102
106
NEGATIVE CLAMP
114
112
52

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/041985

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/158

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 437 547 B2 (SHEA L. PETRICEK ET AL.) 20 August 2002 (2002-08-20) figures 4,5 column 4, line 45 - line 55 column 5, line 56 - line 61	1
X	US 6 049 473 A (YUNGTAEK JANG ET AL.) 11 April 2000 (2000-04-11) figures 6,14 column 3, line 20 - line 54	1
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 June 2009	12/08/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Lund, Michael

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/041985

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/223253 A1 (AN-TUNG CHEN ET AL.) 4 December 2003 (2003-12-04) figure 2 paragraphs [0006], [0007]	1
X	US 6 979 980 B1 (BRYCE L. HESTERMAN ET AL.) 12 January 1993 (1993-01-12) figure 20 column 9, line 52 - line 59 column 10, line 8 - line 17	1
A	US 2004/245970 A1 (PHILIP C. TODD ET AL.) 9 December 2004 (2004-12-09) abstract figure 3 paragraph [0010]	1
A	US 2006/171178 A1 (EMANUIL Y. SHVARTS) 3 August 2006 (2006-08-03) figures 2,3,6 paragraphs [0069], [0070]	1
A	EP 1 528 663 A (ROAL ELECTRONICS) 4 May 2005 (2005-05-04) abstract	1

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.2

Claims Nos.: 2-20

1. The application is not clear to an extent that makes meaningful search of the claims possible. This is in particular caused by a number of essential features missing in claim 1, and general confusion within the set of claims about which features are causing the inventive effect.

1.1 The method claimed in claim 1 is stated to be suited "for protecting against an over-current condition". However, the few technical features mentioned in claim 1 are neither clearly related to the line with the over-current, nor are the technical effects caused by the technical features mentioned in the claim described to influence the current in the line with the over-current. This means that the features mentioned in claim 1, and in the further claims, may be groups of independent features without a clear interaction.
Then the groups of features described in the claims may be chosen, within valid interpretation of the claims, such that the necessary interaction between the groups of features is not present and the inventive effect missing. This leaves it impossible for the person skilled in the art to carry out the invention without requiring him to involve a further inventive step. Independent claim 19 is missing the few technical features of claim 1 which again is an indication that the applicant is not clear upon which features are causing the inventive effect.
Therefore, no common inventive idea is found between these groups of features and no meaningful search can be carried out in general.

1.2 With the interest of the applicant in mind, trying to avoid the application to fall due to an inappropriate set of initial claims, claim 1 has been searched on its literal wording. This means that the first and second currents may be chosen arbitrarily and that the "changing a conduction time of a circuit element" may cause an arbitrary effect as long as it is suited for "for protecting against an over current condition".

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.2), should the problems which led to the Article 17(2)PCT declaration be overcome.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2009/041985

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 2-20
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers allsearchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search reportcovers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2009/041985

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