United States Patent

[11] 3,626,956

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[21] Appl. No. **65,949**
[22] Filed **Aug. 21, 1970**
[45] Patented **Dec. 14, 1971**
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[54] ITEM TRANSPORT DEVIATION DETECTION DEVICE

5 Claims, 5 Drawing Figs.

[52] **U.S. Cl.** **340/259,** 271/57, 340/309.3
[51] **Int. Cl.** **G08b 21/00**
[50] **Field of Search** 340/259, 309.3, 421, 420; 271/57

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ABSTRACT: A device and method for detecting interruptions or deviations of normal item transport in an item transport pathway wherein a signal indicative of an interruption or deviation is generated whenever a transported item takes longer than a predetermined time to be transported between two stations in the pathway, or whenever an item remains longer than a predetermined time at the second of the stations, the two consecutive time conditions being imposed by the same timing element.

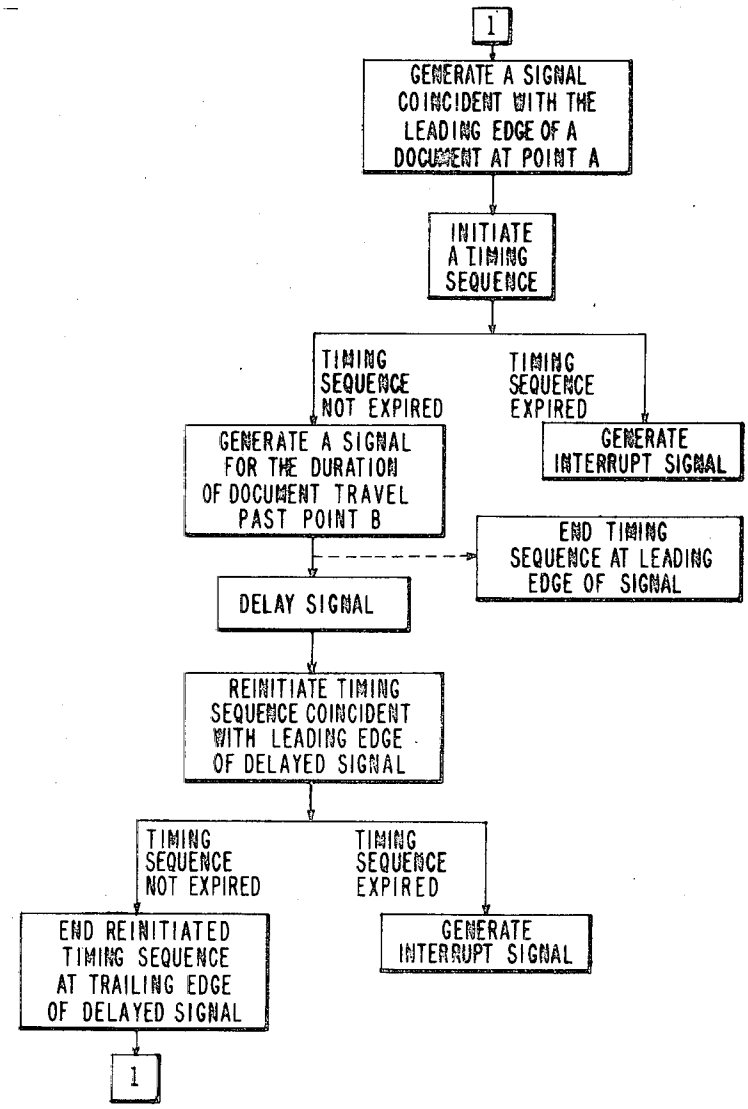

FIG. 1.

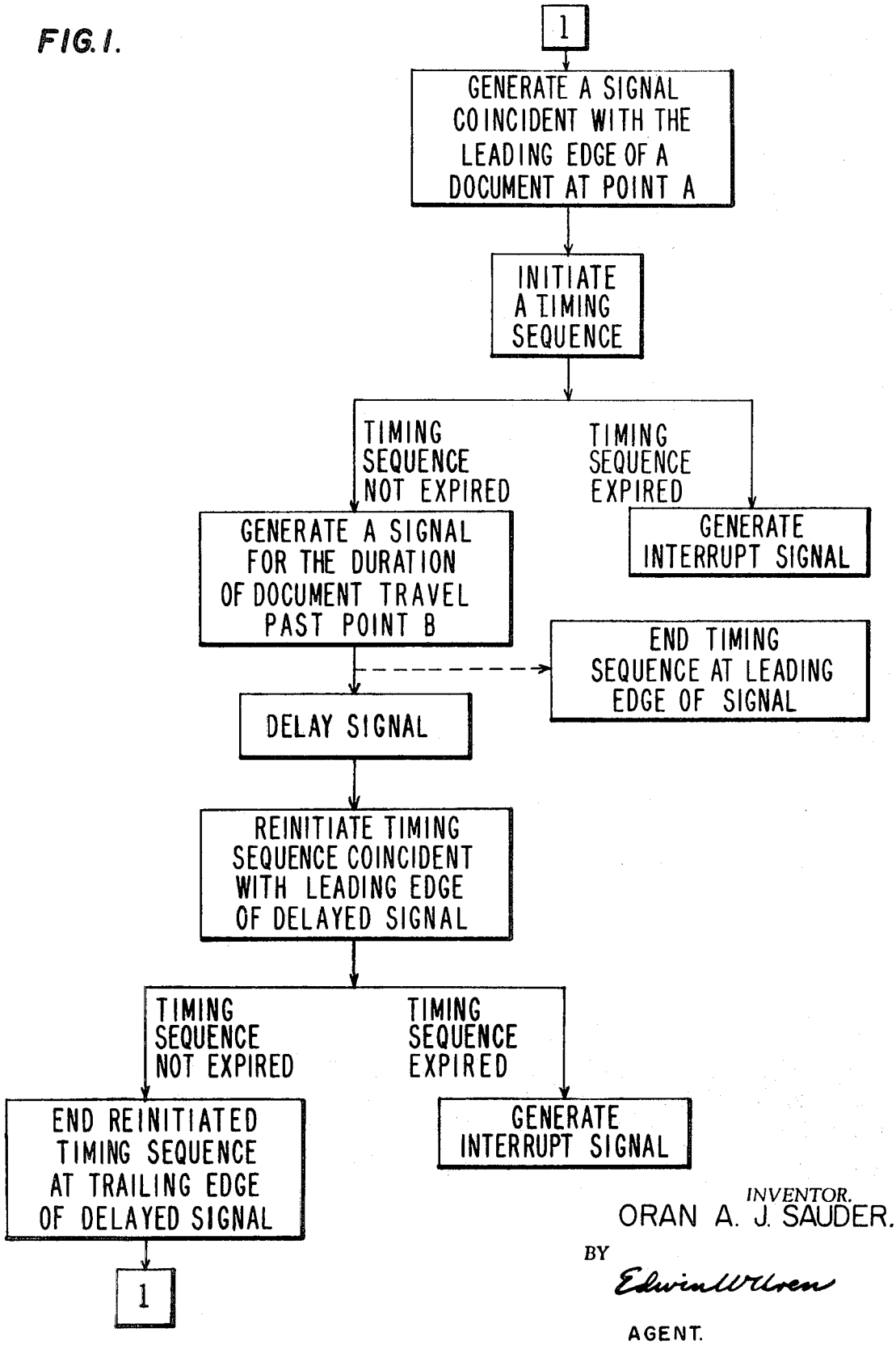

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FIG. 2.

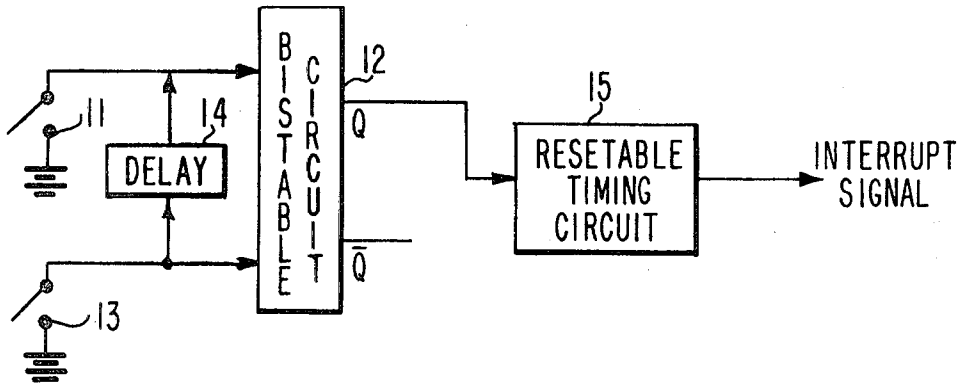

11
14
DELAY
13
BISTABLE CIRCUIT
12
Q
$\bar{Q}$
15
RESETABLE TIMING CIRCUIT
INTERRUPT SIGNAL

FIG. 3.

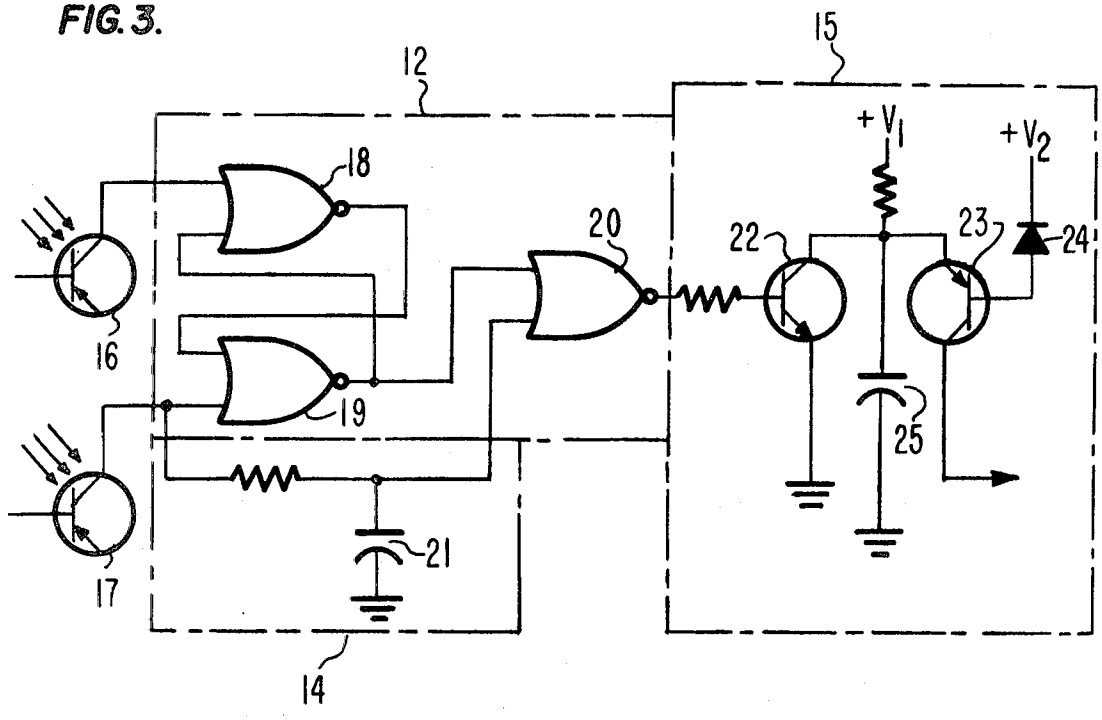

12
15
18
20
16
19
17
21
14
+V1
+V2
22
23
24
25

FIG. 4.

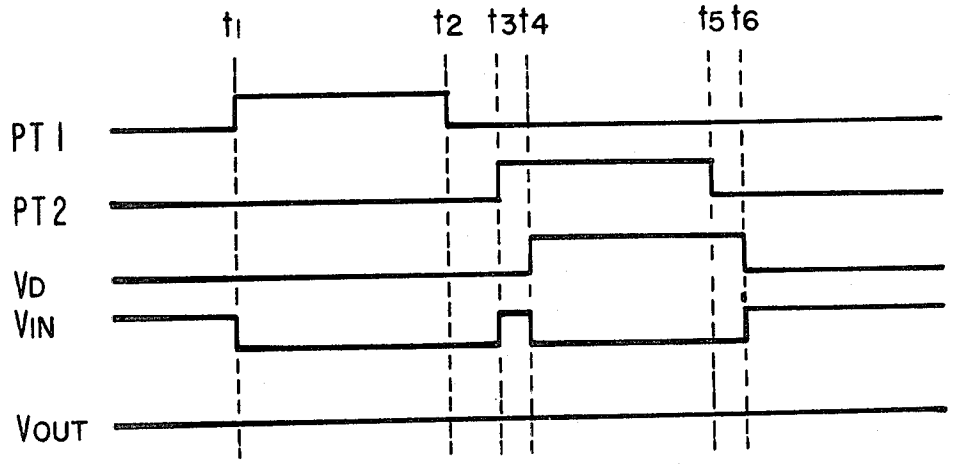
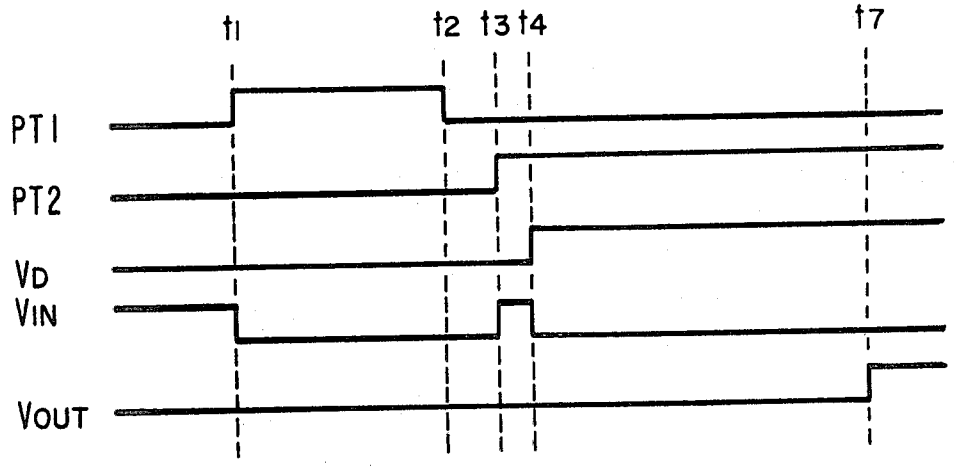

t1
t2
t3t4
t5t6
PT 1
PT2
VD
VIN
VOUT

FIG. 5.


t1
t2
t3 t4
t7
PT 1
PT2
VD
VIN
VOUT

ITEM TRANSPORT DEVIATION DETECTION DEVICE

BACKGROUND

The invention relates generally to item transport monitoring systems and specifically to circuits for detecting jams in document passageways of document-handling equipment.

In the art of high-speed handling of thin, pliable items such as paper documents, precision is required in driving and maneuvering the items through various guides and passageways of the handling equipment. The occurrence of any malfunction in the document transport section of such document-handling equipment generally leads to serious consequences, as when a check inadvertently becomes lodged in the transport passage of a check reader/sorter and causes a large number of following checks to be destroyed, disfigured or misread.

A common method of preventing such adverse consequences of transport malfunctions is to provide means for detecting an initial interruption or deviation in document flow, and to shut off the document-driving mechanism before a large number of documents are destructively impelled into the obstructed area. With the document-driving apparatus so disabled, the dislodged or obstructing document may be removed before a serious jam condition develops.

The antecedents of the present invention serve to detect interruptions in normal document flow, and upon such detection, to generate a signal that is effective to initiate a shutting down of the document-driving mechanism. Known prior art jam detection devices commonly combine two switching members such as phototransistors at selected predetermined locations in the document passageway, to detect the presence of documents at these specific selected locations. Document travel time between these two phototransistors is measured by means of circuitry combining a flip-flop and a timing circuit such as a resettable delay. If the measured time exceeds a predetermined time, either a coincidence detection circuit coupled to the flip-flop and the resettable delay, or the delay itself, serves to generate an electrical signal indicative of an interrupted or deviated document flow condition between the two phototransistors. Prior art jam detection devices accordingly impose one precedent condition to the recognition of an interrupted or delayed document; that is, that the document travel between two fixed positions in a predetermined time. It is obvious that the greater the number of interruption detection circuits that are provided in the document passageway, in order to increase the probability of detecting any document delay occurrences, the greater the number of stations and phototransistors that would need to be used, and the greater the number of precedent conditions that would need to be imposed. A highly reliable detection system of the prior art type would accordingly require more space than is normally available, and be exceedingly costly to build.

SUMMARY OF THE INVENTION

It is generally an object of the present invention to provide a reliable document flow interruption detection system that requires a minimum of space in the transport area, and a minimum number of circuit components per precedent condition imposed.

The invention accomplishes this and other objects by enabling a single timing element or resettable delay to measure the duration of document travel in two contiguous segments of a transport pathway, a precedent condition being imposed for each segment. The time required for the leading edge of a document to be transported between a first and a second point in the transport pathway, and the time interval between the passage of the leading edge and the trailing edge of the document past the second of the points are each measured by the timing element. If either measured time is greater than the predetermined times, as established by the timing element, a signal is generated indicating a deviated document transport condition.

The invention provides that the timing element is reset after measuring the transport duration of the leading edge of a document between the first and second points in the transport pathway, and that an item detection signal from the second switching member is delayed in order to reset the timing element for measuring the interval of time between the passage of the leading and trailing edges of the document past the second switching member.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a flow chart showing the method by which a deviated condition of item flow is detected;

FIG. 2 is a block diagram showing the basic composition of a preferred item transport deviation detection device;

FIG. 3 is a circuit diagram of the transport deviation detection device;

FIG. 4 is a timing diagram illustrating the operation of the transport deviation detection circuit under normal item flow conditions; and

FIG. 5 is a timing diagram illustrating the operation of the transport deviation detection circuit when an item fails to traverse the second switching member in the predetermined time interval.

DETAILED DESCRIPTION

To facilitate a more complete understanding of the subject invention, a specific example or preferred embodiment will hereinafter be described in connection with the drawings. For the purpose of illustration, the jam detection device will be described in conjunction with a check sorter, although it is to be understood that the fundamental concept of the invention may be applied with equal success to any type of document-handling equipment. The check sorter envisioned has a pathway for guiding checks past a series of pockets. Associated with each pocket along the pathway is a diverting gate which is selectively activatable by control circuitry to intercept a check traveling at a high rate of speed down the pathway and to direct it into an associated pocket. Although one or more jam detection devices may be positioned anywhere along the transport path of the envisioned check sorter, for our present purposes it is assumed a single such device is so positioned as to detect a deviation in document flow past a diverting gate, the probability of a document jam at such location being relatively high due to the variable forces that are applied to a document in this area.

The concept of jam detection that is embodied in the present invention imposes two precedent conditions under which a jam or interruption of document flow is detected. The conditions are:

1. That a check travel from a predetermined first point (point A) positioned anteriorly of the gate to a second point (point B) positioned posteriorly of the gate in a prescribed time;

2. That the trailing edge of a check departs from point B in a prescribed time interval following the arrival of its leading edge at point B.

Should either of these conditions not obtain during the flow of a check down the transport pathway, the device would generate an interrupt signal effective either for shutting off the document transport mechanism or for alerting the operator to the time deviation at the associated gate.

The method by which the aforementioned precedent conditions are imposed is illustrated in the flow chart of FIG. 1. First, a switching means detects the leading edge of a document as it passes point A and generates an electrical signal that begins a timing sequence. The duration of the timing sequence is a period of time slightly greater than the time required for the leading edge of a check to pass point A and arrive at point B under normal document transport conditions. If the duration of the timing sequence expires before the leading edge of the check arrives at point B, an interrupt signal is generated indicating that the check travel has been slower

than normal or totally interrupted between point A and point B. If the check arrives at point B before the timing sequence has expired, switching means at point B will serve to generate an electrical pulse during the period that the check passes in front of the switching means at point B. The electrical signal from the switching means at point B is delayed for a period of time that is relatively short compared with its normal duration, thereby permitting the timing circuit that was used to initiate the timing sequence to be reset so that it can be reinitiated at the leading edge of the delayed signal from the switching means at point B. If the reinitiated timing sequence expires before the trailing edge of the delayed signal, an interrupt signal is generated indicating that the check has not passed point B within the prescribed time. If the check has passed point B before the timing sequence has expired the check has arrived in its pocket within the normal and prescribed time.

The circuit components that are combined to carry out the above-described process are shown in FIG. 2. A first switching means **11** located at point A in the document transport pathway is electrically connected to a bistable circuit **12**. A second switching means **13** located at point B in the pathway is also electrically connected to the bistable circuit **12**. The first switching means **11** activates an electrical signal when the leading edge of a check enters its associated position in the transport pathway, or, in other words, passes point A. The second switching means **13** responds electrically to the passage of the entire length of the check past its associated position in the pathway, or in other words, past point B, thus generating an electrical signal that begins with the passage of the leading edge of the check by point B. The electrical signal from the first switching means **11** triggers the bistable circuit **12** to its Q state. Following the electrical signal from the first switching means **11**, a signal from the second switching means **13** triggers the flip flop to its $\overline{Q}$ state. The output from the second switching means **13** at point B in the pathway is also electrically connected to a delay circuit **14**. The output from the delay **14** is electrically connected to the bistable circuit **12** for triggering the circuit to the Q state. The Q state of the bistable circuit **12** is electrically connected to a resettable timing circuit **15** that serves to generate an electrical signal when the Q state of the bistable circuit **12** is maintained for longer than a predetermined time.

As shown in FIG. 3 phototransistors **16** and **17** have been chosen as the switching means at points A and B in the transport pathway. As described above, it is not necessary that the first switching means **11** of the first phototransistor **16** electrically respond to the full length of a bypassing check, but only to the leading edge. A phototransistor nevertheless has been chosen as the preferred switching means at point A, as it achieves the desired operational characteristics while its extraneous characteristic (i.e., that it activates a pulse for the full duration of a bypassing check) has no deleterious effect upon its required characteristics in the circuit design.

The bistable circuit **12** of the jam detection device as illustrated in FIG. 3 includes a common RS flip-flop having two cross-coupled NOR-gates **18** and **19**. A first of the NOR-gates **18** is electrically connected to an appropriately amplified collector output of the first phototransistor **16** and to the output of the second NOR-gate **19**. The second NOR-gate **19** of the flip-flop is electrically connected with the output of the first NOR-gate **18** and an appropriately amplified collector output of the second phototransistor **17**. The bistable circuit **12** has a third NOR-gate **20** that electrically gates the output from the second NOR-gate **19** and a delayed output from the second phototransistor **17**. The delay element **14** of the invention is a capacitor **21** having its positive plate electrically connected to the second phototransistor **17** output and its negative plate to ground.

The resettable timing circuit **15**, as shown in FIG. 3 has an NPN control transistor **22** connected at its base to the output from the third NOR-gate **20** of the bistable circuit **12**. The collector of the control transistor **22** is electrically connected to the emitter of a PNP output transistor **23**. A positive voltage source $+V_1$ is electrically connected at a common node to the collector of the control transistor **22** and to the emitter of the output transistor **23**. The base element of the output transistor is electrically connected to the positive side of the diode **24**. The negative side of the diode **24** is connected to a positive voltage source V_2. The value of V_2 in volts is less than the value of V_1. A timing capacitor **25** has its positive plate connected at the common node with the collector of the control transistor **22** and the emitter of the output transistor **23**. The negative plate of the timing capacitor is electrically connected to ground.

OPERATION

The operation of the subject device will first be described under normal operating conditions; that is, when the document or check travels past point A and point B in the transport pathway in a normal predetermined time interval. With reference to the timing diagram of FIG. 4, a document passing the first phototransistor at point A in the check transport pathway will cause the first phototransistor to generate a pulse (PT_1) having a leading edge at t_1 and a trailing edge at $t2$. Assuming the output of the second NOR-gate **19** is low at time t_1, the output of the first NOR-gate **18** of the bistable circuit **12** goes low at the leading edge of the output pulse from the first phototransistor. The output (V_{in}) from the third NOR-gate **20** of the bistable circuit **12** goes low at the leading edge of the output (PT_1) from the first phototransistor **16** thus beginning a timing sequence. At the trailing edge of the pulse from the first phototransistor **16** no other changes in states occur. When a document proceding along the pathway of the check sorter reaches the second phototransistor **17** at point B in the pathway, the second phototransistor generates a pulse (PT_2). This pulse occurring at t_3 is delayed for a short period of time by the delay capacitor **21** thus allowing the output (V_{in}) from the third NOR-gate **20** to go high until the delay capacitor charges to a predetermined voltage at which time the output from the third NOR gate again goes low. It is this short positive-going pulse occurring at the leading edge of the output from the second phototransistor that permits the timing circuit **15** to reset. When the output (V_{in}) from the third NOR-gate **20** of the bistable circuit **12** is high the base of the control transistor **22** is high thereby biasing the transistor in a conducting state and dropping the voltage at the common node. As the emitter of the output transistor **23** is electrically connected to the common node, the low voltage at the node serves to bias the output transistor in a nonconducting state. When the output (V_{in}) from the third NOR-gate **20** goes low the control transistor **22** is biased to a nonconducting state. As both the control and the output transistors are nonconducting, the voltage across the timing capacitor **25** increases with time. If it attains a high enough voltage before the control transistor **22** again turns on and discharges the timing capacitor **25** the output transistor will turn on, thus generating an interrupt signal (V_{out}).

When the normal flow of documents past the two phototransistors **16** and **17** takes place the period of time in which the output from the third NOR-gate **20** remains low is less than the time required for the timing capacitor **25** to charge to a sufficient voltage value to bias the output transistor **23** in a conducting state. When the second phototransistor **17** at point B in the transport path of a check generates a pulse, a short positive going pulse is displayed at the output of the third NOR-gate **20** of the bistable circuit **12**. This positive-going pulse biases the control transistor **22** to a conducting state which allows the timing capacitor **25** to discharge. After a short delay the output from the third NOR-gate **20** of the bistable circuit **12** again goes low and the charging of the timing capacitor **25** or timing sequence begins again. If the time between the leading edge of a check and the trailing edge of a check passing the second phototransistor **17** is less than the time required for the timing capacitor **25** of the resettable timing circuit **15** to charge to an extent that the out-

put transistor 23 will be biased in a conducting state, the output voltage from the output transistor will remain low until some abnormally slow document in the flow either takes longer than the charging time to travel from the first to the second phototransistor or to traverse the second phototransistor.

In the latter case, for example, the output (PT_2) from the second phototransistor 17 would occur for longer than the duration t_3 to t_5 in FIG. 4. As shown in the timing diagram of FIG. 5, the trailing edge of the output pulse (PT_2) from the second phototransistor 17 has not occurred, at time t_5, meaning that the document passing in front of it has been somehow slowed from its normal rate of movement while passing point B. After the delay has been reset at time t_4 the timing capacitor 25 of the resettable timing circuit 15 again begins to charge. At time t_7 the second phototransistor 17 still has not detected the trailing edge of the document passing thereby and the timing capacitor has charged to a voltage that biases the output transistor 23 in a conducting state. Under these conditions an output pulse (V_{out}), or interrupt signal from the collector of the output transistor 23 indicates a deviation from normal document flow.

What is claimed is:

1. In document handling apparatus having a pathway for guiding transported documents, a method for detecting a deviation in normal document transport between a first and a second stationary point in the pathway comprising the steps of:

generating a first electrical signal coincident with the leading edge of a document passing said first stationary point,

initiating a timing sequence of predetermined duration coincident with said first electrical signal,

generating a second electrical signal for the duration of said document passing said second stationary point,

generating an interrupt signal if the predetermined duration of said timing sequence expires before the beginning of said second electrical signal,

delaying said second electrical signal for a short period of time relative to the full duration thereof,

reinitiating said timing sequence coincident with the delayed beginning of said second electrical signal, and

generating an interrupt signal if the predetermined duration of said reinitiated timing sequence expires before the delayed ending of said second electrical signal.

2. In apparatus for transporting an item along a predetermined pathway, a device for detecting a deviation from a normal rate of item transport comprising:

first switching means stationed adjacent the pathway for electrically responding to the leading edge of an item passing thereby,

second switching means stationed adjacent the pathway at a predetermined distance in the direction of item transport from said first switching means, said second switching means being electrically responsive to the passage of the full length of an item thereby,

means electrically coupled with said second switching means for delaying the electrical response of said second switching means for a substantially short duration relative to the duration of the normal electrical response of said second switching means,

bistable means electrically coupled with said first switching means, said second switching means, and said delaying means for manifesting a first stable electrical state upon an electrical response from said first switching means, for manifesting a second stable electrical state upon an electrical response from said second switching means, and for again manifesting said first stable electrical state for the duration of the delayed electrical response from said delaying means, and

timing means electrically coupled with said bistable means for generating an electrical signal when said bistable means remains in said first stable electrical state for longer than a predetermined period of time, whereby said electrical signal indicates a deviation in the rate of normal item transport between said first and said second switching means or past said second switching means.

3. A device as defined by claim 2 wherein said first and said second switching means are each characterized by a photoelectric element stationed on said pathway and a source of light for switching said element in response to an item passing thereby.

4. A device as defined by claim 2 wherein said delaying means is a capacitor.

5. A device as defined by claim 2 wherein said bistable means includes a flip-flop switchable by an electrical response from said first switching means to a first electrical state and by an electrical response from said second switching means to a second electrical state, and a NOR logical operator electronically gating said first electrical state with said delayed electrical response of said second switching means.

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