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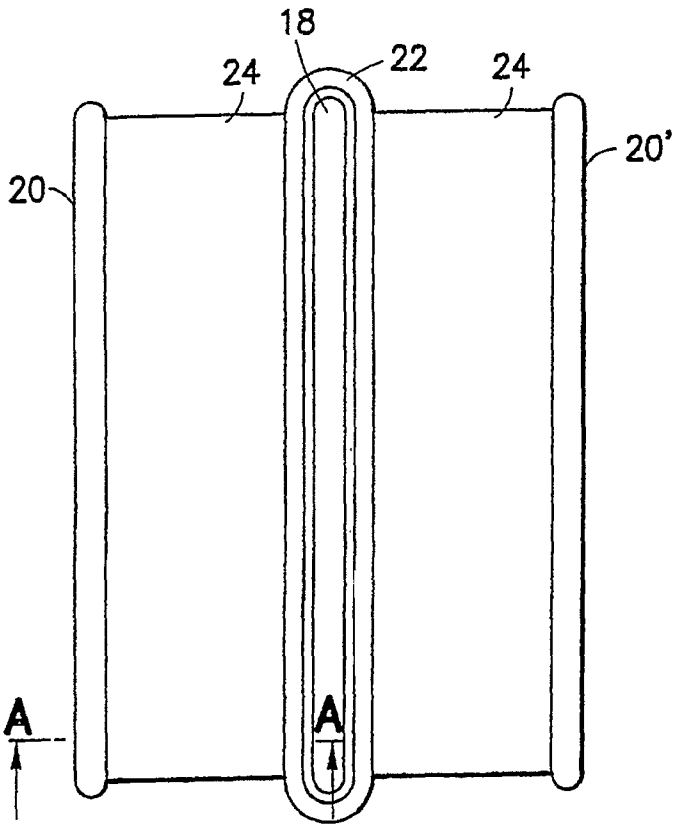
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(54) Title: III-NITRIDE POWER SEMICONDUCTOR WITH A FIELD RELAXATION FEATURE

(57) Abstract: A III-nitride power semiconductor device that includes a field relaxation feature to relax the electric fields around the gate thereof to improve the breakdown voltage of the device.




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# III-NITRIDE POWER SEMICONDUCTOR WITH A FIELD RELAXATION FEATURE

## RELATED APPLICATION

**[0001]** This application is based on and claims benefit of United States Provisional Application Serial No. 60/640,378, filed on December 30, 2004, entitled Ultra Resistive Field Plate, to which a claim of priority is hereby made and the disclosure of which is incorporated by reference.

## BACKGROUND OF THE INVENTION

**[0002]** The present invention relates to a III-nitride heterojunction power semiconductor device.

**[0003]** III-nitride heterojunction power devices are well known. A typical III-nitride power semiconductor device includes a drain electrode, a source electrode and a gate electrode disposed between the drain electrode and the source electrode. The gate electrode controls the current between the source electrode and the drain electrode. To control the current in a high power application, a large negative voltage is applied to the gate electrode in order to change the voltage at the gate electrode rapidly. When a large voltage is applied to the gate electrode rapidly, a high voltage develops between the gate electrode and the drain electrode. The gate may be damaged if the voltage between the gate and the drain electrode exceeds the breakdown voltage of the gate.

**[0004]** The breakdown of the gate is facilitated by the development of large electric fields around the gate. Thus, it is desirable to reduce the intensity of the electric fields around the gate in order to increase the breakdown voltage of the device.

SUMMARY OF THE INVENTION

**[0005]** A power semiconductor device according to the present invention includes a III-nitride based heterojunction, the heterojunction including a first III-nitride layer having a first band gap, and a second III-nitride layer having another band gap over the first III-nitride layer, a first power electrode electrically connected to the second III-nitride layer, a second power electrode electrically connected to the second III-nitride layer, a gate structure disposed between the first power electrode and the second power electrode, and a field relaxation feature disposed over the second III-nitride layer adjacent the gate structure.

**[0006]** In one embodiment of the present invention the field relaxation feature includes an ultra resistive field plate.

**[0007]** In an alternative embodiment, the field plate is disposed over the second III-nitride layer. In one variation of this embodiment, the gate structure is disposed on the field plate and the second III-nitride layer. In another variation, the gate structure is disposed on the field plate. The field plate may formed with a silicon rich SiN, or a compensated III-nitride semiconductor.

**[0008]** In another embodiment, a plurality of floating field rings may be disposed around the gate structure. In a variation of this embodiment the floating field rings may be disposed over the field plate. The guard rings may be coplanar with one another or non-coplanar, and also the guard rings may be coplanar with the gate structure or not. In addition, the guard rings may be independently floating, shorted to one another, shorted to the gate structure, or shorted to one of the power electrodes.

**[0009]** Other features, embodiments and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

**[0010]** Figure 1 shows a top plan view of two adjacently disposed active cells of a device according to the first embodiment of the present invention.

**[0011]** Figure 2 shows a cross-sectional view of a device according to the first embodiment along line A-A viewed in the direction of the arrows.

**[0012]** Figure 3 shows a top plan view of two adjacently disposed active cells of a device according to the second embodiment of the present invention.

**[0013]** Figure 4 shows a cross-sectional view of a device according to the second embodiment along line B-B viewed in the direction of the arrows.

**[0014]** Figure 5 shows a cross-sectional view of a device according to the third embodiment.

**[0015]** Figure 6 shows a cross-sectional view of a device according to the fourth embodiment.

**[0016]** Figure 7 shows a top plan view of two adjacently disposed active cells of a device according to the fifth embodiment of the present invention.

**[0017]** Figure 8 shows a cross-sectional view of a device according to the fifth embodiment along line C-C viewed in the direction of the arrows.

**[0018]** Figure 9 shows a cross-sectional view of a device according to the sixth embodiment.

**[0019]** Figure 10 shows a cross-sectional view of a device according to the seventh embodiment.

**[0020]** Figure 11 shows a cross-sectional view of a device according to the eighth embodiment.

**[0021]** Figure 12 shows a cross-sectional view of a device according to the ninth embodiment.

**[0022]** Figure 13 shows a cross-sectional view of a device according to the tenth embodiment.

**[0023]** Figure 14 shows a cross-sectional view of a device according to the eleventh embodiment.

**[0024]** Figure 15 shows a cross-sectional view of a device according to the twelfth embodiment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

**[0025]** Referring to Figures 1 and 2, a power semiconductor device according to the first embodiment of the present invention includes a III-nitride based heterojunction 10 disposed over a support body 12. Heterojunction 10 includes a first III-nitride semiconductor body 14, and a second III-nitride semiconductor body 16 over first III-nitride semiconductor body 14. A first power electrode 18 (i.e. source electrode) and a second power electrode 20 (i.e. drain electrode) are electrically connected to second III-nitride semiconductor body 16 through a direct ohmic connection or any other suitable means. A gate structure 22 is disposed between first power electrode 18 and second power electrode 20 over second III-nitride semiconductor body 14. In the preferred embodiment of the present invention, gate structure 22 includes a gate electrode which is connected to second III-nitride semiconductor layer 16 through a schottky contact. Alternatively, gate structure 22 may include a gate electrode, which is capacitively connected to second III-nitride semiconductor body through a gate insulation body. It should also be noted that gate structure 22 is disposed around first power electrode 18, and, thus can be operated to turn the channel between second power electrodes 20, 20' simultaneously.

**[0026]** According to one aspect of the present invention a field relaxation feature 24 is disposed over second III-nitride layer 16 adjacent gate structure 22 and between gate structure 22 and second power electrode 20. In the preferred embodiment of the present invention, field relaxation feature 24 is an ultra resistive field plate 25 formed with a highly electrically resistive material, such as, silicon rich SiN, compensated GaN or the like material.

**[0027]** In the first embodiment of the present invention, gate structure 22 is disposed on field plate 25 and second III-nitride semiconductor body 14. That is, field plate 25 extends beneath a portion of gate structure 22.

**[0028]** Referring to Figures 3 and 4, in a power semiconductor device according to the second embodiment of the present invention, gate structure 22 is disposed on field plate 25 only. A power semiconductor device according to the third embodiment of the present invention further includes a plurality of spaced guard rings 26 disposed between gate structure 22 and second power electrode 20. It should be noted that guard rings 26 are disposed around gate structure 22 (see Figure 3).

**[0029]** Referring next to Figure 5, in a power semiconductor device according to the third embodiment of the present invention, a gate insulation body 28 is interposed between second III-nitride semiconductor body 16, and gate structure 22 and field relaxation feature 24. Note that in the third embodiment, gate structure 22 is a gate electrode which is capacitively connected to second III-nitride semiconductor body 16 through gate insulation 28.

**[0030]** Referring to Figure 6, in a power semiconductor device according to the fourth embodiment of the present invention gate insulation body 28 is interposed between field relaxation feature 24 and second III-nitride semiconductor body 16. Similar to the second embodiment, gate structure 22 is disposed on field plate 25 only, unlike the third embodiment in which gate structure 22 and field plate 25 are both disposed on gate insulation body 28. Similar to the third embodiment, gate structure 22 in the fourth embodiment is a gate electrode which is capacitively connected to second III-nitride semiconductor body 16 through field plate 24, and gate insulation body 28.

**[0031]** Referring next to Figures 7 and 8, the field relaxation feature in a power semiconductor device according to the fifth embodiment is a plurality of spaced guard rings 26, which are disposed on second III-nitride semiconductor body 16 between gate structure 22, and second power electrode 20, and disposed around gate structure 22.

**[0032]** Referring to Figure 9, in the sixth embodiment of the present invention, gate insulation body 28 is interposed between second III-nitride semiconductor body 16, guard rings 26 and gate structure 22.

**[0033]** In the seventh embodiment of the present invention, as seen in Figure 10, gate structure 22 is disposed on second III-nitride semiconductor body 16, while guard rings 26 are

disposed on gate insulation body 28. Thus, unlike the fifth and sixth embodiments, guard rings 26 and gate structure 22 are not coplanar. Preferably, gate structure 22 includes a gate electrode which is electrically connected to second III-nitride semiconductor body 16 through a schottky connection.

**[0034]** Referring next to Figure 11, a power semiconductor device according to the eighth embodiment includes all the features of the sixth embodiment (Figure 9) and further includes a field insulation body 30 interposed between gate insulation body 28 and guard rings 26. Thus, similar to the seventh embodiment (Figure 10), guard rings 26 and gate structure 22 are not coplanar.

**[0035]** Referring next to Figure 12, a device according to the ninth embodiment of the present invention includes all of the features of the eighth embodiment except that field insulation 30 in the ninth embodiment beneath guard rings 26 is stepped thereby rendering guard rings 26 non-coplanar. That is, unlike guard rings 26 in the eighth embodiment, guard rings 26 in the ninth embodiment are not coplanar.

**[0036]** In the embodiments discussed above, guard rings 26 are independently floating. That is, guard rings 26 are not referenced to another potential, but are each floating.

**[0037]** Referring to Figure 13, in a device according to the tenth embodiment, guard rings 26 are shorted to one another, whereby all guard rings 26 are referenced to and floating at the same potential, rather than being independently floating.

**[0038]** Referring to Figure 14, in a device according to the eleventh embodiment of the present invention, guard rings 26 can be shorted to one another and shorted to first power electrode 18. Thus, guard rings 26 can be referenced to the potential of first power electrode 18.

**[0039]** Referring next to Figure 15, in a device according to the twelfth embodiment of the present invention, guard rings 26 are shorted to one another, and shorted to gate structure 22. Thus, guard rings 26 are referenced to the same potential as gate structure 22.

**[0040]** In a device according to any one of the embodiments of the present invention, first III-nitride semiconductor body is an alloy from the InAlGaN system, such as GaN, and second

III-nitride semiconductor body 16 is another alloy from the InAlGaN system having a band gap that is different from that of first III-nitride semiconductor 14, whereby a two-dimensional electron gas is formed due to the heterojunction of the first and the second III-nitride semiconductor bodies as is well known in the art. For example, second III-nitride semiconductor body may be formed with AlGaN.

**[0041]** In addition, support body 12 is a combination of a substrate material and if required a buffer layer on the substrate to compensate for the lattice and thermal mismatch between the substrate and first III-nitride semiconductor body 14. For economic reasons, the preferred material for the substrate is silicon. Other substrate materials such as sapphire, and SiC can also be used without deviating from the scope and the spirit of the present invention.

**[0042]** AlN is a preferred material for a buffer layer. However, a multi-layer or graded transitional III-nitride semiconductor body may also be used as a buffer layer without deviating from the scope and the spirit of the present invention.

**[0043]** It is also possible to have the substrate made from the same material as first III-nitride semiconductor body and thus avoid the need for a buffer layer. For example, a GaN substrate may be used when first III-nitride semiconductor body 14 is formed with GaN.

**[0044]** The gate electrode may be composed of n type or p type silicon, or polysilicon of any desired conductivity, and may further include an aluminum, Ti/Al, or other metallic layer over the top surface thereof. Ohmic electrodes may be composed of Ti/Al and may further include other metallic bodies over the top surface thereof such as Ti/TiW, Ni/Au, Mo/Au, or the like. Gate insulation body 28 may be composed of SiN, $Al_2O_3$, $SiO_2$, HfO, MgO, $Sc_2O_3$, or the like. Field insulation body 30 may be composed of $SiO_2$, SiN, $Al_2O_3$, HfO, MgO, $Sc_2O_3$, or the like. Guard rings 26 are preferably made of the same material as that used for the gate electrode to allow for single step fabrication of the gate electrode and guard rings 26.

**[0045]** Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

WHAT IS CLAIMED IS:

1. A power semiconductor device comprising:

a III-nitride based heterojunction, said heterojunction including a first III-nitride layer having a band gap, and a second III-nitride layer having another band gap over said first III-nitride layer;

a first power electrode electrically connected to said second III-nitride layer;

a second power electrode electrically connected to said second III-nitride layer;

a gate structure disposed between said first power electrode and said second power electrode; and

a field relaxation feature disposed over said second III-nitride layer adjacent said gate structure.

2. The power semiconductor device of claim 1, wherein said field relaxation feature includes an ultra resistive field plate.

3. The power semiconductor device of claim 2, wherein said field plate is disposed over said second III-nitride layer.

4. The power semiconductor device of claim 3, wherein said gate structure is disposed on said field plate and said second III-nitride layer.

5. The power semiconductor device of claim 3, wherein said gate structure is disposed on said field plate.

6. The power semiconductor device of claim 2, wherein said field plate is comprised of silicon rich SiN.

7. The power semiconductor device of claim 2, wherein said field plate is comprised of a compensated III-nitride semiconductor.

8. The power semiconductor device of claim 2, further comprising a plurality of floating field rings disposed over said field plate.

9. The power semiconductor device of claim 1, wherein said first III-nitride layer is comprised of GaN and said second III-nitride layer is comprised of AlGaN.

10. The power semiconductor device of claim 1, further comprising a base that includes a substrate, and a buffer layer disposed over said substrate and under said first III-nitride layer.

11. The power semiconductor device of claim 2, wherein said gate structure includes a gate insulation body.

12. The power semiconductor device of claim 11, wherein said gate insulation body is disposed between said field plate and said second III-nitride layer.

13. The power semiconductor device of claim 12, further comprising a plurality of floating field rings disposed over said field plate.

14. The power semiconductor device of claim 1, wherein said field relaxation feature includes a plurality of spaced guard rings.

15. The power semiconductor device of claim 14, wherein said guard rings are disposed over said second III-nitride layer.

16. The power semiconductor device of claim 14, wherein said gate structure includes a gate insulation body, and said guard rings are disposed over said gate insulation body.

17. The power semiconductor device of claim14, wherein said guard rings are disposed on an insulation body.

18. The power semiconductor device of claim 17, wherein said gate structure includes a gate insulation body and said insulation body is disposed over said gate insulation body.

19. The power semiconductor device of claim 18, wherein said guard rings are coplanar.

20. The power semiconductor device of claim 18, wherein said guard rings are non-coplanar.

21. The power semiconductor device of claim 20, wherein said guard rings are shorted to one another.

22. The power semiconductor device of claim 20, wherein said guard rings are floating.

23. The power semiconductor device of claim 20, wherein said guard rings are shorted to one of said power electrodes.

24. The power semiconductor device of claim 20, wherein said gate structure includes a gate electrode and said guard rings are shorted to said gate electrode.

25. The power semiconductor device of claim 14, wherein said guard rings are coplanar.

26. The power semiconductor device of claim 14, wherein said guard rings are non-coplanar.

27. The power semiconductor device of claim 14, wherein said guard rings are shorted to one another.

28. The power semiconductor device of claim 14, wherein said guard rings are floating.

29. The power semiconductor device of claim 14 wherein said guard rings are shorted to one of said power electrodes.

30. The power semiconductor device of claim 14, wherein said gate structure includes a gate electrode and said guard rings are shorted to said gate electrode.

31. The power semiconductor device of claim 14, wherein said first III-nitride layer is comprised of GaN and said second III-nitride is comprised of AlGaN.

32. The power semiconductor device of claim 14, further comprising a base that includes a substrate, and a buffer layer disposed over said substrate and under said first III-nitride layer.

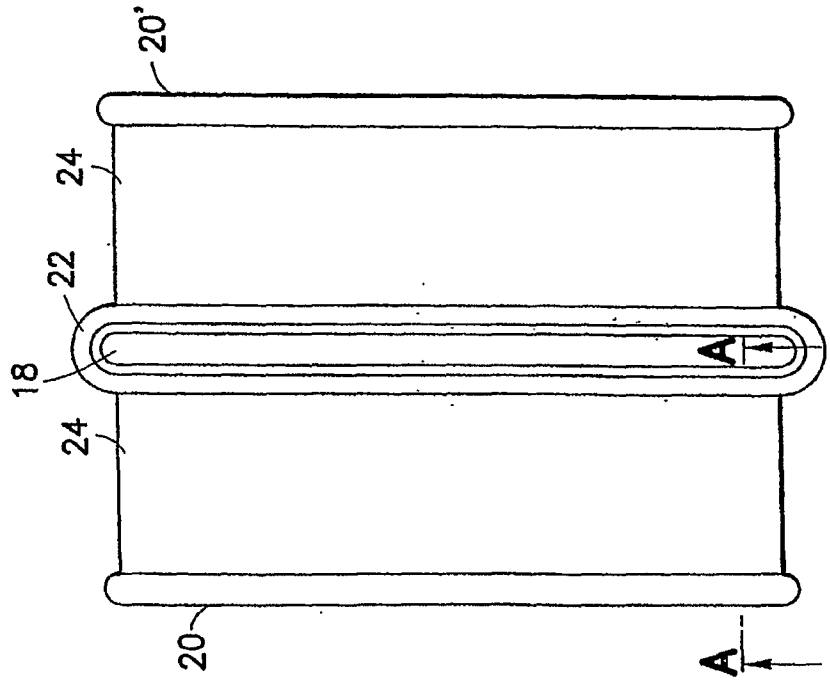

20'
24
22
18
24
20
A
A

FIG.1

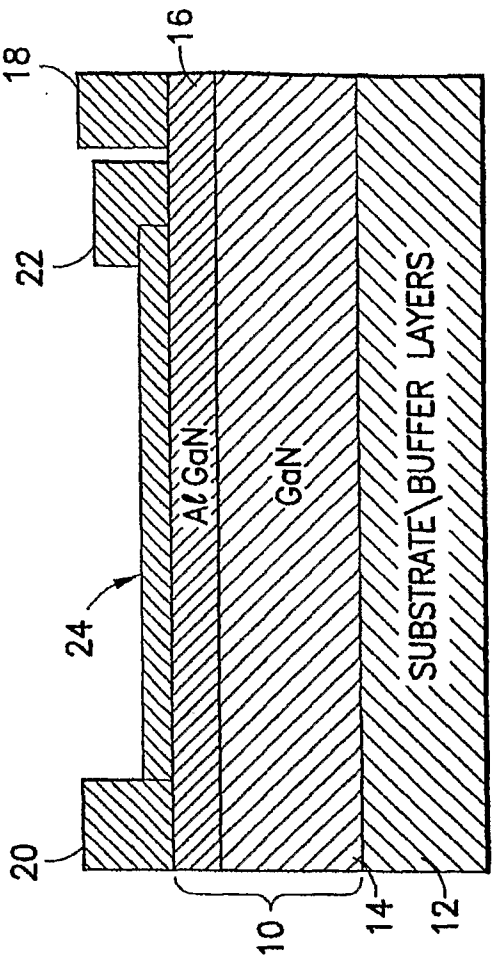

18
16
22
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AlGaN
GaN
SUBSTRATE\BUFFER LAYERS
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14
12

FIG.2

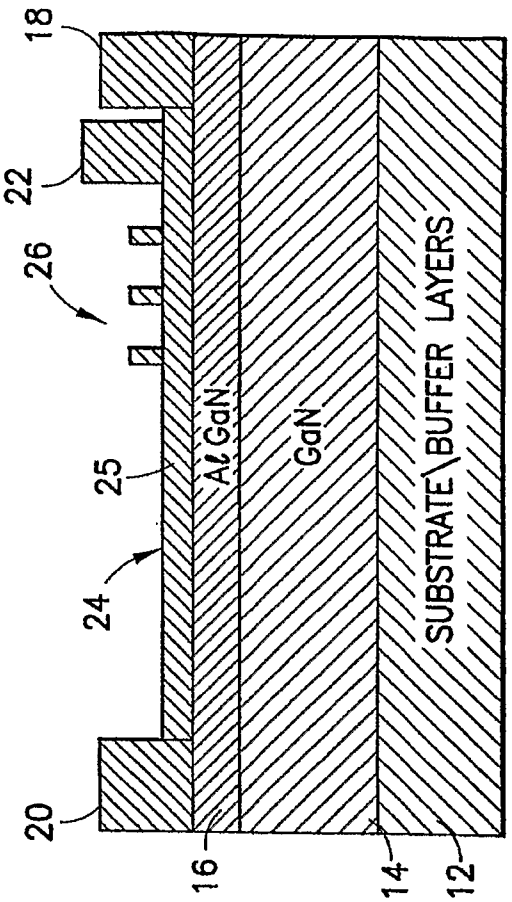

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AlGaN
GaN
SUBSTRATE\BUFFER LAYERS

FIG.4

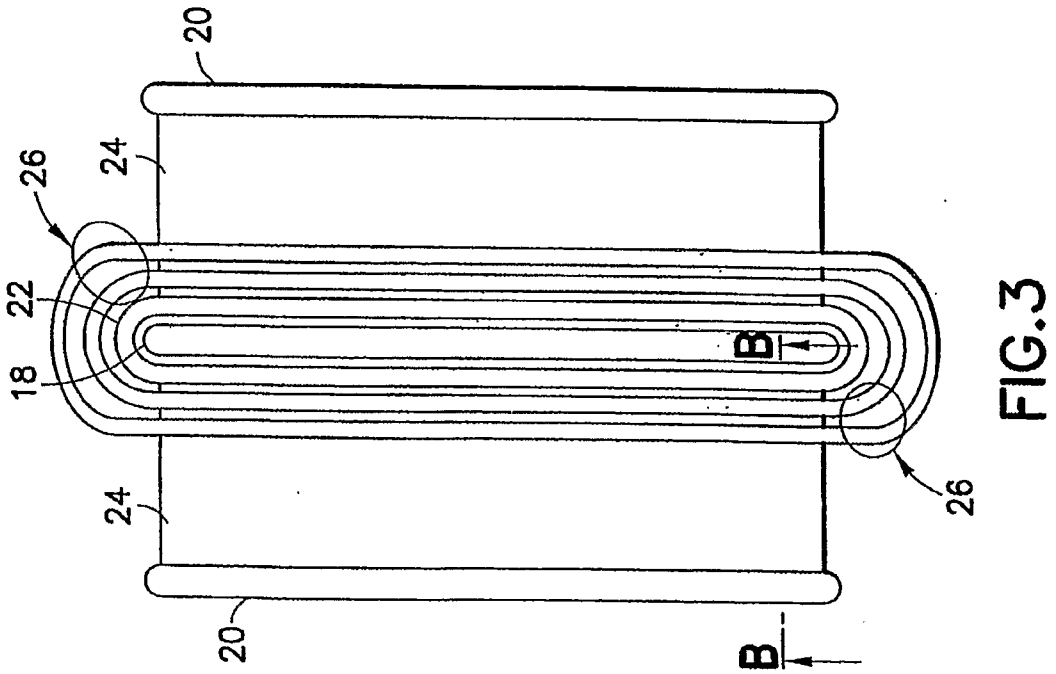

20
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22
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B
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20
26
B

FIG.3

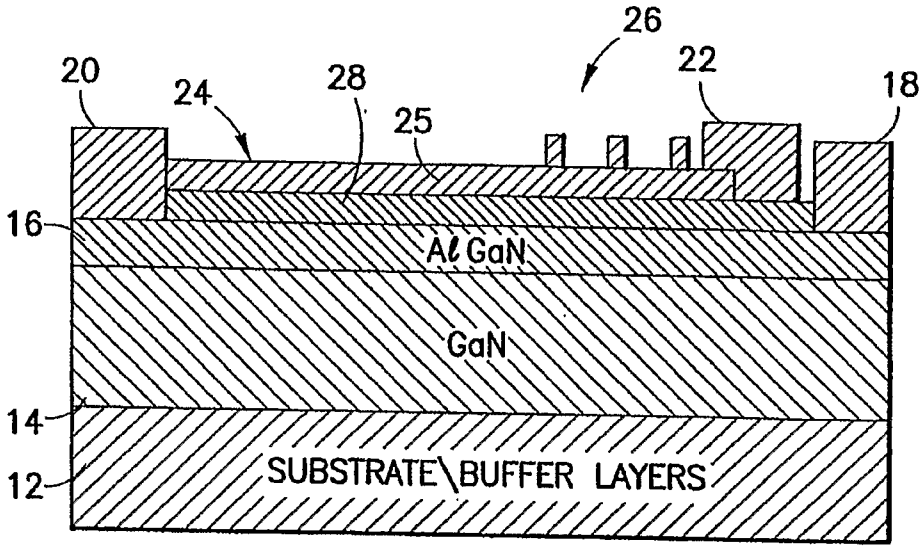

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AlGaN
GaN
14
12
SUBSTRATE\BUFFER LAYERS

FIG.5

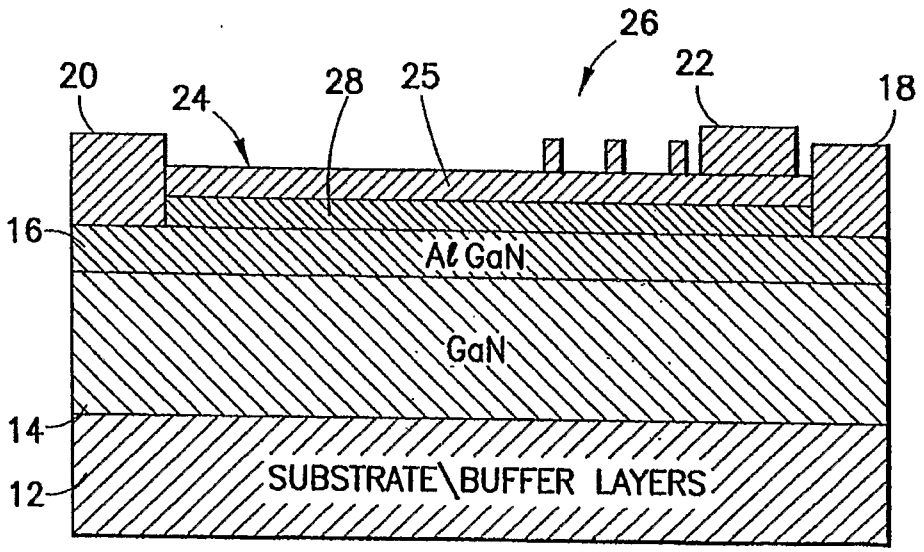

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AlGaN
GaN
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SUBSTRATE\BUFFER LAYERS

FIG.6

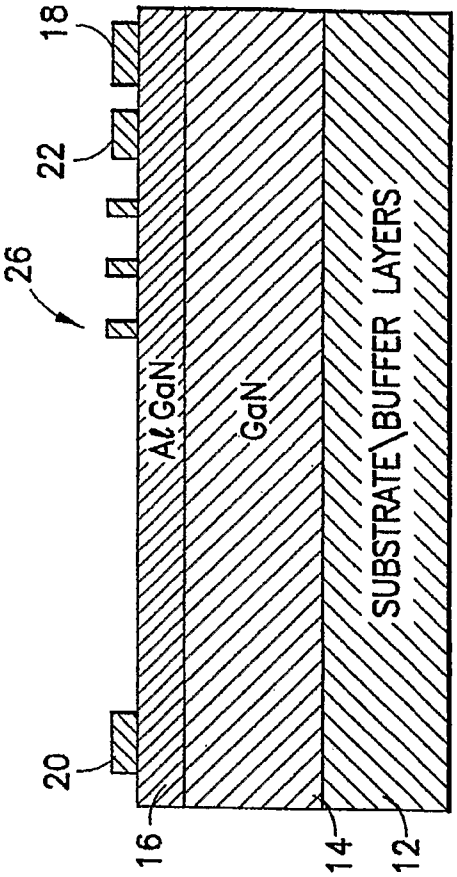



FIG.8

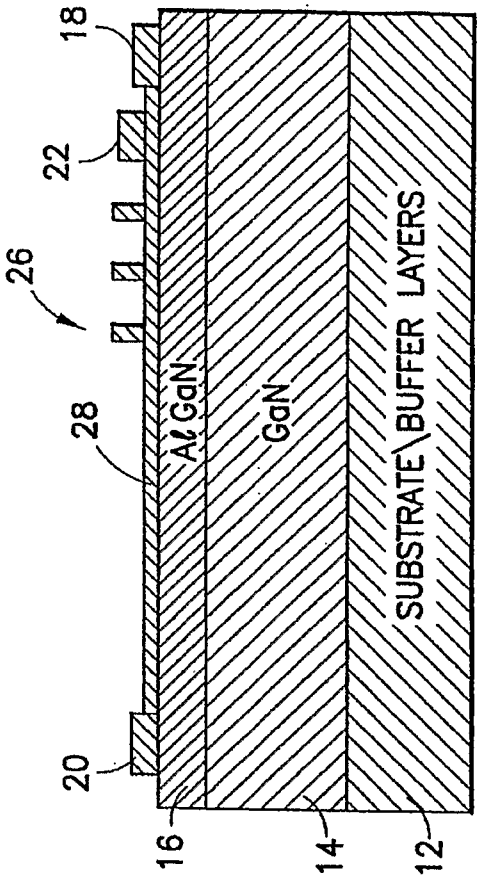



FIG.9

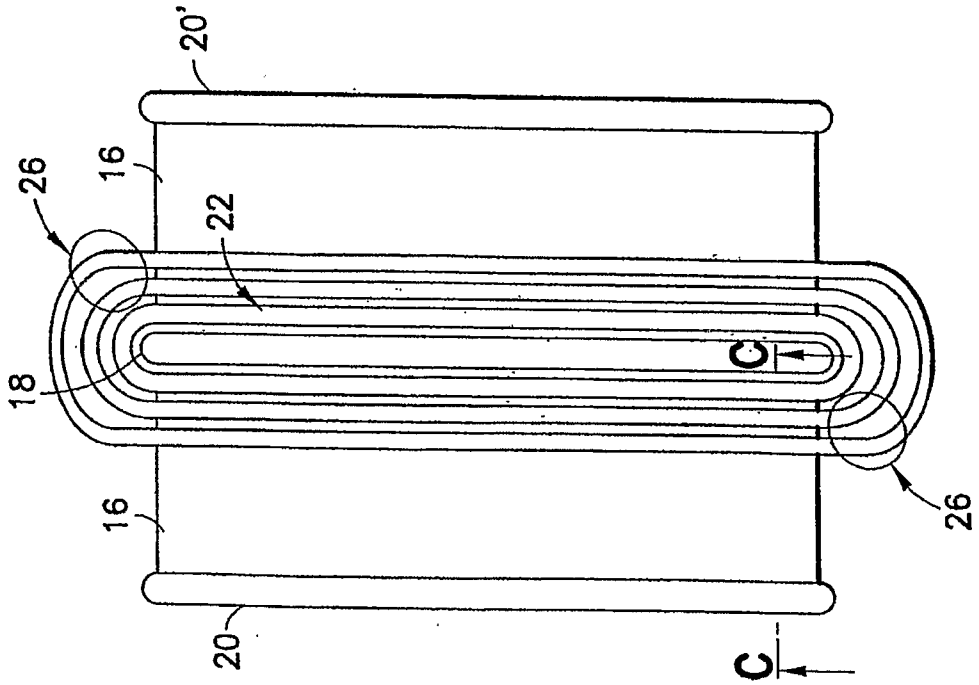



FIG.7

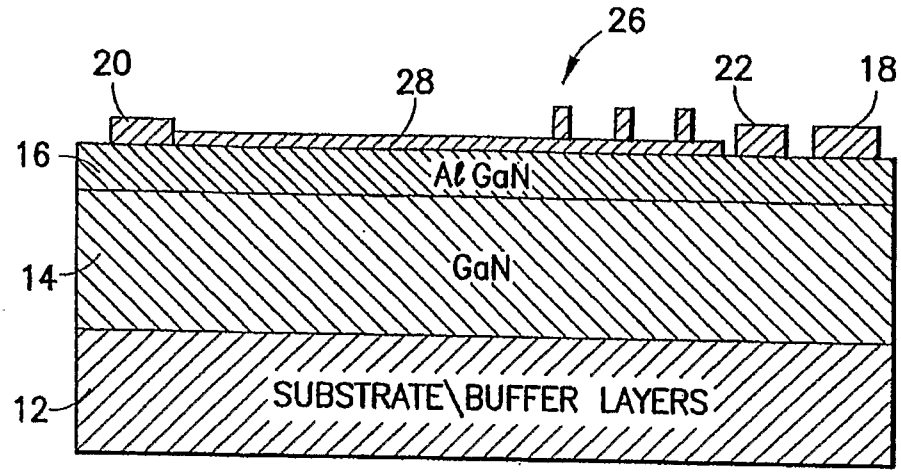

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Al GaN
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GaN
12
SUBSTRATE\BUFFER LAYERS

FIG.10

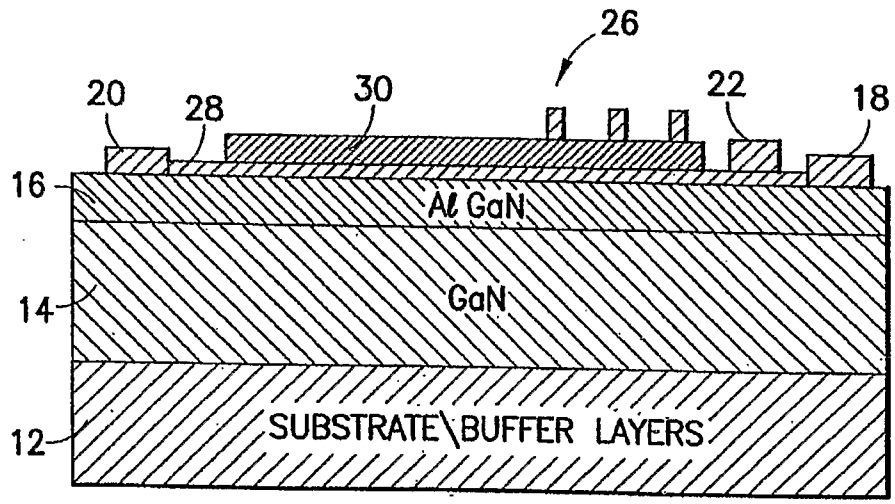

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Al GaN
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SUBSTRATE\BUFFER LAYERS

FIG.11

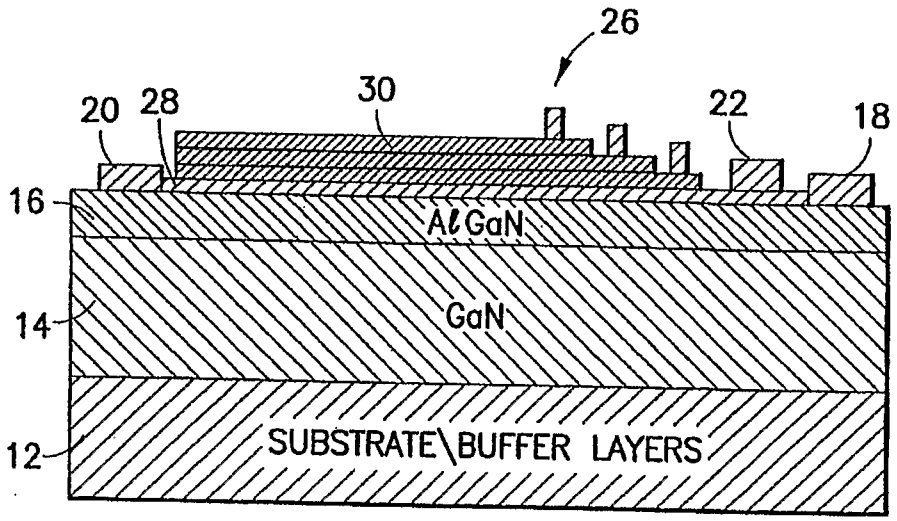

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AlGaN
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GaN
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SUBSTRATE\BUFFER LAYERS

FIG.12

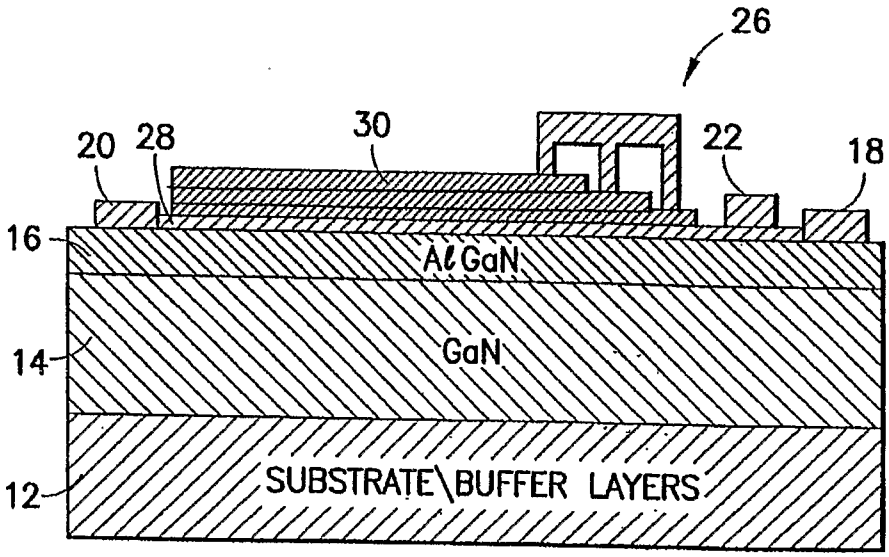

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AlGaN
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GaN
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SUBSTRATE\BUFFER LAYERS

FIG.13

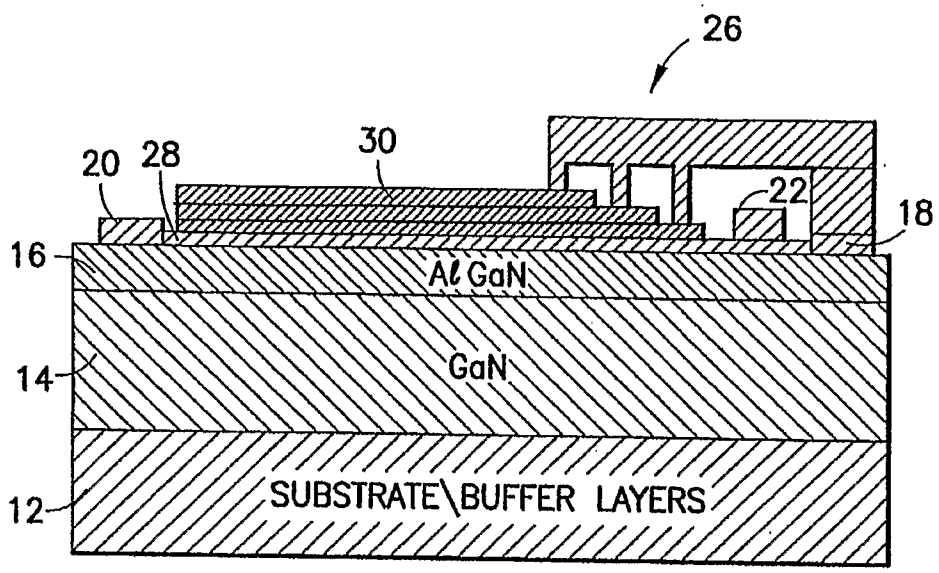

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SUBSTRATE\BUFFER LAYERS

FIG.14

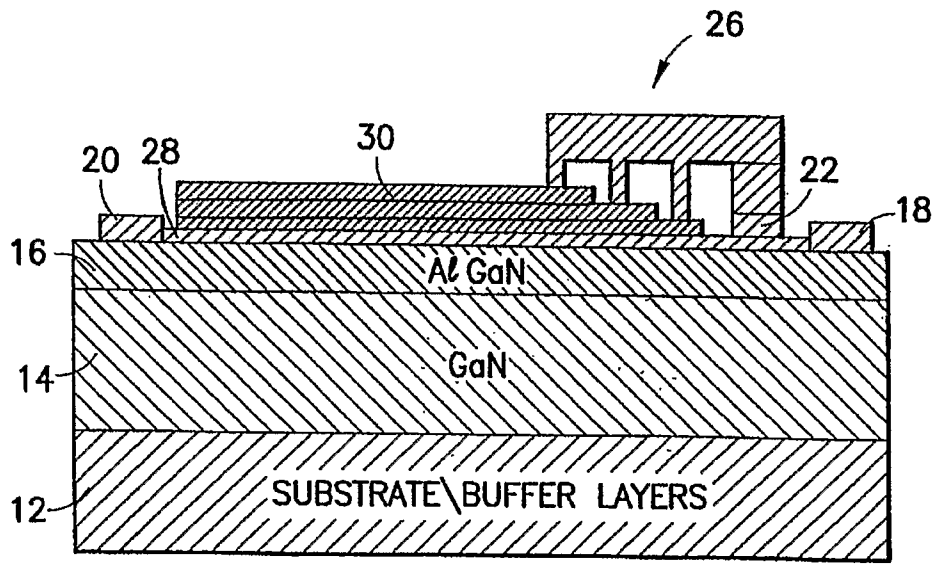

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Al GaN
14
GaN
12
SUBSTRATE\BUFFER LAYERS

FIG.15