

[54] **AUTOMATIC TRAFFIC CONTROLLER WITH PLURAL INPUT RECEIVER CIRCUIT**

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[22] Filed: **Apr. 23, 1971**

[21] Appl. No.: **136,938**

[52] U.S. Cl. **340/41**

[51] Int. Cl. **G08g 1/07**

[58] Field of Search 340/31 A, 31 R, 35, 340/36, 37, 40, 41; 235/150.24

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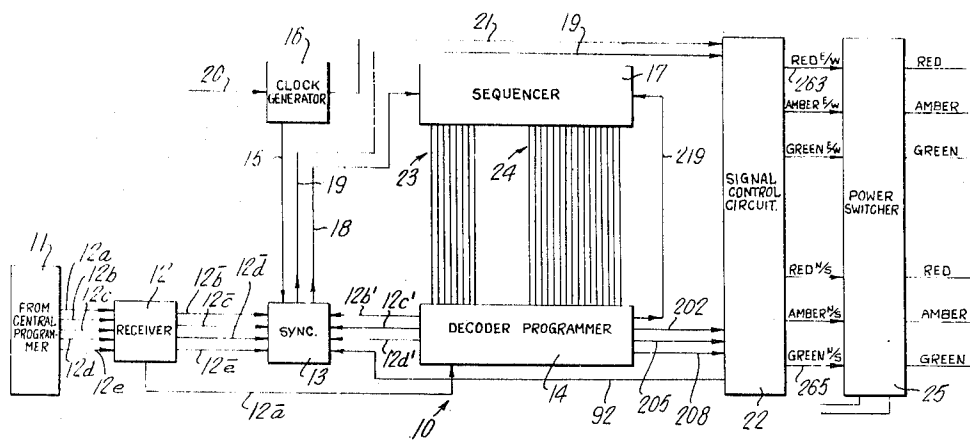
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[57] **ABSTRACT**

An automatic controller system for traffic signal lights comprising a receiver circuit for receiving a plurality of control pulses. A clock generator produces pulse signals exhibiting a particular frequency for enabling the various circuits. A sequencer circuit produces a plurality of output signals representative of a time count for the duration of a complete sequence cycle. A decoder-programmer circuit senses the output signals of the sequencer and generates control signals at preselected time intervals during the sequence cycle to cause sequential operation of said traffic signal lights. Synchronization means are further provided to synchronize each controller cycle at a time determined by the decoder-programmer. The sync. time may be made to occur at any time during the sequence cycle.

14 Claims, 15 Drawing Figures



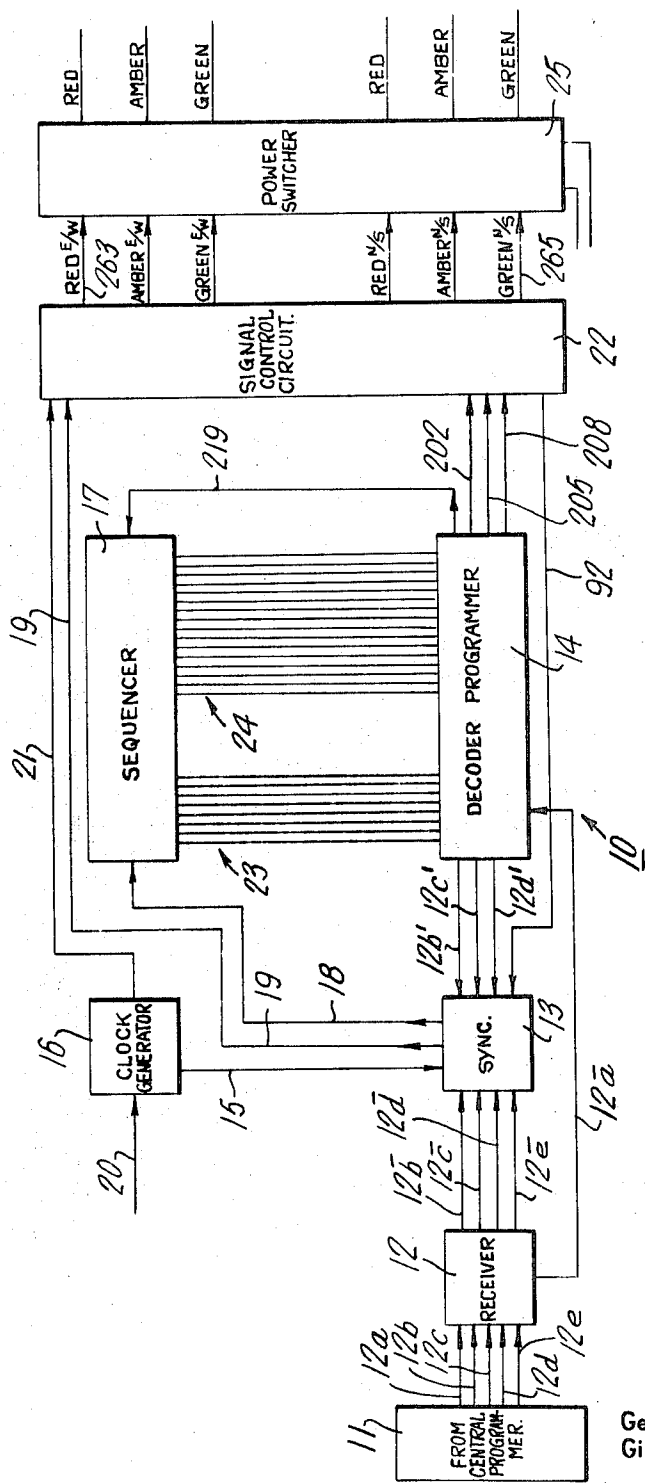
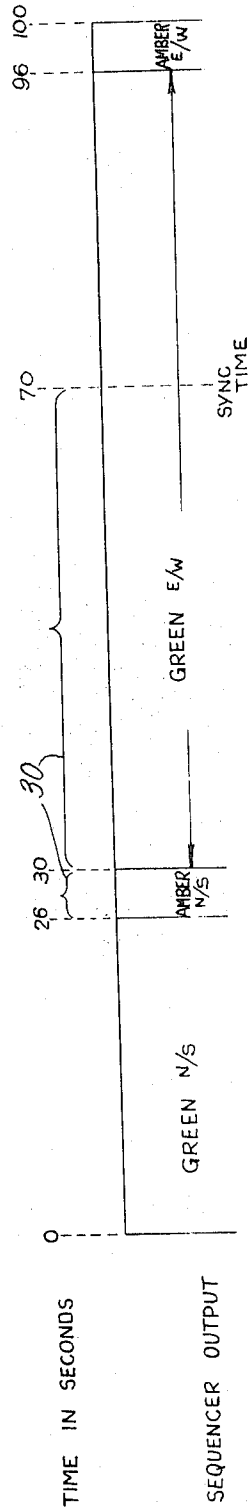
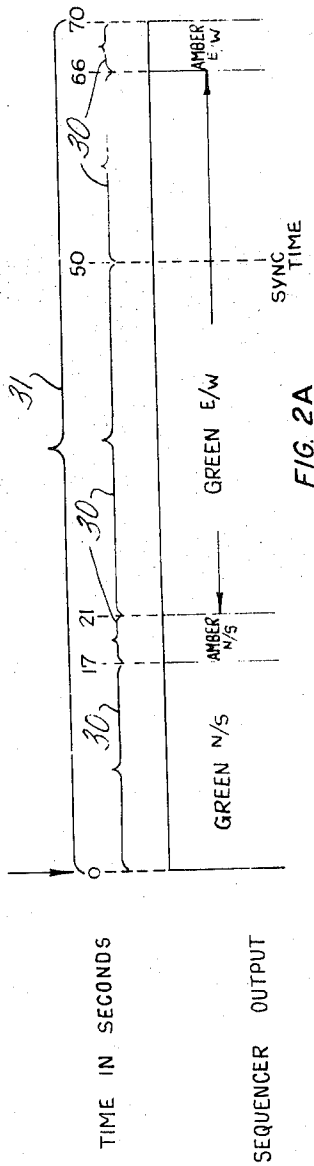


FIG. 1

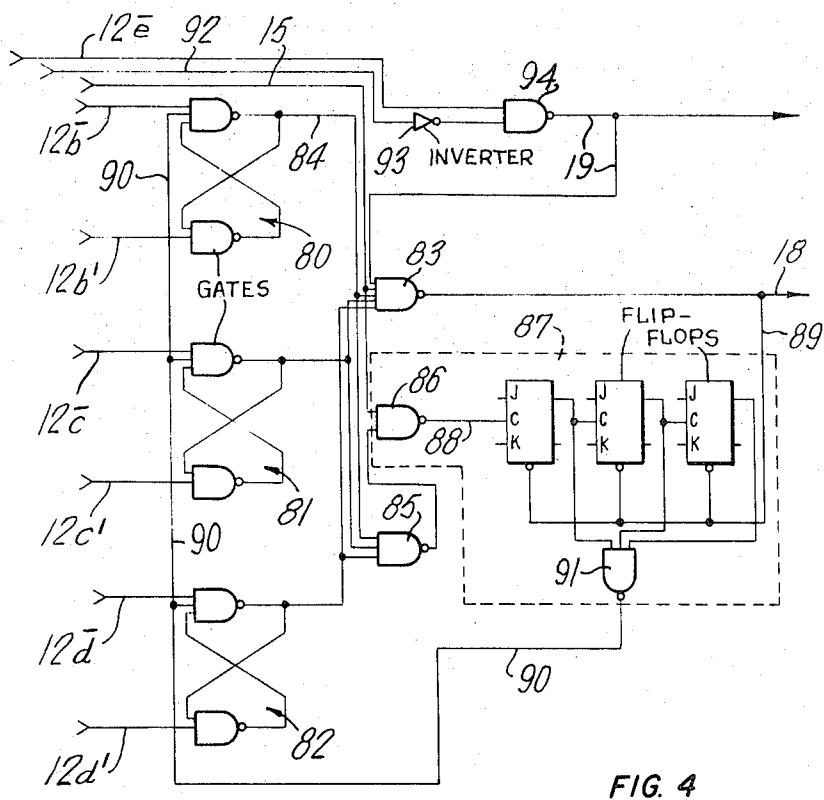
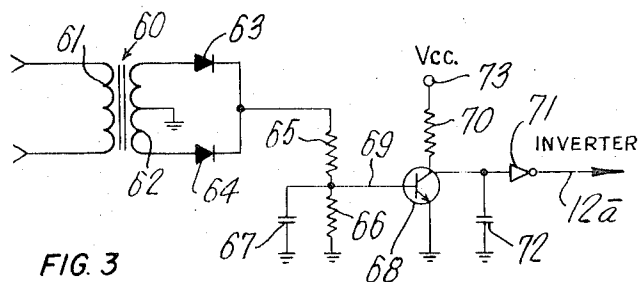
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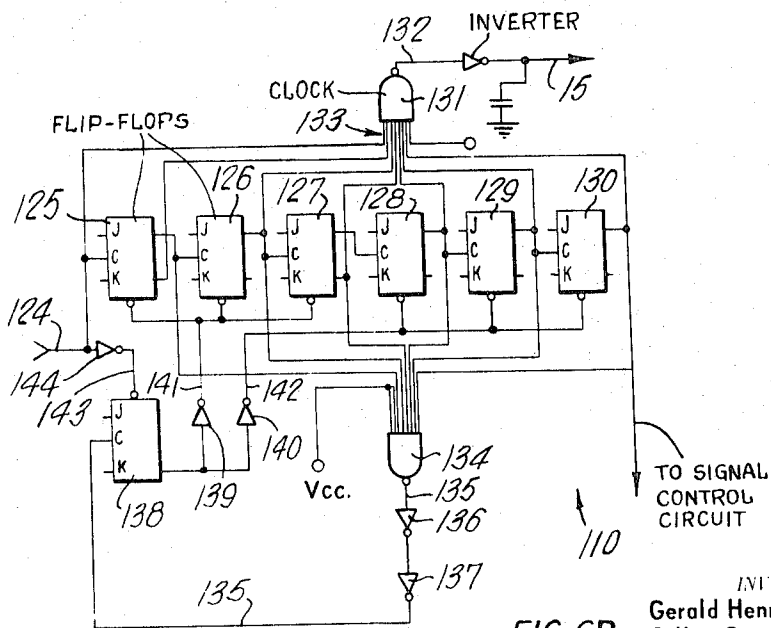
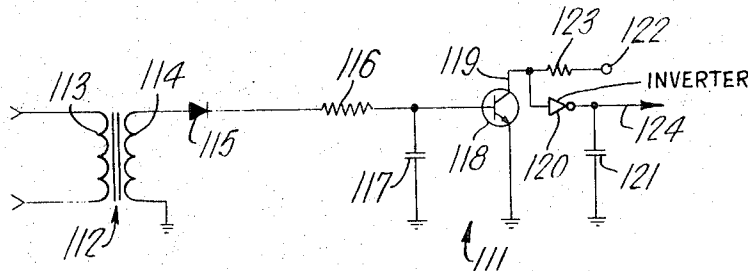
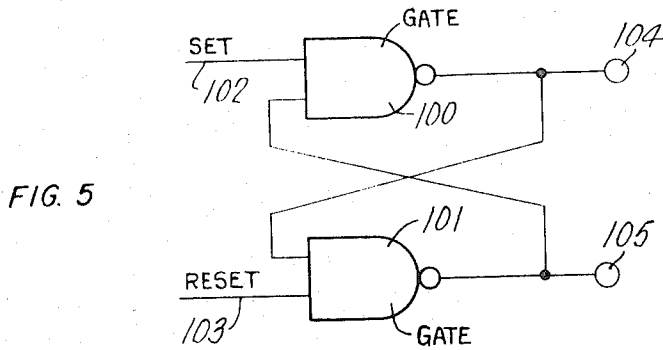
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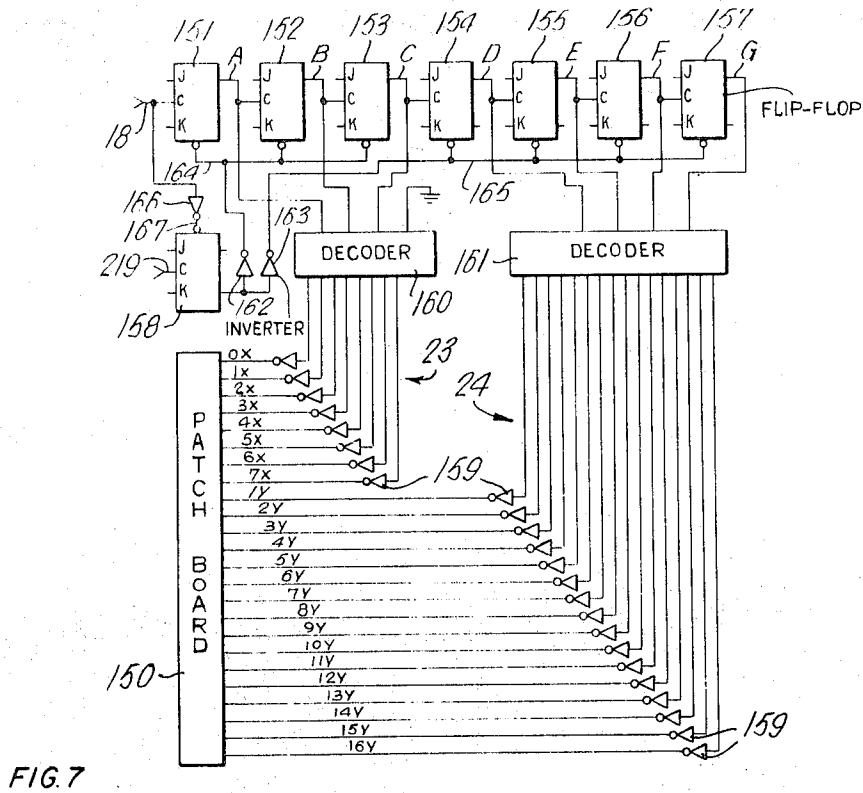


FIG. 7

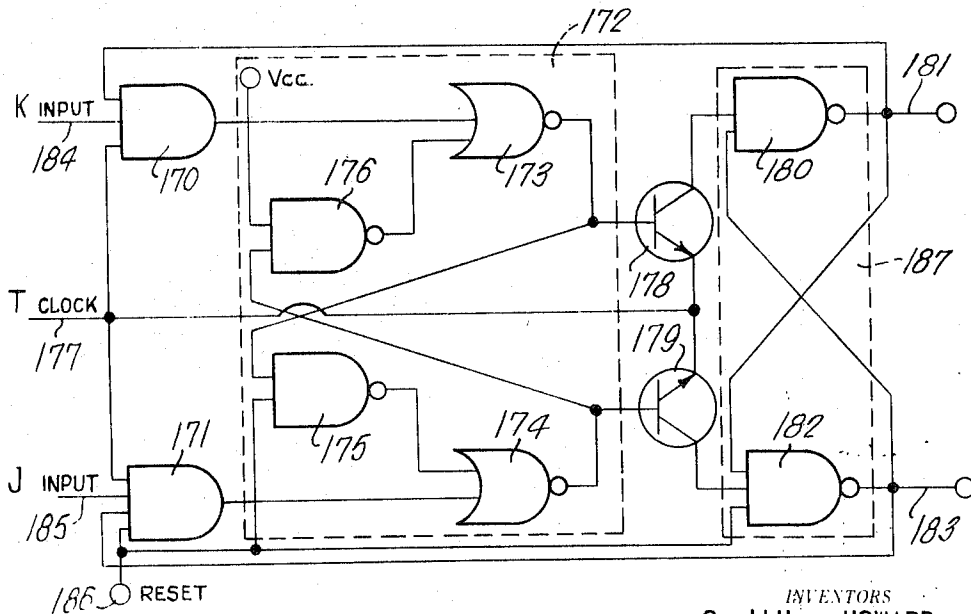


FIG. 8

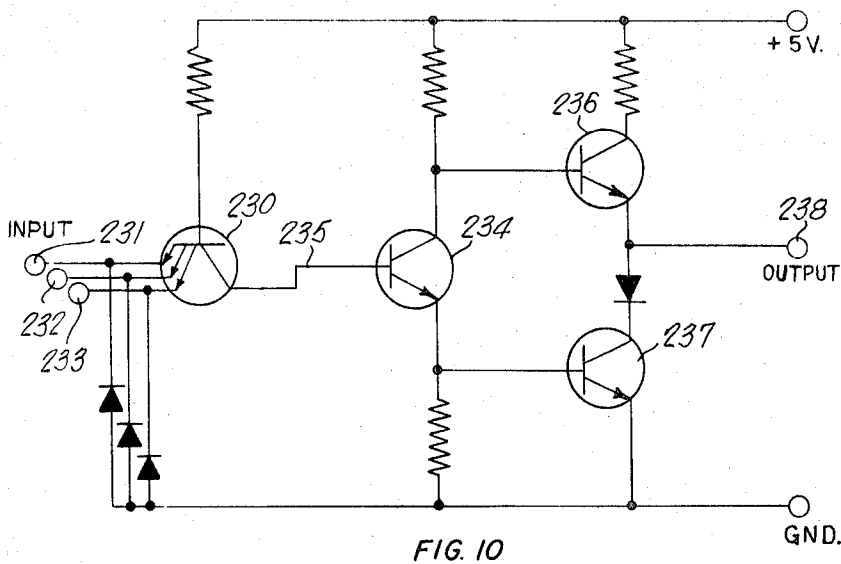
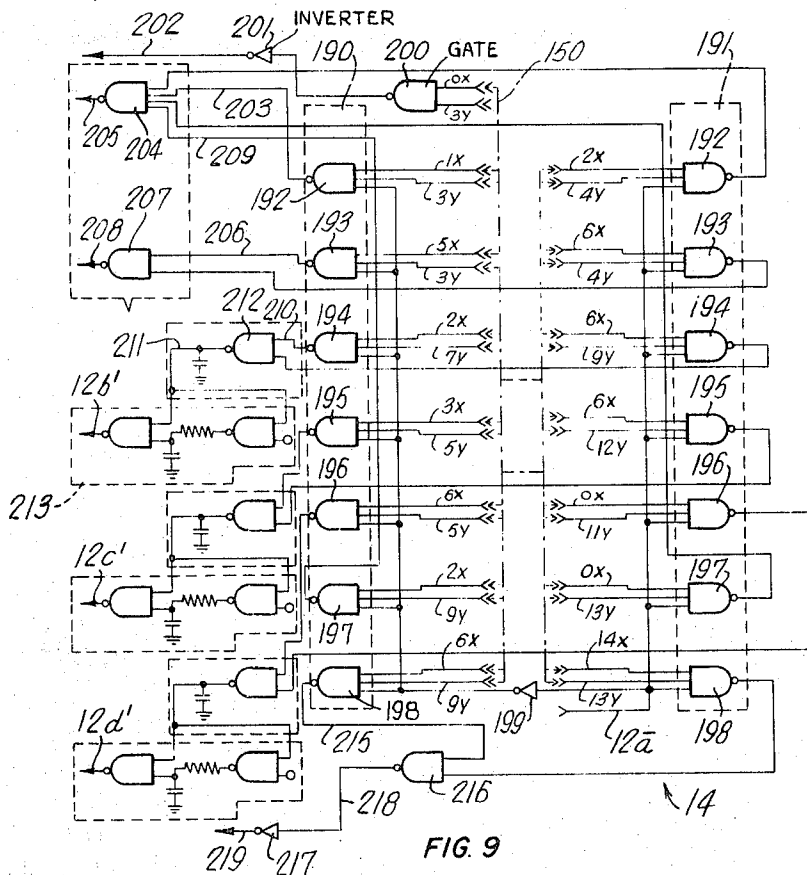
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Patented Oct. 2, 1973

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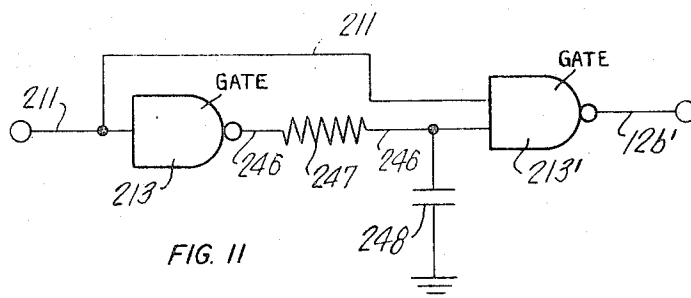


FIG. 11

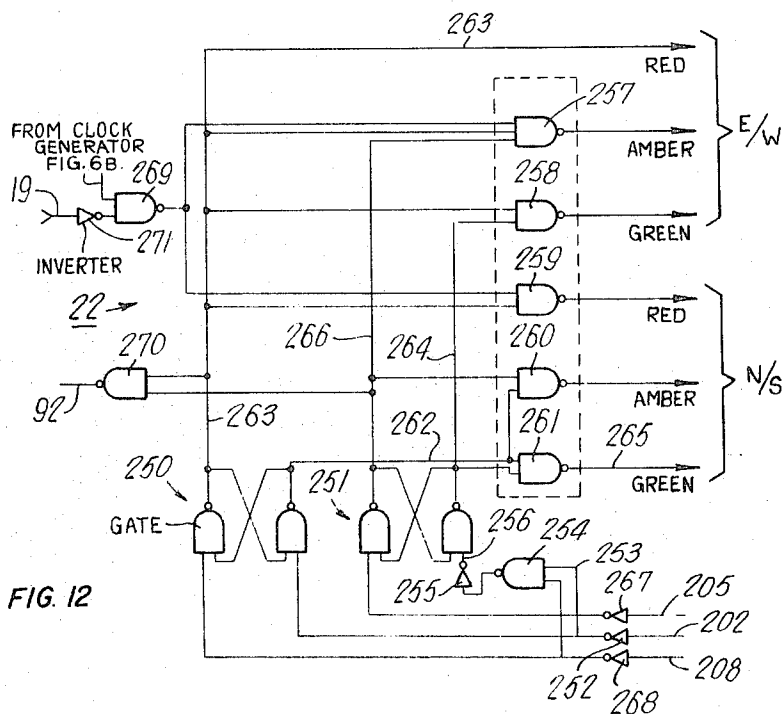


FIG. 12

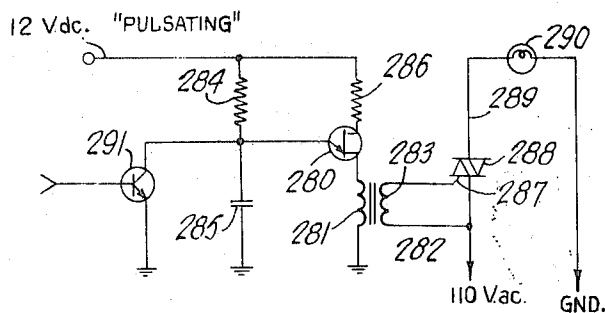


FIG. 13

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AUTOMATIC TRAFFIC CONTROLLER WITH PLURAL INPUT RECEIVER CIRCUIT

BACKGROUND OF INVENTION

1. Field of Invention

This invention relates to an automatic, solid-state, controller system particularly, but not exclusively, adapted to control traffic signal lights.

2. Description of Prior Art

The majority of traffic controller systems presently in use are of the electro-mechanical type utilizing switching relays and thermionic tubes. These types of controller systems have numerous disadvantages. The system's performance may be affected by rise and fall in temperatures above and below the normal average environmental temperatures. Further, the switching times of the mechanical switching devices are relatively long as compared with the switching times of semi-conductor switches. Also, a great many systems are still designed on a predetermined fixed cycle time and cannot be readily modified to change the cycle or sequence time of operation.

Further disadvantages of electro-mechanical controller systems are that the equipment is relatively bulky and requires frequent maintenance checks and replacement parts. Also, these systems operate directly from the common 117 volt AC supply and when a power failure occurs the system is rendered totally inoperative.

Still further disadvantages of electro-mechanical and semi-conductor systems known to date is that these are not constructed to be readily and easily changed to provide modifications in the sequence cycle times and synchronization. Also, these systems cause abrupt signal changes from the sequence to the flash modes, and are often the cause of vehicle collisions at intersections because of the sudden changes in the signals, i.e. RED to flashing AMBER.

SUMMARY OF INVENTION

It is a feature of the present invention to provide an automatic controller system equipped with synchronization and which substantially overcomes the above mentioned disadvantages.

Accordingly, from a broad aspect, the present invention relates to an automatic controller system for traffic signal lights comprising means for receiving a plurality of control pulses from a remote control station. Means are further provided for generating pulse signals exhibiting a particular frequency. A counter is adapted to produce a plurality of output signals representative of a time count for the duration of a complete sequence cycle. Means are further provided for sensing the plurality of output signals and to generate control signals at preselected time intervals during said sequence cycle to cause sequential operation of said traffic signal lights. Synchronization means are further provided to synchronize each controller cycle at a predetermined time during the sequence cycle.

BRIEF DESCRIPTION OF DRAWINGS

An embodiment of the invention will now be described with reference to the accompanying drawings in which:

FIG. 1 is a block diagram of the traffic controller system,

FIG. 2a is a chart illustrating the sequence times of a cycle,

FIG. 2b is a further chart illustrating a further sequence cycle,

FIG. 3 is a schematic diagram of the central control receiver circuit,

FIG. 4 is a detail block diagram of the synchronization circuit,

FIG. 5 is a schematic of the sync. enable flip-flop circuit,

FIG. 6a is a schematic diagram of the clock generator converter circuit,

FIG. 6b is a detail block diagram of the clock generator divider counter,

FIG. 7 is a detail block diagram of the sequencer circuit,

FIG. 8 is a schematic diagram of a J-K flip-flop circuit,

FIG. 9 is a block diagram of the decoder-programmer circuit,

FIG. 10 is a schematic diagram of a NAND gate circuit,

FIG. 11 is a schematic diagram of an RC delay, one-shot circuit,

FIG. 12 is a block diagram of the signal control circuit, and

FIG. 13 is a schematic diagram of a power switching circuit.

DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to the drawings and more particularly to FIGS. 1, 2a and 2b, there is shown a block schematic diagram of the automatic traffic signal light controller 10. The controller 10 is operated from a central programmer 11 remotely located, as for instance at a central traffic control office. The central programmer 11 is connected to a central control receiver circuit 12 at the input of the controller 10 and can provide 117 volts signals on five distinctive input connections 12a, 12b, 12c, 12d and 12e to the receiver 12. Connection 12a connects the cycle control signal which when no voltage is present provides a 70 second sequence cycle (see FIG. 2a) for the signal lights and when a 117 volt signal is present enables the 100 second sequence cycle (see FIG. 2b). Connections 12b, 12c and 12d provide three different synchronization modes which are preselected and patched in the decoder-programmer 14. Only one of these sync. mode circuits are utilized at any given time. Connection 12e provides a flash mode input to switch the traffic signal lights to flashing RED and AMBER.

The input signals received at the receiver 12 are converted into binary 1 or 0 signal outputs, the 1 corresponding to +5 v.d.c. and the 0 to ground. Each of the sync. mode connections and the flash mode are connected to a synchronization circuit 13 via output connections 12b, 12c, 12d and 12e, respectively. The cycle control signal input lead 12a is connected to a decoder-programmer circuit 14 via output lead 12a.

The synchronization circuit 13 synchronizes each sequence cycle of each controller 10 in a traffic network installation comprising a plurality of controllers 10. The sync. circuit 13 is able to synchronize the controller at three different preselected times, from the start of the sequence cycle, in one of the two cycles 31 (FIGS. 2a and 2b). These time intervals are patched in the decoder-programmer 14 before installation. A pulse corresponding to the time stored is fed back to

the sync. circuit 13 via one of the leads 12b', 12c', and 12d' depending on which sync. circuit is enabled.

Clocking pulses for the system are provided by a clock generator 16 which is connected to the 60Hz line voltage at 20. The 60Hz voltage is converted and divided to provide clock pulses, at 1 second intervals, on output connections 15 and 21. Output connection 21 provides the clocking pulses for the RED and AMBER flashing mode, when enabled. Output connection 15 is connected to the sync. circuit 13 which provides the clocking pulses to trigger the sequencer circuit 17, via connection 18, every one second until disabled by the sync. signal pulse fed back to the sync. circuit 13 by the decoder-programmer 14. At that point, the sequencer circuit 17 is disabled. The sync. pulse from the central programmer 11, via receiver 12 and respective connections, will then enable the sequencer 17 to start its next duration cycle when the first clocking pulse is received on connection 18. An 8 second counter is built into the sync. circuit 13 to re-trigger the sequencer circuit 17 should the sync. pulse from the central programmer 11 be late in arriving at the sync. circuit 13.

Flash control connection 19 connects the binary enabling flash signal thereon to initiate the flash mode.

The sequencer circuit 17 is a binary-up counter that can produce a count up to 128 seconds. The output of the sequencer circuit is fully decoded to eight x output connections, group 23, and 16 y output connections, group 24. These outputs are wired to a patch board, which will be described later, in the decoder-programmer 14 to facilitate the decoding of any one of the possible 128 conditions which will enable the various lights during the time sequences 30 of the time sequence cycle 31 in use (see FIGS. 2a and 2b).

The decoder-programmer 14 senses the sequencer outputs and provides the enabling pulses to the signal control circuit 22 which through the power switcher circuit 25 causes the various signal lights to illuminate for a predetermined period of time corresponding to their respective time sequence 30 of the sequence cycle 31. The decoder-programmer 14 also supplies a sync. pulse to the sync. circuit 13 at the proper patched time or condition of the sequencer outputs. When the sequencer has completed a sequence cycle (assuming the 70 second cycle, FIG. 2a), a signal is applied to the sequencer circuit 17 via lead 219 causing the counter to reset and await the next clock pulse from the sync. circuit 13 before starting the next sequence cycle.

The signal circuit 22 comprises a plurality of control gates which senses the input signals from the decoder-programmer 14 and the sync. circuit 13 and provide the proper signals to the power switcher circuit 25 which enables the signal lights during the time sequences of the sequence cycle mode or during the flashing mode.

Referring now to FIG. 3, there is shown the detail schematic diagram of one of the converting circuits of the receiver circuit 12. This circuit merely converts the 117 volts AC input impulses on its associated input line to +5 volt DC logic output level. When 117 volts AC is received on the primary winding 61 of step down transformer 60, the voltage is stepped down to 3.5 volts by the secondary winding 62 and then rectified by means of diodes 63 and 64 connected to each side of the secondary winding 62. The output from the diodes 63 and 64 constitutes the full wave rectified 5 volt signal voltage. This voltage is connected to a resistor 65

which is connected in series to a resistor 66. A capacitor 67 is connected in parallel with resistor 66 and together with resistor 66 and 65 constitutes a low pass filter network. The voltage at the junction of resistors 65 and 66 is applied to the base of transistor 68 via connection 69. Resistor 70 connected to the collector of transistor 68 provides the proper collector voltage from terminal 73 where a constant 5 volt DC supply voltage is present. The collector of transistor 68 is also connected to an inverter 71 which inverts the logic level of the input signal. If the input function is a logic 1, (5 volts DC), the output is a logic 0. The inverter circuit works identically as the NAND gate circuit employed which will be described later. The only difference between the inverter and the NAND gate circuits is the number of inputs. The inverter 71 has only one input whereas the NAND gate has two to 20 inputs. Capacitor 72 connected to the input of the inverter 71 is provided to suppress any noise on the voltage signal at the collector of transistor 68.

When no 117 volts AC signal is applied to the primary winding 61 of step down transformer 60, transistor 68 is cut off, providing a logic 1 at the input of the inverter 71. Inverter 71 will then provide a logic 0 at its output. The rise and fall time of the receiver circuit 12 is made long enough to prevent transient and short duration pulses of 117 volts AC from affecting transistor 68. This feature will also remove false operation of the controller due to relay chatter from the central control programmer 11. A 100 milli-second or longer pulse is required for proper operation of the receiver 12.

Referring now to FIG. 4, there is shown the detail wiring of the sync. circuit 13. The main function of the sync. circuit is to keep the street intersection controller unit 10 synchronized with the central control programmer 11 which is located at the far end. The sync. circuit 13 is able to synchronize the controller 10 at any one of three different intervals in the sequence cycle. These sync. intervals are determined locally and require patching at the patch board in the decoder-programmer 14 for incorporation into the system. The sync. mode connections 12b, 12c and 12d not in use have logic 0's thereon. The connections from the receiver 12 and decoder-programmer 14 as described earlier, are shown herein connected to sync. enabled flip-flop circuits 80, 81 and 82, which will be described in detail later with reference to FIG. 5. A logic 0 on input leads 12b, 12c or 12d keeps the sync. enable flip-flop circuits locked in the set condition which provide a continuous logic 1 signal to the sequencer clock gate 83.

Assuming that a logic 1 signal is present on the first sync. mode, connection 12b and the first sync. decoder lead 12b' from the decoder is also at a logic 1. Also assuming that the first sync. circuit is patched to synchronize at 50 seconds, the sequencer circuit 17 will progress through the sequence cycle and at the 50 second count the decoder-programmer 14 will provide a momentary logic 0 signal (sync. enable signal) on lead 12b' to the reset side of the enable flip-flop circuit 80. Flip-flop circuit 80 will toggle and provide a logic 0 on output lead 84 which is connected to one input of the sequencer clock gate 83, and a logic 0 on the input of timer enable gate 85. The sequencer clock gate circuit 83 disables the clock pulse to the sequencer circuit 17 on lead 18 and the timer enable gate 85 provides a logic 1 on the input of a timer clock gate 86 which in turn

feeds a clock pulse to a time delay counter herein-shown an eight second counter 87 via lead 88. Herein-shown the timer clock gate 86 forms part of the eight second counter circuit 87.

If the sync. pulse from the central control programmer 11 is received within 7 seconds after the 8 second counter 87 is enabled, it will set the sync. enable flip-flop 80 by providing a momentary logic 0 on the sync. enabled lead 12b. This will re-enable the sequencer clock gate 83 to provide once again the clock pulses to the sequencer 17 via lead 18. It will also remove the clock pulse to the 8 second counter 87 by placing a logic 1 on the input of the timer enable gate 85 which in turn places a logic 0 at the input of the timer clock gate 86. It is noted that the reset lead 89 is connected to lead 18 of the sequencer circuit and every clock pulse on this lead will reset the 8 second counter back to 0. Therefore, the 8 second counter is reset by the clocking pulses from gate 83 and becomes ready to count 8 seconds on the next sync. pulse from the decoder-programmer circuit 14.

Assuming that the sync. pulse from the central programmer 11 was not received within the 7 second count of the 8 second counter 87, then, at the count of 7, the 8 second counter 87 would transmit a logic 0 on output lead 90 via a timer decoder gate 91. Output connection 90 connects the logic 0 to the set side of the first enable flip-flop 80 and the same sequence of operation as described hereinabove will be repeated with the exception that it will have delayed the sequencer circuit 17 by an 8 second count. The 8 second timer circuit 87 is provided to delay the sequencer 17 by a maximum of 8 seconds every sequence cycle in case the controller 10 is ahead of the central control programmer sync. pulse. A maximum of 8 complete sequence cycles is necessary to re-synchronize the controller 10 with the central programmer 11.

The sync. circuit 13 also includes a flash enable gate circuit 94 to change the controller to the RED and AMBER flashing mode. During normal RED-AMBER-GREEN operation, the flash signal lead 12e has a logic 0 thereon (no voltage). The flash control lead 92 from the signal control circuit 22 is normally at a logic 1 and consequently the signal on lead 92 (inverted by inverter 93) provides a logic 0 output which is then applied to the input of the flash enable gate 91. The output lead 19 from the flash enable gate 91 is thus at a logic 1.

When the RED and AMBER flashing mode is activated, a logic 1 appears on the flash signal lead 12e, from the receiver circuit 12, and is fed to one of the inputs of the flash enable gate 91. The controller unit 10 continues to operate in the RED-AMBER-GREEN mode until the signal lights switch to AMBER E/W and RED N/S. At this particular time of the sequence, a logic 0 is transmitted to the input of inverter 93 via lead 92. The output of inverter 93 provides a logic 1 on the input of the flash enable gate 91 which now provides a logic 0 at its output lead 19 and consequently to the signal control circuit 22. A logic 0 is also provided to the sequencer clock gate 83 via lead 19, thus the sequencer is disabled and, therefore, locking at this point. The signal control circuit 22 automatically switches to the RED-AMBER flashing mode which is activated by the clocking pulses from the clock generator 16 fed to the signal control circuit via lead 21.

FIG. 5 illustrates the basic operation of the sync. enable flip-flop circuits 80. The circuit comprises two NAND gates 100 and 101 which will be described later with reference to FIG. 10. Assuming the set and reset input leads 102 and 103, respectively, have a logic 1 (5 volts DC) thereon, then for either gate, a 0 would be produced at the output. Because the outputs are crossed coupled to the input of each gate 100 and 101, the two outputs must be in opposite states, i.e. a 1 on terminal 104 and a 0 on terminal 105, or vice versa.

If a 0 is applied to the reset input lead 103 and a 1 to the set input lead 102, the output terminal 105 must become a 1 and terminal 104 a 0. If the set input is a 0 and the reset input is a 1, then terminal 104 becomes a 1 and terminal 105 becomes 0. By applying a momentary 0 level to the reset or set input, the output will become 1 or 0 as desired. The output will remain in this state until a 0 is applied to the alternate input.

Referring now to FIGS. 6a and 6b, there is shown a sine-to-square-wave circuit 111 and a divide-by-60 counter circuit 110, both of which constitute the clock pulse generator 16. As shown in FIG. 6a, the sine-to-square-wave converter 111 is connected to the 117 volt 60 cycle power line via a step-down transformer 112 comprising a primary winding 113 and a secondary winding 114. The voltage at the secondary winding 114 is dropped to 6.3 volts AC and rectified by a diode 115. The signal at the output of diode 115 is applied to a low pass filter network constituted by a resistor 116 and capacitor 117. The output from the low pass filter or resistor 116 is applied to the base of switching transistor 118. Transistor 118 is selected to have a fast rise and decay time which is important for the divide-by-60 counter circuit 110, which will be described later. When the rectified signal voltage rises towards 6.3 volts, transistor 118 saturates at approximately 0.7 volts, causing the collector output 119 to drop to a logic 0. When the rectified signal drops below 0.7 volts, transistor is cut off and the collector output 119 rises to a logic 1 level. To improve the rise and fall time of the 60 cycle signal, an inverter 120 is connected to the collector of transistor 118 and the output of the inverter 120 has sufficiently fast rise and decay times for proper operation of the divide-by-60 counter. Capacitor 121 connected to the output of the divider suppresses any noise on the output voltage signal. Terminal 122 is connected to the 5 volt DC supply and resistor 123 provides the proper voltage to provide a logic 1 to input of inverter 120 when transistor 118 is cut off. The output signal from the inverter 120 is applied to the input of the divide-by-60 counter 110 via lead 124.

Referring now to FIG. 6b, there is shown the detail construction of the divide-by-60 counter 110 as comprising six flip-flops 125 to 130, respectively, and constituting a binary-up counter of 64. A clock decoder gate 131 is connected to the output of the flip-flops 125 to 130 and the output 132 of the clock decoder 131 goes to a logic 0 signal every time flip-flops 126, 128, 129 and 130 are in the set condition and flip-flops 125 and 127 are in the reset condition. The clock decoder inputs 133 are then all at logic 1 level. This condition occurs every time the counter (flip-flops 125 to 130) reaches a count of 58. At count 59, a clock reset gate 134 which is also connected to the outputs of flip-flops 125 to 130, provides a logic 0 at its output 135. The output of the clock reset gate 134 is inverted twice by inverters 136 and 137 to provide a logic 0 to toggle the

flip-flop circuit 138. When flip-flop circuit 138 toggles, it provides a logic 1 at the inputs of inverters 139 and 140 which in turn provide logic 0's on their respective reset lines 141 and 142. The signal on the reset lines resets the divide-by-60 counter 110. The reset of the counter 110 occurs when the 60 cycle pulse from the square wave converter is at a logic 0. When the 60 cycle pulse returns to logic 1, it resets flip-flop circuit 138 because a logic 0 is applied to connection 143 of flip-flop 138 by inverter 144. The inverters 136 and 137 connected to the output of the clock reset gate 134 serve only to delay sufficiently the reset pulse which is connected to the flip-flop 138 via lead 135.

A feature of the clock generator 16 is that it can feasibly be operated, at a street intersection, on a 12 volt DC supply, by merely replacing circuit 111 with a transistor 60Hz oscillator. This would be advantageous where a municipality would want to protect its systems in case of power failures. A stand-by 12 v.d.c. battery could feasibly operate the system for several hours. The only part of the unit which would require modification would be the signal power drivers which will be described later. These would have to be converted to 12 volts DC.

Referring now to FIG. 7, there is shown the sequencer circuit 17. The sequencer is a binary-up counter counting up to 128 seconds and providing fully decoded outputs of eight x and 16 y outputs. These outputs are wired to a patch board 150 in the decoder programmer 14 to facilitate the decoding of any one of the 128 conditions. By patching any one of x outputs with any one of y outputs to any one of the decoder NAND gates (which will be described later), it is possible to select any one of the counter output counts. Referring to the schematic as shown in FIG. 7, it is noted that the first three stages of the counter comprising flip-flops 151, 152 and 153, are wired to a "one of 8" decoder 160, while the last four states, flip-flops 154, 155, 156 and 157, are wired to a "one of 16" decoder 161. The sequencer 17 can be reset to a count of 0 by patching the desired x and y outputs to the reset gate in the decoder programmer, which will be described later. This feature permits the controller to have any sequencer cycle required with a maximum sequence cycle duration of 128 seconds. If longer sequence cycle durations are necessary, the clock frequency must be lower.

The sequencer 17 is the heart of the controller circuit 10. It supplies all pulses necessary for the function of the controller. It consists, as mentioned hereinabove, of a binary counter that produces 128 different codes (flip-flops 151 to 157), a reset flip-flop 158, a one-of-8 decoder 160 and a one-of-16 decoder 161, and inverters 159 are provided at each output of the decoders 160 and 161. The function of the inverters 159 is to invert the logic level of the input signal from the decoders 160 and 161. If the input function is a logic 1, the output of the inverter 159 is a logic 0, and vice versa. The 8 output leads from the decoder 160 and the 16 output leads from the decoder 161 are wired to a patch board 150 to facilitate the decoding of any one of the 128 different codes.

Assuming flip-flops 151 to 157 to be in the reset condition, (all outputs A-G being at a logic 0), then outputs A, B and C which feed decoder 160 will be at logic 0. Output 0 of the decoder 160 would be at a logic 0 and connection 0x to the patch board 150 would be at logic 1 as it is being inverted by inverter 159. Outputs

1x to 7x will be at logic 0. Outputs D, E, F and G from flip-flops 154 and 157, will be at logic 0, therefore, output 1 of decoder 161 will be at logic 0 and connection 1y at a logic 1. Connections 2y to 16y will be at a logic 0. The outputs A to G of each flip-flop, 151 to 157, change state when the clock input signal goes from 1 to 0. When the first pulse appears on connection 18 from the sync. circuit 13, flip-flop 151 toggles and the output A becomes a logic 1. Decoder 160 will shift its logic 0 from output connection 0 to output connection 1. Connection 0x consequently reverts to logic 0 and connection 1x becomes logic 1. Decoder 161 remains the same for the reason that outputs D, E, F and G from flip-flops 154 to 157 have remained unchanged. At the next clock pulse on the input of flip-flop 151, output connection A of flip-flop 151 returns to logic 0 which toggles flip-flop 152. Output connection B of flip-flop 152 becomes logic 1 and output connection A from flip-flop 151 is at logic 0. Decoder 160 shifts from output connection 1 to output connection 2. Output 1x to the patch board 150 reverts back to logic 0 and output connection 2x becomes a logic 1. After the next clocking pulse, output connection A reverts back to logic 1 and output connection B of flip-flop 152 remains at logic 1. Decoder 160 now shifts its logic 0 from output connection 2 to output connection 3 and connection 3x to the patch board becomes a logic 1. It is apparent from the above, that for each input clocking pulse at connection 18, decoder 160 shifts the signal on one output to the adjacent output connection on its right. Decoder 161 works exactly the same way as decoder 160, except that it will shift one to the right every time decoder 160 starts at output 0. Thus, decoder 160 shifts with every clocking pulse at input 18 while decoder 161 shifts with every 8 clocking pulse at input 18. In the decoder-programmer 14, the x and y output connections are combined at the input of a NAND gate to provide a sequence pulse.

Referring now to FIG. 8, there is shown the construction of a J-K flip-flop as used in the 8 second counter (FIG. 4), the counter of FIG. 6b and the counter in the sequencer described in FIG. 7. The J-K flip-flop circuit comprises two input gates 170 and 171, a master gate circuit 172 and a slave circuit 187. Suppose that the master gate circuit 172 is in the state with a logic 1 at the output of its gate 173. The clock input 177 is at a logic 0. The output of the input gate 170 and 171 are at logic 0 regardless of the other inputs because of the 0 clock input 177. The inputs to gate 174 are at a logic 1 and 0, resulting in a 0 at the output of the gate 174. Since the gate 173 output is at logic 1, the connecting transistor switch 178 is "on", applying a 0 to gate 180 of the slave flip-flop circuit 187. This forces a logic 1 at output 181. Since the output of gate 174 is 0, the transistor switch 179 is "off" and all logic 1's are applied to the slave gate 182 resulting in a 0 at output connection 183. Thus, the output of the master flip-flop circuit 172 is imposed on the slave flip-flop circuit 187.

Now supposing that the K and J inputs 184 and 185 respectively are binary 1's or unconnected and the clock input begins to rise towards a logic 1, the J-K flip-flop circuit goes through a four step sequence. STEP 1: The transistor coupling switches 178 and 179 are turned off because their emitters are no longer at 0 volts. When the clock input 177 reaches the true 1 level, the outputs of the K and J input gate 170 and 171

will be determined by the other inputs thereto. In this case all will be 1's except the 0 signal level at output connection 183 which is fed back to the J input gate 171. Thus, the J gate 171 output is still 0 but the output at the K gate 170 is now a logic 1. This makes the output of gate circuit 173 at 0 which in turn makes the output of gate 174 at 1.

STEP 2: As the level of the signal at the clock input 177 begins to drop, it becomes a 0 at the J and K input gates 170 and 171 bringing both gate outputs to 0.

STEP 3: When the level at the clock input connection 177 approaches 0 volts, the transistor switches 178 and 179 can be turned on. In this case, the gate 174 of the master gate circuit 172 has an output which is a logic 1 and which turns on transistor switch 179 changing the output connection 183 to become a logic 1.

STEP 4: The information is transferred from the master flip-flop circuit to the slave flip-flop circuit and the output levels of the slave flip-flop circuit 187 are reversed.

The action of the direct reset input 186 is readily seen in the schematic. A logic 0 at the reset input 186 forces an immediate logic 1 at the output of gate 174 through both input NAND gates 176 and 175. The logic 0 applied to the gate 182 of the slave flip-flop circuit 187, also forces a logic 1 at output connection 183. Thus, the J gate 171 is disabled and both the master and slave flip-flops are reset.

Referring now to FIGS. 7 and 9, there is shown the circuit arrangement of the decoder-programmer 14, which channels the sequencer pulses from the x and y output connections to the various control circuits. The sequencer x and y outputs, 23 and 24 respectively, are cross connected, by means of a patch board 150 to the various control gates in the decoder section as illustrated in FIG. 9. In this circuit, it is noted that there are two identical sets of gates, a first set 190 for a 70 second duration sequence cycle, and a second set 191 for a 100 second duration sequence cycle. These gates are the AMBER N/S 192, the GREEN E/W 193, sync. no. 1, 194, sync. no. 2, 195, sync. no. 3, 196, AMBER E/W 197, and the cycle reset gate 198. The reason for duplicating these gates is that normally, in a large city, the sequence cycle duration is changed during the day to accommodate business, rush hour traffic, after rush hour traffic (100 second sequence cycle duration) and normal traffic flow (70 second duration cycle).

The normal sequence cycle duration is 70 seconds. This cycle is obtained by placing a logic 0 on the cycle control lead 12a. This, in turn, places all the 100 second cycle control gates in an inoperative state, for the reason that a logic 0 on one of the inputs to these NAND gates provides a logic 1 on their outputs regardless of the logic condition on the other inputs. Inverter 199 places a logic 1 on the 70 second sequence cycle set 190 of gates. Because both sets of cycle duration gates 190 and 191 operate in the same manner, the description which follows relates to the 70 second duration sequence cycle only.

Referring to the sequence cycle charts shown in FIGS. 2a and 2b, it can be seen that a sequence cycle is started on a reference point at the beginning of the GREEN N/S gate which point is referred to as the 0 count or the starting point for this system. This gate is identified by numeral 200 and provides a logic 0 pulse at its output when both its inputs, 0x and 1y, are at logic 1's. The 0x and 1y connections are the first connections of the decoder 160 and 161 respectively of the se-

quencer circuit 17 as described hereinabove with reference to FIG. 7. This condition occurs when the sequencer flip-flops 151 to 157 are all reset. The output of the NAND gate 200 is fed to an inverter 201 which inverts the pulse and the output of the inverter is connected to the signal control circuit 22 via lead 202.

The AMBER N/S gate 192 provides a logic 0 pulse at its output 203 when both inputs 1x and 3y are at logic 1. This represents a count of 17 pulses (17 seconds) in the sequencer circuit 17. The output 203 is connected to an AMBER fan-in gate 204 which transmits a logic 1 pulse to the signal control circuit 22 via lead 205.

The GREEN E/W gate 193 provides a logic 0 pulse at its output 206 when both inputs 5x and 3y are at logic 1 (the sequencer has counted 21 pulses equivalent to 21 seconds). The output 206 is then connected to the GREEN E/W fan-in gate 207 which transmits a logic 1 pulse to the signal control circuit 22 via lead 208.

The AMBER E/W gate 197 provides a logic 0 pulse at its output 209 when both inputs 2x and 9y are at logic 1 (the sequencer has counted 66 pulses equivalent to 66 seconds). The output connection 209 of gate 197 is connected to the AMBER fan-in gate 204 which then provides a logic 1 pulse to the signal control circuit via output lead 205.

The AMBER fan-in gate 204 combines all the AMBER pulses which occur at different times of the cycle to only one output 205. Normally, the output 205 of the gate is at a logic 0 but will go to logic 1 whenever one of its inputs goes to logic 0 pulse.

The GREEN E/W fan-in gate 207 combines both outputs of the GREEN E/W gates 193 to provide only one output at connection 208. The output 208 of the GREEN E/W fan-in gate 207 is normally at logic 0, but will go to logic 1 whenever one of the inputs to the gate goes to logic 0 pulse.

The outputs from the inverter 201, the AMBER fan-in gate 204 and the GREEN E/W fan-in gate 207 provide the necessary pulses to the signal control circuit 22 for the operation of the GREEN, AMBER and RED signals for both directions.

The sync. gates 194, 195 and 196 work essentially in the same manner as the signal control pulse gates described hereinabove. When the inputs 2x and 7y on the first sync. gate 194 become a logic 1 (after 50 pulses of the sequencer equal a time delay of 50 seconds), the output 210 of the gate 194 drops to logic 0 and the output 211 of the sync. no. 1 fan-in gate 212 rises to logic 1. The output 211 is connected to the input of a sync. no. 1 one-shot circuit 213, the output 12b' of which drops to logic 0 for approximately 1 micro-second and then rises back to logic 1. Instead of sending a sync. pulse to the sync. circuit 13 with the same duration as the sequence pulse, a very short pulse is preferable in case the sync. pulse from the central control programmer 11 is received at approximately the same time. The output of the one shot circuit 213 is connected to the sync. circuit via lead 12b'.

The second and third gate circuits 195 and 196 work exactly the same way as the first sync. circuit gate 194 except that the time counts of these further gates are different. These times are patched into the decoder-programmer patch board 150 in accordance with the requirements of the network.

The pulse for resetting the sequencer is provided by the cycle reset gate 198 in the decoder 14. When the sequencer circuit 17 reaches the count of 70 (70 seconds), a logic 1 appears on connection 6x and 9y, which are the inputs of the cycle reset gate 198 causing the reset gate output 215 to drop to logic 0. Connection 215 connects to the input of reset fan-in gate 216. The output of the fan-in gate 216 rises to logic 1 and is applied to an inverter 217 via connection 218. The inverter provides an output logic 0 which is connected to the sequencer reset flip-flop 158 (see FIG. 7) of the sequencer circuit 17 via lead 219.

Referring to FIG. 7, it is seen that the sequencer reset flip-flop 158 toggles and provides a logic 1 at the inputs of the reset inverters 162 and 163 which in turn applies a logic 0 on the reset lines 164 and 165 to the flip-flop circuits 151 to 157. The moment the sequencer 17 is reset, the reset gate 216 returns to its original state and awaits the next count. The reset flip-flop 158 (FIG. 7) is reset when the clock provides a logic 1 at the input of inverter 166 via connection 18 from the sync. circuit 13 (see FIG. 7). The inverter 166 places a logic 0 on the reset lead 167 of the reset flip-flop 158. When the reset flip-flop 158 is reset, the reset lines 164 and 165 change to a logic 1, thus causing the counter to continue to advance with each clock pulse at its input 18.

Referring now to FIG. 10, there is shown a typical NAND gate circuit as utilized in the decoder-programmer circuit as shown in FIG. 9. The NAND gate comprises a multiple emitter transistor 230 each of which is connected to a respective input connection 231, 232 and 233. Grounding any one or more of these inputs, forward biases transistor 230 which puts its collector, which is connected to the base of transistor 234 via lead 235, at a low potential and turns off transistor 234. When transistor 234 is turned off, transistor 236 turns on and transistor 237 turns off, and results in a logic 1 output at output connection 238. If, on the other hand, all inputs are unused, or at logic 1 the base collector junction of transistor 230 will conduct, forward biasing the base emitter junction of transistor 234. When transistor 234 is on, transistor 237 is on and transistor 236 is off resulting in a 0 at the output terminal 238. This corresponds to the inverted AND or NAND function for the gate as used in the decoder-programmer 14. The other resistors in the circuit are merely biasing components for the transistor stages.

Referring now to FIG. 11, there is shown the arrangement of the one-shot gate circuit comprising gates 213 and 213' as described hereinabove with reference to FIG. 9. The signal on line 211 is applied to the input of gates 213 and 213' via connection 211. At the output of gate 213, the signal is inverted and delayed by the gate propagation time to give an inverted signal on the line 246. The inverted signal pulse is further delayed in reaching the input of gate 214 by the time constant of the RC circuit comprising resistor 247 and capacitor 248. Thus, the input pulse and the inverted output pulse of gate 213 are slightly displaced in time. The output will be momentary 0 resulting from the overlapping logic 1 levels of the input signal. Therefore, the output pulse on connection 12b' is delayed by a time determined by the RC circuit.

Referring now to FIG. 12, there is shown the signal control circuit 22 which function is to switch the signal lamps (not shown). The directional flip-flop circuit 250 determines which RED and GREEN lamps are to be

activated and the GREEN-AMBER flip-flop circuit 251 determines whether a GREEN or AMBER lamp is lit in one direction.

Assume the sequencer circuit 17 is at 0 count or in the reset condition. The GREEN N/S input connection 202 from the decoder 14 places a logic 1 at the input of inverter 252. The output of inverter 252 is therefore at logic 0. The input 253 of the GREEN fan-in gate 254 from inverter 252 is at logic 0, the output of the gate 254 connected to inverter 255 is at logic 1, and consequently the set input 256 to the GREEN-AMBER flip-flop is at logic 0. This toggles the GREEN-AMBER flip-flop circuit 251 to the set condition. Inverter 252 which is at logic 0 toggles the directional flip-flop circuit 250 to the set condition. The directional flip-flop 250 places a logic 1 on one of the inputs to signal control gates 260 and 261, via wire 262 and a logic 0 on the RED E/W lead via wire 263. The GREEN-AMBER flip-flop circuit 251 places a logic 1 on the other input to signal control gate 261 via wire 264. Since the two inputs to signal control gate 261 are at logic 1, the output 265 to the GREEN N/S is at logic 0. A logic 0 on the output leads of the signal control gates activates the corresponding lamps therefore the GREEN N/S lamp and RED E/W lamp will be lit. Signal control gates 257, 258, 259 and 260 all have logic 0's on one of their inputs via wires 263 and 266, therefore, their outputs are at logic 1.

When the sequencer circuit 17 reaches the count of 17, the input of inverter 267 (AMBER decoder lead) goes to logic 1 consequently, the output to the GREEN-AMBER flip-flop circuit 251 drops to logic 0, making this flip-flop toggle. This places both inputs to signal control gate 260 at logic 1, consequently the output to the AMBER N/S goes to logic 0 and this lamp is activated. Because lead 264 is at logic 0, the signal control gate 261 output reverts to logic 1, and the GREEN N/S lamp is extinguished.

When the sequencer reaches the count of 21, the input of inverter 268 goes to logic 1 and its output goes to logic 0. The GREEN-AMBER flip-flop circuit 251 is set by inverter 255 (output at logic 0), and the directional flip-flop 250 toggles to the reset condition. This places logic 1's on leads 264 and 263. Therefore, the RED E/W is extinguished, the AMBER N/S is extinguished, the GREEN E/W is activated because logic 1's appear on both inputs to signal control gate 258, and the RED N/S is activated because lead 263 is at logic 1 and the input from the flash clock enable gate 269 is at logic 1 (except when the system is in the flashing mode).

When the sequencer circuit 17 reaches the count of 66, the input of inverter 267 goes to logic 1, consequently the GREEN-AMBER flip-flop circuit 251 toggles and places a logic 1 on lead 266. Lead 263 is already at logic 1, therefore, all inputs to signal control gate 257 are at logic 1, and the AMBER E/W lamp is activated. The GREEN E/W is extinguished. This sequence also provides the timing for transferring the system to flashing RED and AMBER mode. At this point, both leads of the flash control gate 270 are at logic 1, consequently, a logic 0 is applied to lead 92. The sync. circuit lead 19 consequently goes to logic 0, and places the output of inverter 271 at logic 1. This allows the flash clock enable gate 269 to activate the AMBER E/W and RED N/S at a 1Hz flash rate. During this

mode, the sequencer circuit 14 does not count because its clock pulse is removed.

When the sequencer 14 reaches the count of 70 (the flash mode inactive) the sequencer counter is reset to 0, and this circuit reverts back to GREEN N/S and RED E/W condition. This sequence is the same as the one of the 0 count.

Referring now to FIG. 13, there is shown one of the electronic switches of the power switcher 25. The electronic switch comprises a unijunction transistor 280 which, when forward biased, passes a pulsating voltage signal to the primary winding 281 of transformer 282. This pulsating voltage is provided from the power supply circuit and is coupled to the drain of transistor 280 via resistor 284 in series with capacitor 285. The pulsating DC voltage across resistor 284 charges capacitor 285, and when the capacitor reaches a predetermined voltage, it triggers the transistor 280 which in turn provides an AC pulse on the secondary winding 283 of transformer 282. Resistor 286 provides the proper bias for transistor 280. The output pulse on the secondary winding 283 is connected to the gate 287 of a triac 288 causing the triac to close after the AC output pulse has reached 20 degrees of its phase, thereby connecting the 110 volts AC live on line 289 to an associated signal light 290, causing the light to illuminate.

The trigger circuit which comprises transistor 280, resistors 284 and 286, capacitor 285 and transformer 282 continues to trigger the triac 288 until the capacitor 285 is shorted out. Transistor 291 is provided for that purpose and its input base connection is fed by the signal control circuit 22. When transistor 291 is forward biased, it shorts out capacitor 285 which, in turn, renders transistor 280 non-conductive. Thus, the signal light 290 is rendered inoperative.

Although a preferred embodiment of the controller circuit has been disclosed, it is within the ambit of the invention to provide equivalent circuit components and arrangement to effect the same sequential operation as broadly defined by the appended claims.

We claim:

1. An automatic controller system adapted to control traffic signal lights comprising a receiver circuit having a plurality of input connections which carry control pulses from a remote control station wherein some of the inputs carry synchronization control pulses and others carry a sequence cycle signal and a flash mode signal to select a particular sequence for said traffic lights and a particular synchronization for the system, a generator connected to a 60 Hz frequency source for generating pulse signals exhibiting a particular traffic signal lights flash frequency and a sequencer triggering frequency, a sequencer circuit comprising a counter adapted to produce a plurality of output signals representative of a count of said generator pulse signals in the duration of a complete sequence cycle of each said traffic lights, means for sensing said plurality of output signals and to generate control signals at preselected time intervals during said sequence cycle to cause sequential operation of said traffic signal lights, synchronization circuit means controlled by said synchronization control pulses and said sequence cycle signal and interconnected with said sequencer circuit for synchronizing said sequence cycle at a predetermined time during said sequence cycle and flash enabling circuit means to enable said traffic signal lights to flash and to

disable said counter at a predetermined time during said sequence cycle.

2. An automatic controller as claimed in claim 1 wherein said receiver circuit comprises a plurality of converter circuits, each said converter circuit being associated with an input connection to said receiver circuit to convert the control pulses on said input connections to binary output signals whereby associated integrated circuits can be activated.

3. An automatic controller as claimed in claim 1 wherein said generator connected to said 60 Hz frequency source comprises a sine-to-square wave circuit and a divide-by-60 counter, said later counter having a decoded flip-flop counter for producing an output frequency of one pulse per second.

4. An automatic controller as claimed in claim 1 wherein said counter comprises a binary-up counter having a plurality of flip-flop circuits, said flip-flop circuits each having an output connection, said flip-flop output connections being connected to either a first or second decoder output group.

5. An automatic controller as claimed in claim 4 wherein said first decoded group is provided with a first group of output connections and said second decoded group is provided with a second group of output connections, said second group having twice as many output connections as said first group, each said output connection having a binary signal thereon, said binary signal of said first group of output connections being caused to change at a sequential rate from one output connection to the adjacent one for each generator pulse signal fed to said sequencer circuit.

6. An automatic controller as claimed in claim 5 wherein said binary signal on the output connections of said second group of output connections is caused to change at a sequential rate from one output connection to the adjacent one each time all of said output connections of said first decoded group have changed binary signals.

7. An automatic controller as claimed in claim 6 wherein said output connections of said first and second decoded groups are each connected to an inverter circuit, said inverters being connected to a patch board to enable sensing said output connections at discrete time counts of said sequencer circuit.

8. An automatic controller as claimed in claim 1 wherein said means for sensing is a decoder-programmer circuit having an integrated switching gate circuit representative of a predetermined sequence cycle, said switching gate circuit having inputs connected in a predetermined manner to a plurality of output connections from a first and second decoded group of output connections from a sequencer circuit and arranged to provide a plurality of control output signals at predetermined time intervals during said sequence cycle.

9. An automatic controller as claimed in claim 8 wherein there is provided two sets of switching gate circuits, each said set being representative of a predetermined sequence cycle, said first set being operable when a binary output signal from said receiving means is connected to one of its switching gates and said second set being operable when said first set is not operated.

10. An automatic controller as claimed in claim 8 wherein said integrated switching gate circuit includes gating circuits for generating control signals at predetermined time intervals during said predetermined se-

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quence cycle to cause said traffic signal lights and said synchronization means to operate and to reset said counter.

11. An automatic controller as claimed in claim 10 wherein said control signals to cause said traffic signal lights to operate are connected to a signal control circuit comprising a plurality of switching gate circuits connected to provide a further control signal to cause an associated switch in a power switcher circuit to connect an operating voltage to an associated one of said traffic signal lights, said associated switch connecting said operating voltage only during a predetermined time interval of said sequence cycle.

12. An automatic controller as claimed in claim 1 wherein said synchronization means is a synchronization circuit having circuit means for receiving and feeding said generator pulse signals to said counter, circuit means for receiving a sync. pulse from said remote control station and from said means for sensing a plurality of output signals whereby said generator pulse signals are disabled from said counter and a time delay counter

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circuit is enabled for a short time interval during said sequence cycle, said generator pulse signals being reconnected to said counter upon arrival of a sync. pulse from said remote control station or after said time delay counter has completed its count.

13. An automatic controller as claimed in claim 12 wherein said sync. pulses from said remote control station and said means for sensing are each fed to a sync. enable flip-flop circuit, said sync. enable flip-flop circuit being connected to a sequence clock gate to disable said generator pulse signals to said counter, said sync. enable flip-flop also being connected to a timer enable gate and a timer clock gate to provide the necessary clock signal to enable said time delay counter.

14. An automatic controller as claimed in claim 13 wherein every generator pulse signal from said sequence clock gate fed to said counter will reset said time delay circuit until a further sync. pulse from said means for sensing is fed to said sync. enable flip-flop circuit.

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