United States Patent

[11] 3,576,432

[72] Inventor **Norman J. Braaten**
King Road, Rte. 1, Eagan Township, Dakota County, Minn. 55068

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[54] **DYNAMIC DIGITAL CALCULATING APPARATUS FOR ANALOG FUNCTIONS**
13 Claims, 11 Drawing Figs.

[52] **U.S. Cl.** **235/150.3,** 235/150.5
[51] **Int. Cl.** **G06j 1/00**
[50] **Field of Search** ..... 235/150.3, 150.31, 150.4, 150.5, .51, .52, .53, 194

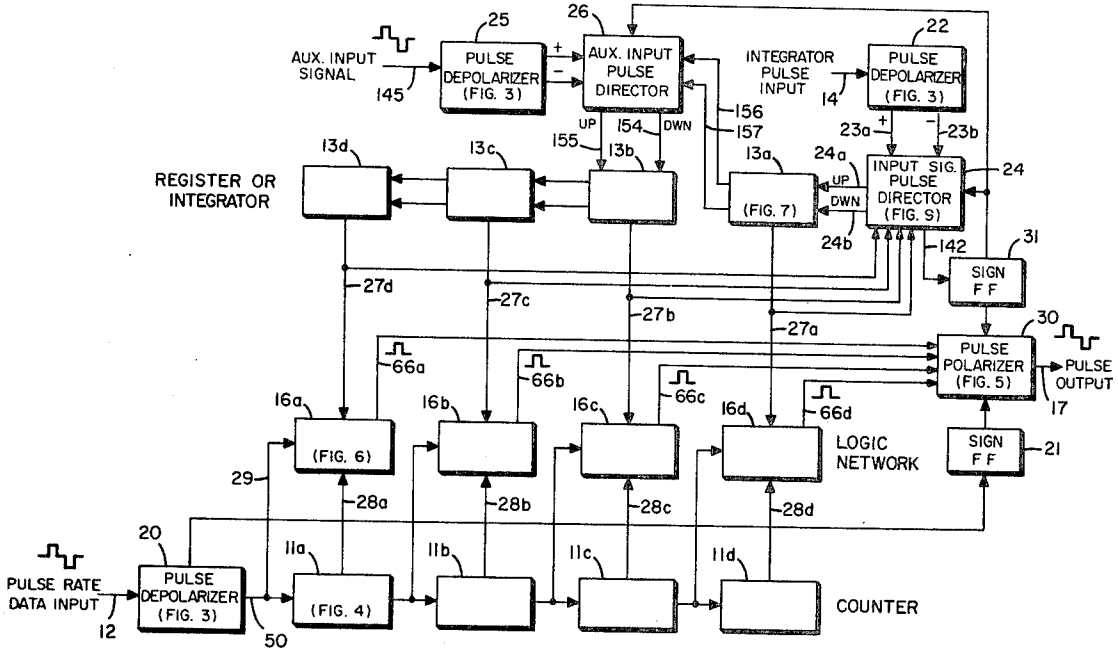
[56] **References Cited**

UNITED STATES PATENTS

2,910,237	10/1959	Meyer et al.	235/150.3
2,913,179	11/1959	Gordon	235/150.3
3,126,476	3/1964	Pariser et al.	235/150.3UX
3,194,950	7/1965	Walls et al.	235/150.5X
3,230,353	1/1966	Greene et al.	235/150.3X

Primary Examiner—Malcolm A. Morrison
Assistant Examiner—Joseph F. Ruggiero
Attorney—Stryker and Jacobson

ABSTRACT: A register means, a counter and logic network for combining the contents of the two form a basic functional module. Although the register means may contain fixed data, in general it and the counter receive variable data in pulse train form. After the data has been suitably processed within a module, the module produces an output signal train of pulses which is a function of the input. The counter is incremented by each signal input pulse, positive or negative. The pulse responsive register is also a counter but it is incremented or decremented according to the sign of the input data. By suitably sensing and recording the sign of the input data, the output data pulses are properly polarized to carry the correct arithmetic sign. All pulses in the system are produced from a common clock frequency source so that all the pulse widths and shapes are substantially the same although the pulse trains may be and generally are of different pulse rates. In general, a number of modules are connected together to form an operative device with the pulse train output of a module serving as the pulse train input to a module.



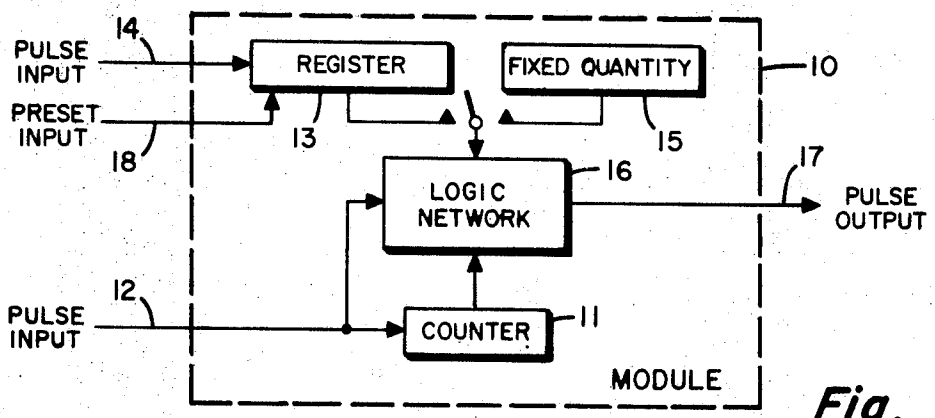


Fig. 1

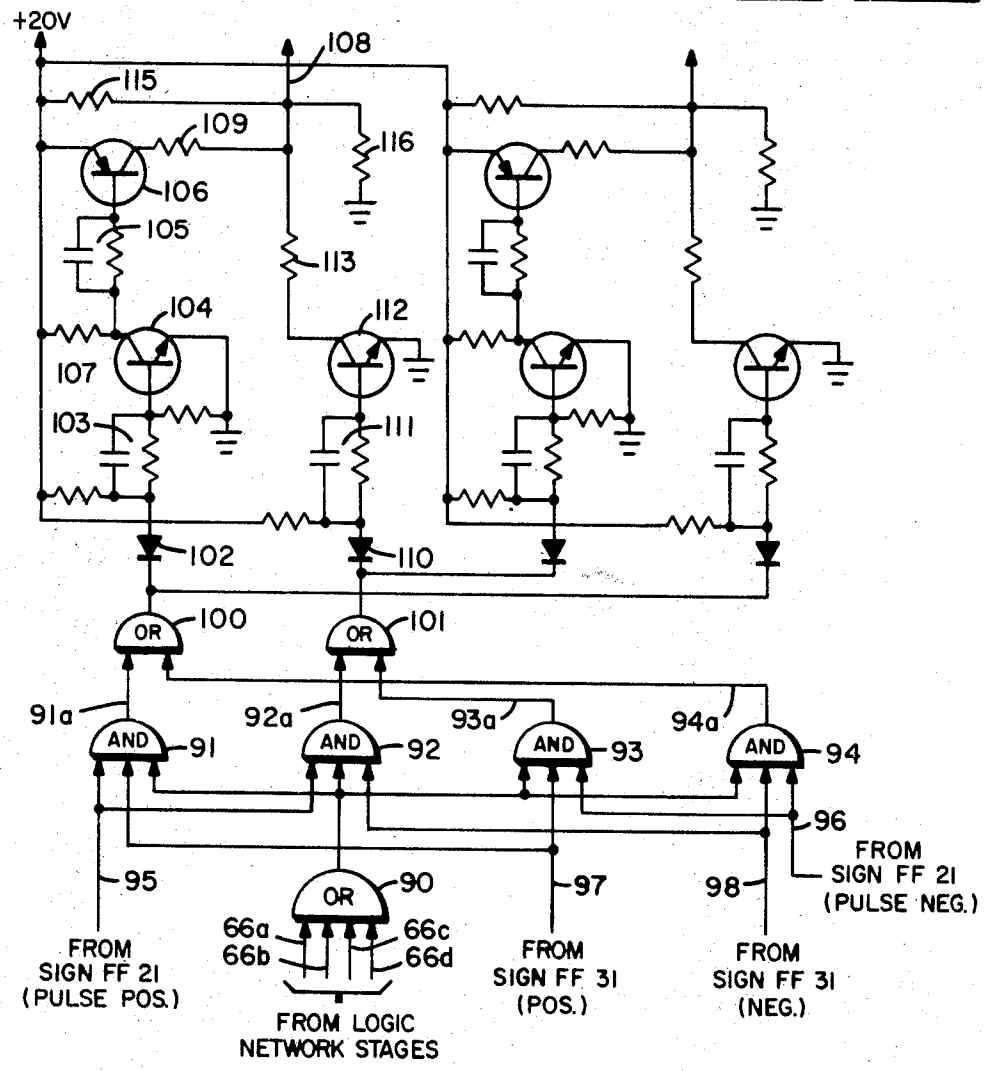


Fig. 5

INVENTOR
NORMAN J. BRAATEN
BY Stryker and Jacobson
ATTORNEYS

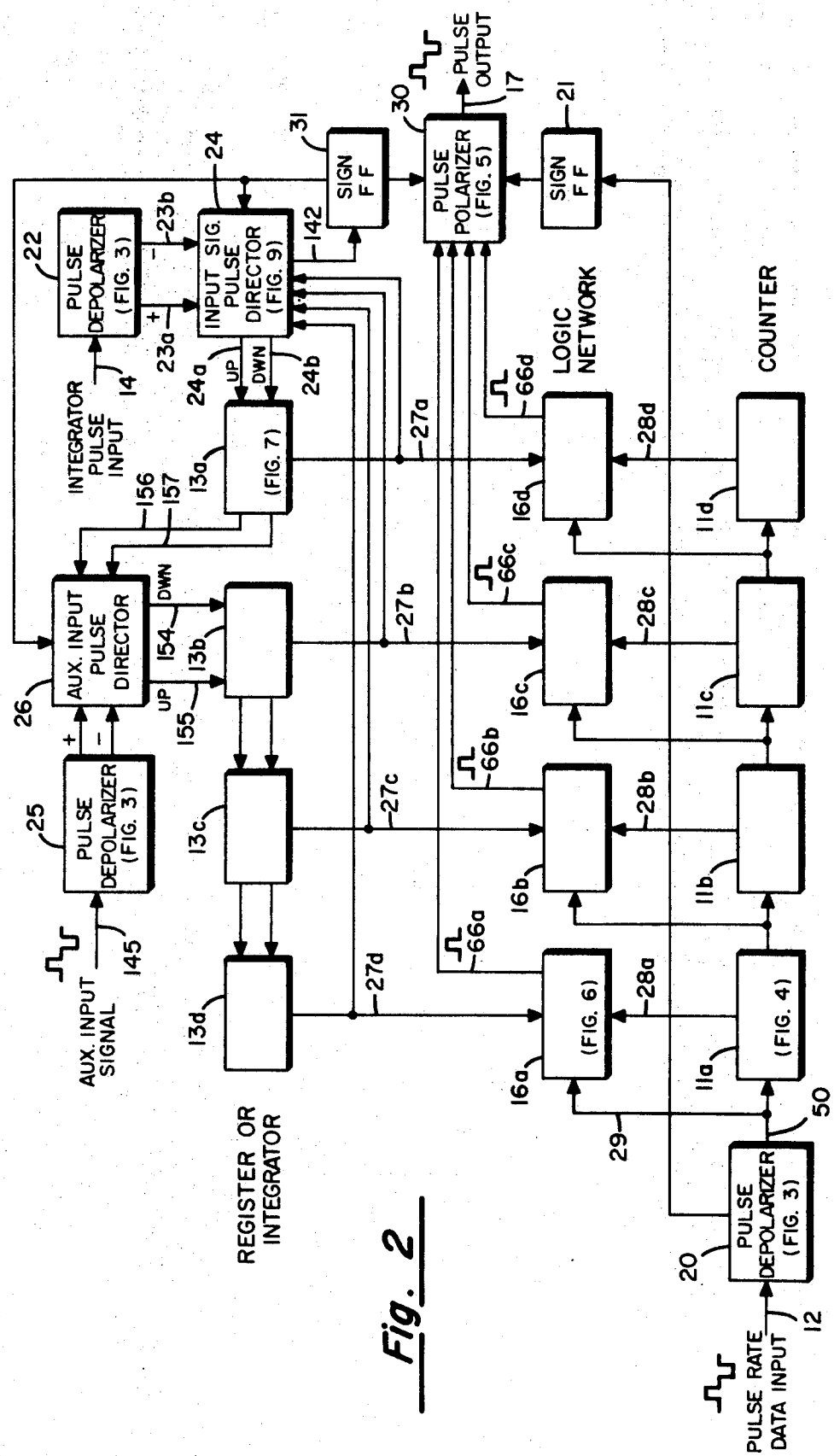

PULSE OUTPUT
17
30
PULSE POLARIZER (FIG. 5)
31
SIGN F F
21
SIGN F F
24
142
PULSE DEPOLARIZER (FIG. 3)
22
23b
INPUT SIG. PULSE DIRECTOR (FIG. 9)
23a
24a
UP
DWN
24b
INTEGRATOR PULSE INPUT
14
LOGIC NETWORK
COUNTER
66d
28d
16d
11d
27a
13a
(FIG. 7)
156
157
AUX. INPUT PULSE DIRECTOR
26
DWN
154
13b
UP
155
66c
28c
16c
11c
27b
PULSE DEPOLARIZER (FIG. 3)
25
66b
28b
16b
11b
13c
27c
AUX. INPUT SIGNAL
145
66a
28a
(FIG. 6)
(FIG. 4)
16a
11a
13d
27d
REGISTER OR INTEGRATOR
29
50
PULSE DEPOLARIZER (FIG. 3)
20
PULSE RATE DATA INPUT
12

Fig. 2

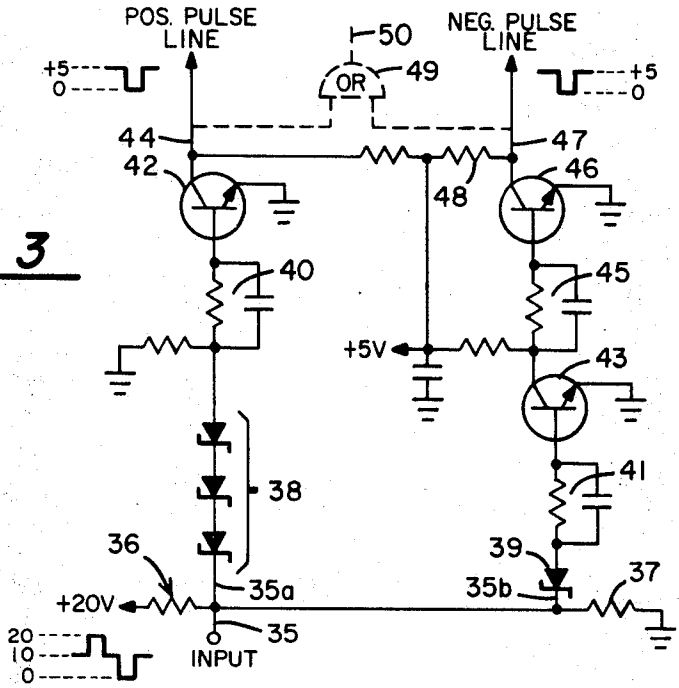

POS. PULSE LINE
NEG. PULSE LINE
50
OR
49
+5
0
44
47
42
48
46
40
45
+5V
43
41
38
36
39
37
+20V
35a
35b
35
20
10
0
INPUT

Fig. 3

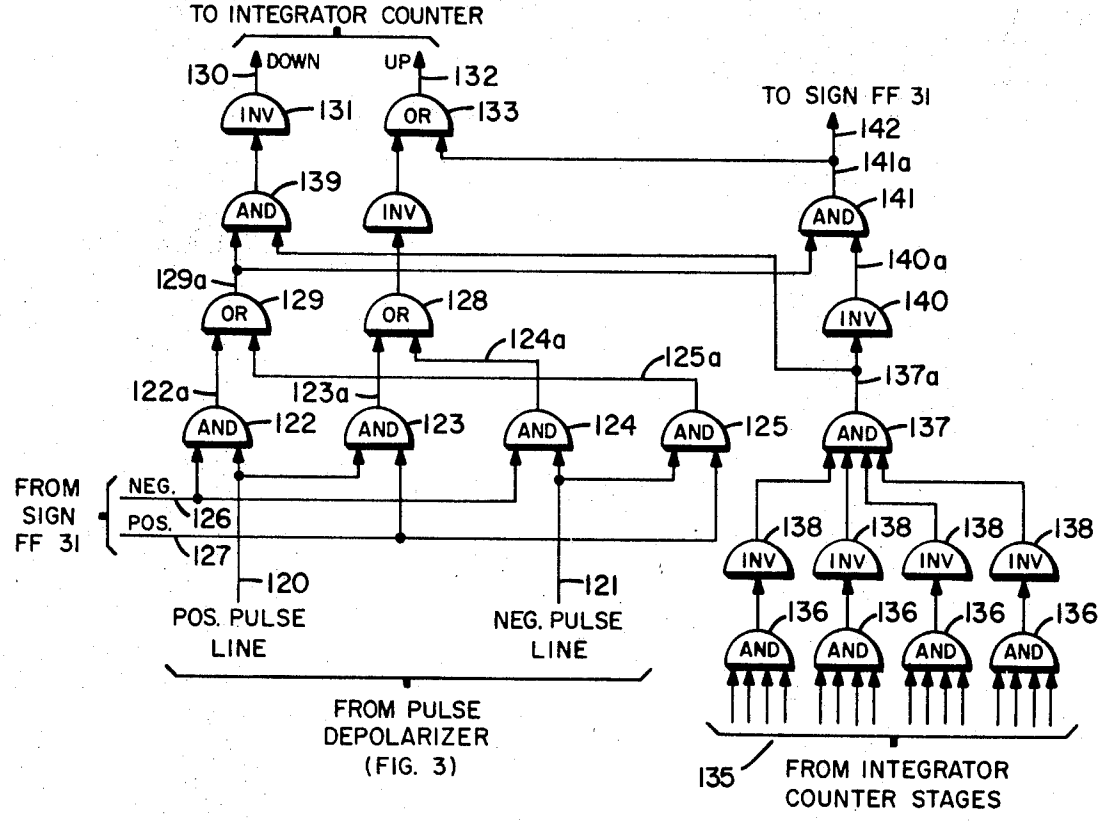

TO INTEGRATOR COUNTER
DOWN
UP
130
132
INV
131
OR
133
TO SIGN FF 31
142
141a
139
AND
INV
AND
141
140a
129a
OR
129
OR
128
INV
140
124a
125a
122a
123a
137a
AND
122
AND
123
AND
124
AND
125
AND
137
FROM SIGN FF 31
NEG.
POS.
126
127
138
138
138
138
INV
INV
INV
INV
136
136
136
136
AND
AND
AND
AND
120
121
POS. PULSE LINE
NEG. PULSE LINE
FROM PULSE DEPOLARIZER (FIG. 3)
135
FROM INTEGRATOR COUNTER STAGES

Fig. 9

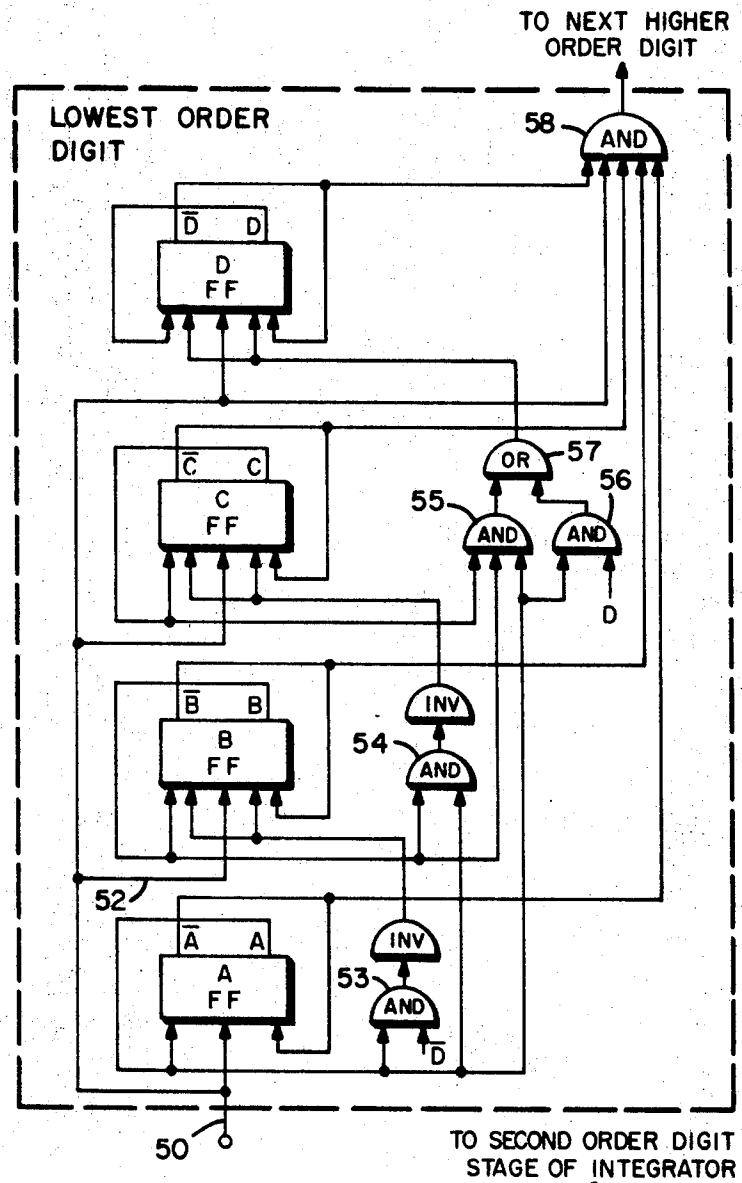

TO NEXT HIGHER ORDER DIGIT
LOWEST ORDER DIGIT
58
AND
D FF
OR
57
56
55
AND
AND
D
C FF
INV
54
AND
B FF
52
INV
53
AND
A FF
50
TO SECOND ORDER DIGIT STAGE OF INTEGRATOR
DOWN
UP
154
158
159
155
OR
OR
FROM LOWER ORDER STAGE OF INT.
DOWN
156
UP
157
148
149
150
151
AND
AND
AND
AND
146
POS.
FROM SIGN FF 31
NEG.
147
152
153
AUX. INPUT POS.
AUX. INPUT NEG.
FROM PULSE DEPOLARIZER

Fig. 4

Fig. 8

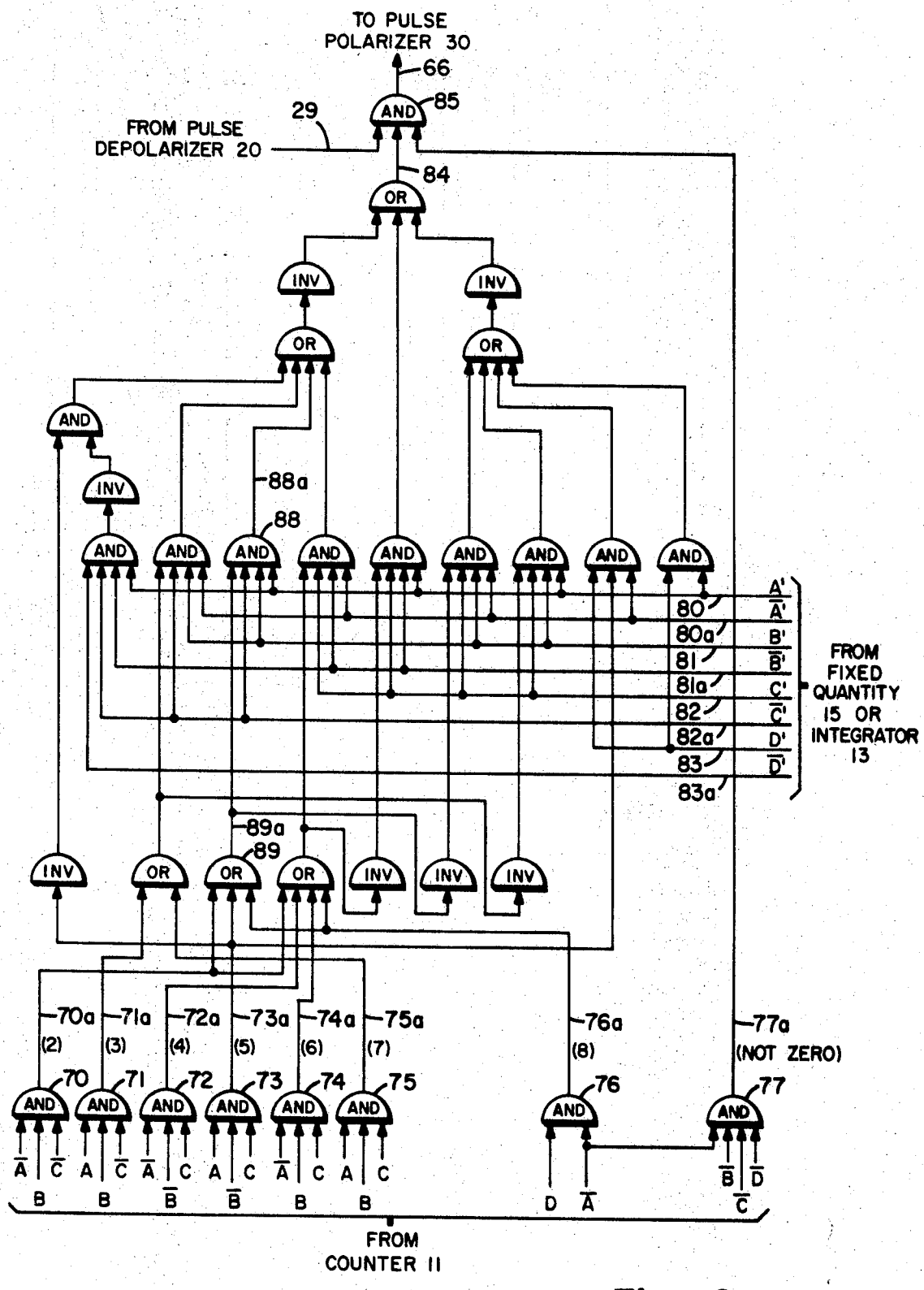

TO PULSE POLARIZER 30
66
AND
85
29
FROM PULSE DEPOLARIZER 20
84
OR
INV
INV
OR
OR
AND
INV
88a
88
AND
AND
AND
AND
AND
AND
AND
AND
AND
A'
Ā'
80
80a
B'
B̄'
81
81a
C'
C̄'
82
82a
D'
D̄'
83
83a
FROM FIXED QUANTITY 15 OR INTEGRATOR 13
89a
89
INV
OR
OR
OR
INV
INV
INV
70a
71a
72a
73a
74a
75a
76a
77a
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(NOT ZERO)
70
71
72
73
74
75
76
77
AND
Ā C A C Ā C A C Ā C A C
B B B̄ B̄ B B
D Ā
B̄ D̄
C̄
FROM COUNTER 11

Fig. 6

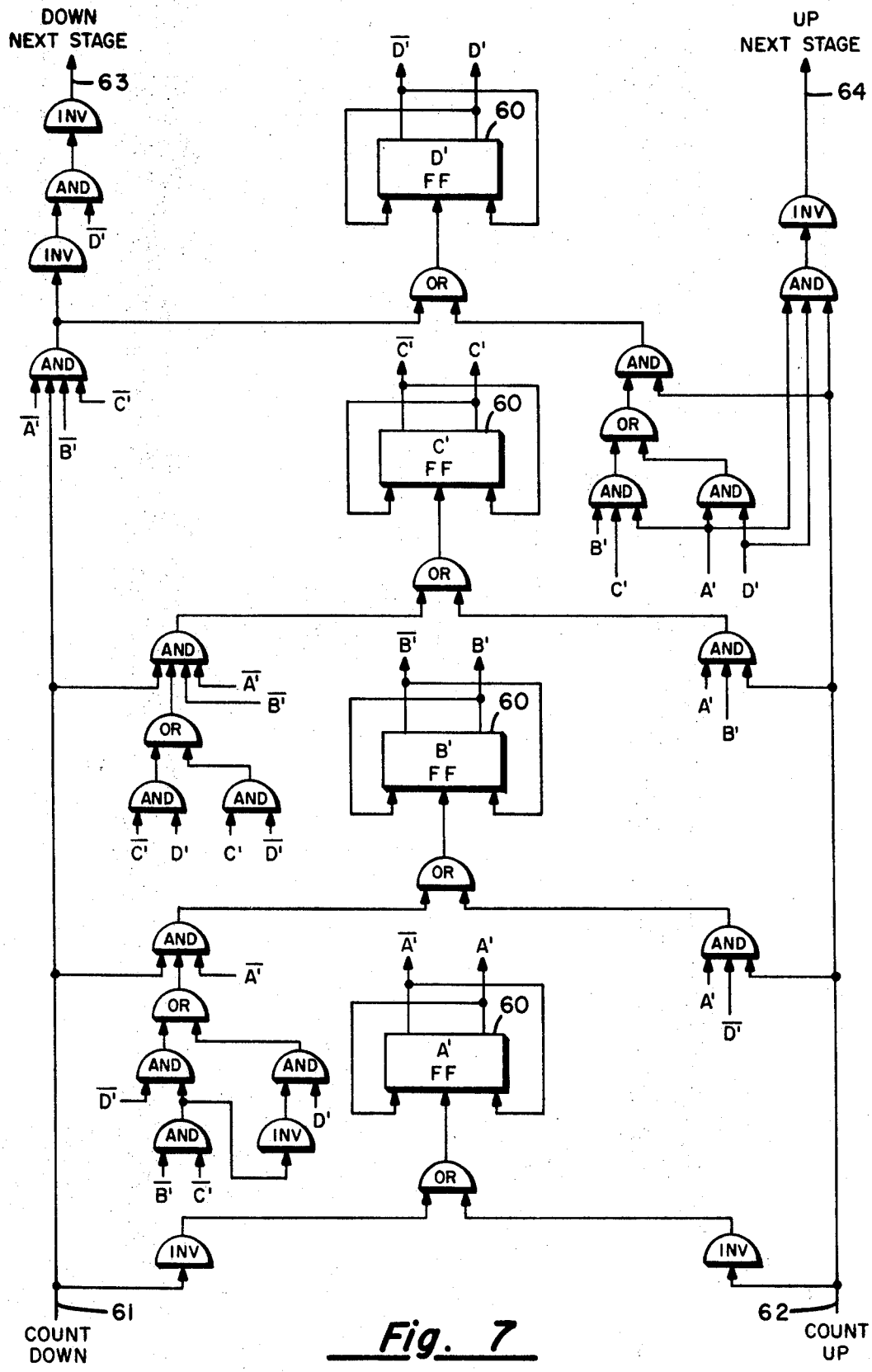

DOWN
NEXT STAGE
63
INV
AND
INV
D'
AND
C'
A'
B'
D'
D'
60
D'
FF
OR
C'
C'
60
C'
FF
OR
B'
B'
60
B'
FF
OR
A'
A'
60
A'
FF
OR
INV
61
COUNT
DOWN
UP
NEXT STAGE
64
INV
AND
AND
OR
AND
AND
B'
C'
A'
D'
AND
A'
B'
AND
A'
D'
AND
A'
OR
AND
AND
C'
D'
C'
D'
AND
A'
B'
OR
AND
AND
D'
AND
INV
D'
B'
C'
INV
62
COUNT
UP

Fig. 7

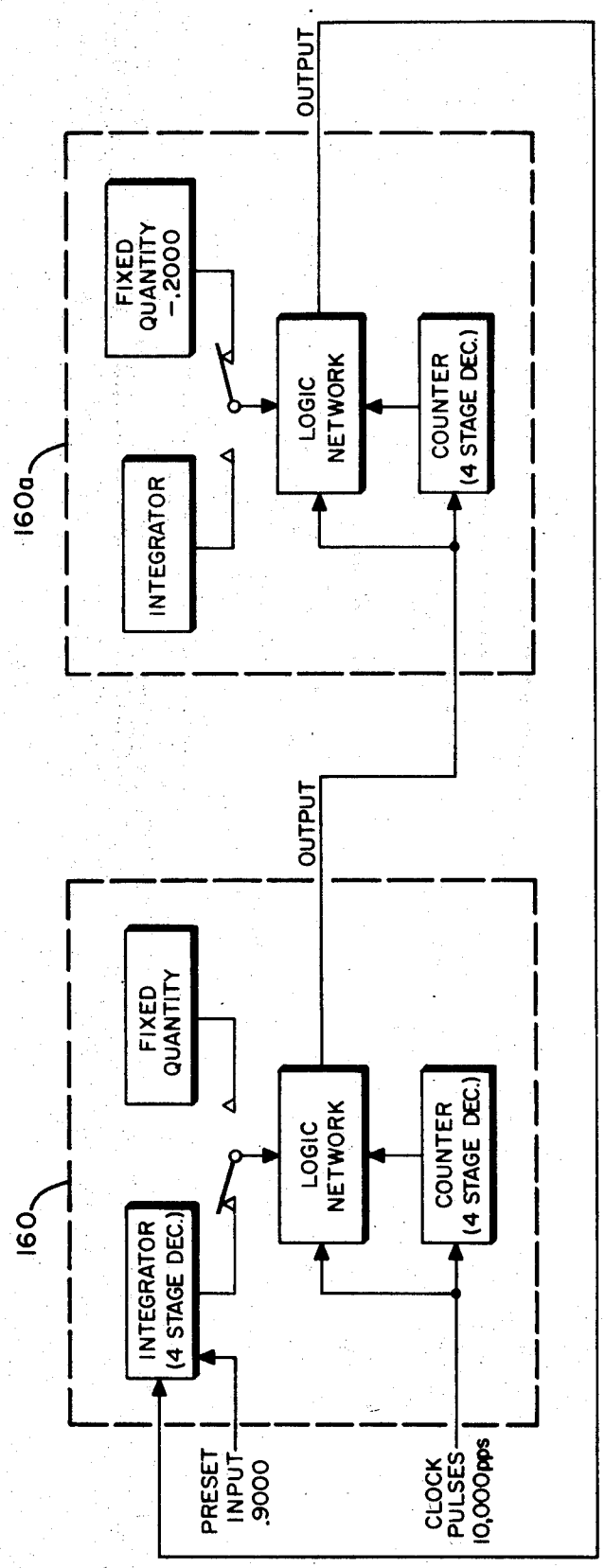

160a
FIXED QUANTITY -.2000
INTEGRATOR
LOGIC NETWORK
COUNTER (4 STAGE DEC.)
OUTPUT
160
FIXED QUANTITY
INTEGRATOR (4 STAGE DEC.)
LOGIC NETWORK
COUNTER (4 STAGE DEC.)
OUTPUT
PRESET INPUT .9000
CLOCK PULSES 10,000pps

Fig. 10

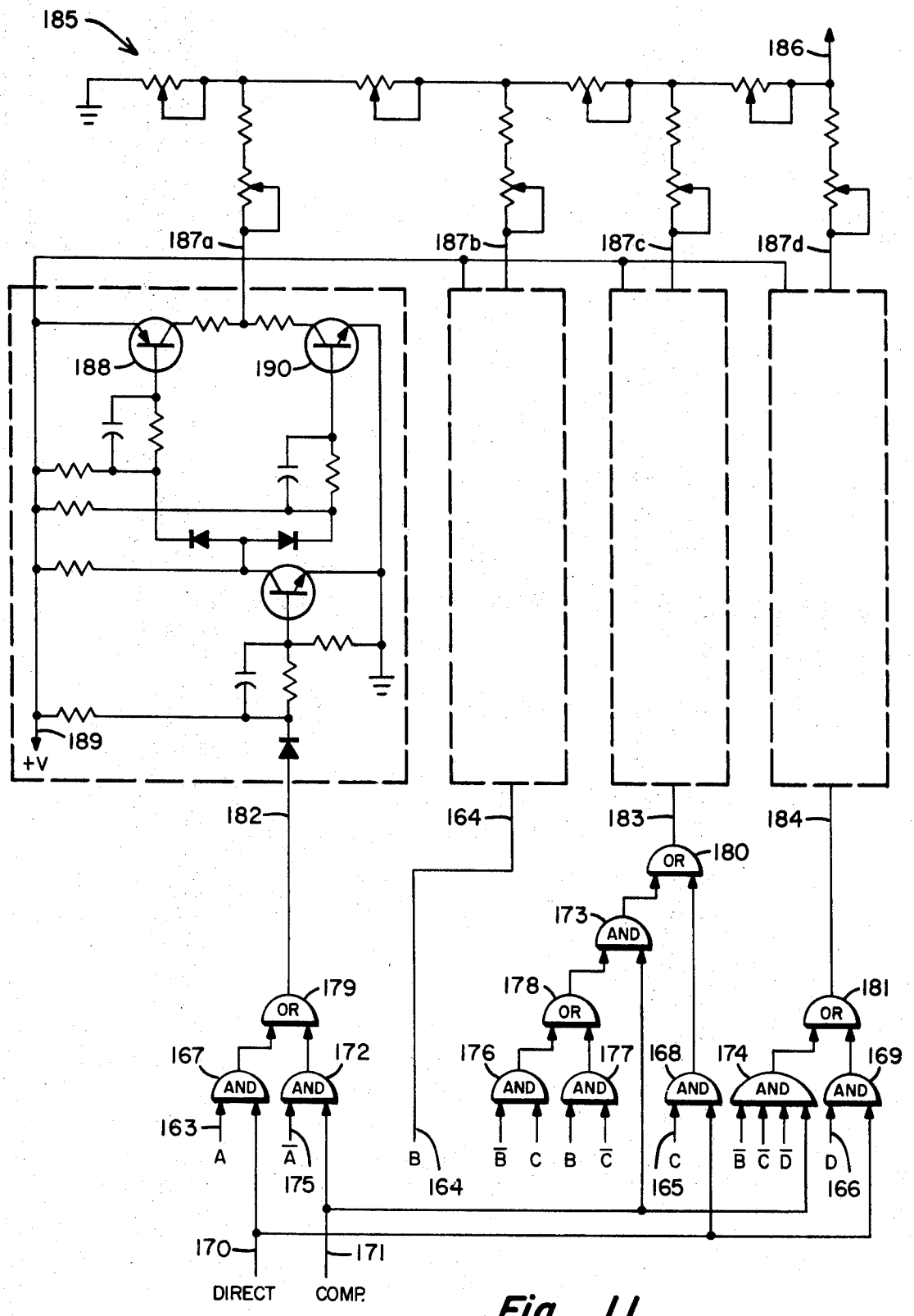

185
186
187a
187b
187c
187d
188
190
189
+V
182
164
183
184
OR
180
173
AND
178
OR
179
OR
181
167
AND
172
AND
176
AND
177
AND
168
AND
174
AND
169
AND
163
A
A
175
B
164
B
C
B
C
C
165
B
C
D
D
166
170
171
DIRECT
COMP.

Fig. 11

DYNAMIC DIGITAL CALCULATING APPARATUS FOR ANALOG FUNCTIONS

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention is directed for use in the field of electronic computing devices. More particularly the invention provides for using digital calculating techniques to perform operations on variable data which heretofore had been for the most part handled in an analog manner.

2. Description of the Prior Art

Over the years analog functions have been performed by feedback amplifier circuits for which the gain and time constants of the circuit are determined by the choice of input and feedback resistance and capacitance. It is essential that the output response of such a device maintain a constant linear proportionality to the input signal. Digital circuits, in contrast, need only distinguish correctly between two well-separated input signal states and must likewise respond by producing either of two extreme output states as required. These two output states may be created, for example, by cutoff or saturation of a variable such as load current. Along this line, the degree of accuracy of gain and the time constant of an analog circuit usually depend on the accuracy and stability of the analog components whereas in digital circuits the equivalent gain and time constant ordinarily can be controlled within certain operational limits by the pulse rate and/or the number of stages in the various control registers. There are also certain other advantages in using digital circuitry for processing analog functions. One advantage is that digital circuits can communicate directly with high speed digital computers thereby eliminating at least in part some of the analog-to-digital conversion circuitry. In some cases this may also in part alleviate a data thru-put bottleneck which often exists in the conversion channels, which in turn limits the rate at which the digital computer can sample the analog variables. When digital circuits are used, the entering of register preset values and the setting of gain coefficients can be done via manually operable switches which are ordinarily much easier to set and read than the multiturn potentiometers usually found in analog circuitry. In addition, digital integrators have no inherent internal signal inversion, i.e., a positive polarity input produces a positive output action. Also, there is no static drift in a digital system. In the absence of any pulse input signals a digital register will hold indefinitely the content value last achieved.

SUMMARY

A basic module is formed having two pulse-responsive registers, one identified as a counter and the other sometimes called an integrator, along with logic circuitry for combining their values and for gating out a suitable train of pulses which is a function of this combination. The pulse train inputs to the registers may represent constant or variable data. The input pulses may be positive or negative going representing positive and negative data, but within the module the pulses are converted to one polarity and then transformed back to the correct polarities at the output of the module. In general, a number of modules of this nature are selectively interconnected by suitable patch cord wiring so that the pulse output of a module serves as an input to a module to produce a highly flexible calculating device. Although only single polarity pulses are used within a module, correct arithmetic operations are performed by providing for sensing and recording the signs of the data and using the signal outputs of these circuits to control the functioning of the data processing circuits.

As a further feature of the invention the multitude of logic elements which make up the modules are the integrated circuit variety and are packaged in the integrated circuit chips to produce a compact unit having relatively low power consumption.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 shows in block diagram form the basic operative units of a module;

FIG. 2 shows in a more detailed block diagram form the various separate parts of the module;

FIG. 3 is an electrical schematic diagram of the pulse depolarizer;

FIG. 4 shows the logical circuit arrangement in the digit stages of the counter;

FIG. 5 shows the logical circuit arrangement and the electrical schematic of the pulse polarizer;

FIG. 6 shows the logical circuit arrangement of the logic network;

FIG. 7 shows the logical circuit arrangement of the register or integrator portion of the module;

FIG. 8 shows the logical circuit arrangement of the auxiliary pulse director;

FIG. 9 shows the logical circuit arrangement of the input signal pulse director;

FIG. 10 illustrates an intermodular hookup for performing a sample function; and

FIG. 11 is an illustrative D/A conversion circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A basic module **10** contains a multistage counter **11** which receives data pulse inputs at **12**, a register **13** which receives data pulse inputs at **14**, an alternate fixed quantity **15** and logic network **16** which combines the contents of the counter **11** with that of register **13** (or fixed quantity **15**) to produce data pulse outputs at **17**. The pulse inputs are a series of clocked pulses which are generally of equal shape and size but usually have different pulse rates. In general, the pulse trains contain positive- and negative-going pulses representing positive and negative data. Counter **11** is incremented by each input pulse, negative or positive, while register **13** counts up or down according to the polarity of its input pulse. Fixed quantity **15** is manually set, by thumb wheels, for example, and register **13** can be preset at **18** in a similar manner. Logic network **16** can be viewed as a logical multiplier with the content of register **13** (or fixed quantity **15**) being the multiplier and the content of counter **11** being the multiplicand and the two being combined to produce a pulse train output at **17** which is a function of the pulse train input at **12**.

In the embodiment which is described herein, counter **11** is a four-digit binary coded decimal (*bcd*) counter and register **13**, sometimes called an integrator, is similarly a four-digit *bcd* register. As will be shown later, register **13** is arranged as a pulse-responsive arithmetic counter. Since its pulse input usually represents some type of data which is a function of time, register **13** effectively sums or integrates the input data so it is sometimes referred to as an integrator. Typically, the clock pulse frequency may be in the order of 100,000 p.p.s. To aid in the explanation, the pulse input at **12** which enters counter **11** will often be referred to as the pulse rate data input and the input at **14** entering register **13** will often be referred to as the integrator pulse input.

Turning next to FIG. 2, there is shown in block diagram detail form the various units making up a module **10** exclusive of fixed quantity **15** and preset input **18**. The pulse rate input at **12** is fed into a pulse depolarizer **20** which takes the negative and positive going pulses and transforms them into all positive going. These are then fed into the lowest order stage **11***a* of counter **11** and into the leftmost stage **16***a* of logic network **16**. The pulse depolarizer **20** senses when there is a change in pulse polarity and feeds a signal to sign flip-flop **21** to trigger it to its opposite state. This then records the change in arithmetic sign of the input data represented by the pulse rate input.

The positive and negative going serial pulses at the integrator pulse input **14** are fed similarly to another pulse depolarizer **22** which transforms all the pulses into positive going. However, each of the pulses appearing at the integrator

pulse input **14** will selectively appear on pulse depolarizer output line **23***a* or **23***b* respectively representing corresponding positive and negative data input pulses. All pulses on lines **23***a* and **23***b* are positive going. As mentioned before, integrator **13** has the property of being incremented or decremented by each input pulse. In this embodiment, register **13** contains absolute quantities with the arithmetic sign of the quantity being determined and recorded or held elsewhere. Therefore, the decision as to whether a particular input pulse at **14** should increment or decrement the contents of the integrator **13** depends on the polarity or arithmetic sign of the input data pulse and the sign of the quantity contained in the integrator. For example, if the content of integrator **13** represents negative 30, a negative going integrator input pulse should increment the counter since it is adding a negative quantity to a previous negative quantity. If the content of the integrator **13** is plus 30, then a negative going input pulse should reduce the content by one by making the integrator count down. The four possible combinations of conditions that could exist are sensed and recorded in a manner which will be described later in greater detail and entered into the input signal pulse director **24**, which then tells the input pulse whether to make integrator **13** count up or down by placing a pulse on the corresponding output line **24***a* or **24***b*. The pulse is then fed into the lowest order stage **13***a* of integrator **13** and is rippled through the remainder stages, if necessary, to correspondingly change the content in a conventional manner so that the content of the register is changed by one for each input pulse. The auxiliary input pulse director **26** is merely an alternate way of feeding a "times 10" input into register **13**. In other words, in some instances it may be useful to be able to feed a pulse train, similar to the integrator pulse train, into the second stage of register **13**, bypassing the lowest order stage. This is done through a pulse depolarizer **25**, which is made similar to pulse depolarizers **20** and **22**, and auxiliary input pulse director **26** which is similar to pulse director **24** and determines whether the input pulse should increment or decrement the contents of the register **13**.

Signal representations of the content of the respective register stages **13***a*—**13***d* are fed into corresponding stages of the logic network, **16***a*—**16***d* through input lines **27***a*—**27***d* and similarly, signal representations of the content of counter stages **11***a*—**11***d* are transmitted through lines **28***a*—**28***d* into the corresponding stages of the logic network **16**. The pulse rate input signal train coming out of pulse depolarizer **20** is also fed into logic network stage **16***a* via line **29** and as the pulse ripples through the respective stages of the counter, if necessary, it is similarly fed into corresponding stages of the logic network. In each of the respective stages of the logic network **16**, the signal representations from the integrator register **13** are combined with those of the counter **11** to selectively gate out a number of the pulse rate data pulses through the corresponding stage of the logic network, this output signal thereby being a function of the content of the register **13**. The pulse outputs from the respective logic network stages **16** *a*—*d* are fed individually into pulse polarizer **30** where they are suitably combined to form a serialized train of pulses having the correct polarity. The conditions which determine the correct polarity for the output pulses are the sign or polarity of the pulse rate input pulses and the sign of the integrator quantity so that signal indications from sign flip-flops **21** and **31** are fed to pulse polarizer **30** to set the polarity of the output data pulses appearing at **17**. This achieves what is commonly known as four-quadrant multiplication. Both sign flip-flops are of a common variety which have two stable states and are flipped to an opposite state, when necessary by a suitable triggering signal. As stated earlier, flip-flop **21** is triggered by a change in polarity of the pulse rate input pulses at **12**. The integrator sign flip-flop **31** is triggered from signal pulse director **24** which contains circuitry to sense when the content of the integrator **13** has changed sign. This will be described later in detail. Sign flip-flop **31** not only feeds a control signal to pulse polarizer **30** but also its state is used in signal pulse directors **24** and **26** to determine whether the pulse inputs at **14** or **145** should make integrator **13** count up or down.

As mentioned earlier, the integrator data pulse train and the pulse rate data input train at input lines **14** and **12** respectively contain both negative and positive going pulses. Ordinarily on each input line there will be a series or sequence of positive going pulses representing a positive quantity or a series of negative going pulses representing a negative quantity rather than alternate negative and positive going pulses, although the latter could occur in some exceptional cases. In the general case, the pulse inputs fed to a module on line **14** (FIG. **1**) or **12** will be pulse train outputs on line **17** from some module. The operation of the pulse depolarizer circuits **20**, as shown schematically in FIG. **3**, will therefore be described for this general case. However, there is one point that should be made here. Although the drawing and the description heretofore and hereafter are concerned with the case of a single integrator pulse input line **14**, the more general case is that there are a plurality of such input lines in a module feeding a single integrator. Each input line, such as **14**, enters a separate pulse depolarizer circuit **22**, which produces outputs on its own lines corresponding to **23***a* and **23***b*. The latter are then combined in a logical OR arrangement (not shown) to produce a single set of positive and negative lines **23***a* and **23***b* into the pulse director **24** where the signals are treated as one combined signal train. Typically, there may be six separate input lines feeding six separate depolarizer circuits and two sets of six input OR's for combining the positive and negative outputs from the latter. This multiple input arrangement requires only that there be a suitable time phasing among the various pulse input signal lines so that data pulses do not appear in exact coincidence with one another. This time phasing is ordinarily easily achieved by suitable selection of input pulse lines from among various clock phasings which are available. Since all of the pulse depolarizers are identical, only one will be described herein.

By means which will be described later in somewhat more detail, at zero or steady-state, i.e., no pulse present, the input line is at a plus 10 volts and the pulses, both negative and positive going, have an amplitude of 10 volts. The input signal line **35**, through a voltage divider biasing network consisting of resistors **36** and **37** between plus 20 volts and ground, splits into paths **35***a* and **35***b*. One of these paths, **35***a*, goes through a set of three 5-volt Zener diodes **38** and the other path **35***b* goes through a single 5-volt Zener diode **39** and, in turn, through RC combinations **40** and **41** to the base of NPN transistors **42** and **43** respectively. The emitter elements of both transistors **42** and **43** are connected to ground and the collector element of transistor **42** is coupled directly to output line **44**. The collector element of transistor **43** is connected through an RC combination **45** and a suitable biasing network from plus 5 volts to the base of NPN transistor **46**. The emitter element of the latter transistor is also connected directly to ground and the collector element is connected directly to output line **47** as well as back to the plus 5-volt source through resistor **48**.

At steady-state condition the input line **35** is at plus 10 volts which is enough to make Zener diode **39** conduct so that transistor **43** is driven to virtual saturation putting its collector at effective ground condition. This in turn puts transistor **46** effectively in the nonconducting condition so that its collector and the output line **47** are essentially at plus 5 volts. At the same time, Zener diodes **38** are still not biased sufficiently to cause them to conduct so that the base of transistor **42** is effectively at ground, keeping it in the nonconducting state so output line **44** is at approximately plus 5 volts potential. A positive going pulse on input line **35** raises it up to approximately plus 20 volts which means that Zener diode **39** is still conducting resulting in output line **47** still being at the plus 5-volt potential level. However, Zener diodes **38** are biased into conduction driving the base of the transistor **42** positive causing it to conduct to virtual saturation to drop the output line **44** connected to the collector element down to approximately ground level. Under the third condition where the input pulse

is negative going, input line 35 is at zero level which brings the Zener diode 39 out of conduction to cut off transistor 43 placing its collector at plus 5 volts which drives the base of transistor 46 positively causing the latter to conduct to virtual saturation and dropping its collector and output line 47 down to approximately ground potential. In summary then, it can be seen that a positive going input pulse produces a negative going pulse output on line 44 and a negative going input pulse produces a negative going output pulse on line 47.

It is illustrated with dotted lines in FIG. 3 that the two output lines 47 and 44 can be combined in logical OR circuit 49 to produce positive polarity pulses on output line 50 in the presence of any input pulse, positive or negative. This is the circuit arrangement which is used to feed the pulse rate inputs at 12 into counter 11 and to the logic network 16 whereas the double line output is the arrangement that is used to feed the integrator pulse inputs at 14 out of pulse depolarizer 22 to lines 23*a* and 23*b*.

The pulse depolarizer 20 feeds pulse outputs to sign flip-flop 21 to cause it to change state whenever the polarity of the input pulse changes. This is done in a conventional manner by connecting the negative pulse line 47 to one side of the flip-flop and the positive pulse line 44 to the other side of the flip-flop so that only a change in pulse polarity will cause the flip-flop to toggle. In this manner the sign of the input pulses in the pulse rate train is recorded for future use as will be described later.

Pulse depolarizer 20 also feeds pulse outputs, all positive going, into one stage of logic network 16 through output line 29 and also to the lowest order stage 11*a* of the counter 11. All four stages of counter 11 are virtually identical so only one will be described in detail as illustrated in FIG. 4. A decimal stage contains four identical binary state flip-flops identified respectively as A, B, C and D. Each of these flip-flops, as well as those in register 13 and elsewhere in the apparatus, are arranged in what is commonly known as the master-slave configuration with each flip-flop actually containing two separate but interconnected flip-flops, one being the master and the other being the slave. Pulse inputs to trigger the flip-flop are fed into the master which responds to the leading edge of the input pulse but the slave does not respond until the trailing edge of the input pulse. In this manner there is no danger of a type of a runaway operation that could occur if the output changed while the input pulse was still being applied, especially in those circuit arrangements wherein the condition of a flip-flop is actually used to control the triggering input action. In any event, this design of the flip-flops is not considered to be a part of the invention and is quite commonplace today.

In a conventional manner, the flip-flop arrangement provides a binary coded decimal (*bcd*) counter stage with each flip-flop representing a different binary digit so that ordinarily the stage is able to count from zero through 15. In converting to decimal, six of these 16 possible counts are eliminated. The counter stage operates in a conventional manner with each input pulse appearing on line 50 toggling the lowest order flip-flop A. The toggling action of other than the lowest order flip-flop is controlled by the states of the various flip-flops through logical AND and OR circuits. The toggling pulse input to flip-flop B appearing on line 52 is gated to AND 53 by the combination of flip-flop A being in the one state and flip-flop D being in the zero state. The only time that flip-flop D is in the one state is at the count of 8 or 9. When it reaches the latter, which is the maximum possible count, the next input pulse should result in all the flip-flops in that stage being at zero, which is the reason for controlling the toggling of the flip-flop B with the state of flip-flop D. The toggling of flip-flop C is controlled conventionally by the condition of flip-flops A and B both being in the one state at AND 54. The toggling of flip-flop D is controlled at AND 55 by all of the lower order stages being in the one state and additionally at AND 56 by flip-flop A being in the one state and flip-flop D being in the one state. This covers the condition of toggling flip-flop D from zero to one when the content of the stage is changing from 7 to 8 and toggling it back from one to zero when the content of the stage is 9 and another pulse is received. These two combinations are OR'd at 57. An input pulse is directed to ripple or pass through to the next higher order digit stage, which is a duplicate of the one described and illustrated in FIG. 4, by the condition of the lower order digit stage being zero which is detected by AND 58.

Register or integrator 13, FIG. 7, is similarly made up of four bed stages with each decimal stage containing four binary state flip-flops 60 identified respectively as A′, B′, C′, and D′ in corresponding binary order. The logic is arranged similarly to that in counter 11 so each stage only counts zero through nine. The manner in which this is accomplished is of no great moment since it is done following normal and well-known logic design techniques. A number of AND, OR and inverter (INV) elements are arranged with proper signal inputs from the various flip-flops within the decimal stage to direct the pulse inputs appearing on lines 61 or 62 into the correct flip-flop 60 within the decimal stage to trigger it to its proper state. It should be pointed out that inverters are used here as well as elsewhere because the polarity of the signal is inverted in each logic element so in order to return the signal back to the desired polarity, in some instances it has to be fed through an inverter. The inverters do neither but invert the signal polarity. The prime (′) designation for the flip-flops is merely to distinguish the integrator 13 stages from those in the counter 11 while using the same letter designations. In the usual and commonplace manner, outputs from the inverted side of the respective flip-flops in the *bcd* stage are designated with a line or bar symbol above the flip-flop letter designation.

The critical feature here which distinguishes integrator 13 from counter 11 is its ability to count up or down, that is, increment or decrement by one for each input pulse received. A pulse appearing on input line 61 causes the content of the integrator to decrease by one and a pulse received on line 62 causes the content of the integrator to increase by one. For clarity, inputs to the various logic elements are identified by letter designation from the respective similarly identified outputs of the various flip-flops rather than by showing a solid line electrical connection. Each of the three remaining stages of the integrator register 13 are identical to that shown in FIG. 7. The pulses appearing at lines 61 and 62 are all of one polarity, in this case positive going. In the event the content of a decimal stage is zero, a pulse appearing on the "countdown" line 61 ripples through this stage and appears on output line 63. Correspondingly, if the content is 9 and a pulse appears on the "count up" line 62, it passes through to appear on output line 64 to provide a pulse input to the next higher order stage. In the commonplace manner, signal representations of the direct or inverted state of each flip-flop in the stage are available for decoding the numerical content of the register or for providing signal representations to be combined with corresponding representations from counter 11 in the logic network 16.

Turning next to the logic network 16, its function is essentially to perform a stage-by-stage logical multiply of the content of integrator 13 with the pulse rate input signal and produce a signal pulse train representing the results. The output signal pulses from each of the four stages of the logic network, 16*a*—16*d*, appearing on lines 66*a*—66*d* respectively, (FIG. 2) are then combined in pulse polarizer 30 into a pulse train appearing on the output line 17.

Turning to FIG. 6, there is shown in detail the arrangement of logic network stage 16*a*. At the bottom of the drawing are a group of AND's 70—77 having inputs from respective flip-flops in counter stage 11*a* identified with appropriate letters. It can be seen that the output signal representations from AND's 70—76 appearing on output lines 70*a*—76*a* respectively represent that the content of the counter stage ranges in arithmetic value from two to eight. When the input conditions to AND 77 are met, its output line 77*a* represents that the content of the counter stage is some value other than zero. The arithmetic values that these respective output lines represent

are shown parenthetically in the drawing near the corresponding line.

At the right-hand side of FIG. 6, are a group of signal lines coming from either the fixed quantity source **15** or integrator **13** (FIG. 1). Lines **80—83** carry the signal representations of the direct output of the corresponding flip-flops in the integrator **13** or its equivalent in the fixed quantity source **15** and lines **80*a*—83*a*** are for the corresponding inverted outputs. In the usual fashion, when a given line is active, it represents the corresponding binary condition of its associated flip-flop from which the content of the source can be determined. For example, if lines **80, 81, 82** and **83*a*** are active, the fixed quantity or the integrator stage has an arithmetic value of **7**.

The decoded arithmetic values appearing on signal lines **70*a*—76** representing values two through eight are combined with the signal representations of the content of the fixed quantity source or the integrator, appearing on lines **80—83** and **80*a*—83*a***, in a number of additional logical AND and OR circuits with some inverters included which are used to obtain proper polarity signals. The results of this further combination which appears on line **84**, is combined with the signal representation on line **77*a*** (not zero) to gate the pulses on line **29** from pulse depolarizer **20** through AND **85** to output line **66**.

An example is best used to describe the operation of the logic network. Taking a typical case of an integrator **13** and counter **11** containing four decimal stages, it can be seen that if the integrator contains its maximum value possible, 9999, that for every 10,000 pulse rate data pulses on line **12** there should appear 10,000 (less one) pulses on output line **17**. For all practical purposes this is multiplication by one. It is impossible to achieve multiplication exactly by one but it can be approached by adding register stages. For descriptive purposes let it be assumed, for example, that integrator **13** contains the quantity 3,000. This means that three of 10 pulse rate data pulses on line **12** should be gated out to appear on output line **17**. It naturally follows that if integrator **13** contained the quantity 300, then only three out of every 100 pulses should be gated out and mutatis mutandi for the integrator contents 30 and three. In the first example, it might be relatively easy to arrange a system in which for every group of 10 pulses, the first three are allowed out and the next seven are blocked. This, however, produces spurts of pulse energy on the output line followed by extended gaps or quiescent periods. Although this would produce a correct signal representation of the numerical quantity, it may produce some undesirable side effects on the circuitry. It has been found preferable to try to space the pulses more evenly so that the pulses and gaps are more evenly distributed in the signal train. This is achieved by giving each pulse in a group of 10 pulses a sequence order number, i.e., the first sequential pulse being given number **1**, second pulse **2**, etc., through **9**. Then an arbitrary decision is made as to which of these pulses out of a group of 10 should be passed through to represent the numerical value. This selection, although arbitrary, is made in an effort to see that on the average the pulses will be evenly distributed. The selections shown in Table **1** illustrate how this is done.

TABLE 1

	Pulse sequence No.
Multiplier:	
1	5
2	3, 7
3	2, 5, 8
4	2, 4, 6, 8
5	1, 3, 5, 7, 9
6	1, 3, 4, 6, 7, 8
7	1, 2, 4, 5, 6, 8, 9
8	1, 2, 3, 4, 6, 7, 8, 9
9	All

Turning again to the example and back to FIG. **6**, it should be kept in mind that the same pulses that are appearing on line **29** for being gated out to the output line **66** are also being fed into the corresponding digit order stage of counter **11** which, in essence, merely counts these pulses. If it is assumed that the counter stage starts from zero (which it must always do after each 10,000 pulses) and that integrator **13** contains the quantity 3,000, then initially all lines **70*a*—77*a*** from counter **11** are inactive while lines **80, 81, 82*a*** and **83*a*** from integrator **13** are active. Lines **80, 81** and **82*a*** provide three of the four inputs to AND **88**. Line **83*a*** is not used here as an input because it would be redundant. By its inherent operation, as earlier described, the integrator stage cannot possible contain a quantity other than the number three when lines **80, 81** and **82*a*** are active. If the integrator content remains stable, whenever the fourth input to AND **88** is active output line **88*a*** becomes active and through succeeding OR's, AND's and INV's will satisfy the conditions to gate a pulse appearing on line **29** out to line **66**.

The fourth input to AND **88** is output line **89*a*** from OR **89** and the three input lines to the latter are **70*a***, **73*a*** and **76*a*** respectively representing quantities **2, 5** and **8** in the counter stage. This means that when the counter stage reaches any of those three values, line **89*a*** will become active to produce the necessary fourth input to AND **88**. After two pulse rate data pulses are received by the stage of counter **11**, line **70*a*** will become active to satisfy OR **89** and produce the proper conditions at AND **88** so that a pulse will be gated out to line **66**. It should be noted that the pulse rate data pulse which sets the counter stage to this quantity is not the one that is gated out through AND **85** because of inherent delays in decoding through the logic network. After the counter stage is set to two, it is the next sequential pulse that is gated out. This next sequential pulse also increments counter stage **11** so that it now contains value three and the input conditions to AND **88** are no longer fully satisfied. Only after a total of five input pulses have been received by the counter are the conditions once again fully satisfied at the input to AND **88** to result in an output pulse being gated out to line **66**. Similarly, when the counter stage reaches the value eight the same conditions are met. It can be seen then that out of 10 pulse rate data pulses received, only three are gated to the output line and they are those pulses identified by sequence order numbers **2, 5** and **8** so that the pulses are distributed quite uniformly over the range of 10 pulses. The logic network operates in the same manner for each of the possible values contained in the counter **11** and the integrator **13** so there will be produced on the output line **66** from each corresponding logic network stage a series of pulses of the desired number and in a suitable spacing arrangement. Referring back to FIG. **2**, it should be noted that the most significant digit order stage **13*d*** of integrator **13** is combined with the least significant digit order stage **11*a*** of counter **11** to produce the results in the manner described.

The positive going signal pulse trains appearing on output lines **66*a*—66*d*** from the logic network stages provide inputs to OR **90** (FIG. **5**) in pulse polarizer **30**. The output of OR **90** is fed as a separate input to each of four different AND's **91—94**. It should be noted that if the pulse rate data signal is negative and the integrator contains a positive quantity or if the pulse rate data signal is positive and the integrator contains a negative quantity, then the corresponding output pulse should be negative. If both the integrator content and the pulse rate data are positive or negative then the output pulse should be positive. This four-quadrant multiplication is accomplished in pulse polarizer **30** as shown in FIG. **5**. An input to AND's **91** and **92** appearing on line **95** comes from sign flip-flop **21** which reflects the polarity of the pulse rate data signal pulses and is active when this pulse is positive going. This is obtained merely by taking the signal designation from the direct output side of the flip-flop. The signal indication from sign flip-flop **21** that the pulse rate data signal is negative going appears on line **96** which provides inputs to AND's **93** and **94**. On line **97** a signal indication showing that the content of integrator **13** is positive is received from flip-flop **31** and is an

input to AND's 91 and 93. Lastly, on line 98 a signal indication of integrator 13 containing a negative quantity is received from flip-flop 31 and applied as inputs to AND's 92 and 94. It can be seen then that if both the pulse rate data signal and the integrator content are positive the input conditions to AND 91 are satisfied so that pulses coming in on lines 66*a*—66*d* will be produced on output line 91*a* through AND 91. If the integrator content is negative and the pulse rate data signal is also negative going the input conditions for AND 94 are satisfied, producing a pulse on its output line, 94*a*, for each pulse received by OR 90. These pulses are then combined in OR 100. In a similar fashion, if the pulse rate data signal is negative and the integrator content is positive, the input conditions for AND 93 are satisfied to produce an output on line 93*a*. If the pulse rate data signal is positive and the integrator content is negative, the input condition for AND 92 are satisfied and pulse outputs will appear on line 92*a*. The signals on lines 92*a* and 93*a* are combined in OR 101. Therefore, OR 101 can be considered to be the negative OR and OR 100 to be considered to be the positive OR.

The output of OR's 100 and 101 are fed to identical circuits so only one of these circuits will be described. The output of OR 100 is fed through diode 102 and RC combination 103 to the base element of NPN transistor 104. The base element is biased through a suitable voltage divider network of series resistors running from +20 volt to ground. The collector element of transistor 104 is coupled through RC circuit 105 to the base element of PNP transistor 106. Power for this collector and base circuit is obtained through resistor 107 from the 20-volt source. The collector element of transistor 106 is connected to output line 108 through resistor 109 and the 20-volt energy source is coupled to the output line 108 through a suitable voltage divider network consisting of resistors 115 and 116.

OR 101 is coupled through diode 110 and RC network 111 to the base element of NPN transistor 112 which has appropriate connections to the 20-volt source. The collector element of transistor 112 is coupled to output line 108 through resistor 113. Using the same illustration as made earlier with respect to describing the operation of the circuit shown in FIG. 3, when there is no signal present or when the lines are at steady-state condition, the +20-volt source maintains output line 108 at +10 volts. A positive pulse output from OR 100 applied to the base element of transistor 104 causes the latter to conduct to bring its collector down toward ground potential. The latter is then transmitted through RC 105 to the base element of PNP transistor 106 causing it to conduct fairly heavily. Resistors 115 and 116 from the +20-volt source to ground are of the same value to produce the +10-volt level on line 108 when in the quiescent condition. The value of resistor 109 is substantially less than either resistor 115 or 116. When transistor 106 is turned on and it conducts to virtual saturation, resistor 115 is effectively shorted out and the +20-volt potential level is effectively applied to line 108 thereby producing a positive going pulse in response to the call for same by one of the inputs to OR 100. A positive output from OR 101 fed through diode 110 and RC 111 to the base of transistor 112 similarly causes it to conduct to virtual saturation. Resistor 113 being of a very small value effectively shorts out resistor 116 driving line 108 down to virtual ground level thereby producing a negative going pulse in response to the call for same by one of the inputs to OR 101. In this manner then the single polarity pulses within the operating module are now transformed back to their correct polarity for further use as a continuous signal train. The only reason for the parallel transistorized circuits which are driven by each of the OR's 100 and 101 is to produce inverted outputs for each if such is desired in the equipment.

As stated earlier, the pulse train appearing at output line 17 contains both positive and negative going pulses representing data having positive and negative quantities and is, in general, the form of the pulse train signals that are applied in as data inputs at 12 and 14. As described earlier, the integrator pulse inputs at 14 go through a pulse depolarizer 22 (FIG. 3) from which they are outputted as positive going pulses on either positive line 23*a* or negative line 23*b*. Before proceeding, it is well to point out that the form of the pulse trains which is described herein is quite an arbitrary selection. The steady-state condition of +10 volts with negative and positive pulses having 10-volt magnitudes is purely a matter of choice and other selections can be made with corresponding modifications to the circuitry involved. Similarly, the 5-volt pulse swing which is used internally in the module is merely a matter of choice and other energy levels and pulse magnitudes can be selected and the circuits designed accordingly.

Positive line 44 and negative line 47 from depolarizer 22 (FIG. 3), respectively corresponding to lines 23*a* and 23*b* in FIG. 2, are respectively coupled to lines 120 and 121 in FIG. 9. Line 120 provides an input to AND's 122 and 123 and line 121 provides an input to AND's 124 and 125. Since the function of the pulse director 24 is to direct the incoming pulse to either the count up or count down lines 24*a* or 24*b* (FIG. 2) corresponding to lines 62 and 61 of integrator 13 (FIG. 7), the factors which affect this decision must be taken into account. If the sign of the input data pulse on line 14 and the sign of the numerical quantity contained in the integrator 13 are both negative or positive, then the input pulse should make the integrator count up. If the two are of opposite sign, then the input pulse should cause the integrator to decrement or count down.

Let it be assumed that sign flip-flop 31 activates line 126 when the integrator content is negative and activates line 127 when the integrator content is positive. Assuming the former case and that the input data pulse is negative so line 121 is active, then the input conditions to AND 124 are satisfied to activate its output line 124*a* and produce an input to OR 128. On the other hand, if the input data pulse is positive, line 120 is active to satisfy the input conditions to AND 122 and correspondingly, activate its output line 122*a* and provide an input to OR 129. In a similar fashion, if sign flip-flop 31 designates that the content of the integrator is positive, line 127 becomes active to satisfy the input conditions to AND 125 to produce an input to OR 129 through line 125*a* if the input data pulse is negative or the input conditions to AND 123 will be satisfied to produce an input to OR 128 through line 123*a* in the event the input data pulse is positive. It follows, except for a rare exception which will be described shortly, that an input to OR 129 will produce an output pulse on the down line 130 from inverter 131 and an input to OR 128 will correspondingly produce a pulse on up line 132 from OR 133. These output lines are coupled in some manner, not shown, to their corresponding respective lines 61 and 62 in integrator 13 (FIG. 7).

Working in conjunction with the pulse director is what is referred to as a "pass-through-zero" circuit arrangement. This circuit has the twofold function of informing sign flip-flop 31 that the sign of the content of the integrator register 13 has changed (which occurs whenever the quantity in the register passes through zero value) and at this pass-through-zero condition prevents a pulse from appearing on the countdown line 130. This is because, as stated earlier, the content of the integrator is always an absolute quantity yet may be of a negative sign. For example, if the integrator 13 initially contained some positive number such as 10 and there followed 10 consecutive negative input data pulses, the content of the register would be reduced to zero. If this were followed by another negative pulse, ordinarily all the stages in the integrator would be changed from zero to nine, setting the integrator to its maximum quantity. Some devices do operate in this manner and always carry a sign bit or other designation along with the number. In this instance it was decided to record and hold an indication of the sign of the quantity contained in the integrator but that the integrator should hold the absolute quantity. Therefore, if a positive quantity in the integrator is being reduced by a series of negative pulses, the first negative pulse after the integrator has reached zero should make the integra-

tor increase or count up by one. Mutatis mutandi for a negative quantity in the integrator.

Decoding of the content of the integrator to get a signal indication when the quantity reaches zero is accomplished by feeding a signal indication from each flip-flop in the integrator, via input lines collectively identified with reference numeral **135**, into a group of four AND's **136**. The outputs from the latter, in turn, provide four inputs to AND **137** through INV's **138** which merely provide a proper polarity to the signal into AND **137**. Output line **137***a* is activated or up at all times except when the condition occurs that the integrator quantity reaches zero. This means that one of the inputs to AND **139** is always up except for that single instance so that with the proper combination of signs of the input data pulse and the integrator quantity, down line **130** will be activated in the manner described earlier. However, when the condition occurs where the integrator content is reduced to zero so that line **137***a* is down, the down line **130** cannot be activated because one of the inputs to AND **139** is unsatisfied. Concurrently, however, through INV **140** the input to AND **141** through line **140** *a* is satisfied so that a pulse signal output from OR **129** appearing on line **129***a* which would otherwise produce a pulse on down line **130**, is detoured to AND **141** to produce an output pulse on output line **141***a* to provide an input to OR **133** and a corresponding output on up line **132**. At the same time a pulse also appears on line **142** to toggle or trigger sign flip-flop **31** to its opposite state thereby recording the fact that the sign of the integrator quantity has changed. This, then, will be reflected back to pulse director **24** by a change in the active state of lines **126** and **127**. Later pulses appearing on lines **120** and **121** will then produce outputs at lines **130** or **132** in the normal fashion.

The second stage, **13***b*, of register or integrator **13** has an auxiliary input through which the integrator can be incremented by an amount greater than unity by each input pulse. In this instance, with the input being fed into the second decimal digit stage, the integrator content increases by 10 for each auxiliary input pulse appearing on line **145** (FIG. **2**). The auxiliary input pulse director **26** operates similarly to pulse director **24** and means are provided for feeding input pulses coming from the lowest order digit on up to the next higher order digit stage.

Turning to FIG. **8**, sign flip-flop **31** provides a signal indication on lines **146** when the sign of the integrator quantity is positive and on line **147** when the sign of the quantity in the integrator is negative. These signal indications are combined in AND's **148**, **149**, **150** and **151** with signal indications appearing on auxiliary input lines **152** and **153** respectively representing that the auxiliary input signals are positive and negative. It can be seen quickly that in the event the auxiliary input signal and the integrator quantity have opposite signs, down line **154** will be active through OR **158** whereas if both have the same sign, up line **155** will be active through OR **159**. When the auxiliary input is not being used, the normal inputs from the lower order digit stage **13***a* will appear on lines **156** and **157** to produce the proper signals on the down and up lines **154** and **155** through OR's **158** and **159**. Lines **154** and **155** are the input lines to the second stage, **13***b*, of integrator **13**.

EXAMPLE

The following is a relatively simple example of how the present invention can be used to perform what is ordinarily an analog function by using digital pulse techniques. It should be understood, of course, that this is a mere illustration and no limitation is intended. The example involves the simulation of the change in the potential across a capacitor which is discharging into a resistive load. The charge voltage on the capacitor is expressed by,

$$E_c = Eoe^{\frac{-t}{RC}}$$

where Eo is the initial potential across the capacitor at $t=0$ and t is time in seconds. Using arbitrarily chosen values, assume that Eo is equal to 0.9 and 1/RC is equal to 0.2. This could indicate that a 1-farad capacitor which is initially charged to a potential of 0.9 volts is being discharged through a resistance of 5 ohms. The problem is to simulate the rate of change of the potential.

To accomplish this, two modules of the nature described earlier are connected together in the manner as illustrated in FIG. **10**. A fixed frequency clock pulse of 10,000 pulses per second (10 KPPS) is fed into the pulse rate input of module **160**. The integrator in module **160** is preset to contain a value of 0.9000, representing the initial charge in coulombs. The output of module **160** is fed into the pulse rate input of module **160***a*. The latter contains a fixed quantity of −0.2000, equal to the value 1/RC, instead of a changing value in an integrator. The output from module **160***a* is fed back as an input to the integrator in module **160**. Although the circuit operation is dynamic, for the purposes of explanation and description there are some static conditions which can be considered. The initial preset quantity in module **160** is combined with the 10 KPPS clock input in the logic network to produce an output signal having a frequency of 9 KPPS. This signal fed into the pulse rate input of module **160***a* is then combined in its logic network with the fixed quantity of −0.2000, producing a signal output of negative going 1800 PPS. This pulse train, being fed back to the input of the integrator in module **160**, now changes the quantity in the latter and it in turn produces an output signal pulse train, through the operation of the logic network, which is a function of this changing quantity. The continuous circulatory operation in this manner produces values in the integrator of module **160** which at any instant represent the charge on the capacitor. These values will fall toward zero asymptotically as is the case with the charge on the capacitor and with the same time constant.

To obtain an indication of the function being performed by the unit, it is, of course, necessary to either read out the data continuously or periodically. This data can be applied to utilization devices such as visual displays in the form of oscilloscopes or plotters or the like or other apparatus for further processing or for controlling certain operations. The significant or important data generally appears within a module in integrator **13**. This data can be fed out to utilization devices by parallel readout and decoding of the content of the stages of the integrator. This manner of readout may be appropriate where the data is being fed to another digital device or where it is being used to drive numbered display tubes or the like. However, where the utilization device is analog in nature, such as an oscilloscope, it is generally necessary to convert this digital information into a corresponding analog quantity. A variety of circuits, generally referred to as digital to analog (*d/a*) converters, have been designed and used over a number of years for this purpose. The circuit described below is merely intended to be illustrative and no limitation thereto is intended.

If it is assumed that a potential of 1 volt should be produced for every 1,000 steps or counts, then a four-decimal stage register or integrator containing the maximum possible value should produce 9.999 volts (which can be rounded off to 10). If the integrator contains its maximum negative quantity, a −10-volt signal output should be produced. However, if for certain reasons all output values must be positive, then the zero point could be arbitrarily set to the +10-volt level so that a maximum positive content will produce a +20 volt potential level and maximum negative quantity results in zero or ground potential level. Turning to FIG. **11** which illustrates a read out system including a *d/a* converter for a single decimal stage, a direct output from each of flip-flops A, B, C and D in a decimal stage appears on input lines **163**, **164**, **165** and **166** respectively. The inputs from flip-flops A, C and D are gated at AND's **167**, **168** and **169** respectively with a signal on line **170** which represents that the content of the register or integrator is positive. This can be and is ordinarily obtained

from the sign flip-flop **31** (FIG. **2**). The B input does not have to be gated because an analysis has shown that the state of the B flip-flop is read out directly whether the quantity contained in the integrator or register is positive or negative. In the event the number contained in the integrator stage is negative, the complement line **171** is activated from sign flip-flop **31** to provide a gating input to AND's **172**, **173** and **174**. To accommodate the operation of the integrator to the *d/a* output level requirements, when the integrator contains a negative quantity the nine's complement is used to provide the readout signals to the *d/a* circuitry. At AND **172** the inverted output of flip-flop A appearing on line **175** is gated by the signal on complement line **171**. Analysis has revealed that the nine's complement will produce a signal representation of binary one value from the C flip-flop only when B and C are of opposite binary values. This is achieved logically in AND's **176** and **177** whose outputs are then combined in OR **178** which has its output gated through AND **173** by the complement signal on line **171**. It can be also shown that the nine's complement will produce a binary one value from the D flip-flop only when flip-flops B, C and D are all in the zero condition. This condition is logically derived at AND **174**.

The two possible conditions under which a signal output of binary one are obtained from the A flip-flop are combined in OR **179**, the conditions for the C flip-flop to produce a binary one signal output are combined in OR **180** and the conditions for the D flip-flop to produce a binary one value output are combined in OR **181**. These in turn produce outputs on their respective output lines **182**, **183** and **184**. As stated earlier, the sign of the quantity in the register or integrator does not affect the signal readout from the B flip-flop so its output always appears on line **164**. To review briefly, the reason the nine's complement values are used for negative quantities in this illustration is that the register or integrator quantities are of absolute magnitude which would always appear positive to outside devices which would not produce the proper output signal.

The *d/a* conversion circuit to which the direct or nine's complement signal indications are fed is not considered a novel part of the invention since circuits of this nature have been used before in the *d/a* converter field. Therefore, only a superficial description of the operation of the circuit will be given. It can be assumed that the fixed and variable resistances, identified as a group by reference numeral **185**, are selected and arranged to produce an output voltage level on output line **186** of the desired quantity in accordance with the values appearing on the input signal lines **187A**, **187B**, **187C** and **187D** from the respective circuits associated with the corresponding flip-flops in the integrator stage. It can be shown that a signal indication of value one on line **182** will result in transistor **188** conducting to effectively place +V from line **189** onto output line **187A**. In the event a zero signal indication appears on line **182**, transistor **190** becomes operative to put line **187A** to ground or zero potential. In a similar fashion either +V or ground will appear on lines **187B**, C and D in accordance with the input signal appearing on lines **164**, **183** and **184**. When the corresponding decimal stage contains its maximum value, nine, output line **186** will be at its maximum potential level.

Taking an illustrative example, assume a given stage of the integrator contains the value seven or binary **0111**. This results in lines **182**, **164** and **183** being active and **184** being inactive so that +V appears at **187A**, **187B** and **187C** and ground appears at **187D**. The result is a potential of some level representing this quantity appearing on line **186**. If the same register stage contains negative seven, the nine's complement output which is produced is binary **0010**. This results in lines **182**, **183** and **184** being in the zero or inactive condition and line **164** being in the active or one condition. Only line **187B** is then at the +V level so the arrangement of resistors **185** produces a potential level equal to two-sevenths that for the plus 7 value but of positive polarity. It naturally follows that for a four-stage register or integrator there would be a group of circuits similar to those appearing in FIG. **11**, one for each stage of the register or integrator.

The foregoing has been a detailed description of the structural and functional aspects of the invention. The following is a philosophical description of the invention and the illustrative embodiment.

This invention concerns a parallel network of digital elements for the purpose of solving algebraic and differential equations. The philosophy of system organization and parallel interconnection is similar to that used in commercial analog computers of the operational amplifier type. The principal difference here is that rather than operational amplifiers the elements are digital circuits operating on discrete quantities.

An illustrative block diagram of such a system is shown below:

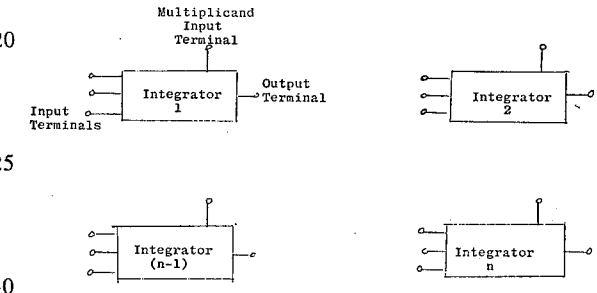


ILLUSTRATION 1

Each integrator element has one or more regular input terminals and has an input-output transfer function of the form:

$$I_A,\ \text{output} = K\int_{t_1}^{t_2}[I_1(t)+I_2(t)+I_3(t)\ \cdots\ +I_n(t)]dt$$

or

$$I_B,\ \text{output}(s) = K\left(\frac{I_1(s)+I_2(s)+I_3(s)\ \cdots\ +I_n(s)}{s}\right)$$

so that the output is a function of the time integral of the sum of the input signals. A system containing a multiplicity of such integrating elements may be used to effect a continuous solution of a given equation or a given set of simultaneous equations. For this purpose any input terminal may be connected to any output terminal (including the output of the same element) in any combination necessary to effect a solution of a given equation or set of equations.

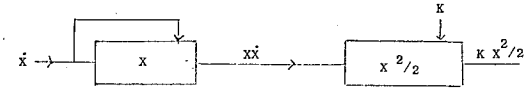
Each integrating element is also provided with a separate terminal called a multiplicand input terminal. If a direct integral function, such as that implied in equations I_A and I_B, is intended, a constant input signal, K, is applied to the multiplicand input terminal. The result, as shown in equations I_A and I_B, is that the integral of the sum of the input signals is multiplied by a constant factor, K.

Alternatively, a variable signal, M, representing a problem variable, may be applied to the multiplicand input terminal to create an output signal as in equations 2_A and 2_B:

$$2_A,\ \text{Output} = \int \{M(t)\ [I_1(t)+I_2(t)+I_3(t)\ \ldots I_n(t)]\}\ dt$$

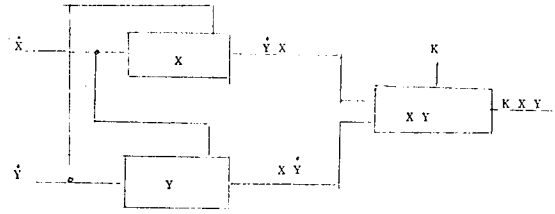
$$2_B,\ \text{output} = M(s)\ \left[\frac{I_1(s)+I_2(s)+I_3(s)\ \ldots I_n(s)}{s}\right]$$

A few simple but typical examples of interconnected integrating elements follow:



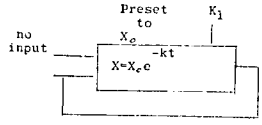
$$K\int X\,\dot{X}\,dt = \frac{K\,X^2}{2}$$

Illustration 2



$$K\int(\dot{X}Y + \dot{Y}X)\,dt = KXY$$

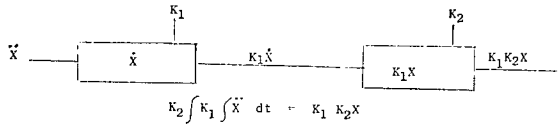
Illustration 3



$\dot{X} = KX$ $\qquad \dot{X} = K(X_oe^{-kt}) = KX$

An exponential is the only function whose derivative is proportional to the function itself.

Illustration 4



$$K_2\int K_1\int\ddot{X}\,dt = K_1K_2X$$

Illustration 5

The digital integration technique employed in this invention is pulse rate integration. All system input pulses originate in a multiphase pulse clock, and all pulses are derived initially from a constant frequency, constant amplitude, constant width pulse generator which is not considered a part of this invention so its details are of no particular concern. Such generators are well known and in wide use. The pulses emanating from the constant source are allocated in equal or unequal ratio, as desired, among a multiplicity of clock phase output terminals where they are available for system use. Again, the allocation scheme is not a part of this invention and may be achieved in any convenient manner, such as with ring counters or other well-known techniques. The reason for having multiple clock phases is that when two or more input terminals of an integrator element are used for the implementation of a given equation, there is no possibility of pulse coincidence. That is, two pulses will not arrive at the same time on different input terminals. This ensures that the integrator will respond to each input pulse separately.

The pulse rate integrator counters are preferably, but not necessarily, the binary coded decimal type, with the quantity stored in the register representing the absolute magnitude of the integral. A separate bistable circuit holds the sign or polarity of the integral. The integrators can accept either positive or negative value pulse rate inputs, and also one or more input pulse rate signals of each polarity value simultaneously. Other implementations such as pure binary notation in ones-complement form would function equally well to perform pulse rate integration. If a parallel network of input-output connections is to be made, as selected by an operator to solve specific equations, the output signals must be in a form suitable for use by the input circuitry. Therefore, the output signals are also pulse sequences, and are produced by the digital quantity stored within an integrator register in the role of a controlling agent or multiplier acting on the pulse sequence supplied to the multiplicand input terminal in the role of a controlled agent or multiplicand. Selective gating of each pulse of the multiplicand input terminal sequence creates an output terminal pulse sequence which represents the product of the multiplier and the multiplicand

Although the described embodiment employs a binary coded decimal pulse rate multiplier, other pulse rate multipliers which are consistent with the system parameters could be used in other embodiments under the teachings of this invention for the solution of algebraic and differential equations.

It should be emphasized that while a pulse rate multiplier is a functional part of this invention, the novelty here resides in the fact that a multiinput bidirectional pulse rate integrator counter register is used as the multiplier control register for a pulse rate multiplier circuit to create an output pulse sequence proportional to (*a*) the integral of the merged input pulse sequences of the integrator register and also proportional to (*b*) the multiplicand input pulse sequence of the pulse rate multiplier circuit. This product output pulse sequence is composed of pulses which are identical in height, width, and other important characteristics compared to the two types of aforementioned input pulse sequences, and is therefore itself suitable to serve as an input pulse sequence to other integrator elements in a parallel network arrangement of such elements. This makes it possible to generate solutions of integral-differential equations in a more accurate, versatile, rapid, and stable fashion than has been possible heretofore.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

I claim:

1. Digital calculating apparatus, comprising in combination:

a. multiple-stage, pulse-responsive counter means;

b. means for producing output signal representations of the numerical content of said counter;

c. a pulse train source;

d. means coupled to said source for feeding said train of pulses into said counter means for counting the number of said pulses;

e. multiple-stage register means including an input for inserting a numerical quantity and means for at least temporarily holding said numerical quantity;

f. means for producing output signal representations of the numerical content of said register;

g. logic means combining the output signal representations of said counter means with those of said register means for producing signal representations of the results of said logical combinations;

h. gating means;

i. means coupled to the input of said counter means for feeding said train of input pulses into said gating means; and

j. means for coupling the signal representations from said logic means to said gating means for selectively gating said train of pulses through said gating means in accordance with the logically combined contents of said counter and said register.

2. The invention as described in claim **1** wherein said register means comprises a second pulse-responsive, counter means and further including means for feeding a train of pulses into said second counter means.

3. The invention as described in claim **2** wherein said second counter means is characterized by being able to selectively count up or down.

4. The invention as in claim **3** further including: means for sensing the polarity of the input pulses; circuit means responsive to said sensing means for making all input pulses the same polarity; and means coupled to said sensing means for recording signal indications of the polarity of the first counter input pulses.

5. The invention as in claim **4** further including: means coupled to said second counter means for sensing a change in sign of the quantity contained in said second counter means; means responsive to said change-in-sign sensing means for recording signal indications of said change in sign; and means responsive in part to said latter means for directing the input pulses to said second counter means to count up or down.

6. The invention as set forth in claim 5 further including: another digital calculating apparatus containing a multiple-stage pulse-responsive counter means having means for producing output signal representations of the numerical content of said counter, a pulse train source, means coupled to said source for feeding said train of pulses into said counter means for counting the number of said pulses, a second pulse-responsive counter means characterized by being able to selectively count up or down, means for feeding a train of pulses into said second counter means, means for producing output signal representations of the numerical content of said second counter means, logic means combining the output signal representations of said fist counter means with those of said second counter means for producing signal representations of the results of said logical combinations, gating means, means coupled to the input of said first counter means for feeding said train of input pulses into said gating means, means for coupling the signal representations from said logic means to said gating means for selectively gating said train of pulses through said gating means in accordance with the logically combined contents of said first and second counter means, means for sensing the polarity of the input pulses to said first and second counter means, circuit means responsive to said sensing means for making the input pulses to said first and second counter means all of the same polarity, means coupled to said sensing means for recording signal indications of the sensed polarity of the input pulses to said first counter means; and means for feeding the output from the gating means of one of said digital calculating apparatus to the input of a counter means in the other of said digital calculating apparatus whereby the output of said one digital calculating apparatus constitutes a pulse train source for the other of said digital calculating apparatus.

7. The invention as described in claim 4 wherein said circuit means for making all input pulses the same polarity comprises: a pair of parallel circuit paths connected in common to a single input line; a separate output line for each of said parallel paths; and means responsive to the input pulse on said input line for energizing only one of said circuit paths to produce a pulse on its output line when the input pulse is positive and for energizing only the other circuit path to produce a pulse on its output line when the input pulse is negative.

8. The invention as described in claim 5 further including: circuit means operatively responsive to said polarity recording means and said change-in-sign recording means coupled to the output of said gating means for selectively controlling the polarity of the respective output pulses.

9. The invention as in claim 5 wherein said change-in-sign sensing means comprises means coupled to each stage of the second counter for producing a signal indication when the content of said second counter reaches zero.

10. A computing device using digital techniques for normally analog functions, comprising in combination:

a. register means containing quantized signal representations of analog data;
b. means for combining the signal representations in said register means with fixed frequency clock pulses for producing said quantized analog data in pulse train form;
c. pulse-responsive counter means for summing input pulses;
d. means for feeding said analog data in pulse train form from said combining means to the input of said counter means for continually summing said pulses; and
e. means for producing signal output representations of the content of said counter means to provide a signal indication of the integration of the analog data.

11. The invention as set forth in claim 10 wherein said register means is a pulse-responsive counter means and further including means for continually feeding quantized data into said register means.

12. A computing device using digital techniques for normally analog functions, comprising in combination:

a. multiple-stage, pulse-responsive, digital counter means;
b. means for producing output signal representations of the numerical content of said counter means;
c. a pulse train source;
d. means for feeding the pulses from said source into said counter means for continually counting up the number of pulses;
e. multiple-stage register means including an input for inserting numerical quantities and means for at least temporarily holding the inserted numerical quantities;
f. means for producing output signal representations of the content of said register;
g. signal responsive logic means for combining the output signal representations of said counter means with those of said register means in a predetermined logical fashion and for producing signal representations of the results of said logical combinations;
h. logical gating means;
i. means for feeding the pulses from said pulse train source to an input of said gating means; and
j. means for coupling the signal representation from said first-mentioned logic means to another input of said gating means for selectively passing a train of pulses through said gating means for producing a pulse train which is a function of the content of said register means.

13. The invention as set forth in claim 12 wherein the first-mentioned logic means is arranged to produce signal outputs to said gating means for passing through pulses which are distributed in a substantially uniform manner along the pulse train.