

Jan. 19, 1965

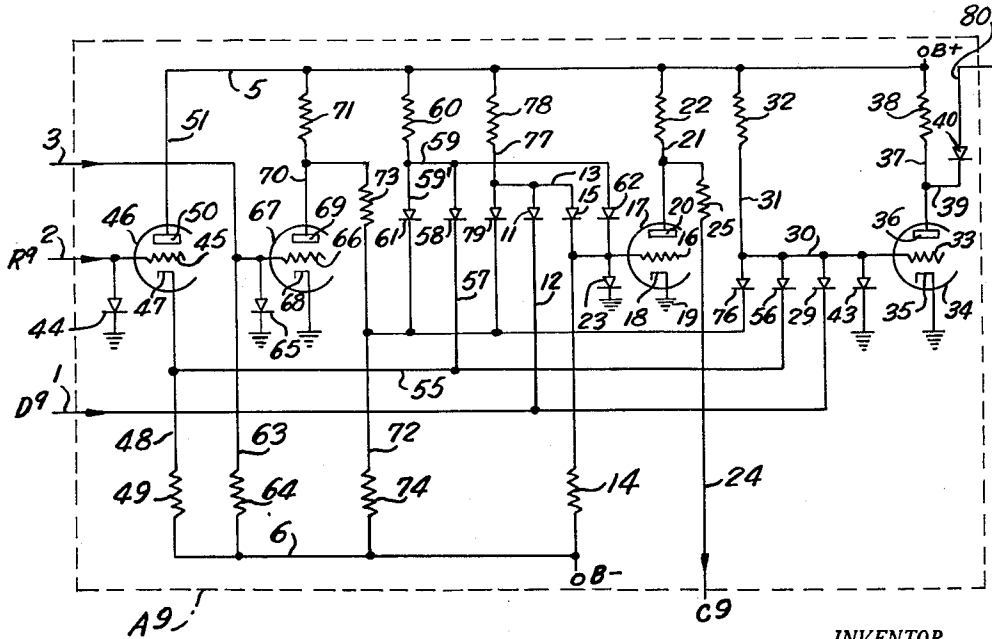
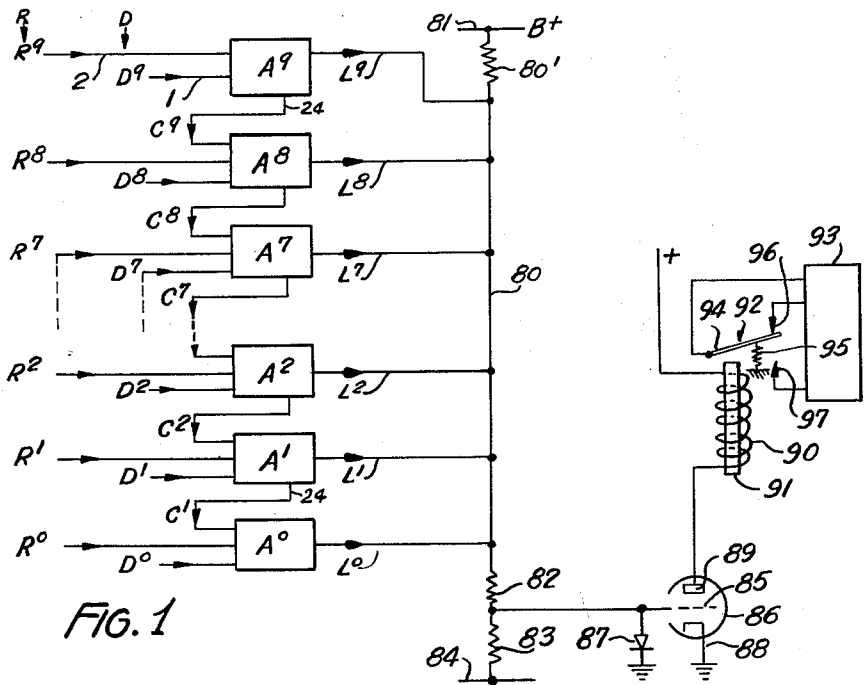
R. H. SCHUMAN

3,166,733

NUMBER COMPARING SYSTEMS

Filed April 21, 1960

2 Sheets-Sheet 1



INVENTOR.
RALPH H. SCHUMAN
BY *Hudson Doughton*
Williams, David & Hoffman
ATTORNEYS

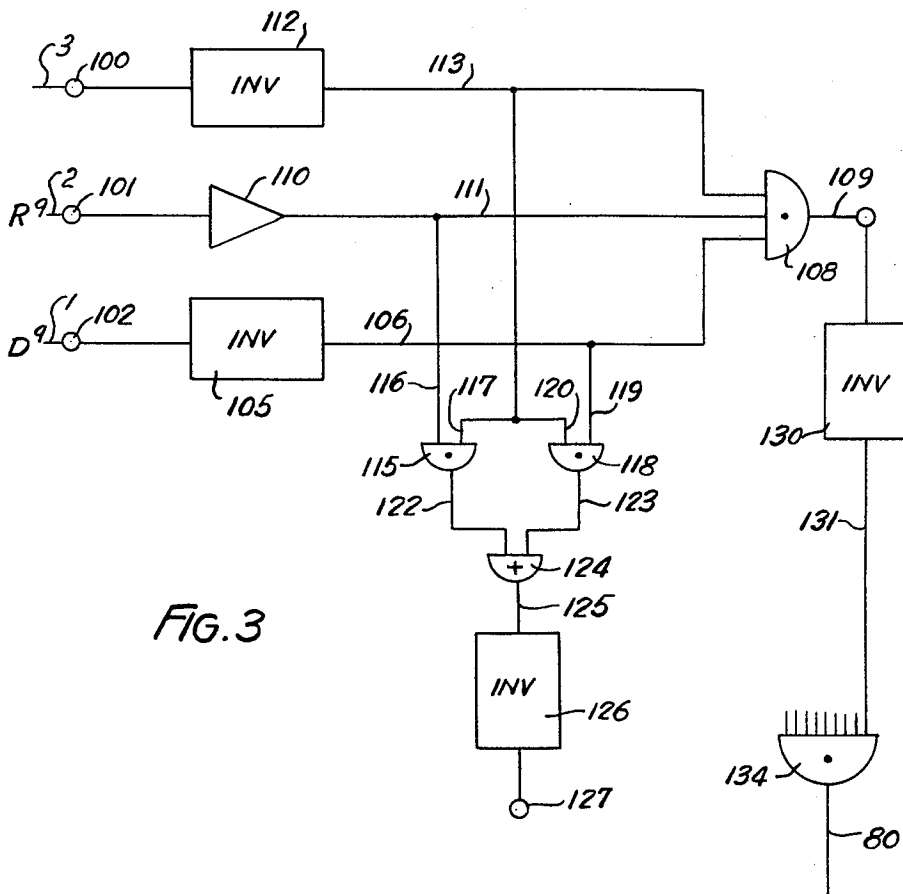
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BY *Hudson, Broughton,
Williams, David & Hoffmann*
ATTORNEYS

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Ralph H. Schuman, Cleveland, Ohio, assignor to The Warner & Swasey Company, Cleveland, Ohio, a corporation of Ohio

Filed Apr. 21, 1960, Ser. No. 23,742

3 Claims. (Cl. 340—146.2)

This invention relates to number comparing systems and particularly to electrical systems for comparing binary numbers.

According to the present invention a system is provided which is arranged to produce a first output condition when one of the compared numbers is greater than the other of the compared numbers and to produce a second different output condition when the other number is greater than or equal to the one number. The system is capable of comparing binary numbers having any number of digit places and may include one or more stages depending upon the number of digit places in the numbers which are to be compared. When numbers having a plurality of digit places are compared then a corresponding number of stages are employed which are interconnected so that each stage compares the digits in corresponding digit places.

Each stage produces a comparison output voltage and a conditioning voltage. The conditioning voltage produced by each stage is applied to the following stage which compares digits in the next lower digit place. The conditioning voltage operates to condition the following stage so as to prevent the production of a comparison output voltage thereby which indicates that one number is larger than the other number when in fact a preceding stage has indicated that the other number is larger than the one number.

Each stage is also energized by a pair of digit input voltages which represent digits of the binary numbers to be compared. The digit input voltages each have two values with each value being representative of a separate binary number. A plurality of AND circuits are included in each stage to be responsive to digit input voltages and to the conditioning voltage from the preceding stage. Each AND circuit operates to produce a predetermined voltage only if all of the voltages energizing the AND circuit are at their more positive values. The voltages produced by operation of the AND circuits determine the values of the comparison voltage and the conditioning voltage.

It is therefore an object of the invention to provide a novel and improved electrical system for comparing magnitudes of a plurality of binary numbers.

It is another object of the invention to provide an improved electrical system for comparing two binary numbers which produces a first output condition when one of the numbers is greater than the other number, and which produces a second output condition when the other number is greater than or equal to the one number.

It is a further object of the invention to provide an electrical system for comparing binary numbers including a plurality of stages each of which is to be energized in accordance with a pair of voltages representing digits in corresponding digit places of the numbers and each of which produces a comparison output voltage and a conditioning voltage which is applied to the following stage to be energized in accordance with voltages representing digits of the numbers in the next lower digit place.

It is still another object of the invention to provide an electrical system for comparing magnitudes of binary numbers which includes a plurality of AND circuits responsive to input voltages which represent digits of the numbers.

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Other objects of the invention will become apparent from the following description taken in conjunction with the accompanying drawings in which

FIG. 1 is a diagrammatic representation in block form of an electrical system incorporating the teachings of the present invention;

FIG. 2 is an electrical circuit diagram of one of the stages forming a part of the system illustrated in FIG. 1; and

FIG. 3 is a logic diagram of the comparator stage shown in FIG. 2.

Referring now to the drawings, there is diagrammatically illustrated in FIG. 1 a comparing system incorporating the teachings of the invention and including a plurality of stages shown in block form and represented by the reference characters A^0 through A^9 . The system of the present invention is capable of comparing binary numbers having any number of digit places and for purposes of illustration the system is shown as including ten stages for comparing two binary numbers each including ten digit places.

Each stage is arranged to compare two digits in corresponding digit places of the two binary numbers. The binary numbers to be compared are represented by the reference characters R and D. The digits of the binary number R are represented by the reference characters R^0 through R^9 with R^9 representing the digit in the highest digit place. In a similar manner the digits of the binary number D are represented by the reference characters D^0 through D^9 with D^9 representing the digit in the highest digit place.

The stages A^0 through A^9 are adapted to compare digits in corresponding digit places of the binary numbers. As an example, the stage A^9 compares the digits R^9 and D^9 in the highest digit place of the numbers R and D. Each of the stages produces a comparison voltage and a conditioning voltage. In the stage which compares the digits in the highest digit place, which in the described embodiment is the stage A^9 , the comparison voltage has different values which indicate respectively whether one of the digits is greater than the other digit or whether the other digit is greater than or equal to the one digit. The conditioning voltage produced by each stage is applied to the following stage which compares digits in the next lower digit place so as to condition the following stage in a manner preventing the production of a comparison voltage by the following stage which indicates that one number is larger than the other number when in fact the preceding stage has determined that the other number is larger than the one number.

As an example, if the digits R^9 and D^9 , which in the instant embodiment are the digits in the highest digit places of the numbers R and D, are compared by the stages A^9 and it is found that the digit D^9 is greater than the digit R^9 , then obviously the number D is greater than the number R. When this occurs the conditioning voltage produced by the stage A^9 operates to prevent the following stages from producing a comparison voltage having a value indicating that the number R is larger than the number D even if one of the following stages is energized in accordance with a voltage representing a digit R which is greater than a digit D in the corresponding digit place.

In FIG. 2 there is illustrated a circuit diagram of one of the stages A^0 through A^9 . These stages are identical in construction and for this reason only one of the stages will be described in detail. For purposes of description details of the stage A^9 will be set forth.

The stage A^9 includes three input conductors 1, 2 and 3 which are to be energized respectively by voltages which represent the digits D^9 and R^9 and the conditioning volt-

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age produced by the preceding stage. However, inasmuch as the stage A⁹ is the first stage in the system there will be no conditioning voltage applied thereto. The voltages applied to the conductors 1 and 2 each have values which represent different values of the digit represented thereby. In the illustrated embodiment a voltage of zero volts represents a digit D⁹ of (0) and a voltage of minus twenty-four volts represents a digit D⁹ of (1). A voltage of zero volts represents a digit R⁹ of (1) and a voltage of minus twenty-four volts represents a digit R⁹ of (0).

A plurality of diodes are included in the circuit to control the flow of current therein. These diodes may be crystal diodes or dry rectifiers or any unidirectional asymmetric current carrying device which changes its impedance according to the relative magnitudes and/or polarities of voltages applied thereto.

A conductor 5 represents the B+ line and may have applied thereto a voltage of the order of plus two hundred volts. A conductor 6 is the B- line and may have a voltage applied thereto of approximately minus two hundred volts. A diode 11 is included in a conductor 12 which is connected to the conductor 1 and to a conductor 13 connected to the conductor 6 through a resistor 14. The conductor 13 includes a diode 15 and is connected to the control electrode 16 of an electroresponsive valve device 17 which is illustrated in the form of a conventional vacuum tube. The tube 17 includes a cathode 18 connected to ground as at 19 which may have a voltage of zero volts. The plate electrode 20 of the tube 17 is connected to the conductor 5 through a conductor 21 including a resistor 22. The electrode 16 is connected to ground through a diode 23. A conductor 24 including a resistor 25 is connected to the plate electrode 20. The conductor 24 constitutes the conditioning voltage output conductor to which is applied a conditioning voltage which in turn is applied to the stage A⁸.

The conductor 1 includes a diode 29 and is connected to a conductor 30 which in turn is connected to a conductor 31 connected to the conductor 5 through a resistor 32. The conductor 30 is connected to a control electrode 33 of a vacuum tube 34 having a cathode 35 which is connected to ground. The tube 34 also includes a plate electrode 36 which is connected to the conductor 5 through a conductor 37 which includes a resistor 38. A conductor 39 is connected to the plate 36 and includes a diode 40. The conductor 39 constitutes the comparison voltage output conductor to which is applied a voltage having values which indicate whether or not the digit R⁹ is greater than the digit D⁹. The electrode 33 is connected to ground through a diode 43.

The input conductor 2 is connected to ground through a diode 44 and is also connected to the grid electrode 45 of a vacuum tube 46 having a cathode 47 connected to the conductor 6 through a conductor 48 including a resistor 49. The plate electrode 50 of the tube 46 is connected through a conductor 51 to the conductor 5. A conductor 55 including a diode 56 is connected to the cathode 47 and to the conductor 30 and a conductor 57 including a diode 58 is connected to the conductor 55 and to a conductor 59. The conductor 59 includes a diode 62 and is connected to the electrode 16 of tube 17 and to a conductor 59' between a resistor 60 and a diode 61 included in the conductor 59'. The conductor 59' is connected to the conductors 5 and 31.

The input conductor 3 is connected to the conductor 6 through a conductor 63 which includes a resistor 64. The conductor 3 is also connected to ground through a diode 65 and leads to a grid electrode 66 of a vacuum tube 67 having a cathode 68 connected to ground. The plate electrode 69 of the tube 67 is connected to the conductor 5 through a conductor 70 including a resistor 71. A conductor 72 including resistors 73 and 74 is connected to the plate 69 and to the conductor 6. The conductor 31 includes a diode 76 and is connected to the conductor

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72 between the resistors 73 and 74. The conductor 13 is connected to a conductor 77 which includes a resistor 78 and a diode 79 and which is connected to conductors 5 and 31.

The diodes 29, 56 and 76 are poled in the same direction to permit current flow therethrough from the conductor 5. These diodes constitute part of an AND circuit which operates to establish a voltage which is applied to the grid 33 of the tube 34 to render the tube 34 conductive in response to the application of voltages to the diodes which effect blocking of all the diodes as will presently appear.

Diodes 58 and 61 are poled in the same direction to permit current flow therethrough from the conductor 5 and form part of an AND circuit which operates to establish a voltage at the upper terminal of the resistor 14 to render the tube 17 conductive in response to application of voltages to the diodes 58 and 61 effective to block both of the diodes. The diodes 11 and 79 are poled in the same direction so as to permit current flow therethrough from the conductor 5 and form part of an AND circuit which operates to establish a voltage at the upper terminal of the resistor 14 for rendering the tube 17 conductive in response to the application of voltages to the diodes 11 and 79 effective to block both of these diodes.

The diodes 15 and 62 are poled in the same direction to permit current flow therethrough from the conductor 5 to the resistor 14. The diodes 15 and 62 form part of an OR circuit which establishes a voltage at the upper terminal of resistor 14 which changes in a positive direction in response to operation of the AND circuits including diodes 11, 58, 61 and 79. The diode 40 also forms part of an OR circuit which operates in response to operation of the AND circuit including diodes 29, 56 and 76 as will presently appear.

As stated previously, the conductor 39 constitutes the comparison voltage output conductor for the stage A⁹ and in FIG. 1 such conductor is represented by the reference character L⁹. Each of the stages A⁰ through A⁸ includes a conductor corresponding to the conductor 39 and these conductors are represented respectively by the reference characters L⁰ through L⁸. In the illustrated embodiment the conductors L⁰ through L⁹ are connected to a conductor 80 which is connected through a resistor 80' to a conductor 81 which may have a voltage of the order of plus two hundred volts applied thereto. The conductor 80 is connected through resistors 82 and 83 to a conductor 84 which may have applied thereto a voltage of approximately minus two hundred volts. The grid electrode 85 of a vacuum tube 86 is connected to a point between the resistors 82 and 83 and is connected to ground through a diode 87. The tube 86 has a cathode 88 connected to ground and a plate 89 connected to a coil 90 which surrounds a magnetic core 91. The coil 90 and the core 91 control operation of a switch device 92 which in turn controls the operation of a translating device represented by the block 93, and which may assume various forms.

The arrangement is such that when current flows in any of the conductors L⁰ through L⁹ from the conductor 80 the tube 86 is rendered nonconductive which in turn results in deenergization of the coil 90 so that the movable contact 94 is urged to its illustrated position under the action of a spring 95 into engagement with a fixed contact 96 and out of engagement with a fixed contact 97. This operation results, as will presently appear, when the binary number R is greater than the binary number D. When the number D is greater than or equal to the number R the system of FIG. 1 operates such that no current flows in any of the conductors L⁰ through L⁹, whereby the tube 86 is in a conductive condition and the coil 90 is energized. When this occurs the contact 94 is moved from its illustrated position into engagement

with the fixed contact 97 to establish a second output condition. The device 93 may comprise any device which is to be controlled by means of the comparing system of the present invention.

The operation of the comparing system may now be described in detail. Let it be assumed initially that the digits R^9 and D^9 are equal and that each of these digits is a (0). It will be recalled that a (0) for the digit R is represented by a voltage of minus twenty-four volts and that a (0) for the digit D is represented by a voltage of zero volts. For these conditions then the tube 46 is nonconductive with the result that the voltage at the upper terminal of resistor 49 is substantially the same as the voltage of the conductor 2 so that the diodes 56 and 58 are unblocked to permit current flow therethrough in the forward direction. It is noted that a conditioning voltage is not applied to the conductor 3 of the stage A^9 inasmuch as this stage is responsive to digits of the binary numbers in the highest digit places. In the absence of a conditioning voltage the tube 67 is nonconductive so that current flowing through conductor 72 establishes a voltage at the upper terminal of the resistor 74 which is sufficiently positive to cause the diodes 61, 76 and 79 to be blocked. Also, the zero voltage which is applied to the conductor 1 results in blocking of the diodes 11 and 29.

From the foregoing it is seen that the diode 56 is unblocked and therefore the AND circuit which includes this diode does not operate so that the tube 34 is nonconductive. This results in the establishment of a voltage at the lower terminal of the resistor 38 which is approximately that of the conductor 5 and which blocks the diode 40 to prevent current flow from the conductor 80 through the conductor L^9 . The tube 86 is therefore conductive to provide the first output condition.

In addition, since the diodes 11 and 79 are blocked, the AND circuit including the diodes 11 and 79 operates with the result that the voltage at the upper terminal of the resistor 14 becomes sufficiently positive due to the current flow from the conductor 5 through the conductor 13, the diode 15 and the resistor 14 so that the tube 17 is conductive. This causes the lower end of the resistor 25 to assume a voltage which is of the order of minus twenty-four volts which constitutes a conditioning voltage C^9 applied to the stage A^8 for the next lower digit places. The effect of this conditioning voltage will be described hereinafter.

From the foregoing it has been demonstrated that current does not flow in the conductor L^9 when each of the digits R^9 and D^9 is a (0). The same result is realized when each of these digits is a (1). For this condition the voltage applied to the conductor 2 is approximately zero volts which is a more positive voltage than the minus twenty-four volts of the previous example. Also, a voltage of minus twenty-four volts is applied to the conductor 1 for a (1) of the digit D^9 which is a more negative voltage than the zero voltage of the previous example. For these conditions the tube 46 is conductive with the result that the diodes 56 and 58 are blocked. At the same time the voltage applied to the conductor 1 is effective to unblock the diodes 11 and 29. Since there is no conditioning voltage applied to the conductor 3 the tube 67 is nonconductive so that diodes 61, 76 and 79 are blocked. Since the diode 29 is unblocked the AND circuit including the diode 29 does not operate. In addition, the AND circuit including the now blocked diodes 58 and 61 operates and current flows from conductor 5 through conductor 59, diode 62 and resistor 14 to render the tube 17 conductive as before. The other stages A^8 through A^0 also operate to prevent current flow in the conductors L^8 through L^0 when voltages representing digits having equal values are applied to the conductors 1 and 2.

Let it now be assumed that the digit R^9 is greater than the digit D^9 , for which case the digit R^9 is a (1) and

the digit D^9 is a (0). With this condition the voltages applied to the conductors 1 and 2 are at their more positive values and effect blocking of the diodes 11, 29, 56 and 58. Since a conditioning voltage is not applied to the conductor 3 the diodes 61, 76 and 79 are also blocked. As a result, all three of the AND circuits operate and when the AND circuit including diodes 29, 56 and 76 operates, current flows from conductor 5 through conductor 30 and diode 43 to render tube 34 conductive which establishes a voltage at the lower terminal of resistor 38 having a value of approximately fifty volts. The diode 40 is therefore unblocked and current flows from conductor 80 through conductor L^9 to render tube 86 nonconductive for providing the second output condition.

Furthermore, when the AND circuits including diodes 11, 58, 61 and 79 operate, current flows from conductor 5 through diodes 15 and 62 which establishes a voltage at the upper terminal of resistor 14 effective to render tube 17 conductive which produces a conditioning voltage of the order of minus twenty-four volts. As will presently appear the conditioning voltage serves its conditioning function only when the digit D^9 is greater than the digit R^9 .

When the digit R^9 is greater than the digit D^9 , the number R is naturally greater than the number D and current flows in at least the conductor L^9 to give the second output condition. If any or all of the digits D^8 through D^0 is greater than the digits R^8 through R^0 then the corresponding conductors L^8 through L^0 have no current therein as will be explained presently, but this does not render the tube 86 conductive as long as current flows in at least one of the conductors L^0 through L^9 .

Let it be assumed now that the digit D^9 is greater than the digit R^9 , for which assumption the digit D^9 is a (1) and the digit R^9 is a (0). With this condition the voltages applied to conductors 1 and 2 are at their more negative values and cause the diodes 11, 29, 56 and 58 to be unblocked. In addition, the diodes 61, 76 and 79 are blocked due to the absence of a conditioning voltage on the conductor 3. Since the diode 29 is unblocked the AND circuit including this diode does not operate so that the tube 34 is nonconductive. This results in blocking of the diode 40 to prevent current flow in the conductor L^9 .

Furthermore, neither of the AND circuits including the diodes 11, 58, 61 and 79 operates because the diodes 11 and 58 are unblocked. The resulting current flow establishes a voltage at the upper terminal of resistor 14 which renders the tube 17 nonconductive so that a more positive voltage appears at the lower terminal of the resistor 25 than would occur if the tube 17 were conductive. This voltage is observed to be zero volts compared to the minus twenty-four volts resulting when the tube 17 is conductive. This conditioning voltage is applied to the stage A^8 .

It is apparent that when the digit D^9 is greater than the digit R^9 the number D is greater than the number R. In order to prevent the following stages A^8 through A^0 from producing current flow in the conductors L^8 through L^0 in the event that any or all of the digits R^8 through R^0 applied thereto is greater than the digits D^8 through D^0 , the conditioning voltage C^9 resulting from the stages A^9 is effective to unblock the diode 76 in the next following stage A^8 to prevent operation of the AND circuit including this diode. The voltage C^9 resulting when D^9 is greater than R^9 has a value of zero volts and when applied to the conductor 3 of stage A^8 , causes conduction of tube 67 whereby a voltage is established at the upper terminal of resistor 74 which has a value of minus twenty-four volts. This voltage causes unblocking of the diodes 61, 76 and 79 in stage A^8 .

Since diode 76 is unblocked, the tube 34 in stage A^8 is nonconductive which prevents current flow in conductor L^8 . Also, since diodes 61 and 79 are unblocked neither of the AND circuits including these diodes can operate with the result that tube 17 is nonconductive.

This establishes a conditioning voltage C^8 from stage A^8 which is also zero volts. When voltage C^8 is applied to the stage A^7 the same result occurs in that the voltage C^7 has a value of zero volts. The same is also true of the stages A^6 through A^0 and when one of the digits D^9 through D^0 is first observed to be greater than one of the digits R^9 through R^0 , the resulting conditioning voltage prevents current flow in conductors L^9 through L^0 even though a digit of the number R in a lower digit place is greater than a digit of the number D in such lower digit place.

FIG. 3 is a logic diagram of the circuit of FIG. 2 and the operation of the circuit of FIG. 2 may be best summarized by reference to FIG. 3. The comparator stage of FIG. 3 is shown as having a control terminal 100 to which the conductor 3 is connected, a digit input terminal 101 to which the digit R^9 is applied, a digit input terminal 102 to which the digit D^9 is applied. The digit D^9 is, in FIG. 3, assumed to have a high level for a (1) and a low level for (0), the same as the digit R^9 , and the terminal 102 is connected to the input of an inverter or complementor 105 for complementing the digit D^9 so that the output connection 106 from the complementor 105 is at a low level when the digit D^9 is at a low level and at a high level when the digit D^9 is (0). The output connection 106 of the inverter 105 corresponds to the conductor 1 in FIG. 2 and is connected to an AND gate 108 as one of the three inputs thereto. The AND gate 108 corresponds to the AND gate provided by the diodes 29, 56, 76 of FIG. 2 and has an output connection 109 corresponding to the conductor 30 of FIG. 2. The terminal 101 to which the digit R^9 is applied is connected to another input of the AND gate through a pulse amplifier 110 provided by the triode 46, the output of the pulse amplifier being connected to the AND gate 108 by a connection 111 corresponding to the connection 55 of FIG. 2. Similarly, the control terminal 100 is connected to one input of the AND gate 108 but the voltage level thereon is inverted or complemented by an inverter 112, corresponding to tube 67 of FIG. 2 and having its input, corresponding to conductor 3 of FIG. 2, connected to the terminal 100 and its output connected to the third input of the AND gate 108 by a connection 113. Normally a low level voltage is applied to the control terminal 100; this low level voltage is complemented by the inverter 112 so that a high level voltage is applied over connection 113 to the AND gate 108 to condition the gate to operate. The gate 108 will operate to provide a high level voltage at the output of the AND gate when the other input connections 111, 106 are also at a high level and this only occurs when the digit R^9 is (1) and the digit D^9 is (0). Consequently, the AND gate 108 will operate to produce a high level at its output connection 109 only when the digit R^9 is greater than the digit D^9 ; for all other conditions, the output of gate 108 is at a low level. It will be appreciated that, if a high level voltage is applied to the control terminal 100, the voltage level on connection 113 will be down and the output of gate 108 will remain at a low level regardless of the digits applied to the terminals 101, 102. A low level at the output of gate 109 signifies that the digit R is less than or equal to the digit D , or that terminal 100 is at a high level. Thus, it can be seen that the circuitry thus far described provides logic gating means for discriminating the condition that the R digit is greater than the D digit and terminal 100 is at a low level and that the output of the AND gate 108 will be at a high level for this condition and at a low level for all other conditions of the terminals 100, 101 and 102.

Second logic gating means is provided for indicating when the digit D is greater than the digit R . To this end, a two-input AND gate 115 (diodes 58 and 61 of FIG. 2) has one input 116 connected to the connection 111 to which the digit R is applied and an input 117 connected to the connection 113 to which the control signal is ap-

plied. Similarly, a two-input AND gate 118 (diodes 11, 79 of FIG. 2) is provided which has one input 119 connected to the connection 106 to which the complement of the digit D is applied, and a second input 120 which is connected to the connection 113. When the terminal 100 is at a low level, the connection 113 is at a high level and gates 115, 118 are conditioned to operate and the gate 115 will operate if the digit R is (1) and a high level voltage will appear on its output connection 122, and the gate 118 will operate if the digit D is (0) and a high level voltage will appear on its output connection 123. The outputs of the AND gates 115, 118 are connected to the input of an OR gate 124 (diodes 15, 62 of FIG. 2) having an output connection 125 connected to the input of an inverter or complementor 126 (tube 17 of FIG. 2), the output of which is connected to a terminal 127 (conductor 24 of FIG. 2). It can be seen that a high level output will appear on the connections 122, 123 for any condition where the R digit is (1) or where the D digit is (0) provided the connection 113 is at a high level; and, accordingly, for any such condition, the output of the OR gate 125 will be at a high level, the output of the inverter circuit 126 at a low level, and the voltage at terminal 127 will be at a low level. The only condition where neither the R digit is (1) nor the D digit (0) is when the D digit is (1) and R is (0). Under this condition, the AND gates 122, 123 will not be operated when connection 113 is at a high level and the voltage at terminal 127 will be at a high level.

It will also be appreciated that the voltage at terminal 127 will be at a high level even if the D digit is not greater than the digit R , if the voltage level at terminal 100 is at a high level to cause the connection 113 to be at a low voltage level to lower the voltage levels on connections 117, 120 to the AND gates 115, 118 so that these AND gates cannot operate.

The terminals 127 of the various stages correspond to the output conductor 24 of FIG. 2 and the terminals are connected to the input terminal 100 of the following stage so that, if one stage indicates that the digit D is greater than the digit R , the low level normally at terminal 127 of that stage will change to a high level to raise the terminal 100 of the next lesser significant stage to a high level to cause the output AND gate 108 of that stage to be at a low level and the output terminal 127 of that stage to be at a high level. This assures that all subsequent stages will have a low level output on the output connection from the AND gate 108.

The output connections 109 of the AND gates 108 of the various comparator stages are connected to the conductor 80 through an inverter or complementor 130 which corresponds to the triode 34 of FIG. 2. Each inverter 130 complements the output of the corresponding AND gate 108 so that the output from the inverter on an output connection 131 therefrom is at a low level for the high level output of AND gate 108 which occurs when the condition that R is greater than D is satisfied. The output connections 131 of all the stages are connected to an AND gate provided by the diodes 40 of FIG. 2 and having an output conductor 80 so that all of the output connections 131 must be raised from a low level to a high level before the AND gate 134 operates to provide a high level at its output conductor 80. Consequently, it can be seen that, if the digit R is greater than D in the most significant stage, the output connection 131 from that stage will be at a low level and the AND gate 134 will never operate to raise the output thereof to a high level. Consequently, the AND gate 134 indicates that R is greater than D when its output is at a low level. If the most significant digit of the R number is equal to the most significant digit of the D number, the output of the stage on its output connection 131 will be up, since the output of the AND gate 119 will be down conditioning the gate 134 to operate. Consequently, if all the other digits are equal and all the other connections 131 are at a high

level, the gate 134 will operate and, therefore, the output of AND gate 134 will be at a high level if all digits are equal.

If the D digit is larger in the most significant stage, stage A⁹, than the R digit, the output of the most significant comparator stage A⁹ on its output connection 131 will be at a high level, conditioning the gate 134 to operate and the voltage at the output terminal 127 of the most significant stage A⁹ will also be at a high level to cause the output AND gate of the next lesser significant stage A⁸ to be at a low level to cause the output connection 131 of the stage A⁸ to be at a high level and the output level of the terminal 127 to be at a high level. This causes terminal 100 of the stage A⁷ to be at a high level to cause the output connection 131 and the output terminal 127 of the stage A⁷ to be at their high levels which, in turn, causes the outputs of the other lesser significant stages to have high levels on their output connections 131 and terminals 127 to cause the operation of the AND gate 134 so that it will have a high level on its output connection when the D number is greater than the R number.

It will be understood that if the first several digits of the numbers being compared are equal, the output connections 131 of these stages will be at a high level to condition the AND gate 134 to operate, and the output terminals 127 of the stages will be at a low level to condition the following stages to compare digits. But at the first stage at which the D digit is greater than the R digit, the output level of the terminal 127 of that stage will be at a high level to cause the following stage and all the subsequent stages to assume a low level output at their AND gates 103 and a high level output at their output connections 131. From the foregoing, it can be seen that the output of AND gate 134 is at a high level when R is less than or equal to D, and at a low level when R is greater than D.

Although the invention has been described with reference to certain specific embodiments thereof, numerous modifications are possible and it is desired to cover all modifications falling within the spirit and scope of the appended claims.

Having described my invention, I claim:

1. A comparator for comparing two multidigit numbers having binary valued digits represented by bivalued electrical signals and comprising a comparator stage for each digit of the numbers with the stages being arranged in the order of significance of the digits; the stages intermediate the most significant stage and the least significant stage comprising first and second input terminals for the respective digits of the numbers to be compared and a control terminal, said control terminal being adapted to have a bivalued electrical signal applied thereto for control purposes, first AND gating means connected to said terminals for detecting the condition that the digit applied to the stage of one number is larger than the digit applied to the stage of the other number and that said control terminal is at a first level and having a first output for said condition and a second output for all other conditions of said terminals, second logic gating means connected to said terminals for detecting the condition that the applied digit of said one of said numbers is less than the applied digit of the other number and said control terminal is at said first level and having a first output for the defined condition and a second output for all other conditions of said terminals, the least significant stage of said compara-

tor comprising a control terminal and first and second digit input terminals and first AND gating means for discriminating the condition when the control terminal of the stage is at a first level and the digit applied thereto of said one number is larger than the applied digit of the other number and said most significant stage having digit input terminals and first AND gating means for discriminating the condition that the most significant digit of said one number is larger than the corresponding digit of said other number and having a first output for the defined condition and a second output for all other conditions and second logic gating means for discriminating the condition that the most significant digit of said one number is less than the corresponding digit and having a first output under the defined condition and a second output for all other conditions, and means for connecting the output of the second gating means of the more significant stages of the comparator to the control terminal of the next lesser significant stage, and logic means for discriminating between the condition when all of said first AND gating means have their said first output and the condition when less than all of said first AND gating means have their first output.

2. A comparator as defined in claim 1 wherein the second logic gating means of the stages of lesser significance than the said most significant stage each includes AND gate means having inputs connected to the said terminals of the stage and conditioned to operate when the control terminal of the stage is at its said first level to provide said first output when the digit of said other number is the larger of the applied digits and ineffective to operate to provide said first output when the control terminal is at its second level.

3. A comparator stage for comparing binary valued digits and for providing a first output indicating that one is larger than the other and a second output for other conditions, said stage comprising a control terminal and first and second digit input terminals, an output AND gate having first, second and third inputs, means connecting said first, second and control terminals respectively to said first, second and third inputs of said AND gate and including means for complementing the digit value applied to said second terminal, the voltage at said control terminal conditioning said AND gate to operate when at a predetermined level, an output OR gate, a first AND gate having one input connected to be controlled by the voltage level at said first input of said AND gate, a second AND gate having one input connected to be controlled by the voltage level at said second input of said output AND gate, and said first and second AND gates each having a second input connected to be controlled by the voltage level at said third input for said output AND gate, and means connecting the outputs of said first and second AND gates to respective inputs of said OR gate.

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