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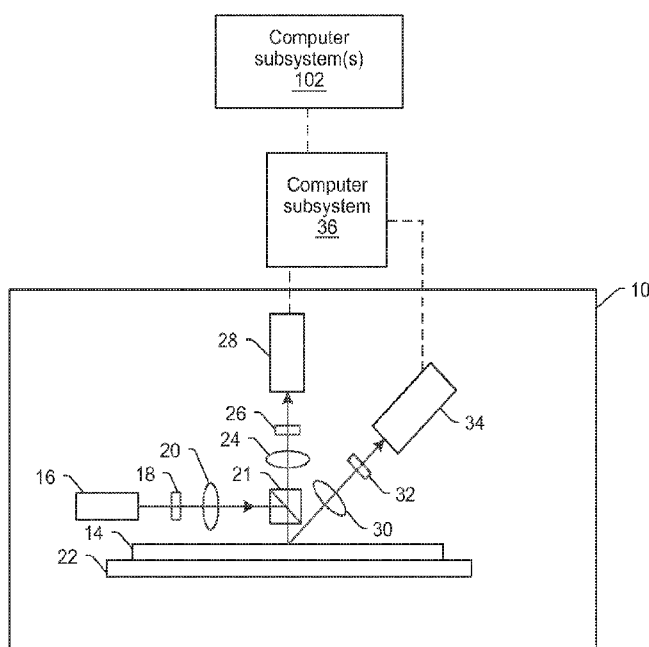


Fig. 1

(57) **Abstract:** Methods and systems for detecting defects on a wafer are provided. One system includes one or more computer subsystems configured for generating a rendered image based on information for a design printed on the wafer. The rendered image is a simulation of an image generated by the optical inspection subsystem for the design printed on the wafer. The computer subsystem(s) are also configured for comparing the rendered image to an optical image of the wafer generated by the optical inspection subsystem. The design is printed on the wafer using a reticle. In addition, the computer subsystem(s) are configured for detecting defects on the wafer based on results of the comparing.



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OPTICAL DIE TO DATABASE INSPECTION

BACKGROUND OF THE INVENTION

5 1. Field of the Invention

This invention generally relates to methods and systems for detecting defects on a wafer by optical die to database inspection.

10 2. Description of the Related Art

The following description and examples are not admitted to be prior art by virtue of their inclusion in this section.

15 Fabricating semiconductor devices such as logic and memory devices typically includes processing a substrate such as a semiconductor wafer using a large number of semiconductor fabrication processes to form various features and multiple levels of the semiconductor devices. For example, lithography is a semiconductor fabrication process that involves transferring a pattern from a reticle to a resist arranged on a semiconductor
20 wafer. Additional examples of semiconductor fabrication processes include, but are not limited to, chemical-mechanical polishing (CMP), etch, deposition, and ion implantation. Multiple semiconductor devices may be fabricated in an arrangement on a single semiconductor wafer and then separated into individual semiconductor devices.

25 Inspection processes are used at various steps during a semiconductor manufacturing process to detect defects on wafers to promote higher yield in the manufacturing process and thus higher profits. Inspection has always been an important part of fabricating semiconductor devices such as ICs. However, as the dimensions of

semiconductor devices decrease, inspection becomes even more important to the successful manufacture of semiconductor devices.

Many reticle inspection methods detect defects on reticles using die-to-database type comparisons. Such inspection typically involves acquiring a microscope image of a reticle. From a database that describes the intended pattern on the reticle, an image that the inspection microscope is expected to observe of that reticle may be calculated or simulated. The acquired optical image may then be compared to the calculated or simulated image to detect defects on the reticle. Such reticle inspection methods have proven useful for a number of uses. However, such reticle inspection methods are not capable of finding process-induced defects (i.e., defects that would be printed on a wafer due to the interaction between the reticle and the process of printing the reticle on the wafer).

Some reticle inspections are performed using wafers that have been printed with the reticles. In this manner, defects that are detected on the wafer can be used to determine if there are defects on the reticle that was used to print the wafer. Some such inspections are performed on optical platforms by comparing an inspected image frame to a reference frame, where the reference frame is a sample of the image generated from the wafer. Examples for reference image frames are: images from adjacent dies, images from a standard reference die on the same wafer or a different wafer, and images from the adjacent cells (in an array structure).

Currently, die to database inspection performed for wafers exists only on a scanning electron microscope (SEM) inspection platform. However, due to the throughput constraints (e.g., due to the physics of electron beam tools), only a substantially small number of locations (i.e., not the entire wafer and not entire dies on the wafer) can be checked. In addition, inspection performed by electron beam inspection of wafers is too slow to qualify every reticle for which qualification is needed.

Furthermore, with the advent of multiple patterning step lithography process, and as a result needing multiple reticle qualifications for a single lithography process, the number of reticles for which qualification must be performed should grow substantially.

5 The currently available optical inspection methodologies that involve comparing wafer images to a reference wafer image to detect defects on a wafer cannot serve some of the use cases for which such inspection is performed. For example, such currently used optical inspections cannot detect repeater defects within dies printed with a single die reticle. One example of such a use case is for extreme ultraviolet (EUV) mask
10 qualification. In particular, due to the lack of a pellicle, particles on the mask when printed on the wafer become repeater defects on the wafer. Therefore, such defects will cancel each other out in die-to-die comparisons and not be detected. In addition, such currently used optical inspections cannot be used for design intent checks. For example, a reference image generated from part of a wafer contains the process variation.
15 Therefore, comparison of such a reference image with a different wafer image will cancel out the process variation in both images rendering the process variation undetectable. Furthermore, before the process becomes mature, it is difficult to find a “golden” reference die. For example, a user may have no idea which die or dies can be used as a “golden” reference die for comparison with other dies on a wafer.

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 Accordingly, it would be advantageous to develop systems and/or methods for detecting defects on a wafer that do not have one or more of the disadvantages described above.

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SUMMARY OF THE INVENTION

 The following description of various embodiments is not to be construed in any way as limiting the subject matter of the appended claims.

One embodiment relates to a system configured to detect defects on a wafer. The system includes an optical inspection subsystem that includes at least a light source and a detector. The light source is configured to generate light that is directed to a wafer. The detector is configured to detect light from the wafer and to generate output responsive to the detected light. The system also includes one or more computer subsystems configured for generating a rendered image based on information for a design printed on the wafer. The rendered image is a simulation of an image generated by the optical inspection subsystem for the design printed on the wafer. The computer subsystem(s) are also configured for comparing the rendered image to an optical image of the wafer generated by the optical inspection subsystem. The design is printed on the wafer using a reticle. The computer subsystem(s) are further configured for detecting defects on the wafer based on results of the comparing. The system may be further configured as described herein.

Another embodiment relates to a computer-implemented method for detecting defects on a wafer. The method includes steps for each of the functions of the one or more computer subsystems described above. The steps of the method are performed by one or more computer systems. The method may be performed as described further herein. In addition, the method may include any other step(s) of any other method(s) described herein. Furthermore, the method may be performed by any of the systems described herein.

An additional embodiment relates to a non-transitory computer-readable medium storing program instructions executable on a computer system for performing a computer-implemented method for detecting defects on a wafer. The computer-implemented method includes the steps of the method described above. The computer-readable medium may be further configured as described herein. The steps of the computer-implemented method may be performed as described further herein. In

addition, the computer-implemented method for which the program instructions are executable may include any other step(s) of any other method(s) described herein.

BRIEF DESCRIPTION OF THE DRAWINGS

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Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

10 Fig. 1 is a schematic diagram illustrating a side view of an embodiment of a system configured as described herein;

Figs. 2-6 are flow charts illustrating various embodiments of steps that may be performed by one or more computer subsystems described herein; and

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Fig. 7 is a block diagram illustrating one embodiment of a non-transitory computer-readable medium storing program instructions executable on a computer system for performing one or more of the computer-implemented methods described herein.

20

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and
25 alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The terms “design” and “design data” as used herein generally refer to the physical design (layout) of an IC and data derived from the physical design through
5 complex simulation or simple geometric and Boolean operations. The design may include any other design data or design data proxies described in commonly owned U.S. Patent Nos. 7,570,796 issued on August 4, 2009 to Zafar et al. and 7,676,077 issued on March 9, 2010 to Kulkarni et al., both of which are incorporated by reference as if fully set forth herein. In addition, the design data can be standard cell library data, integrated
10 layout data, design data for one or more layers, derivatives of the design data, and full or partial chip design data.

In general, however, the design information or data cannot be generated by imaging a wafer with a wafer inspection system. For example, the design patterns
15 formed on the wafer may not accurately represent the design for the wafer and the wafer inspection system may not be capable of generating images of the design patterns formed on the wafer with sufficient resolution such that the images could be used to determine information about the design for the wafer. Therefore, in general, the design information or design data cannot be generated using a physical wafer. In addition, the “design” and
20 “design data” described herein refers to information and data that is generated by a semiconductor device designer in a design process and is therefore available for use in the embodiments described herein well in advance of printing of the design on any physical wafers.

25 Turning now to the drawings, it is noted that the figures are not drawn to scale. In particular, the scale of some of the elements of the figures is greatly exaggerated to emphasize characteristics of the elements. It is also noted that the figures are not drawn to the same scale. Elements shown in more than one figure that may be similarly configured have been indicated using the same reference numerals. Unless otherwise

noted herein, any of the elements described and shown may include any suitable commercially available elements.

One embodiment relates to a system configured to detect defects on a wafer. In
5 general, the embodiments described herein are configured for optical die-to-database
(DB) inspection of wafers. In other words, the embodiments described herein are
generally configured for comparing an optical image of a wafer printed with a reticle to a
rendered image generated from a DB to detect defects on the wafer.

10 The wafer may include any wafer known in the art. The design is printed on the
wafer using a reticle. The design may be printed on the wafer using the reticle in any
suitable manner known in the art (e.g., by depositing one or more materials on a wafer
and performing a lithography process on the wafer to transfer the design from the reticle
to the wafer). The wafer may also be a short loop wafer, meaning a wafer on which not
15 all process steps required to ultimately form a functioning device have been performed.
In other words, the wafer may or may not be a full loop wafer. For example, the wafer
may be a wafer on which only the process steps described above (e.g., deposition,
lithography, and possibly etch) have been performed. As such, the wafer may not include
one or more layers (patterned and/or unpatterned) formed under the layer of the wafer
20 being inspected. In this manner, the process steps that are performed on the wafer prior
to the inspection described herein may include only those required to transfer a design for
the wafer from a reticle to the wafer. The reticle may include any reticle known in the art
such as reticles configured for use with extreme ultraviolet (EUV) light or another
suitable type of light.

25

One embodiment of such a system is shown in Fig. 1. The system includes an
optical inspection subsystem that includes at least a light source and a detector. The light
source is configured to generate light that is directed to a wafer. The detector is

configured to detect light from the wafer and to generate output responsive to the detected light.

In the embodiment of the system shown in Fig. 1, optical inspection subsystem 10 includes an illumination subsystem configured to direct light to wafer 14. The illumination subsystem includes at least one light source. For example, as shown in Fig. 1, the illumination subsystem includes light source 16. In one embodiment, the illumination subsystem is configured to direct the light to the wafer at one or more angles of incidence, which may include one or more oblique angles and/or one or more normal angles. For example, as shown in Fig. 1, light from light source 16 is directed through optical element 18 and then lens 20 to beam splitter 21, which directs the light to wafer 14 at a normal angle of incidence. The angle of incidence may include any suitable angle of incidence, which may vary depending on, for instance, characteristics of the wafer and the defects to be detected on the wafer.

15

The illumination subsystem may be configured to direct the light to the wafer at different angles of incidence at different times. For example, the inspection subsystem may be configured to alter one or more characteristics of one or more elements of the illumination subsystem such that the light can be directed to the wafer at an angle of incidence that is different than that shown in Fig. 1. In one such example, the inspection subsystem may be configured to move light source 16, optical element 18, and lens 20 such that the light is directed to the wafer at a different angle of incidence.

In some instances, the inspection subsystem may be configured to direct light to the wafer at more than one angle of incidence at the same time. For example, the illumination subsystem may include more than one illumination channel, one of the illumination channels may include light source 16, optical element 18, and lens 20 as shown in Fig. 1 and another of the illumination channels (not shown) may include similar elements, which may be configured differently or the same, or may include at least a light

source and possibly one or more other components such as those described further herein. If such light is directed to the wafer at the same time as the other light, one or more characteristics (e.g., wavelength, polarization, etc.) of the light directed to the wafer at different angles of incidence may be different such that light resulting from illumination of the wafer at the different angles of incidence can be discriminated from each other at the detector(s).

In another instance, the illumination subsystem may include only one light source (e.g., source 16 shown in Fig. 1) and light from the light source may be separated into different optical paths (e.g., based on wavelength, polarization, etc.) by one or more optical elements (not shown) of the illumination subsystem. Light in each of the different optical paths may then be directed to the wafer. Multiple illumination channels may be configured to direct light to the wafer at the same time or at different times (e.g., when different illumination channels are used to sequentially illuminate the wafer). In another instance, the same illumination channel may be configured to direct light to the wafer with different characteristics at different times. For example, in some instances, optical element 18 may be configured as a spectral filter and the properties of the spectral filter can be changed in a variety of different ways (e.g., by swapping out the spectral filter) such that different wavelengths of light can be directed to the wafer at different times. The illumination subsystem may have any other suitable configuration known in the art for directing light having different or the same characteristics to the wafer at different or the same angles of incidence sequentially or simultaneously.

In one embodiment, light source 16 may include a broadband plasma (BBP) light source. In this manner, the light generated by the light source and directed to the wafer may include broadband light. However, the light source may include any other suitable light source such as a laser. The laser may include any suitable laser known in the art and may be configured to generate light at any suitable wavelength or wavelengths known in the art. In addition, the laser may be configured to generate light that is monochromatic

or nearly-monochromatic. In this manner, the laser may be a narrowband laser. The light source may also include a polychromatic light source that generates light at multiple discrete wavelengths or wavebands.

5 Light from optical element 18 may be focused to beam splitter 21 by lens 20. Although lens 20 is shown in Fig. 1 as a single refractive optical element, it is to be understood that, in practice, lens 20 may include a number of refractive and/or reflective optical elements that in combination focus the light from the optical element to the wafer. The illumination subsystem shown in Fig. 1 and described herein may include any other
10 suitable optical elements (not shown). Examples of such optical elements include, but are not limited to, polarizing component(s), spectral filter(s), spatial filter(s), reflective optical element(s), apodizer(s), beam splitter(s), aperture(s), and the like, which may include any such suitable optical elements known in the art. In addition, the system may be configured to alter one or more of the elements of the illumination subsystem based on
15 the type of illumination to be used for inspection.

 The inspection subsystem may also include a scanning subsystem configured to cause the light to be scanned over the wafer. For example, the inspection subsystem may include stage 22 on which wafer 14 is disposed during inspection. The scanning
20 subsystem may include any suitable mechanical and/or robotic assembly (that includes stage 22) that can be configured to move the wafer such that the light can be scanned over the wafer. In addition, or alternatively, the inspection subsystem may be configured such that one or more optical elements of the inspection subsystem perform some scanning of the light over the wafer. The light may be scanned over the wafer in any
25 suitable fashion.

 The inspection subsystem further includes one or more detection channels. At least one of the one or more detection channels includes a detector configured to detect light from the wafer due to illumination of the wafer by the inspection subsystem and to

generate output responsive to the detected light. For example, the inspection subsystem shown in Fig. 1 includes two detection channels, one formed by collector 24, element 26, and detector 28 and another formed by collector 30, element 32, and detector 34. As shown in Fig. 1, the two detection channels are configured to collect and detect light at different angles of collection. In some instances, one detection channel is configured to detect specularly reflected light, and the other detection channel is configured to detect light that is not specularly reflected (e.g., scattered, diffracted, etc.) from the wafer. However, two or more of the detection channels may be configured to detect the same type of light from the wafer (e.g., specularly reflected light). Although Fig. 1 shows an embodiment of the inspection subsystem that includes two detection channels, the inspection subsystem may include a different number of detection channels (e.g., only one detection channel or two or more detection channels). Although each of the collectors are shown in Fig. 1 as single refractive optical elements, it is to be understood that each of the collectors may include one or more refractive optical element(s) and/or one or more reflective optical element(s).

The one or more detection channels may include any suitable detectors known in the art. For example, the detectors may include photo-multiplier tubes (PMTs), charge coupled devices (CCDs), and time delay integration (TDI) cameras. The detectors may also include any other suitable detectors known in the art. The detectors may also include non-imaging detectors or imaging detectors. In this manner, if the detectors are non-imaging detectors, each of the detectors may be configured to detect certain characteristics of the scattered light such as intensity but may not be configured to detect such characteristics as a function of position within the imaging plane. As such, the output that is generated by each of the detectors included in each of the detection channels of the inspection subsystem may be signals or data, but not image signals or image data. In such instances, a computer subsystem such as computer subsystem 36 of the system may be configured to generate images of the wafer from the non-imaging output of the detectors. However, in other instances, the detectors may be configured as

imaging detectors that are configured to generate imaging signals or image data. Therefore, the system may be configured to generate the output described herein in a number of ways.

5 It is noted that Fig. 1 is provided herein to generally illustrate a configuration of an inspection subsystem that may be included in the system embodiments described herein. Obviously, the inspection subsystem configuration described herein may be altered to optimize the performance of the system as is normally performed when designing a commercial inspection system. In addition, the systems described herein may
10 be implemented using an existing inspection system (e.g., by adding functionality described herein to an existing inspection system) such as the 28xx and 29xx series of tools that are commercially available from KLA-Tencor. For some such systems, the methods described herein may be provided as optional functionality of the system (e.g., in addition to other functionality of the system). Alternatively, the system described
15 herein may be designed “from scratch” to provide a completely new system.

Computer subsystem 36 of the system may be coupled to the detectors of the inspection subsystem in any suitable manner (e.g., via one or more transmission media, which may include “wired” and/or “wireless” transmission media) such that the computer
20 subsystem can receive the output generated by the detectors during scanning of the wafer. Computer subsystem 36 may be configured to perform a number of functions using the output of the detectors as described herein and any other functions described further herein. This computer subsystem may be further configured as described herein.

25 This computer subsystem (as well as other computer subsystems described herein) may also be referred to herein as computer system(s). Each of the computer subsystem(s) or system(s) described herein may take various forms, including a personal computer system, image computer, mainframe computer system, workstation, network appliance, Internet appliance, or other device. In general, the term “computer system” may be

broadly defined to encompass any device having one or more processors, which executes instructions from a memory medium. The computer subsystem(s) or system(s) may also include any suitable processor known in the art such as a parallel processor. In addition, the computer subsystem(s) or system(s) may include a computer platform with high
5 speed processing and software, either as a standalone or a networked tool.

If the system includes more than one computer subsystem, then the different computer subsystems may be coupled to each other such that images, data, information, instructions, etc. can be sent between the computer subsystems as described further
10 herein. For example, computer subsystem 36 may be coupled to computer subsystem(s) 102 (as shown by the dashed line in Fig. 1) by any suitable transmission media, which may include any suitable wired and/or wireless transmission media known in the art. Two or more of such computer subsystems may also be effectively coupled by a shared computer-readable storage medium (not shown).

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The one or more computer subsystems described above are configured for generating a rendered image based on information for a design printed on the wafer. The rendered image is a simulation of an image generated by the optical inspection subsystem for the design printed on the wafer. For example, as shown in Fig. 2, the computer
20 subsystem(s) may be configured to acquire design database 200, which may include design polygons 202 or other design information described herein. The computer subsystem(s) may use simulation software 204 to generate rendered image 206 from design database 200. Therefore, the computer subsystem(s) may use design polygons 202 as input to a simulation that outputs rendered image 206, one of example of which is
25 shown in Fig. 2 as rendered image 208.

In this manner, the computer subsystem(s) are configured for modeling an optical inspection image from design. In other words, the computer subsystem(s) are configured for generating a simulated optical image from design. The modeling can be performed in

a number of different manners described further herein. For example, the computer subsystem(s) may model from design (polygons) with estimated near field and an accurate or approximate optical system model. In another example, the computer subsystem(s) may model from a stack of geometry and material information to calculate
5 the near field and an accurate or approximate optical system model.

The computer subsystem(s) are also configured for comparing the rendered image to an optical image of the wafer generated by the optical inspection subsystem and detecting defects on the wafer based on results of the comparing. The design is printed
10 on the wafer using a reticle. For example, as shown in Fig. 2, physical wafer 210 may be printed with the design for the wafer using the reticle. In one such example, design 212 may be printed on wafer 210. Imaging hardware 214 (i.e., an optical inspection subsystem as described herein) may then generate optical image 216 of the physical wafer. One example of such an optical image is shown in Fig. 2 as optical image 218.
15 The computer subsystem(s) may then perform compare and detect, as shown in step 220, by comparing rendered image 206 and optical image 216 and detecting defects based on the comparison results. For example, the computer subsystem(s) may subtract rendered image 208 from optical image 218 thereby generating difference image 222. In this manner, the computer subsystem(s) may be configured for comparing the optical wafer
20 image to a rendered image from design.

The computer subsystem(s) may then detect defects on the wafer in any suitable manner using the difference image. For example, the computer subsystem(s) may apply one or more defect detection algorithms and/or methods to the difference image. In one
25 such example, the computer subsystem(s) may compare signals or data in difference image 222 to a threshold. Any of the signals or data that are above the threshold may be identified as defects or potential defects, while any of the signals or data that are below the threshold may not be identified as defects or potential defects. Of course, many other defect detection algorithms and methods are known in the art, and the embodiments

described herein are not limited to any one defect detection algorithm or method. In other words, the results of the comparison described herein may be input to any suitable defect detection algorithm and/or method known in the art.

5 In some embodiments, the one or more computer subsystems are further configured for determining if the reticle passes qualification based on the detected defects. Determining if the reticle passes qualification based on the defects detected on the wafer may be performed in any suitable manner known in the art. One advantage of the embodiments described herein is that they can perform die-to-DB inspection for EUV
10 mask qualification. Different from normal optical masks, an EUV mask qualification system is not currently available because of the lack of actinic EUV mask inspection systems. However, the embodiments described herein may be used for reticle qualification of any type of reticle known in the art. In this manner, the printability of the reticle on wafer may be validated through the die-to-DB optical wafer inspection
15 described herein as part of reticle qualification.

 The embodiments described herein may also be configured for performing process window qualification (PWQ) such as that described in U.S. Patent Nos. 6,902,855 to Peterson et al. issued on June 7, 2005, 7,418,124 to Peterson et al. issued on August 26,
20 2008, 7,769,225 to Kekare et al. issued on August 3, 2010, 8,041,106 to Pak et al. issued on October 18, 2011, and 8,213,704 to Peterson et al. issued on July 3, 2012, which are incorporated by reference as if fully set forth herein. The embodiments described herein may include any step(s) of any method(s) described in these patents and may be further configured as described in these patents. A PWQ wafer may be printed as described in
25 these patents.

 In another embodiment, the one or more computer subsystems are configured for determining a performance of one or more process steps performed on the wafer based on the detected defects. In one such embodiment, the wafer is a short loop wafer. For

example, a short loop wafer may be manufactured with only a subset of all of the layers that would be formed on the wafer to fabricate a fully functioning device. Such wafers may be used to check only specific process steps such as a lithography step and/or an etch step. The performance of the one or more process steps performed on the wafer based on
5 the detected defects may be determined in any suitable manner.

The die-to-DB for optical wafer inspection described herein is new technology. In particular, currently, there is no optical die-to-DB methodology available for wafer inspection. In addition, the die-to-DB for optical wafer inspection has a number of
10 important advantages over other currently available methods for detecting defects on wafers. For example, the embodiments described herein can detect die-to-die repeater defects and variations from design. In addition, the embodiments described herein do not rely on using a standard reference die generated from a physical wafer for use as the DB to which wafer die images are compared. For example, standard reference dies can be
15 used as proxies for detecting die-to-die repeater defects. However, oftentimes, it is not known which die is suitable for use as a standard reference die. Furthermore, there is no inspection technology available today to check the design intent.

Scanning electron microscope (SEM) die-to-DB inspection for wafers is currently
20 available. SEM die-to-DB is commonly used today for several use cases such as for detection of critical dimension (CD) variation, where the sensitivity requirement can be as small as 2 nm. However, SEM die-to-DB is not fast enough to serve the needs of wafer inspection. For example, currently, due to throughput constraints (due to the physics of the SEM imaging process), only a substantially small number of locations can
25 be checked. In contrast, the optical die-to-DB inspection described herein can inspect an entire wafer within an acceptable time period. In this manner, the optical die-to-DB inspection described herein can be performed much faster than SEM die-to-DB. In addition, the die-to-DB inspection described herein can be performed for any wafer known in the art and for qualifying any reticle known in the art. Therefore, the

embodiments described herein enable users to do integration debugging of any new reticle that they may not have time to do with the current electron beam solutions. In addition, since SEM has substantially higher resolution than optical inspection tools and only images the top layer of a wafer, rendering a SEM image from design is relatively
5 easy. For example, SEM images can look substantially similar to design except that the corners may be rounded. In addition, SEM die-to-DB inspection can have challenges in detection for nuisance issues.

In comparison, optical die-to-DB is a much more difficult problem than SEM die-
10 to-DB due to optical limitations in resolution and required accuracy and throughput in simulation to create a practical product. Due to its technical difficulty, optical die-to-DB for wafer inspection is not currently available in the industry.

Some reticle inspection methods use a near field approximation for detecting
15 defects on reticles. For example, the near field at the reticle plane may be approximated based on a thin film assumption and information about the optical path of the reticle inspection subsystem. This thin film assumption assumes the near field at the reticle plane is close to design (for lithography only one layer), which holds when wavelength and feature size are approximately the same. With today's design rule, the feature size is
20 much smaller than wavelength even for reticles, where the feature size is 4x the feature size on wafers. Therefore, reticle plane near field approximations are becoming more and more challenging in reticle inspection. On wafers, it is even more challenging due to the 4x shrink of feature size.

25 In one embodiment, generating the rendered image includes converting polygons in the information for the design to a gray scale image. For example, as shown in Fig. 3, design polygons 300 such as design polygons 302 may be converted to gray scale image 306 by DB Raster 304. In particular, the DB Raster may convert polygons 300 to a gray scale image. DB Raster may be performed in any suitable manner. For example, the

design polygons may be used to generate an intermediate binary image. Downsampling and anti-aliasing may then be performed on the intermediate binary image to generate the gray scale image. In this manner, gray scale image 306 may be a raw gray scale image. Features in the raw gray scale image may have dimensions (e.g., CD) that are equal to the original design dimensions.

In one such embodiment, converting the polygons is performed with sub-pixel accuracy. In other words, the computer subsystem(s) may convert polygons in the design to a gray scale image with sub-pixel accuracy. Sub-pixel accuracy means that the gray scale image should be able to represent polygons with dimensions (e.g., width or height) smaller than one pixel. For example, if there is a polygon with a height of 0.31 pixels, that height should be reflected in the gray scale image properly (as 0.31 pixels). In addition, the gray scale image should reflect the polygon position with sub-pixel accuracy. For example, if a first polygon is centered at 31.3 pixels and a second polygon is centered at 42.7 pixels, the gray scale image should be able to represent the non-integer distance between the polygons, which is 11.4 pixels (42.7 pixels - 31.3 pixels). In contrast, many DB raster methods in use today can only handle polygons with sizes that are an integer of pixel number.

In another such embodiment, generating the rendered image includes generating a modified gray scale image by applying bias correction and corner rounding to the gray scale image. For example, as shown in Fig. 3, DB model 308 may use gray scale image 306 as input to produce modified gray scale image 310. By applying the bias correction and corner rounding to the gray scale image, the features shown in the modified gray scale image may have different dimensions and different corner rounding than the features shown in the gray scale image. For example, very often, real pattern sizes on wafers are different from the as-designed CDs due to lithography process error. Such differences are generally referred to in the art as "bias." Therefore, by modifying the gray scale image to account for such bias, the rendered images generated as described

herein will simulate the optical images that would be produced by the inspection subsystem much more accurately. Appropriate bias corrections and corner rounding may be acquired from any suitable source in any suitable manner (e.g., experimentally or empirically). The bias may also be expressed in any suitable manner (e.g., as a constant
5 for a constant bias or as a function for a nonlinear bias).

In some such embodiments, generating the rendered image also includes estimating a near field of the wafer based on the modified gray scale image and the information for the design printed on the wafer. For example, as shown in Fig. 3, near
10 field estimation 312 may use modified gray scale image 310 as input to produce estimated near field 314. The information for the design used for the near field estimation may include material parameters, three dimensional (3D) effects, wavelength and angle dependency, etc. The estimated near field of the wafer is a simulation of an electromagnetic (EM) field that would be generated at or near the top surface of the wafer
15 (i.e., at the wafer plane) by the interaction of the materials and their geometry of the wafer and the light directed to the wafer by the optical inspection subsystem. The estimated near field may include amplitude as shown in left side of estimated near field 314 and phase as shown in right side of estimated near field 314. The estimated near field may also be or include complex numbers. The estimated near field may be
20 estimated in a number of different manners. For example, the near field may be estimated by Kirchhoff/thin mask approximation, thick mask approximation, rigorous EM simulation (e.g., finite-difference time-domain (FDTD)), rigorous EM simulation added to thin mask approximation, and any other suitable approximation, function, or model known in the art.

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In one such embodiment, generating the rendered image includes generating an initial rendered image that is another simulation of the image generated by the optical inspection subsystem for the design printed on the wafer based on the near field and an optical model of the optical inspection subsystem. Therefore, in the embodiments

described herein, the input to optical modeling is the near field estimation and not the design database. For example, as shown in Fig. 3, optical model 316 may use estimated near field 314 as input to generate initial rendered image 318. The optical model may model with and without aberrations of the optical inspection subsystem. Generating the
5 initial rendered image may be performed using an incoherent model, a Partial Coherence Model, the Partial Coherence - Hopkins Formulation, a linear convolution model, a linear convolution model with Hermitian quadratic form, Robust Principal Component Analysis (Robust PCA), an Abbe imaging method, a rigorous EM model, and any other suitable approximation, function, or model known in the art.

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In a further embodiment, generating the rendered image also includes generating the rendered image from the initial rendered image by modifying the initial rendered image to minimize differences between the initial rendered image and the optical image generated by the optical inspection subsystem. For example, as shown in Fig. 3, dynamic
15 compensation 320 performed by the computer subsystem(s) may modify initial rendered image 318 to generate rendered image 322, one example of which is shown in Fig. 3 as rendered image 324. The dynamic compensation may be performed to compensate for differences between the rendered image and an optical image such as gain and offset of the images (e.g., for tone mismatches and relatively small misalignment between the
20 images) and differences in the images due to aberrations of the optical inspection subsystem. In addition, since the simulations described herein may intentionally be not completely rigorous, and since the materials/dimensions of features printed on the wafer may vary from design in unpredictable ways, run time compensation may be performed to reduce differences between the rendered image and the optical image. Smaller
25 differences between the rendered image and the optical image mean that the rendered image is more similar to the optical image. In this manner, there will be significantly fewer nuisances and false defects detected by performing the dynamic compensation described herein.

In one such example, the gray scale of a rendered image may be slightly smaller than the gray scale of an optical image, and/or the rendered image may not be aligned with the optical image very well. So, simply comparing the rendered image with the optical image and detecting defects based on the comparison results may produce a significant number of nuisance defects. Therefore, the dynamic compensation described herein can be designed to reduce such systematic differences between the rendered image and the optical image. Such differences in gray scale and/or alignment can be dynamically compensated for using any suitable model, algorithm, or function known in the art. In another such example, tool aberration in the optical imaging can cause the real optical image to be different from the expected optical image. Examples of such tool aberrations include, but are not limited to, lens decentering and wafer defocus. All aberrations can cause phase errors across the exit pupil of the imaging lens (compared with the expected ideal phase distribution). By far, the most common way to describe aberrations in optical imaging systems is using Zernike polynomials. Therefore, the dynamic compensation described herein may use a description of the aberrations such as Zernike polynomials or any other suitable description of optical imaging system aberrations known in the art to modify the rendered image to thereby minimize differences between the rendered image and the optical image. Such modification may be performed using any suitable model, algorithm, or function known in the art.

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As further shown in Fig. 3, optical image 326, one example of which is shown in Fig. 3 as optical image 328, may be acquired by the computer subsystem(s) from the inspection subsystem (or a computer readable storage medium in which the image was stored) and compared to rendered image 322. Such comparisons may generate difference image 330. The comparisons between the rendered image and the optical image may be performed for defect detection, which may be performed as described further herein. The comparisons between the rendered image and the optical image may also or alternatively be performed for one or more other purposes. For example, in some instances, rendered and optical images corresponding to the same (or substantially the same) portions of the

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design may be compared for alignment of the rendered image (and therefore the design) to the optical images. Such alignment may be performed for a number of reasons including setting up optical die-to-DB inspection as well as other reasons such as setting up or modifying one or more parameters used for dynamic compensation 320.

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The computer subsystem(s) may perform general wafer inspection in three phases. For example, the computer subsystem(s) may estimate modeling parameters from selected sites. In one such example, the computer subsystem(s) may perform offline training (for selected sites) 400 as shown in Fig. 4. The computer subsystem(s) may then
10 render images for an entire die. For example, the computer subsystem(s) may perform offline rendering (for a whole die on the wafer) 418 as shown in Fig. 4. In addition, the computer subsystem(s) may apply dynamic compensation (e.g., for gain/offset and aberration) in real time inspection for the whole wafer (or sampled dies). For example, as shown in Fig. 4, the computer subsystem(s) may perform online inspection (for a whole
15 wafer) 432.

“Offline” as that term is used herein is meant to indicate that the step(s), process(es), flow(s), etc. that are performed offline are not performed during an inspection of a wafer (e.g., not performed while the wafer is being scanned by an
20 inspection subsystem). In contrast, “online” as that term is used herein is meant to indicate that the step(s), process(es), flow(s), etc. that are performed online are performed during an inspection of a wafer (e.g., performed while the wafer is being scanned by an inspection subsystem).

25 In one such example, in some embodiments, the one or more computer subsystems are configured for training one or more models used for generating the rendered image based on: one or more additional rendered images for one or more selected sites on one or more other wafers generated by performing generating the rendered image for the one or more selected sites; and one or more optical images

generated by the optical inspection subsystem for the one or more selected sites on the one or more other wafers. For example, as shown in Fig. 4, offline training (for selected sites) 400 may use design polygons 402 as input to DB raster 404, which may be performed as described above. A gray scale image produced by DB raster 404 may be input to DB model 406, which may output a modified gray scale image as described further herein. The modified gray scale image produced by DB model 406 may be input to near field estimation 408, which may produce an estimated near field for the wafer as described further herein. The estimated near field may be input to optical model 410, which may output an initial rendered image as described further herein. The initial rendered image may be input to dynamic compensation 412, which may output rendered image 414. The computer subsystem(s) may then perform a comparison between the rendered image and an optical image, as shown in step 416.

The results of the comparison of the rendered image and the optical image may be used to determine errors (e.g., a sum of squared errors (SSE)) in the rendered image compared to the optical image. Those errors can be used to train one or more parameters of one or more of the step(s) performed by the computer subsystem(s). For example, the errors can be used to train one or more parameters of DB model 406 such as the parameters used for bias correction and/or corner rounding. In addition, the errors may be used to train one or more parameters of optical model 410. Furthermore, the arrows between the DB model and the optical model are meant to indicate that the learning that is performed based on the comparisons between the rendered image and the optical image may be a nonlinear/recursive process for the overall modeling performed by the computer subsystem(s). In addition, the errors may be used to adjust one or more parameters used for dynamic compensation (e.g., to account for day to day drifting in the parameter(s) of the optical inspection subsystem which can affect one or more characteristics of the optical image on a day to day basis).

In one such embodiment, the initial rendered image is generated for a whole die in the design printed on the wafer. For example, the computer subsystem(s) may perform offline rendering (for a whole die) 418 as shown in Fig. 4. Such offline rendering may include using design polygons 420 as input to DB raster 422, which may be performed as
5 described above. A gray scale image produced by DB raster 422 may be input to DB model 424, which may output a modified gray scale image as described further herein. DB model 424 used for offline rendering may be the DB model trained in offline training 400. The modified gray scale image produced by DB model 424 may be input to near field estimation 426, which may produce an estimated near field for the wafer as
10 described further herein. The estimated near field may be input to optical model 428, which may output offline rendered image 430, which may be an initial rendered image as described further herein. Optical model 428 used for offline rendering may be the optical model that is trained in offline training 400.

15 The offline rendered image 430 for the whole die may be made up of multiple smaller rendered images that in combination span the whole die on the wafer. For example, the simulation steps described herein may be performed separately for different portions of a die, and then the results of the simulation steps may be combined in any manner to produce simulation results for a larger portion of the die (e.g., a subswath or a
20 swath) or for the entire die. Alternatively, the simulation steps may be performed for all of the design for the whole die such that the results produced by any one simulation step are for an entire die on a wafer.

In one such embodiment, generating the rendered images includes modifying an
25 initial rendered image to minimize differences between the initial rendered image and the optical image generated by the optical inspection subsystem, the initial rendered image is generated offline, and generating the rendered image is performed online. For example, the initial rendered image may be generated offline as shown in offline rendering 418 in Fig. 4. In addition, generating the rendered image may be performed as shown in online

inspection 432, which may be performed for the whole wafer. In particular, as shown in Fig. 4, offline rendered image 434, which may be the offline rendered image generated by offline rendering 418 (i.e., offline rendered image 430), may be input to dynamic compensation 436, which may be the dynamic compensation that was trained in offline training 400, and which may be performed as described further herein. Dynamic compensation 436 may produce rendered image 438, which may be then compared to an optical image for defect detection and/or another purpose described herein. Therefore, the dynamic compensation may modify the initial rendered image that is generated offline to minimize differences between the initial rendered image and the optical image generated by the inspection subsystem thereby generating the rendered image, and the dynamic compensation may be performed online (i.e., during an inspection of the wafer).

In another such embodiment, the initial rendered image is generated for a whole die in the design printed on the wafer, and generating the rendered image is performed for an entirety of the wafer. For example, as described above, offline rendering 418 may be performed for a whole die on the wafer while online inspection 432 may be performed for an entirety of the wafer meaning that the rendered images must be generated for an entirety of the wafer (e.g., all of the dies on the wafer).

As described above, in some embodiments, the rendered image may be generated by estimating the near field of the wafer. In some instances, the near field estimation can be replaced by a near field calculation if full stack geometry and material information is available for a wafer. In one embodiment, generating the rendered image includes calculating a near field of the wafer based on the information for the design printed on the wafer, and the information for the design printed on the wafer includes geometry and material characteristics. For example, as shown in Fig. 5, geometry and material information 500 may be input to near field calculation 502. The geometry and material information may be a stack of geometry and material information (e.g., in a technology computer aided design (TCAD) format) for the wafer. The information for the design

used for the near field calculation may also include design geometry, material parameters, wavelength and angle dependency, etc. The near field calculation may be performed in a number of ways. For example, when the 3D stack of wafer design is known in both geometry and material, the near field at the wafer plane can be calculated by solving
5 Maxwell's equations (rigorous coupled wave analysis (RCWA) or FDTD method). The near field calculation may produce near field 504. The calculated near field of the wafer is a simulation of an EM field that would be generated at or near the top surface of the wafer (i.e., at the wafer plane) by the interaction of the materials and geometry of the wafer and the light directed to the wafer by the optical inspection subsystem. The
10 calculated near field may include amplitude as shown in left side of calculated near field 504 and phase as shown in right side of calculated near field 504. The calculated near field may also be or include complex numbers.

In one such embodiment, generating the rendered image also includes generating
15 an initial rendered image that is another simulation of the image generated by the optical inspection subsystem for the design printed on the wafer based on the near field and an optical model of the optical inspection subsystem. For example, as shown in Fig. 5, optical model 506 may use calculated near field 504 as input to generate initial rendered image 508. The optical model may model with and without aberrations of the optical
20 inspection subsystem. The initial rendered image may be simulated based on the inspector's optical characteristics using any of the approximations, functions, or models described herein.

In a further embodiment, generating the rendered image includes generating the
25 rendered image from the initial rendered image by modifying the initial rendered image to minimize differences between the initial rendered image and the optical image generated by the optical inspection subsystem. For example, as shown in Fig. 5, dynamic compensation 510 performed by the computer subsystem(s) may modify initial rendered image 508 to generate rendered image 512, one example of which is shown in Fig. 5 as

rendered image 514. The dynamic compensation may be performed as described further herein.

As further shown in Fig. 5, optical image 516, one example of which is shown in
5 Fig. 5 as optical image 518, may be acquired by the computer subsystem(s) as described herein and compared to rendered image 512. Such comparisons may generate difference image 520. The comparisons between the rendered image and the optical image may be performed for defect detection, which may be performed as described further herein. The comparisons between the rendered image and the optical image may also or alternatively
10 be performed for one or more other purposes described herein.

Like instances in which the computer subsystem(s) estimate the near field of the wafer, when the computer subsystem(s) calculate the near field, the computer subsystem(s) may perform general wafer inspection in three phases. For example, the
15 computer subsystem(s) may estimate modeling parameters from selected sites. In one such example, the computer subsystem(s) may perform offline training (for selected sites) 600 as shown in Fig. 6. The computer subsystem(s) may then render images for an entire die. For example, as shown in Fig. 6, the computer subsystem(s) may perform offline rendering (for a whole die on the wafer) 614. In addition, the computer subsystem(s)
20 may apply dynamic compensation (e.g., for gain/offset and aberration) in real time inspection for the whole wafer (or sampled dies). For example, as shown in Fig. 6, the computer subsystem(s) may perform online inspection (for a whole wafer) 624.

In some embodiments, the one or more computer subsystems are configured for
25 training one or more models used for generating the rendered image based on: one or more additional rendered images for one or more selected sites on one or more other wafers generated by performing generating the rendered image for the one or more selected sites; and one or more optical images generated by the optical inspection subsystem for the one or more selected sites on the one or more other wafers. For

example, as shown in Fig. 6, offline training (for selected sites) 600 may use geometry and material information 602, which may include any such information described herein, as input to near field calculation 604, which may produce a calculated near field for the wafer as described further herein. The calculated near field may be input to optical
5 model 606, which may output an initial rendered image as described further herein. The initial rendered image may be input to dynamic compensation 608, which may output rendered image 610. The computer subsystem(s) may then perform a comparison between the rendered image and an optical image, as shown in step 612.

10 The results of the comparison of the rendered image and the optical image may be used to determine errors (e.g., a sum of squared errors (SSE)) in the rendered image compared to the optical image. Those errors can be used to train one or more parameters of one or more of the step(s) performed by the computer subsystem(s). For example, the errors can be used to train one or more parameters of optical model 606. In addition, the
15 errors may be used to adjust one or more parameters used for dynamic compensation (e.g., to account for day to day drifting in the parameter(s) of the optical inspection subsystem which can affect one or more characteristics of the optical image on a day to day basis).

20 In one such embodiment, the initial rendered image is generated for a whole die in the design printed on the wafer. For example, the computer subsystem(s) may perform offline rendering (for a whole die) 614 as shown in Fig. 6. Such offline rendering may include using geometry and material information 616, which may include any of such information described herein, as input to near field calculation 618, which may produce a
25 calculated near field for the wafer as described further herein. The calculated near field may be input to optical model 620, which may output offline rendered image 622, which may be an initial rendered image as described further herein. Optical model 620 used for offline rendering 614 may be the optical model that is trained in offline training 600. The

offline rendered image may be otherwise generated as described further herein for the whole die.

In one such embodiment, generating the rendered images includes modifying an
5 initial rendered image to minimize differences between the initial rendered image and the
optical image generated by the optical inspection subsystem, the initial rendered image is
generated offline, and generating the rendered image is performed online. For example,
the initial rendered image may be generated offline as shown in offline rendering 614 in
Fig. 6. In addition, generating the rendered image may be performed as shown in online
10 inspection 624, which may be performed for the whole wafer. In particular, as shown in
Fig. 6, offline rendered image 626, which may be the offline rendered image generated
by offline rendering 614 (i.e., offline rendered image 622) may be input to dynamic
compensation 628, which may be the dynamic compensation that was trained in offline
training 600, and which may be performed as described further herein. Dynamic
15 compensation 628 may produce rendered image 630, which may be then compared to an
optical image for defect detection and/or any other purposes described herein. Therefore,
the dynamic compensation may modify the initial rendered image that is generated
offline to minimize differences between the initial rendered image and the optical image
generated by the inspection subsystem thereby generating the rendered image, and the
20 dynamic compensation may be performed online (i.e., during an inspection of the wafer).
In this manner, generating the rendered image may be performed online.

In another such embodiment, the initial rendered image is generated for a whole
die in the design printed on the wafer, and generating the rendered image is performed for
25 an entirety of the wafer. For example, as described above, offline rendering 614 may be
performed for a whole die on the wafer while online inspection 624 may be performed
for an entirety of the wafer meaning that the rendered images must be generated for an
entirety of the wafer (e.g., all of the dies on the wafer).

In one embodiment, generating the rendered image is performed for only one or more areas in the design printed on the wafer such that generating the rendered image is not performed for an entirety of the design. The areas(s) are also referred to herein as “hot spots” or “small blocks.” Areas, hot spots, and small blocks as those terms are used
5 herein can be defined as a unit of the circuit structure that repeats many times on a die. An example size of the areas, hot spots, and small blocks is about 500 nm by about 500 nm. In this manner, the embodiments described herein may perform the steps described herein for only some portions, but not an entirety, of a die. The hot spots and/or small blocks may be identified and/or selected in any suitable manner. For example, the hot
10 spots and/or small blocks may be care areas in the design in which inspection is to be performed. In addition, or alternatively, the hot spots and/or small blocks may be relatively small portions of the design that are repeated two or more times within the design. In this manner, generating the initial rendered image may be performed for only one small block, but that same initial rendered image may be dynamically compensated
15 (possibly in different manners) and then compared to multiple optical images generated at different instances of the same small block of the design printed on the wafer. Generating the rendered image for only one or more areas may otherwise be performed as described herein (e.g., as shown in Figs. 3 and 5).

20 The computer subsystem(s) may be configured for hot spot or small block wafer inspection in three phases. For example, the computer subsystem(s) may estimate modeling parameters from selected sites. In one such example, the computer subsystem(s) may perform offline training 400 shown in Fig. 4 and 600 shown in Fig. 6 in which the selected sites are replaced with selected hot spot and/or small block sites.
25 The computer subsystem(s) may also render images for all hot spots/small blocks for one die. For example, the computer subsystem(s) may perform offline rendering 418 as shown in Fig. 4 and 614 as shown in Fig. 6, but instead of performing the offline rendering for the whole die as shown in Figs. 4 and 6, the offline rendering is performed for all hot spots and/or small blocks in one die. In addition, the computer subsystem(s)

may apply dynamic compensation (e.g., for gain/offset and aberration) in real time inspection of all hot spots/small blocks in a whole wafer (or sampled dies). For example, the computer subsystem(s) may be configured for performing online inspection 432 as shown in Fig. 4 and 624 as shown in Fig. 6 except that instead of the online inspection
5 being performed for the whole wafer as shown in Figs. 4 and 6, the online inspection is performed for only hot spots and/or small blocks on the whole wafer.

In an embodiment, the computer subsystem(s) are configured for training one or more models used for generating the rendered image based on: two or more additional
10 rendered images for two or more areas on one or more other wafers generated by performing generating the rendered image for the two or more areas; and two or more optical images generated by the optical inspection subsystem for the two or more areas on the one or more other wafers. These steps may be performed as described herein (as shown in offline training 400 shown in Fig. 4 and offline training 600 shown in Fig. 6),
15 where the selected sites are the two or more areas (e.g., two or more hot spots and/or small blocks).

The training performed for a first of the two or more areas is performed differently than the training performed for a second of the two or more areas. In this
20 manner, the modeling parameters may be customized for each hot spot/small block type. For example, if a first hot spot includes a first portion of the design having first characteristics (e.g., dense lines) and a second hot spot includes a second portion of the design having second characteristics (e.g., sparse contact holes) that are different from the first characteristics, the first and second hot spots may be printed on the wafer
25 differently (e.g., with different bias and corner rounding) and may be imaged by the optical inspection subsystem differently (e.g., with different resolution, contrast, etc.). Therefore, one or more models (e.g., the DB model and/or the optical model) used for generating rendered images for the different hot spots would preferably be customized to account for such differences in the processes involved in generating actual optical images

of the different hot spots. Therefore, the offline training may generate hot spot (or small block) specific model(s) based on rendered image(s) and optical image(s) that correspond to the hot spot (or small block) for which the model(s) are being trained. Such training may otherwise be performed as described herein.

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In one such embodiment, generating the rendered image includes modifying an initial rendered image to minimize differences between the initial rendered image and the optical image generated by the optical inspection subsystem, the initial rendered image is generated offline, and generating the rendered image is performed online. These steps
10 may be performed as described further herein and shown in Figs. 4 and 6.

In another such embodiment, the initial rendered image is generated for all of the two or more areas in a die in the design printed on the wafer, and generating the rendered image is further performed online for all of the two or more areas in an entirety of the
15 wafer. For example, as described above, the offline rendering of the initial rendered image may be performed for all hot spots and/or small blocks on one die. In addition, as described further herein, the online inspection may be performed for all hot spots and/or small blocks on a whole wafer.

20 The infrastructure for software and hardware that performs the preparation, setup and inspection described herein may be configured in a variety of different ways. For example, in one embodiment, the one or more computer subsystems include two or more computer subsystems, and at least one of the two or more computer subsystems is not part of a tool that includes the optical inspection subsystem. In this manner, the computer
25 subsystem(s) may include at least one computer subsystem that is not part of the optical inspection tool (e.g., computer subsystem 102 shown in Fig. 1) and at least one computer subsystem that is part of the optical inspection tool (e.g., computer subsystem 36 shown in Fig. 1). Such a configuration may be advantageous when it is more suitable to perform

some of the step(s) described herein offline (e.g., using computer subsystem 102) while other steps are more suitably performed online (e.g., using computer subsystem 36).

In a further embodiment, the one or more computer subsystems include at least
5 one virtual inspection system also commonly referred to as a virtual inspector (VI). A VI can be generally defined as a computer system that can store massive amounts of output generated for a wafer by an inspection subsystem such that the output can be “played back” in a manner that mimics real time acquisition of the output during which a virtual inspection can be performed for the wafer using only the stored output. Examples of
10 such virtual inspectors are illustrated in U.S. Patent Nos. 8,126,255 issued on February 28, 2012 to Bhaskar et al. and 9,222,895 issued on December 29, 2015 to Duffy et al., which are incorporated by reference as if fully set forth herein. The computer subsystem(s) described herein may be further configured as described in these patents.

15 In the embodiments described herein, a VI may be particularly useful for performing one or more offline steps during setup and/or for storage of the various information and/or images generated and/or used in the embodiments described herein. For example, a VI may be particularly useful for setup of the die-to-DB inspection described herein. In one such example, a VI may be configured for extracting design
20 clips (i.e., relatively small portions of an entire design of a die on a wafer) from a design database or file. In addition, a VI may be configured for generating the initial rendered images described herein and storing the initial rendered images. In addition, since the VI may be capable of storing massive amounts of images generated for physical wafers (i.e., actual wafers), the VI may be particularly suitable for tuning one or more parameters of
25 one or more of the models described herein using both simulated images and actual wafer images.

A VI may also be configured for performing one or more of the steps described herein online. For example, a VI may be configured to perform the die-to-DB inspection

(i.e., the image compare and defect detection steps described herein) online (and offline as well). Furthermore, since a VI may include multiple image computer nodes, performance of any of the steps described herein can be distributed across the multiple image computer nodes thereby providing advantages for throughput. Furthermore, the rendered images may be stored on the VI and then transferred to one or more other computer subsystems (e.g., a computer subsystem that is part of an optical inspection tool) as those other computer subsystem(s) need the rendered images (e.g., for online optical die-to-DB inspection).

10 The computer subsystem(s) may also include a prep station for whole die design clip and image rendering preparation, with multiple cores of CPU/GPU/FPGA and storage. In addition, the computer subsystems may be coupled by a network between the prep station and a computer subsystem of the inspection tool to transfer rendered images. The computer subsystem(s) may also include a design/TCAD based offline image rendering engine on the prep station or the inspection tool. The computer subsystem(s) may further include a design/TCAD based offline training engine on the prep station or the inspection tool.

20 In some such embodiments, the infrastructure used for preparing the design database may include a database in which design information is stored (e.g., one or more reticle design files (RDFs)) and a server coupled to the database and image computer(s) and/or VI(s). The server and/or the image computer(s) and/or VI(s) may extract design clips from the database thereby preparing the design database for use by the embodiments described herein. The image computer(s) and/or the VI(s) may store the extracted design clips in a design clip database, which may have any suitable format known in the art.

25 The infrastructure used for design rendering may include the image computer(s) and/or VI(s) of the infrastructure configured for preparing the design data. The image computer(s) and/or VI(s) may be configured to render the design (e.g., from the design

clips stored in the design clip database) to generate the rendered images described herein. In addition, the image computer(s) and/or the VI(s) may store the rendered images in a rendered image database, which may have any suitable format known in the art.

5 The infrastructure configured for performing the die-to-DB inspection may include image computer(s), which may be different from the image computer(s) included in the infrastructure configured for preparing the design database and the image computer(s) included in the infrastructure configured for design rendering. The image computer(s) included in the infrastructure for performing the die-to-DB inspection may
10 be configured to acquire the rendered images from the rendered image database. These image computer(s) may also acquire the optical images generated by the optical inspection subsystem and perform one or more steps using the rendered and optical images such as pixel-to-design alignment (PDA) and defect detection. In this manner, the image computer(s) may perform inspection with a rendered die image.

15 The infrastructure configured for the inspection may also include one or more user interfaces coupled to the image computer(s) such that the results produced by the image computer(s) can be provided to a user through the one or more user interfaces and/or such that input and/or instructions can be received from the user through the one
20 or more user interfaces. The user interface(s) may include any suitable user interfaces known in the art (e.g., such as a user interface that is used by commercially available inspection tools and configured to have the capability described herein).

Each of the embodiments of the system described herein may be further
25 configured according to any other embodiment(s) described herein.

Another embodiment relates to a computer-implemented method for detecting defects on a wafer. The method includes steps for each of the functions of the computer

subsystem(s) described above. The optical inspection subsystem is configured as described herein.

Each of the steps of the method may be performed as described further herein.

5 The method may also include any other step(s) that can be performed by the inspection subsystem and/or computer subsystem(s) or system(s) described herein. The steps of the method are performed by one or more computer systems, which may be configured according to any of the embodiments described herein. In addition, the method described above may be performed by any of the system embodiments described herein.

10

An additional embodiment relates to a non-transitory computer-readable medium storing program instructions executable on a computer system for performing a computer-implemented method for detecting defects on a wafer. One such embodiment is shown in Fig. 7. In particular, as shown in Fig. 7, non-transitory computer-readable
15 medium 700 includes program instructions 702 executable on computer system 704. The computer-implemented method may include any step(s) of any method(s) described herein.

Program instructions 702 implementing methods such as those described herein
20 may be stored on computer-readable medium 700. The computer-readable medium may be a storage medium such as a magnetic or optical disk, a magnetic tape, or any other suitable non-transitory computer-readable medium known in the art.

The program instructions may be implemented in any of various ways, including
25 procedure-based techniques, component-based techniques, and/or object-oriented techniques, among others. For example, the program instructions may be implemented using ActiveX controls, C++ objects, JavaBeans, Microsoft Foundation Classes ("MFC"), SSE (Streaming SIMD Extension) or other technologies or methodologies, as desired.

Computer system 704 may be configured according to any of the embodiments described herein.

5 All of the methods described herein may include storing results of one or more steps of the method embodiments in a computer-readable storage medium. The results may include any of the results described herein and may be stored in any manner known in the art. The storage medium may include any storage medium described herein or any other suitable storage medium known in the art. After the results have been stored, the
10 results can be accessed in the storage medium and used by any of the method or system embodiments described herein, formatted for display to a user, used by another software module, method, or system, etc.

Further modifications and alternative embodiments of various aspects of the
15 invention will be apparent to those skilled in the art in view of this description. For example, methods and systems for detecting defects on a wafer are provided. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the invention. It is to be understood that the forms of the invention shown and described herein are to be
20 taken as the presently preferred embodiments. Elements and materials may be substituted for those illustrated and described herein, parts and processes may be reversed, and certain features of the invention may be utilized independently, all as would be apparent to one skilled in the art after having the benefit of this description of the invention. Changes may be made in the elements described herein without departing
25 from the spirit and scope of the invention as described in the following claims.

WHAT IS CLAIMED IS:

1. A system configured to detect defects on a wafer, comprising:
 - 5 an optical inspection subsystem comprising at least a light source and a detector,
wherein the light source is configured to generate light that is directed to a
wafer, and wherein the detector is configured to detect light from the
wafer and to generate images responsive to the detected light; and
 - 10 one or more computer subsystems configured for:

generating a rendered image based on information for a design printed on
the wafer, wherein the rendered image is a simulation of an image
generated by the optical inspection subsystem for the design
15 printed on the wafer;

comparing the rendered image to an optical image of the wafer generated
by the optical inspection subsystem, wherein the design is printed
on the wafer using a reticle; and
 - 20 detecting defects on the wafer based on results of the comparing.
2. The system of claim 1, wherein said generating comprises converting polygons in
the information for the design to a gray scale image.
- 25 3. The system of claim 2, wherein said converting the polygons is performed with
sub-pixel accuracy.

4. The system of claim 2, wherein said generating further comprises generating a modified gray scale image by applying bias correction and corner rounding to the gray scale image.

5 5. The system of claim 4, wherein said generating further comprises estimating a near field of the wafer based on the modified gray scale image and the information for the design printed on the wafer.

6. The system of claim 5, wherein said generating further comprises generating an
10 initial rendered image that is another simulation of the image generated by the optical inspection subsystem for the design printed on the wafer based on the near field and an optical model of the optical inspection subsystem.

7. The system of claim 6, wherein said generating further comprises generating the
15 rendered image from the initial rendered image by modifying the initial rendered image to minimize differences between the initial rendered image and the optical image generated by the optical inspection subsystem.

8. The system of claim 1, wherein said generating comprises calculating a near field
20 of the wafer based on the information for the design printed on the wafer, and wherein the information for the design printed on the wafer comprises geometry and material characteristics.

9. The system of claim 8, wherein said generating further comprises generating an
25 initial rendered image that is another simulation of the image generated by the optical inspection subsystem for the design printed on the wafer based on the near field and an optical model of the optical inspection subsystem.

10. The system of claim 9, wherein said generating further comprises generating the rendered image from the initial rendered image by modifying the initial rendered image to minimize differences between the initial rendered image and the optical image generated by the optical inspection subsystem.

5

11. The system of claim 1, wherein the one or more computer subsystems are further configured for training one or more models used for said generating based on: one or more additional rendered images for one or more selected sites on one or more other
10 wafers generated by performing said generating for the one or more selected sites; and one or more optical images generated by the optical inspection subsystem for the one or more selected sites on the one or more other wafers.

12. The system of claim 11, wherein generating the rendered image comprises
15 modifying an initial rendered image to minimize differences between the initial rendered image and the optical image generated by the optical inspection subsystem, wherein the initial rendered image is generated offline, and wherein generating the rendered image is performed online.

20 13. The system of claim 12, wherein the initial rendered image is generated for a whole die in the design printed on the wafer, and wherein generating the rendered image is further performed online for an entirety of the wafer.

14. The system of claim 1, wherein said generating is performed for only one or more
25 areas in the design printed on the wafer such that said generating is not performed for an entirety of the design.

15. The system of claim 1, wherein the one or more computer subsystems are further configured for training one or more models used for said generating based on: two or

more additional rendered images for two or more areas on one or more other wafers generated by performing said generating for the two or more areas; and two or more optical images generated by the optical inspection subsystem for the two or more areas on the one or more other wafers, and wherein said training performed for a first of the two or
5 more areas is performed differently than said training performed for a second of the two or more areas.

16. The system of claim 15, wherein generating the rendered image comprises modifying an initial rendered image to minimize differences between the initial rendered
10 image and the optical image generated by the optical inspection subsystem, wherein the initial rendered image is generated offline, and wherein generating the rendered image is performed online.

17. The system of claim 16, wherein the initial rendered image is generated for all of
15 the two or more areas in a die in the design printed on the wafer, and wherein generating the rendered image is further performed online for all of the two or more areas in an entirety of the wafer.

18. The system of claim 1, wherein the one or more computer subsystems comprise
20 two or more computer subsystems, and wherein at least one of the two or more computer subsystems is not part of a tool that includes the optical inspection subsystem.

19. The system of claim 1, wherein the one or more computer subsystems comprise at
least one virtual inspection system.

25

20. The system of claim 1, wherein the one or more computer subsystems are further configured for determining if the reticle passes qualification based on the detected defects.

21. The system of claim 1, wherein the one or more computer subsystems are further configured for determining a performance of one or more process steps performed on the wafer based on the detected defects.

5 22. The system of claim 21, wherein the wafer is a short loop wafer.

23. A non-transitory computer-readable medium, storing program instructions executable on a computer system for performing a computer-implemented method for detecting defects on a wafer, wherein the computer-implemented method comprises:

10

generating a rendered image based on information for a design printed on a wafer, wherein the rendered image is a simulation of an image generated by an optical inspection subsystem for the design printed on the wafer, wherein the optical inspection subsystem comprises at least a light source and a
15 detector, wherein the light source is configured to generate light that is directed to the wafer, and wherein the detector is configured to detect light from the wafer and to generate images responsive to the detected light;

15

comparing the rendered image to an optical image of the wafer generated by the optical inspection subsystem, wherein the design is printed on the wafer using a reticle; and

20

detecting defects on the wafer based on results of the comparing, wherein said generating, said comparing, and said detecting are performed by one or
25 more computer subsystems.

25

24. A computer-implemented method for detecting defects on a wafer, comprising:

generating a rendered image based on information for a design printed on a wafer,
wherein the rendered image is a simulation of an image generated by an
optical inspection subsystem for the design printed on the wafer, wherein
the optical inspection subsystem comprises at least a light source and a
5 detector, wherein the light source is configured to generate light that is
directed to the wafer, and wherein the detector is configured to detect light
from the wafer and to generate images responsive to the detected light;

10 comparing the rendered image to an optical image of the wafer generated by the
optical inspection subsystem, wherein the design is printed on the wafer
using a reticle; and

15 detecting defects on the wafer based on results of the comparing, wherein said
generating, said comparing, and said detecting are performed by one or
more computer subsystems.

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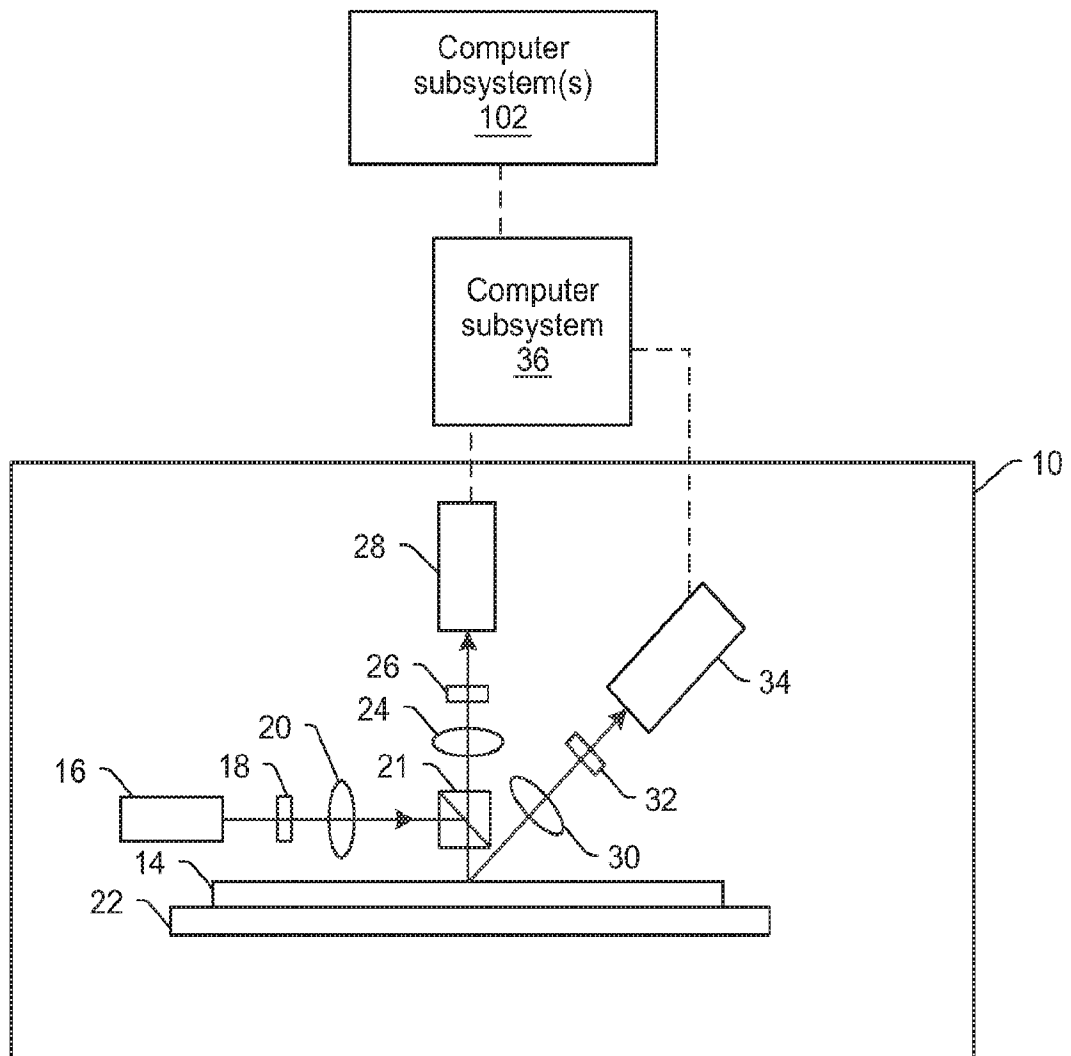


Fig. 1

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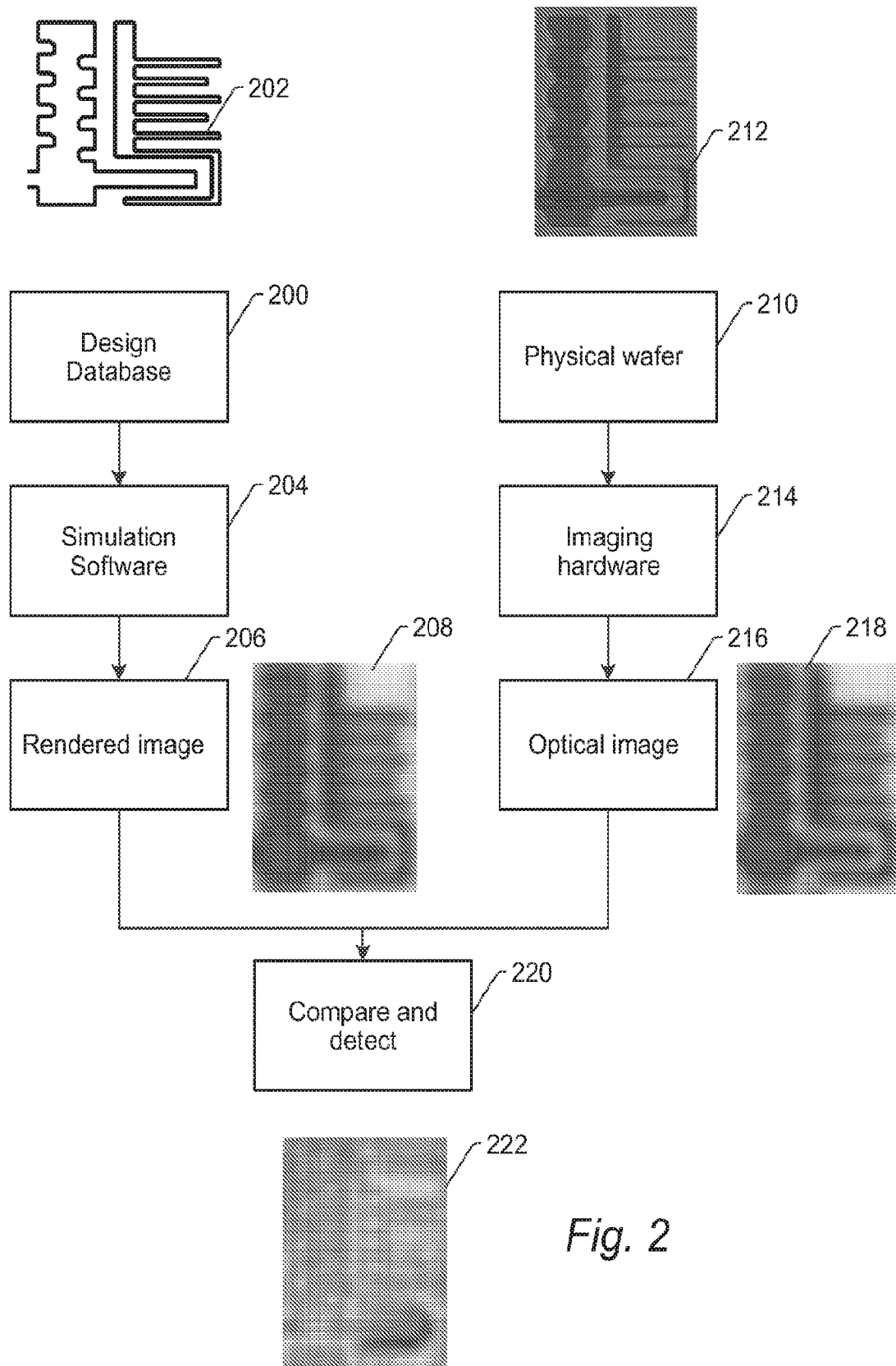
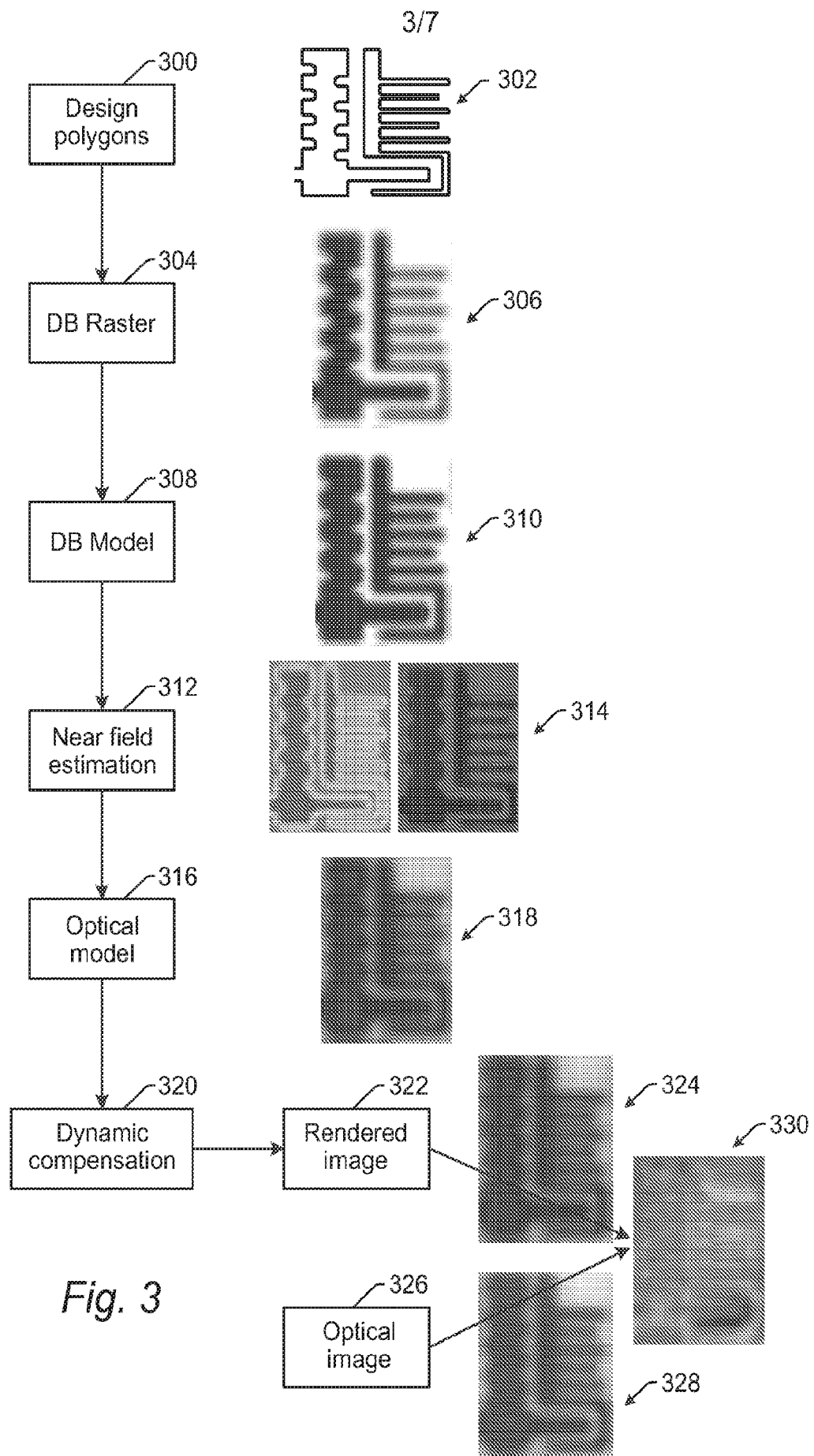


Fig. 2



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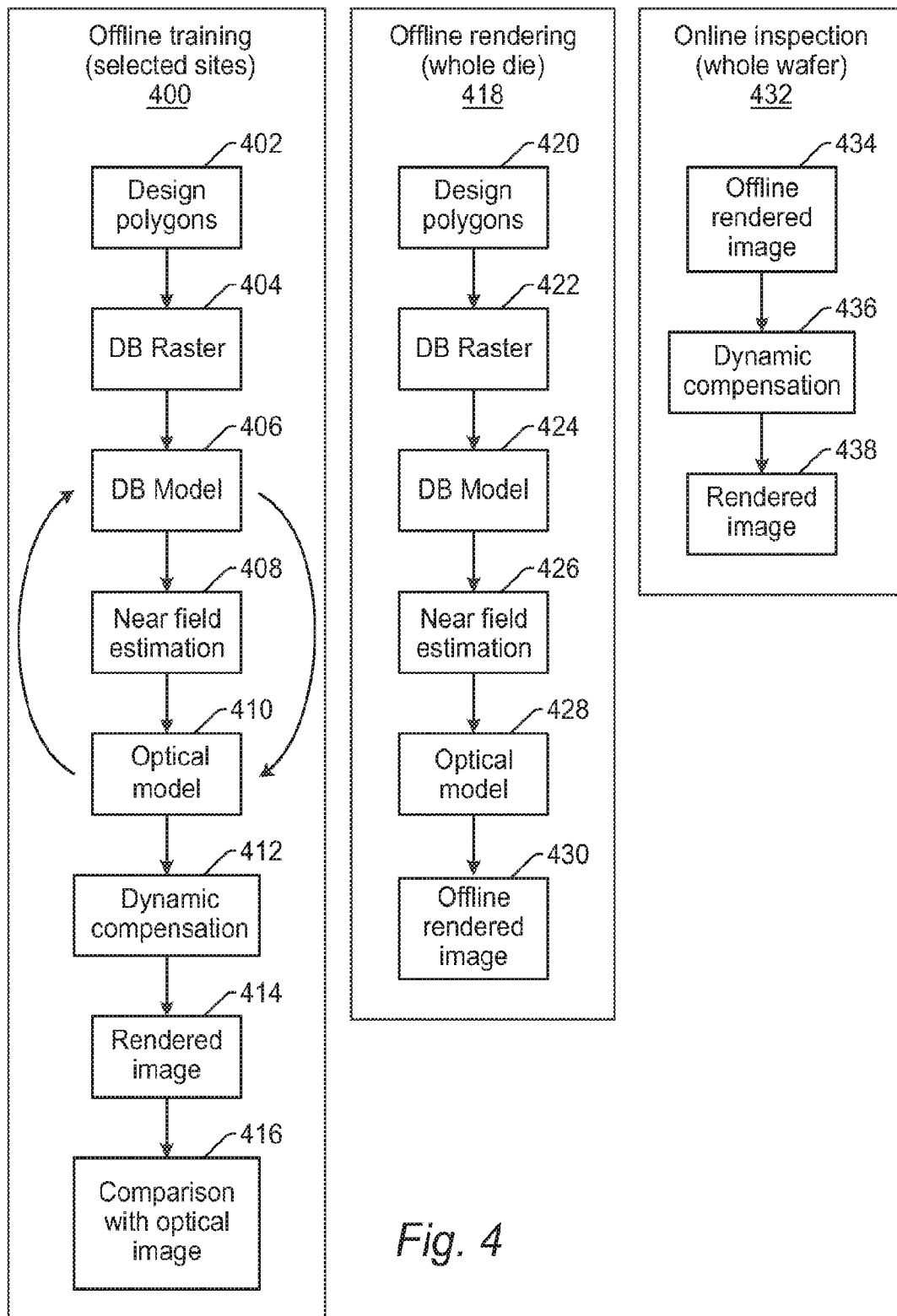


Fig. 4

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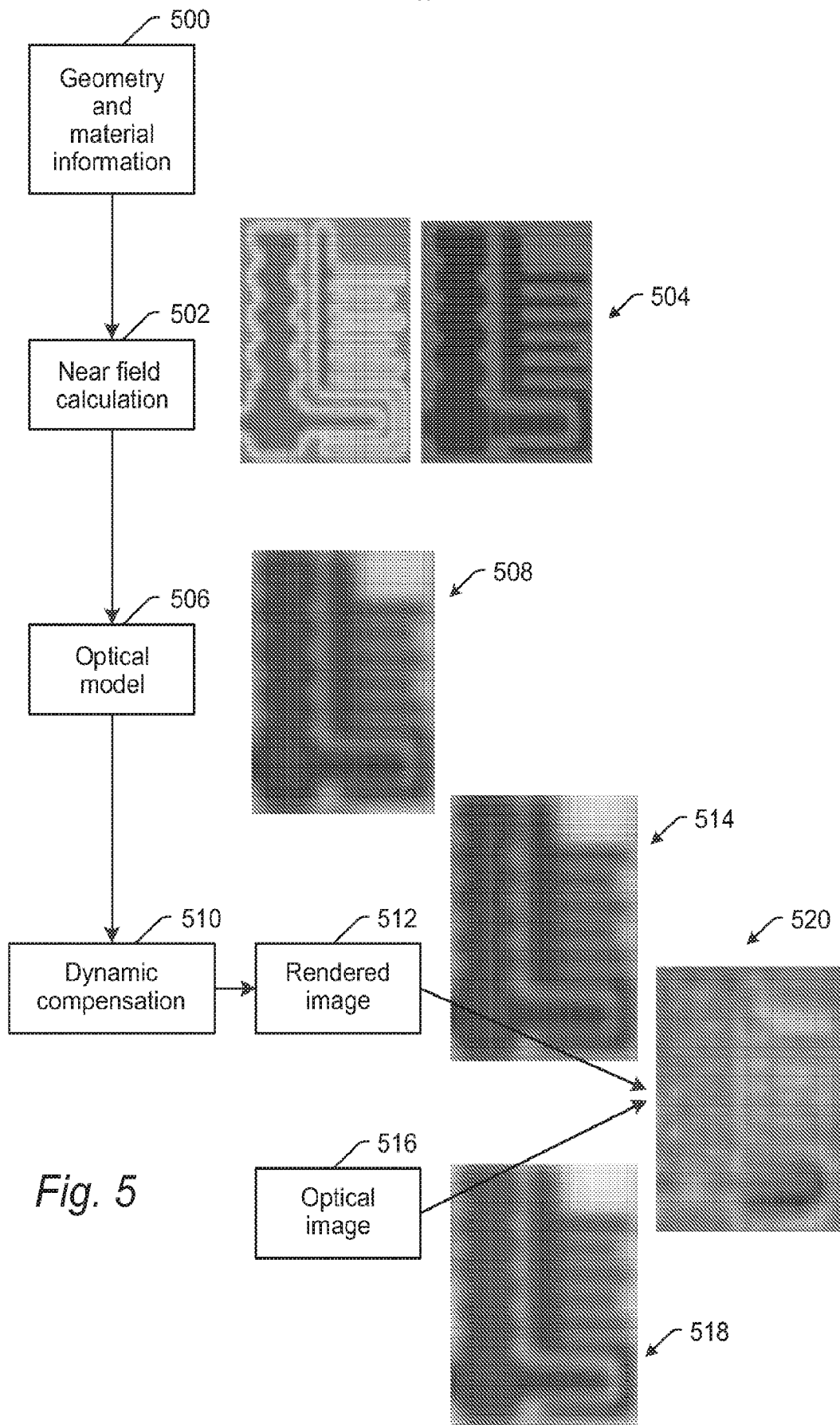
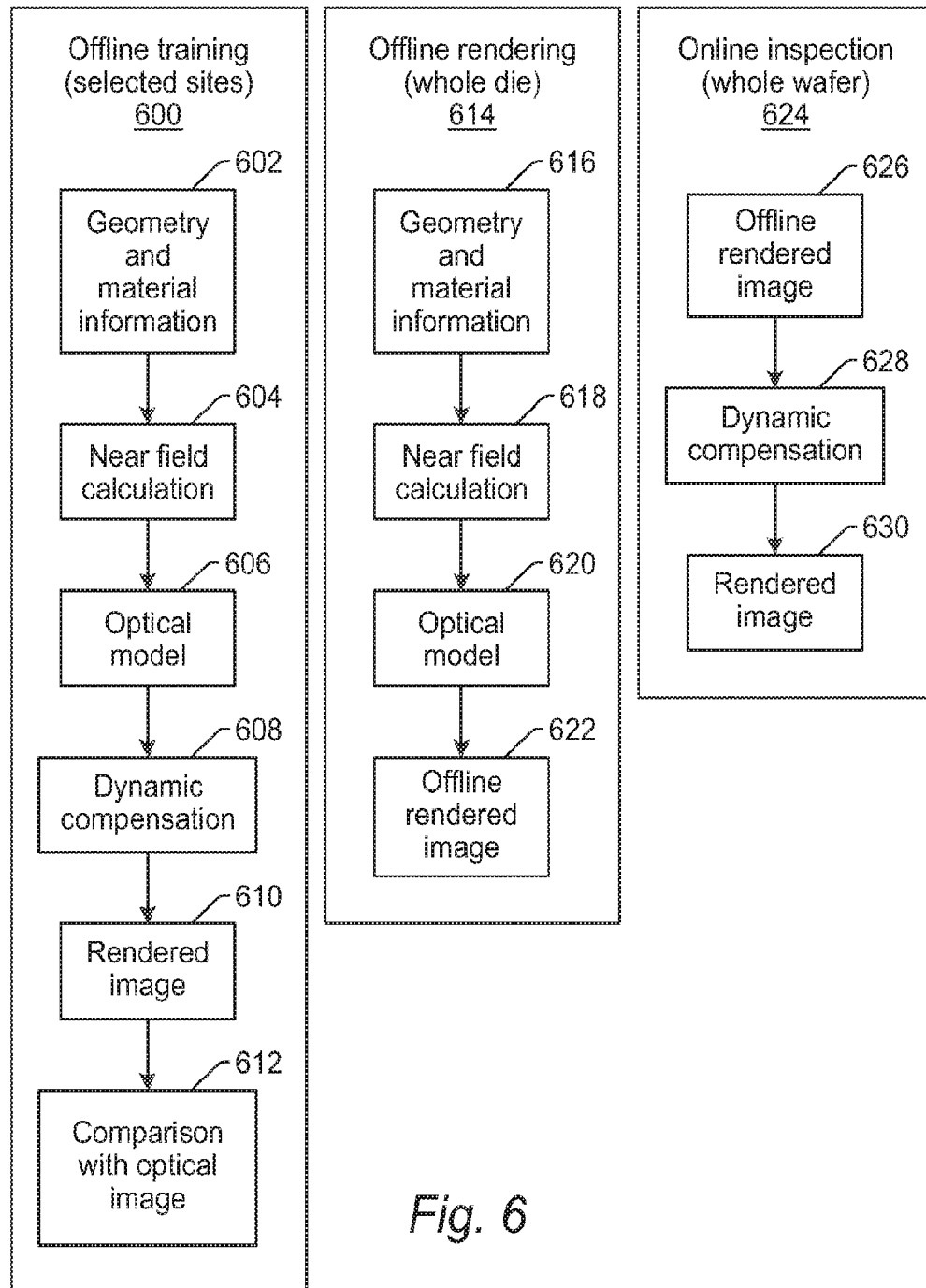
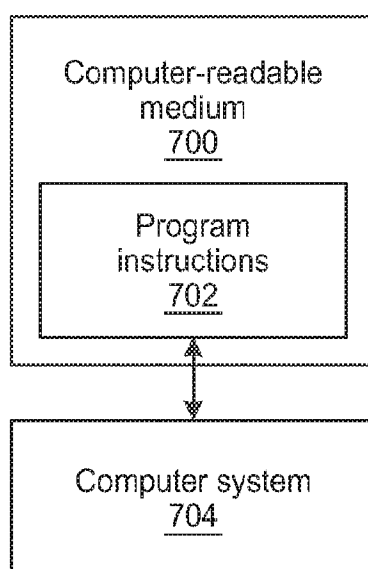


Fig. 5

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*Fig. 6*

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*Fig. 7*

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/66(2006.01)i, G01N 21/95(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/66; G06F 17/50; G01N 37/00; G06K 9/00; G06K 9/62; G01N 21/88; G01N 21/95

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: light, detect, defect, substrate, image, compare, render, database

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011-0276935 A1 (CHRISTOPHE FOUQUET et al.) 10 November 2011	1-3, 14, 18, 20-24
A	See abstract, paragraphs [0037], [0044], [0052], [0101], [0120] and figure 1.	4-13, 15-17, 19
Y	US 2008-0167829 A1 (ALLEN PARK et al.) 10 July 2008	1-3, 14, 18, 20-24
	See abstract, paragraph [0032] and figure 2.	
Y	US 2010-0208979 A1 (GORDON ABBOTT et al.) 19 August 2010	2-3, 14
	See abstract, paragraphs [0048], [0069] and figures 1-3.	
A	US 2004-0086171 A1 (CHUNG-SAM JUN et al.) 06 May 2004	1-24
	See abstract, paragraphs [0050]-[0072] and figures 3-5.	
A	US 2012-0092657 A1 (YUKIHIRO SHIBATA et al.) 19 April 2012	1-24
	See abstract, paragraphs [0033]-[0069] and figures 1-4D.	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 June 2016 (30.06.2016)

Date of mailing of the international search report

30 June 2016 (30.06.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/025715

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