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(54) **Title:** INTEGRATED CIRCUIT PACKAGE AND METHOD OF FORMING SAME

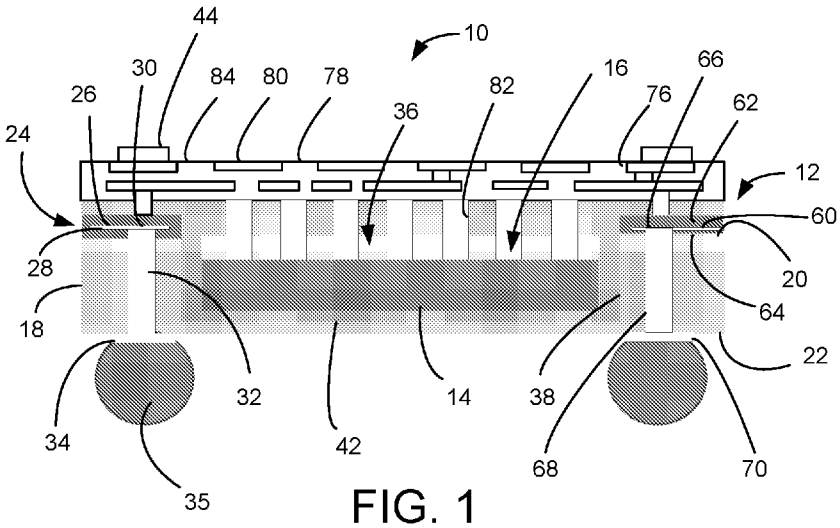


FIG. 1

(57) **Abstract:** Various embodiments of an integrated circuit package are disclosed. The package includes an interposer and an electronic device coupled to the interposer at a device interface. The interposer includes a semiconductor substrate, a device interface disposed on or in a first major surface of the substrate, and an interconnect region disposed on the first major surface of the substrate adjacent to the device interface. The interconnect region includes an inorganic nonconductive layer disposed on the first major surface of the substrate and a patterned conductive layer disposed at least partially within the inorganic nonconductive layer. The interposer further includes a conductive via disposed through the substrate between a conductive pad of the patterned conductive layer and the second major surface of the substrate. The conductive via electrically connects the conductive pad with a conductive region or component disposed adjacent to the second major surface of the substrate.

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INTEGRATED CIRCUIT PACKAGE AND METHOD OF FORMING SAME

[0001] This application claims the benefit of U.S. Provisional Patent Application, Serial No. 63/526,768, filed July 14, 2023, the entire content of which is incorporated herein by reference.

TECHNICAL FIELD

[0002] This disclosure generally relates to an integrated circuit package, and more particularly, an integrated circuit package that includes an interposer having an interconnect region disposed on a substrate of the interposer.

BACKGROUND

[0003] A wide variety of electronic assemblies such as those that are utilized for implantable medical devices (IMDs) employ electronic circuitry, e.g., for providing electrical stimulation of body tissue and/or monitoring a physiologic condition. Such IMDs may deliver electrical therapy energy in the form of shocking energy and stimulating pulses to selected body tissue. These IMDs typically include output circuitry for generating the electrical energy under prescribed conditions and at least one lead bearing a stimulation electrode for delivering the electrical energy to the selected tissue. For example, cardiac pacemakers and implantable cardioverter-defibrillators (ICDs) have been developed for maintaining a desired heart rate during episodes of bradycardia or for applying cardioversion or defibrillation therapies to the heart upon detection of serious arrhythmias. Other nerve, brain, muscle, and organ tissue stimulating medical devices are also known for treating a variety of conditions.

[0004] Currently available IMDs, including ICDs and implantable pulse generators (IPGs), typically include a metallic housing that is hermetically sealed and, therefore, is impervious to body fluids, and a header or connector assembly mounted to the housing for making electrical and mechanical connection with one or more leads. Such devices also possess telemetry capabilities for communicating with external devices. Over the past several years, IMDs have evolved from relatively bulky devices to complex miniaturized devices that exhibit increasing functionality. For example, numerous improvements have been made in cardioversion/defibrillation leads and electrodes that have enabled the cardioversion/defibrillation energy to be precisely delivered to selected one or more

portions of upper and lower heart chambers, thereby dramatically reducing the delivered shock energy required to cardiovert or defibrillate the heart chamber. High voltage output circuitry has also been improved to provide monophasic, biphasic, or multi-phase cardioversion/defibrillation shock or pulse waveforms, sometimes with particular combinations of cardioversion/defibrillation electrodes, that are efficacious in lowering the required shock energy to cardiovert or defibrillate the heart.

[0005] The miniaturization of IMDs is driving size and cost reduction of all IMD components, including the electronic circuitry components, where it is desirable to increase the density and reduce the size of such components so that the overall circuitry can be more compact. As the dimensions of IMDs decrease, the electronic circuits of the IMD are formed as integrated circuits to fit within a minimal space. Furthermore, as the dimensions of the components are also being reduced, it is desirable to improve the use of the dimensions within the IMD package.

[0006] One response to this desire has been through technological improvements to the packaging for the devices in which the output circuitry is included through such packaging techniques as reconstituted wafer packaging. In particular, development efforts in reconstituted wafer packaging, also known as fan out wafer level packaging, focus on producing thinner and smaller electronic packages.

SUMMARY

[0007] In general, the present disclosure provides various embodiments of an integrated circuit package that includes an interposer and an electronic device coupled to the interposer at a device interface. The interposer includes a semiconductor substrate and an interconnect region disposed on a first major surface of the substrate adjacent to the device interface that is disposed on or in the first major surface of the substrate. The interconnect region can include an inorganic nonconductive layer disposed on the first major surface of the substrate and a patterned conductive layer disposed at least partially within the inorganic nonconductive layer. A conductive via can be disposed through the substrate between a conductive pad of the patterned conductive layer of the interconnect region and a second major surface of the substrate. The conductive via can electrically connect the conductive pad with a conductive region or component such as a conductive pad that is disposed adjacent to the second major surface of the substrate.

[0008] This disclosure includes without limitation the following clauses:

[0009] Clause 1: An integrated circuit package including an interposer and an electronic device coupled to the interposer at a device interface. The interposer includes a semiconductor substrate having a first major surface, a second major surface, and the device interface disposed on or in the first major surface; an interconnect region disposed on the first major surface of the substrate adjacent to the device interface, where the interconnect region includes an inorganic nonconductive layer disposed on the first major surface of the substrate and a patterned conductive layer disposed at least partially within the inorganic nonconductive layer, where the patterned conductive layer includes a conductive pad; and a conductive via disposed through the substrate between the conductive pad of the patterned conductive layer of the interconnect region and the second major surface of the substrate. The conductive via electrically connects the conductive pad with a conductive region or component disposed adjacent to the second major surface of the substrate.

[0010] Clause 2: The package of Clause 1, where the interposer further includes a second interconnect region disposed on the first major surface of the substrate adjacent to the device interface. The second interconnect region includes an inorganic nonconductive layer disposed on the first major surface of the substrate and a patterned conductive layer disposed at least partially within the inorganic nonconductive layer, where the patterned conductive layer includes a second conductive pad. The second interconnect region further includes a second conductive via disposed through the substrate between the second conductive pad of the patterned conductive layer of the second interconnect region and the second major surface of the substrate, where the second conductive via electrically connects the second conductive pad with a second conductive region or component disposed adjacent to the second major surface of the substrate.

[0011] Clause 3: The package of Clause 2, further including a redistribution layer disposed over the interconnect region, the second interconnect region, and the device, where the redistribution layer is electrically connected to the device and at least one of the conductive pad or the second conductive pad.

[0012] Clause 4: The package of any one of Clauses 1–3, where the conductive via extends through a portion of a thickness of the inorganic nonconductive layer of the interconnect region.

[0013] Clause 5: The package of Clause 4, where the conductive via extends through a portion, but not all, of the thickness of the inorganic nonconductive layer of the interconnect region.

[0014] Clause 6: The package of Clause 4, where the conductive via extends to the conductive pad within the inorganic nonconductive layer of the interconnect region.

[0015] Clause 7: The package of any one of Clauses 1–6, where the inorganic nonconductive layer of the interconnect region includes an oxide.

[0016] Clause 8: The package of Clause 7, where the inorganic nonconductive layer of the interconnect region includes silicon dioxide.

[0017] Clause 9: The package of any one of Clauses 1–6, where the inorganic nonconductive layer of the interconnect region includes a nitride.

[0018] Clause 10: The package of Clause 9, where the inorganic nonconductive layer of the interconnect region includes silicon nitride.

[0019] Clause 11: The package of any one of Clauses 1–10, where the device interface includes a cavity.

[0020] Clause 12: The package of Clause 11, where the cavity is disposed in the first major surface of the substrate.

[0021] Clause 13: The package of any one of Clauses 1–12, further including a solder bump disposed on and electrically connected to the conductive region or component disposed adjacent to the second major surface of the substrate.

[0022] Clause 14: The package of any one of Clauses 1–13, where the substrate includes silicon.

[0023] Clause 15: A method of forming an integrated circuit package, including disposing an interconnect region on a first major surface of a semiconductor substrate of an interposer. Disposing the interconnect region includes disposing an inorganic nonconductive layer on a first major surface of the substrate, and disposing a patterned conductive layer at least partially within the inorganic nonconductive layer, where the patterned conductive layer includes a conductive pad. The method further includes disposing a device interface on or in the first major surface of the substrate; coupling an electronic device to the substrate at the device interface; and disposing a redistribution layer over the interconnect region and the device, where the redistribution layer is electrically connected to the device and the conductive pad. The method further includes

disposing a conductive via through the substrate between a second major surface of the substrate and the conductive pad of the patterned conductive layer of the interconnect region; and disposing a conductive region or component adjacent to the second major surface of the substrate and electrically connecting the conductive region or component to the conductive pad utilizing the conductive via.

[0024] Clause 16: The method of Clause 15, where disposing the interconnect region further includes disposing a second inorganic nonconductive layer on the patterned conductive layer, and disposing a second patterned conductive layer at least partially within the second inorganic nonconductive layer.

[0025] Clause 17: The method of any one of Clauses 15–16, where the device interface includes a cavity, where disposing the device interface includes disposing the cavity in the first major surface of the substrate.

[0026] Clause 18: The method of any one of Clauses 15–17, where the conductive via extends through a portion of a thickness of the inorganic nonconductive layer of the interconnect region.

[0027] Clause 19: The method of Clause 18, where the conductive via extends through a portion, but not all, of the thickness of the inorganic nonconductive layer of the interconnect region.

[0028] Clause 20: The method of Clause 18, where the conductive via extends to the conductive pad within the inorganic nonconductive layer of the interconnect region.

[0029] Clause 21: The method of any one of Clauses 15–20, where the inorganic nonconductive layer of the interconnect region includes an oxide.

[0030] Clause 22: The method of Clause 21, where the inorganic nonconductive layer of the interconnect region includes silicon dioxide.

[0031] Clause 23: The method of any one of Clauses 15–20, where the inorganic nonconductive layer of the interconnect region includes a nitride.

[0032] Clause 24: The method of Clause 23, where the inorganic nonconductive layer of the interconnect region includes silicon nitride.

[0033] Clause 25: The method of any one of Clauses 15–24, where the substrate includes silicon.

[0034] Clause 26: The method of any one of Clauses 15–25, further including disposing a conductive pad on the redistribution layer such that the redistribution layer is between the

conductive pad and the first major surface of the substrate, where the conductive pad is electrically connected to the redistribution layer.

[0035] Clause 27: The method of Clause 26, further including disposing a solder bump on the conductive pad such that the solder bump is electrically connected to the conductive pad.

[0036] Clause 28: The method of any one of Clauses 15–27, further including disposing the redistribution layer on a carrier after the redistribution layer has been disposed over the interconnect region and the electronic device.

[0037] Clause 29: The method of Clause 28, further including planarizing the second major surface of the substrate prior to disposing the conductive region or component adjacent to the second major surface of the substrate.

[0038] Clause 30: An implantable medical device including a housing and an integrated circuit package disposed within the housing, where the package includes an interposer and an electronic device coupled to the interposer at a device interface. The interposer includes a semiconductor substrate having a first major surface, a second major surface, and the device interface disposed on or in the first major surface; an interconnect region disposed on the first major surface of the substrate adjacent to the device interface, where the interconnect region includes an inorganic nonconductive layer disposed on the first major surface of the substrate and a patterned conductive layer disposed at least partially within the inorganic nonconductive layer, where the patterned conductive layer includes a conductive pad; and a conductive via disposed through the substrate between the conductive pad of the patterned conductive layer of the interconnect region and the second major surface of the substrate, where the conductive via electrically connects the conductive pad with a conductive region or component disposed adjacent to the second major surface of the substrate.

[0039] All headings provided herein are for the convenience of the reader and should not be used to limit the meaning of any text that follows the heading, unless so specified.

[0040] The terms “comprises” and variations thereof do not have a limiting meaning where these terms appear in the description and claims. Such terms will be understood to imply the inclusion of a stated step or element or group of steps or elements but not the exclusion of any other step or element or group of steps or elements.

[0041] In this application, terms such as "a," "an," and "the" are not intended to refer to only a singular entity but include the general class of which a specific example may be used for illustration. The terms "a," "an," and "the" are used interchangeably with the term "at least one." The phrases "at least one of" and "comprises at least one of" followed by a list refers to any one of the items in the list and any combination of two or more items in the list.

[0042] The phrases "at least one of" and "comprises at least one of" followed by a list refers to any one of the items in the list and any combination of two or more items in the list.

[0043] As used herein, the term "or" is generally employed in its usual sense including "and/or" unless the content clearly dictates otherwise.

[0044] The term "and/or" means one or all of the listed elements or a combination of any two or more of the listed elements.

[0045] As used herein in connection with a measured quantity, the term "about" refers to that variation in the measured quantity as would be expected by the skilled artisan making the measurement and exercising a level of care commensurate with the objective of the measurement and the precision of the measuring equipment used. Herein, "up to" a number (e.g., up to 50) includes the number (e.g., 50).

[0046] Also herein, the recitations of numerical ranges by endpoints include all numbers subsumed within that range as well as the endpoints (e.g., 1 to 5 includes 1, 1.5, 2, 2.75, 3, 3.80, 4, 5, etc.).

[0047] These and other aspects of the present disclosure will be apparent from the detailed description below. In no event, however, should the above summaries be construed as limitations on the claimed subject matter, which subject matter is defined solely by the attached claims, as may be amended during prosecution. The details of one or more aspects of the disclosure are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the techniques described in this disclosure will be apparent from the description and drawings, and from the claims.

BRIEF DESCRIPTION OF DRAWINGS

[0048] FIG. 1 is a schematic cross-section view of one embodiment of an integrated circuit package.

[0049] FIG. 2 is a schematic top plan view of the integrated circuit package of FIG. 1.

[0050] FIG. 3 is a schematic cross-section view of a portion of an interconnect region and via of the integrated circuit package of FIG. 1.

[0051] FIG. 4 is a schematic view of one embodiment of an implantable medical device that includes the integrated circuit package of FIG. 1.

[0052] FIGS. 5A–G are schematic cross-section views of one embodiment of a method of forming the integrated circuit package of FIG. 1, where FIG. 5A is a schematic cross-section view of an interconnect region disposed on a first major surface of a semiconductor substrate of an interposer; FIG 5B is a schematic cross-section view of additional inorganic nonconductive sublayers and patterned conductive layers of the interconnect region disposed on the semiconductor substrate; FIG. 5C is a schematic cross-section view of a device interface disposed on or in the first major surface of the substrate; FIG. 5D is a schematic cross-section view of an electronic device coupled to the substrate at the device interface; FIG. 5E is a schematic cross-section view of a redistribution layer over the interconnect region, the device interface, and the device; FIG. 5F is a schematic cross-section of a carrier disposed on the redistribution layer; and FIG. 5G is a schematic cross-section view of one or more conductive vias disposed through the substrate.

DETAILED DESCRIPTION

[0053] In general, the present disclosure provides various embodiments of an integrated circuit package that includes an interposer and an electronic device coupled to the interposer at a device interface. The interposer includes a semiconductor substrate and an interconnect region disposed on a first major surface of the substrate adjacent to the device interface that is disposed on or in the first major surface of the substrate. The interconnect region can include an inorganic nonconductive layer disposed on the first major surface of the substrate and a patterned conductive layer disposed at least partially within the inorganic nonconductive layer. A conductive via can be disposed through the substrate between a conductive pad of the patterned conductive layer of the interconnect region and a second major surface of the substrate. The conductive via can electrically connect the conductive pad with a conductive region or component such as a conductive pad that is disposed adjacent to the second major surface of the substrate.

[0054] In some currently available electronic packages, cracking can occur in inorganic nonconductive layers that contact vias that extend through a substrate of the package. In particular, cracking can occur at a junction between the via and the redistribution layer that is disposed on the substrate and over the electronic device (e.g., die). Such cracking can in turn lead to current leakage and degradation of electronic signals from the package.

[0055] One or more embodiments of integrated circuit packages described herein can exhibit various advantages over these currently-available packages. For example, an active interposer can be utilized as a substrate for the package, where the interposer includes one or more interconnect regions or structures disposed adjacent to a device interface (e.g., cavity) of the substrate. Such interconnect regions can include one or more inorganic nonconductive layers and one or more patterned conductive layers disposed at least partially within the inorganic nonconductive layers. At least one of the patterned conductive layers can include a conductive pad or pads that can be electrically connected to a conductive via that extends through the substrate between the conductive pad and a second major surface of the substrate. A conductive region or component (e.g., conductive pad) disposed adjacent to the second major surface of the substrate can be electrically connected to the conductive pad or pads of the patterned conductive layer of the interconnect region by the via. Although not wishing to be bound by any particular theory, the one or more inorganic nonconductive layers of the interposer can provide additional rigidity and stiffness to the patterned conductive layers that can help prevent flexing of the patterned conductive layers that may cause cracking of the nearby inorganic nonconductive layer and lead to leakage of current within the package.

[0056] FIGS. 1–3 are various views of one embodiment of an integrated circuit package 10. The package 10 includes an interposer 12 and an electronic device 14 coupled to the interposer at a device interface 16. The interposer 12 includes a semiconductor substrate 18 having a first major surface 20, a second major surface 22, and the device interface 16 (FIG. 5C) disposed on or in the first major surface. The interposer 12 further includes an interconnect region or structure 24 disposed on the first major surface 20 of the substrate 18 adjacent to the device interface 16, where the interconnect region includes an inorganic nonconductive layer 26 disposed on the first major surface of the substrate and a patterned conductive layer 28 disposed at least partially within the inorganic nonconductive layer. The patterned conductive layer 28 includes a conductive pad 30. Further, the interposer 12

includes a conductive via 32 disposed through the substrate 18 between the conductive pad 30 of the patterned conductive layer 28 of the interconnect region 24 and the second major surface 22 of the substrate, where the conductive via electrically connects the conductive pad with a conductive region or component 34 disposed adjacent to the second major surface of the substrate, or otherwise electrically connects (or provides an electrical connection between) the interconnect region and the second major surface of the substrate/interposer.

[0057] The interposer 12 of the package 10 can include any suitable interposer 12. Although depicted as including a single interposer 12, the package 10 can include any suitable number of interposers.

[0058] Further, the package 10 can include any suitable electronic device 14. Further, the package 10 can include any suitable number of devices 14 disposed in any suitable arrangement or array. In one or more embodiments, one or more electronic devices 14 can be disposed in a cavity 36 (serving as the device interface) of the substrate 18. Although depicted as including one device 14 per cavity 36, in one or more embodiments, two or more devices can be disposed within a single cavity. In one or more embodiments, one or more devices 14 can be disposed in the cavity 36 such that the device is completely within the cavity. For example, each device 14 can have a device height measured in a direction orthogonal to the first major surface 20 of the substrate 18 that is no greater than a height of the cavity 36 within which the device is disposed. In one or more embodiments, the device height of one or more devices 14 can be greater than the height of the cavity 36 within which the respective device is disposed.

[0059] The package 10 can include any suitable type of device 14. In one or more embodiments, the device 14 can include one or more high-voltage dies that can be utilized, e.g., in an implantable medical device (see, e.g., implantable medical device 100 of FIG. 4). As used herein, the term "high-voltage die" refers to an electronic component or device that is operable with a potential greater than about 50 V across any two electrical terminals or contacts of the component. Such high-voltage components may be further operable at DC voltages greater than about 100 V, and even further may be operable at DC voltages greater than about 500 V, 1000 V, 1600 V, 3000 V and even greater, perhaps in the tens of thousands or more volts. In one or more embodiments, the package 10 can include one or more devices 14 that include low-voltage dies. In one or more embodiments, the one or

more devices 14 can include one or more field effect transistors (FETs), metal oxide semiconductors (MOS), MOSFETs, insulated gate bipolar junction transistors (IGBT), thyristors, bipolar transistors, diodes, MOS-controlled thyristors, resistors, capacitors, etc. In one or more embodiments, two or more devices 14 can be arranged in a stacked relationship.

[0060] The interposer 12 of the package 10 can include any suitable substrate 18. Further, the substrate 18 can include any suitable material, e.g., metallic, polymeric, or inorganic materials and combinations thereof. In one or more embodiments, the substrate 18 can be a nonconductive or dielectric substrate that provides electrical isolation between various conductors, vias, dies, etc. In one or more embodiments, the substrate 18 can be a semiconductor substate that includes one or more semiconductor materials, e.g., silicon. In one or more embodiments, such semiconductor substrate 18 can be doped using any suitable dopant.

[0061] For convenience and without intending to be limiting, FIG. 1 depicts the substrate 18 as a monolithic (i.e., single) layer. In one or more embodiments, the substrate 18 can include any suitable number of layers, where the layers can be formed from the same or different materials. Further, the substrate 18 can have any suitable dimensions. For example, the substrate 18 can have any suitable thickness as measured in a direction orthogonal to the first major surface 20 of the substrate. Further, the substrate 18 can be formed using any suitable technique.

[0062] Disposed on or in the first major surface 20 of the substrate 18 is the device interface 16. The package 10 can include any suitable device interface 16, e.g., a ball grid array, one or more conductive pads, a wire bond frame, etc. As shown in FIGS. 1, 5C, 5D, the device interface 16 includes the cavity 36 that is disposed in the first major surface 20 of the substate 18. The device interface 16 is configured to facilitate attachment of the electronic device 14 to the interposer 12 and/or electrically couple the electronic device 14 to at least one of the interconnect region 24 or a redistribution layer 76 using any suitable technique.

[0063] The interconnect region or structure 24 of the interposer 12 is disposed on or in the first major surface 20 of the substrate 18 adjacent to the device interface (e.g., cavity 36). The interconnect region 24 can be a single layer or layers. In one or more embodiments, the interconnect region 24 can be an interconnect structure having a first interconnect

region (i.e., region 24) and a second interconnect region 60 as is further described herein. In one or more embodiments, such interconnect structure can include a third interconnect region 72 and a fourth interconnect region 74 (FIG. 2). The interconnect region or structure 24 can include any suitable number of regions.

[0064] The interconnect region 24 can include one or more inorganic nonconductive layers 26 and one or more patterned conductive layers 28 each disposed at least partially in the one or more inorganic nonconductive layers. As shown in FIG. 1, the interconnect region 24 includes the inorganic nonconductive layer 26 and the patterned conductive layer 28 disposed at least partially within the inorganic nonconductive layer. The interconnect region 24 as shown in FIG. 1 includes a single inorganic nonconductive layer 26 and a single patterned conductive layer 28 for clarity. Such interconnect region 24 is shown in in greater detail in FIG. 3, which is a schematic cross-section view of the interconnect region and a portion of the conductive via 32.

[0065] The inorganic nonconductive layer 26 can include any suitable material or materials, e.g., polyimide, bismaleimide triazine, polybenzoxazole, photoresist, glass, quartz, sapphire, etc. In one or more embodiments, the inorganic nonconductive layer 26 can include an electrically insulative material. In one or more embodiments, the inorganic nonconductive layer 26 can include an oxide, e.g., silicon dioxide, aluminium oxide, hafnium oxide, tantalum oxide, zirconium oxide, and other suitable metal or inorganic oxides. In one or more embodiments, the inorganic nonconductive layer 26 can include a nitride, e.g., silicon nitride, silicon oxynitride, and other suitable metal or inorganic nitrides.

[0066] Further, the inorganic nonconductive layer 26 can have any suitable dimensions. In one or more embodiments, the inorganic nonconductive layer 26 can include two or more layers or sublayers, and each sublayer can include the same or different materials. For example, as shown in FIG. 3, the inorganic nonconductive layer 26 can include a first sublayer 56–1, a second sublayer 56–2, a third sublayer 56–3, a fourth sublayer 56–4, and a fifth sublayer 56–5 (collectively sublayers 56). The sublayers 56 can be disposed using any suitable technique. In one or more embodiments, the sublayers 56 can be laminated together to form the inorganic nonconductive layer 26. Although depicted as including five sublayers 56, the inorganic nonconductive layer 26 can include any suitable number of sublayers.

[0067] The inorganic nonconductive layer 26 can be formed using any suitable technique. In one or more embodiments, the inorganic nonconductive layer 26 can be formed on the first major surface 20 of the substrate 18. In one or more embodiments, the inorganic nonconductive layer 26 can be formed separately and then connected to the first major surface 20 of the substrate 18, e.g., by laminating layer to the substrate.

[0068] The interconnect region 24 can also include any suitable elements or components, e.g., one or more vias 58 (FIG. 3) that extend between one or more of the patterned conductive layers 28 and that electrically connect the conductive layers to each other or to one or more elements or components external to the interconnect region.

[0069] Disposed at least partially within the inorganic nonconductive layer 26 is the patterned conductive layer 28. In one or more embodiments, the patterned conductive layer 28 can be disposed entirely within the inorganic nonconductive layer 26. The interconnect region 24 can include any suitable number of patterned conductive layers disposed on or within the inorganic nonconductive layer 26. As shown in FIG. 3, the interconnect region 24 includes a first patterned conductive layer 28–1, a second patterned conductive layer 28–2, a third patterned conductive layer 28–3, a fourth patterned conductive layer 28–4, and a fifth patterned conductive layer 28–5 (collectively patterned conductive layers 28).

[0070] Each patterned conductive layer 28 can include any suitable type of conductive layer or layers, e.g., one or more redistribution or routing layers. The patterned conductive layer 28 can be electrically connected to additional patterned conductive layers, devices, conductive pads, etc. using one or more conductive vias 58 that are disposed within the inorganic nonconductive layer 26. The patterned conductive layer 28 can include any suitable conductive material and be formed using any suitable technique as is further described herein. Further, patterned conductive layer 28 can be disposed at least partially within or on the inorganic nonconductive layer 26 or sublayers 56 using any suitable technique or techniques.

[0071] The patterned conductive layer 28 can be disposed in any suitable location within the inorganic nonconductive layer 26. In one or more embodiments, the patterned conductive layer 28 can be disposed between two sublayers 56, at least partially within a sublayer, or entirely within a sublayer.

[0072] As mentioned herein, the patterned conductive layer 28 can include one or more conductive pads 30. The conductive pads 30 can be any suitable portion or portions of the patterned conductive layer 28. Each conductive pad 30 can take any suitable shape and have any suitable dimensions.

[0073] The package 10 can include any suitable number of interconnect regions. For example, as shown in FIG. 1, the package 10 includes the second interconnect region 60 disposed on the first major surface 20 of the substrate 18 adjacent to the device interface 16. The second interconnect region 60 includes an inorganic nonconductive layer 62 disposed on the first major surface 20 of the substrate 18 and a patterned conductive layer 64 disposed at least partially within the inorganic nonconductive layer. In one or more embodiments, the inorganic nonconductive layer 62 of the second interconnect region 60 can be a portion of the inorganic nonconductive layer 28 of the interconnect region 24. Further, in one or more embodiments, the patterned conductive layer 64 can be a portion of the patterned conductive layer 28 of the interconnect region 24. The patterned conductive layer 64 includes a second conductive pad 66.

[0074] The second interconnect region 60 also includes a second conductive via 68 disposed through the substrate 18 between the second conductive pad 66 of the patterned conductive layer 64 of the second interconnect region 60 and the second major surface 22 of the substrate 18. The second conductive via 68 electrically connects the second conductive pad 66 with a second conductive region or component 70 disposed adjacent to the second major surface 22 of the substrate 18, or otherwise electrically connects (or provides an electrical connection between) the second interconnect region 60 and the second major surface of the substrate/interposer.

[0075] The second interconnect region 60 can be formed using any suitable technique, e.g., the same techniques described herein that can be utilized to form interconnect region 24. In one or more embodiments, the first and second interconnect regions 24, 60 can be formed as a single interconnect region and then isolated using any suitable technique. If isolated, the first and second interconnect regions 24, 60 can be electrically connected using any suitable technique. In one or more embodiments, the first and second interconnect regions 24, 60 are portions of a single interconnect region or structure.

[0076] The package 10 can include one or more additional interconnect regions. For example, as shown in FIG. 2, the package 10 includes the third interconnect region 72 and

the fourth interconnect region 74. The interconnect regions 24, 60, 72, 74 can each be disposed adjacent to the device interface 16. The third and fourth interconnect regions 72, 74 can be any suitable interconnect region, e.g., similar to interconnect region 24.

[0077] The interposer 12 can further include one or more conductive vias 32 that are disposed through the substrate 18 and extend between the one or more conductive pads 30 of the patterned conductive layer 28 of the interconnect region 24 and the second major surface 22 of the substrate 18. The package 10 can include any suitable number of conductive vias 32. In one or more embodiments, each interconnect region 24, 60, 72, 74 can be electrically connected to the second major surface of the substrate 18/interposer 12, e.g., to conductive regions or components disposed on the second major surface 22 of the substrate 18 using one or more conductive vias that are formed through the substrate. The conductive via 32 can include any suitable conductive material. Further, the conductive via 32 can take any suitable shape and have any suitable dimensions. And the conductive via 32 can be formed using any suitable technique as is further described herein.

[0078] The conductive via 32 can electrically connect one or more conductive pads 30 of the interconnect region 24 and one or more conductive regions or components 34 disposed adjacent to the second major surface 22 of the substrate 18 using any suitable technique. In one or more embodiments, the conductive via 32 extends through a portion of a thickness of the inorganic nonconductive layer 26 of the interconnect region 24 as shown in FIG. 1. In one or more embodiments, the conductive via 32 extends through a portion, but not all, of the thickness of the inorganic nonconductive layer 26 of the interconnect region 24. In one or more embodiments, the conductive via 32 extends to the conductive pad 30 within the inorganic nonconductive layer 26 of the interconnect region 24. Any suitable conductive region or component 34 can be electrically connected by the conductive via 32 to one or more conductive pads 30, e.g., at least one of a conductive pad, solder bump, ball grid array, landing pad, capacitor, resistor, passive integrated capacitor system, logic circuit, analog circuit, crystals, oscillator, accelerometer, and any suitable active or passive component, etc. In one or more embodiments, the conductive region or component 34 can include one or more solder bumps 35 as shown in FIG. 1.

[0079] In one or more embodiments, the package 10 can further include a redistribution layer 76 disposed over the interconnect regions 24, 60, and the electronic device 14. In one or more embodiments, the redistribution layer 76 can be disposed over the device interface

16. In one or more embodiments, the redistribution layer 76 can be disposed on one or more of the interconnect regions 24, 60. In one or more embodiments, one or more passivation layers 42 can be disposed over at least one of the interconnect region 24, second interconnect region 60, third interconnect region 72, fourth interconnect region 74, or the device interface 16. Further, the redistribution layer 76 can be disposed on at least a portion of the passivation layer 42.

[0080] The redistribution layer 76 can include any suitable redistribution layer. As shown in FIG. 1, the redistribution layer 76 includes one or more dielectric layers 78 and one or more patterned conductive layers 80 disposed on or at least partially within the dielectric layers 78. The dielectric layer 78 can include any suitable nonconductive material. For convenience and without intending to be limiting, the illustration depicts dielectric layer 78 as a monolithic (single) layer. In one or more embodiments, the dielectric layer 78 can include two or more layers or sublayers, and each layer can include the same or different materials. Further, the dielectric layer 78 can have any suitable dimensions and can be formed using any suitable technique or techniques.

[0081] Disposed within the dielectric layer 78 is the patterned conductive layer 80. The redistribution layer 76 can include any suitable number of patterned conductive layers. The patterned conductive layer 80 can include any suitable type of conductive layer, e.g., one or more redistribution layers. The patterned conductive layer 78 can be electrically connected to additional patterned conductive layers, devices, conductive pads, etc. using one or more conductive vias that are disposed within the dielectric layer 78. The patterned conductive layers 80 can be formed using any suitable technique, e.g., the same techniques described herein regarding the patterned conductive layer 28 of interconnect region 24.

[0082] The redistribution layer 76 can be electrically connected to one or more of the interconnect regions 24, 60, 72, 74 using any suitable technique. Further, the redistribution layer 76 can be electrically connected to the electronic device 14 using any suitable technique. For example, one or more conductive vias 82 can electrically connect the electronic device 14 to the redistribution layer 76. Further, one or more electronic devices or components (not shown) can be disposed adjacent to an upper surface 84 of the redistribution layer 76 can be electrically connected to the redistribution layer using any suitable technique. Any suitable device or component can be disposed on the upper surface 84 of the redistribution layer 76, e.g., one or more of the devices or components

described herein regarding electronic device 14. In one or more embodiments, one or more conductive pads 44 can be disposed on the redistribution layer 76 using any suitable technique. Such conductive pads 44 can be electrically connected to one or more of the patterned conductive layers 80 of the redistribution layer 76 using any suitable technique.

[0083] The various embodiments of integrated circuit packages described herein can be utilized in any suitable electronic system. For example, one or more embodiments of integrated circuit packages described herein can be utilized in an IMD, ICD, IPG (e.g., a pacemaker such as a leadless pacemaker), insertable cardiac monitor, implantable diagnostic monitor, deep brain stimulator, implantable neurostimulator, injectable neurostimulator, implantable ventricular assist device, etc.

[0084] FIG. 4 is a schematic plan view of one embodiment of an implantable medical device (IMD) 100. The IMD 100 includes a housing 102 and electronic components 104 disposed within the housing. The electronic components 104 can include any suitable electronic devices, e.g., at least one of a capacitor, resistor, passive integrated capacitor system, logic circuit, analog circuit, crystal, accelerometer, RF circuit, antenna, transformer, connector, etc. In one or more embodiments, the electronic components 104 include the integrated circuit package 10. The integrated circuit package 10 can be electrically connected to other electronic components 104 using any suitable technique or techniques. Also disposed within the housing 102 of the IMD is a power source 106 that is electrically connected to the electronic components using any suitable technique or techniques. The power source 106 can include any suitable power source or combination of power sources, e.g., one or more batteries, capacitors, inductive-coupled energy devices, photovoltaic devices, betavoltaic devices, alphavoltaic devices, and thermo-electric devices.

[0085] Any suitable technique can be utilized to form the integrated circuit package 10 of FIGS. 1–3. For example, FIGS. 5A–G are various schematic cross-section views of one embodiment of a method 300 of forming the integrated circuit package 10. Although described in reference to the integrated circuit package 10 of FIGS. 1–3, the method 300 can be utilized to form any suitable integrated circuit package. Further, the method 300 is illustrated as including one electronic device 14; however, the method can be utilized to form integrated circuit packages that include two or more devices. In one or more

embodiments, the method 300 can be utilized to form two or more integrated circuit packages 10 simultaneously utilizing one or more wafers.

[0086] In FIG. 5A, the interconnect region 24 is disposed on the first major surface 20 of the semiconductor substrate 18 using any suitable technique. In one or more embodiments, at least a portion of the inorganic nonconductive layer 26 of the interconnect region 24 can be disposed on the first major surface 20 of the substrate 18 using any suitable technique, e.g., chemical vapor deposition, plasma enhanced chemical vapor deposition, thermal oxidation, physical vapor deposition, atomic layer deposition, molecular layer deposition, etc. In embodiments where the inorganic nonconductive layer 26 includes sublayers, the first sublayer 56–1 can be disposed on the substrate 18 as shown in FIG. 5A. Further, the patterned conductive layer 28 can be disposed on or at least partially within the inorganic nonconductive layer 26 using any suitable technique. For example, in one or more embodiments, a continuous conductive layer 28-1 can be disposed on or in the first sublayer 56–1 of the inorganic nonconductive layer 26 and can then be patterned using any suitable technique or techniques, e.g., photoresist application, photolithography, electroless plating, electroplating, chemical etching, dry etching, physical vapor deposition, etc. As shown in FIG. 5B, any suitable additional sublayers 56–2, 56–3, 56–4, 56–5 (FIG. 3) can be disposed on the first sublayer 56–1 using any suitable technique. Further, any suitable number of additional patterned conductive layers 28–2, 28–3, 28–4, and 28–5 (FIG. 3) can be disposed at least partially within the inorganic nonconductive layer 26 using any suitable technique. Although not shown, one or more of the patterned conductive layers 28 can be electrically connected using any suitable technique, e.g., one or more conductive vias can be disposed within the inorganic nonconductive layer 26 that extend between two or more patterned conductive layers 28.

[0087] As shown in FIG. 5C, the device interface 16 can be disposed on or in the first major surface 20 of the substrate 18 using any suitable technique. In one or more embodiments where the device interface 16 includes or is included in the cavity 36, such cavity can be disposed in the first major surface 20 of the substrate 18, e.g., by drilling, laser drilling, chemical etching, plasma etching, stamping, etc. Formation of the cavity 36 can define interconnect region 24, second interconnect region 60, third interconnect region 72, and fourth interconnect region 74 (FIGS. 1–2).

[0088] The optional passivation layer or layers 42 can be disposed over one or more of the interconnect regions 24, 60, 72, and 74 as shown in FIG. 5D using any suitable technique. Such passivation layer 42 can include any suitable nonconductive material. Further, the passivation layer 42 can be disposed over one or more recessed surfaces 38 of the cavity 36. In one or more embodiments, one or more passivation layers or encapsulants can be disposed on and around the electronic device 14 and within the cavity 36 using any suitable technique. Any suitable nonconductive material can be utilized for the passivation layers and encapsulants. Further, one or more electronic devices 14 can be coupled to the substrate 18 at the device interface 16 as shown in FIG. 5D using any suitable technique.

[0089] As shown in FIG. 5E, one or more redistribution layers 76 can be disposed over one or more of the interconnect regions 24, 60, 72, 74 and the electronic device 14 using any suitable technique. Further, any suitable technique can be utilized to electrically connect the redistribution layer 76 to the device 14 and the conductive pads 30, 66. In one or more embodiments, one or more conductive pads 44 can be disposed on the redistribution layer 76 using any suitable technique, wherein the redistribution layer is between the conductive pads 44 and the first major surface 20 of the substrate 18. Such conductive pads 44 can be electrically connected to the redistribution layer 76 using any suitable technique. In one or more embodiments, one or more solder bumps (not shown) can be disposed on the conductive pads 44 using any suitable technique.

[0090] A carrier 302 can be disposed on the redistribution layer 76 after the redistribution layer has been disposed over the interconnect regions 24, 60, 72, 74 and the electronic device 14 as shown in FIG. 5F using any suitable technique. Further, one or more portions of the second major surface 22 of the substrate 18 can be removed, e.g., by grinding and/or planarizing the substrate using any suitable technique. Such planarization occurs before the conductive region or components 34, 70 are disposed adjacent to the second major surface 22 of the substrate 18.

[0091] As shown in FIG. 5G, the carrier 302 can be removed, and one or more conductive vias 32, 68 can be disposed through the substrate 18 between the second major surface 22 of the substrate and the conductive pads 30, 66 of the patterned conductive layers 28, 64 of the interconnect regions 24, 60 suing any suitable technique. For example, in one or more embodiments, an opening or trench can be formed using any suitable technique or techniques (e.g., the same techniques described herein utilized to form the cavity 36), and

a conductive material can be disposed within the opening to form the conductive vias 32, 68. Additional conductive vias can be disposed through the substrate 18 that electrically connect conductive pads of the third and fourth interconnect regions 72, 74 and any additional interconnect regions to conductive regions or components disposed on the second major surface 22 of the substrate 18 using any suitable technique.

[0092] Further, the conductive region or components 34, 70 can be disposed adjacent to the second major surface 22 of the substrate 18 using any suitable technique as is also shown in FIG. 5E. The conductive region or components 34, 70 can be electrically connected to the conductive pads 30, 66 utilizing the conductive vias 32, 68.

[0093] It should be understood that various aspects disclosed herein may be combined in different combinations than the combinations specifically presented in the description and accompanying drawings. It should also be understood that, depending on the example, certain acts or events of any of the processes or methods described herein may be performed in a different sequence, may be added, merged, or left out altogether (e.g., all described acts or events may not be necessary to carry out the techniques). In addition, while certain aspects of this disclosure are described as being performed by a single module or unit for purposes of clarity, it should be understood that the techniques of this disclosure may be performed by a combination of units or modules associated with, for example, a medical device.

[0094] In one or more examples, the described techniques may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored as one or more instructions or code on a computer-readable medium and executed by a hardware-based processing unit. Computer-readable media may include computer-readable storage media, which corresponds to a tangible medium such as data storage media (e.g., RAM, ROM, EEPROM, flash memory, or any other medium that can be used to store desired program code in the form of instructions or data structures and that can be accessed by a computer).

[0095] Instructions may be executed by one or more processors, such as one or more digital signal processors (DSPs), general purpose microprocessors, application specific integrated circuits (ASICs), field programmable logic arrays (FPGAs), or other equivalent integrated or discrete logic circuitry. Accordingly, the term "processor" as used herein may refer to any of the foregoing structure or any other physical structure suitable for

implementation of the described techniques. Also, the techniques could be fully implemented in one or more circuits or logic elements.

WHAT IS CLAIMED IS:

1. An integrated circuit package comprising an interposer and an electronic device coupled to the interposer at a device interface, wherein the interposer comprises:

a semiconductor substrate comprising a first major surface, a second major surface, and the device interface disposed on or in the first major surface;

an interconnect region disposed on the first major surface of the substrate adjacent to the device interface, wherein the interconnect region comprises an inorganic nonconductive layer disposed on the first major surface of the substrate and a patterned conductive layer disposed at least partially within the inorganic nonconductive layer, wherein the patterned conductive layer comprises a conductive pad; and

a conductive via disposed through the substrate between the conductive pad of the patterned conductive layer of the interconnect region and the second major surface of the substrate, wherein the conductive via electrically connects the conductive pad with a conductive region or component disposed adjacent to the second major surface of the substrate.

2. The package of claim 1, wherein the interposer further comprises:

a second interconnect region disposed on the first major surface of the substrate adjacent to the device interface, wherein the second interconnect region comprises an inorganic nonconductive layer disposed on the first major surface of the substrate and a patterned conductive layer disposed at least partially within the inorganic nonconductive layer, wherein the patterned conductive layer comprises a second conductive pad; and

a second conductive via disposed through the substrate between the second conductive pad of the patterned conductive layer of the second interconnect region and the second major surface of the substrate, wherein the second conductive via electrically connects the second conductive pad with a second conductive region or component disposed adjacent to the second major surface of the substrate.

3. The package of claim 2, further comprising a redistribution layer disposed over the interconnect region, the second interconnect region, and the device, wherein the redistribution layer is electrically connected to the device and at least one of the conductive pad or the second conductive pad.

4. The package of any one of claims 1–3, wherein the conductive via extends through a portion of a thickness of the inorganic nonconductive layer of the interconnect region.

5. The package of claim 4, wherein the conductive via extends through a portion, but not all, of the thickness of the inorganic nonconductive layer of the interconnect region.

6. The package of claim 4, wherein the conductive via extends to the conductive pad within the inorganic nonconductive layer of the interconnect region.

7. A method of forming an integrated circuit package, comprising:

disposing an interconnect region on a first major surface of a semiconductor substrate of an interposer, wherein disposing the interconnect region comprises:

disposing an inorganic nonconductive layer on a first major surface of the substrate; and

disposing a patterned conductive layer at least partially within the inorganic nonconductive layer, wherein the patterned conductive layer comprises a conductive pad;

disposing a device interface on or in the first major surface of the substrate;

coupling an electronic device to the substrate at the device interface;

disposing a redistribution layer over the interconnect region and the device, wherein the redistribution layer is electrically connected to the device and the conductive pad;

disposing a conductive via through the substrate between a second major surface of the substrate and the conductive pad of the patterned conductive layer of the interconnect region; and

disposing a conductive region or component adjacent to the second major surface of the substrate and electrically connecting the conductive region or component to the conductive pad of the patterned conductive layer utilizing the conductive via.

8. The method of claim 7, wherein disposing the interconnect region further comprises:

disposing a second inorganic nonconductive layer on the patterned conductive layer; and

disposing a second patterned conductive layer at least partially within the second inorganic nonconductive layer.

9. The method of any one of claims 7–8, wherein the conductive via extends through a portion of a thickness of the inorganic nonconductive layer of the interconnect region.

10. The method of claim 9, wherein the conductive via extends through a portion, but not all, of the thickness of the inorganic nonconductive layer of the interconnect region.

11. The method of claim 9, wherein the conductive via extends to the conductive pad within the inorganic nonconductive layer of the interconnect region.

12. The method of any one of claims 7–11, further comprising disposing a conductive pad on the redistribution layer such that the redistribution layer is between the conductive pad and the first major surface of the substrate, wherein the conductive pad is electrically connected to the redistribution layer.

13. The method of any one of claims 7–12, further comprising disposing the redistribution layer on a carrier after the redistribution layer has been disposed over the interconnect region and the electronic device.

14. The method of claim 13, further comprising planarizing the second major surface of the substrate prior to disposing the conductive region or component adjacent to the second major surface of the substrate.

15. An implantable medical device comprising a housing and an integrated circuit package disposed within the housing, wherein the package comprises an interposer and an electronic device coupled to the interposer at a device interface, wherein the interposer comprises:

a semiconductor substrate comprising a first major surface, a second major surface, and the device interface disposed on or in the first major surface;

an interconnect region disposed on the first major surface of the substrate adjacent to the device interface, wherein the interconnect region comprises an inorganic nonconductive layer disposed on the first major surface of the substrate and a patterned conductive layer disposed at least partially within the inorganic nonconductive layer, wherein the patterned conductive layer comprises a conductive pad; and

a conductive via disposed through the substrate between the conductive pad of the patterned conductive layer of the interconnect region and the second major surface of the substrate, wherein the conductive via electrically connects the conductive pad with a conductive region or component disposed adjacent to the second major surface of the substrate.

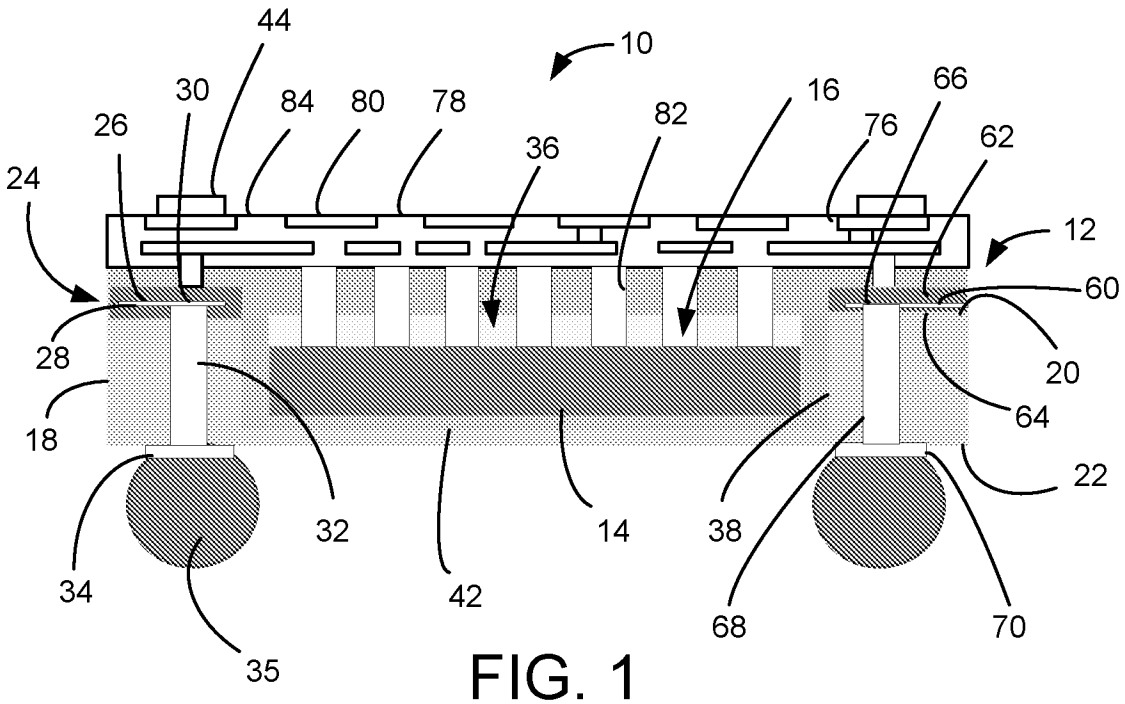

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FIG. 1

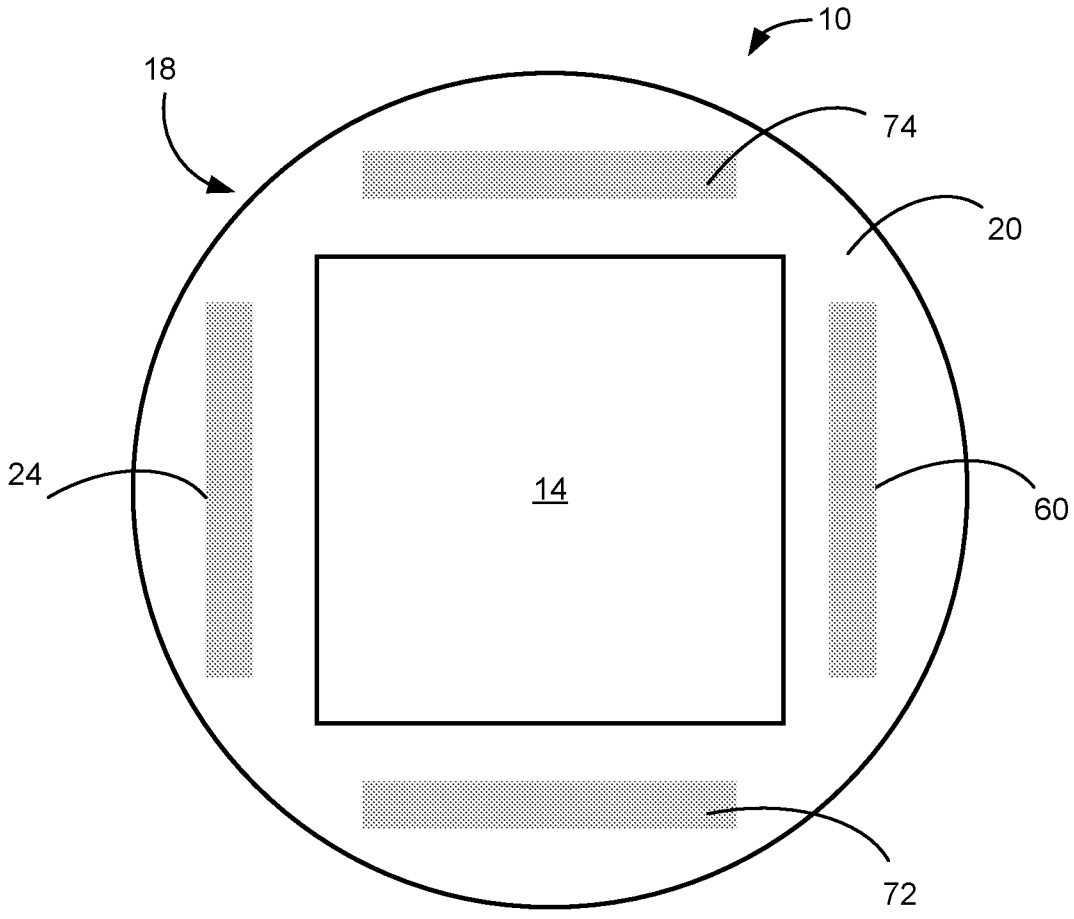

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FIG. 2

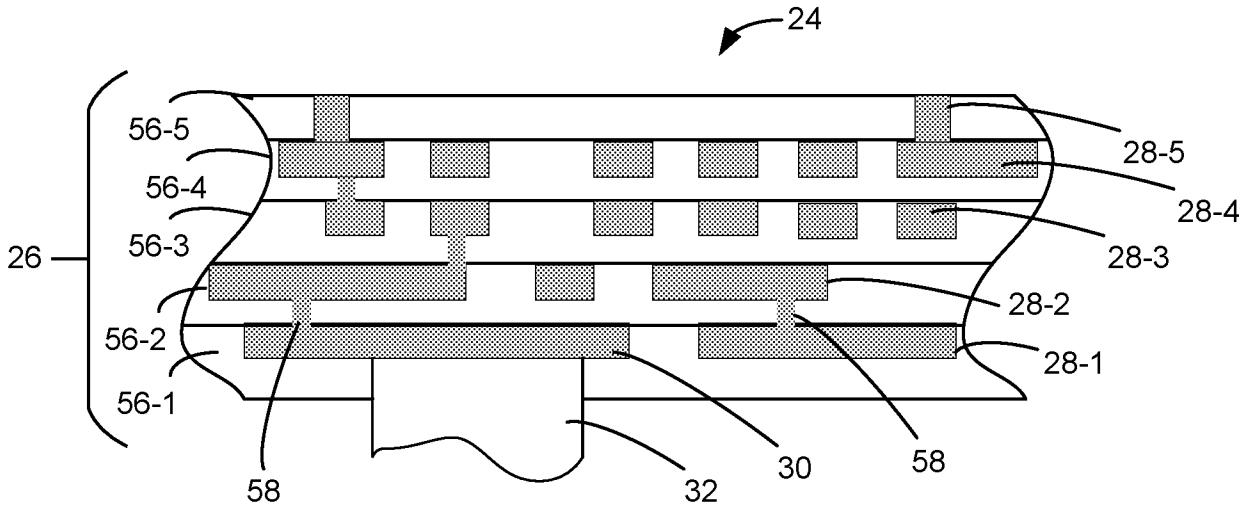

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28-2
28-1

FIG. 3

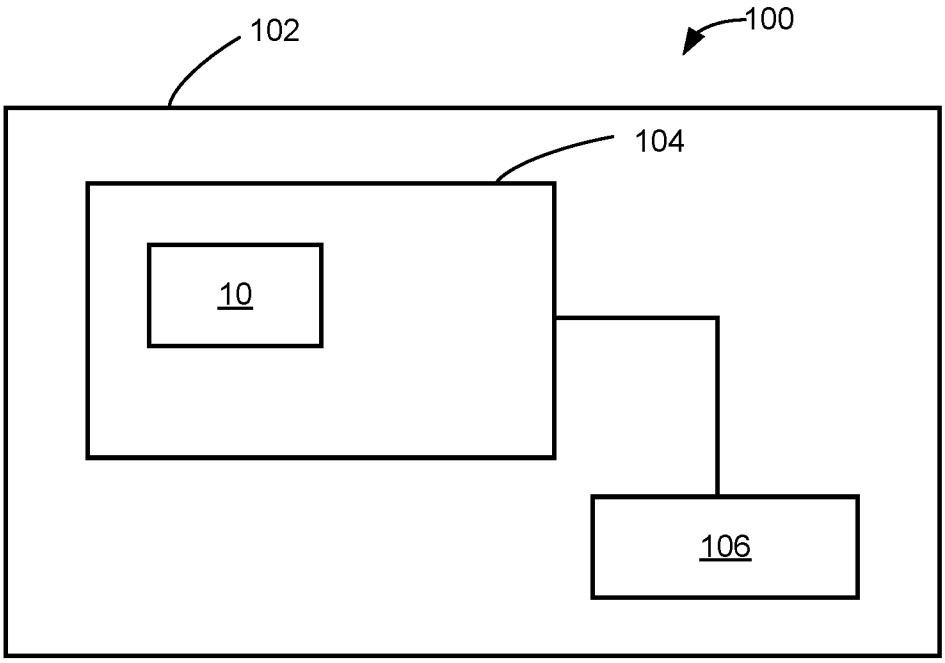

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FIG. 4

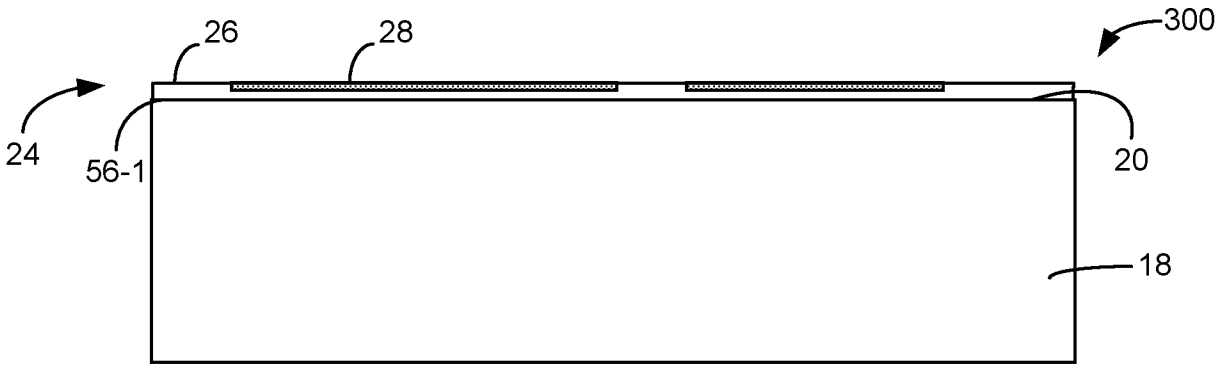


FIG. 5A

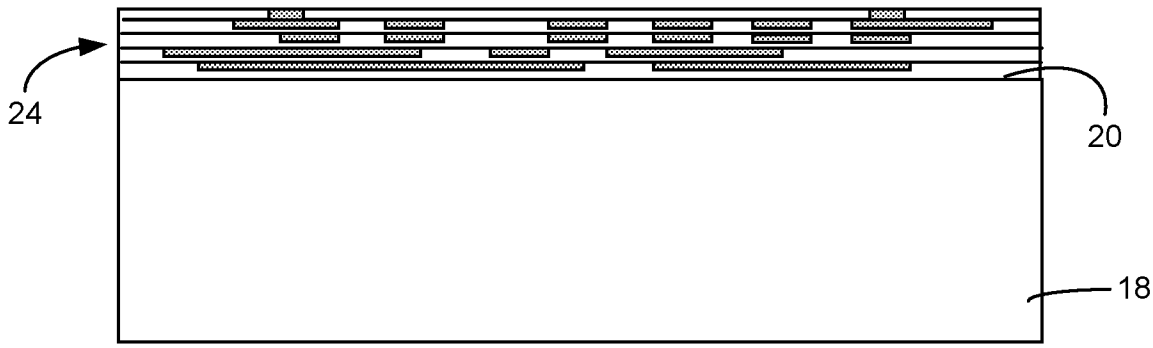


FIG. 5B

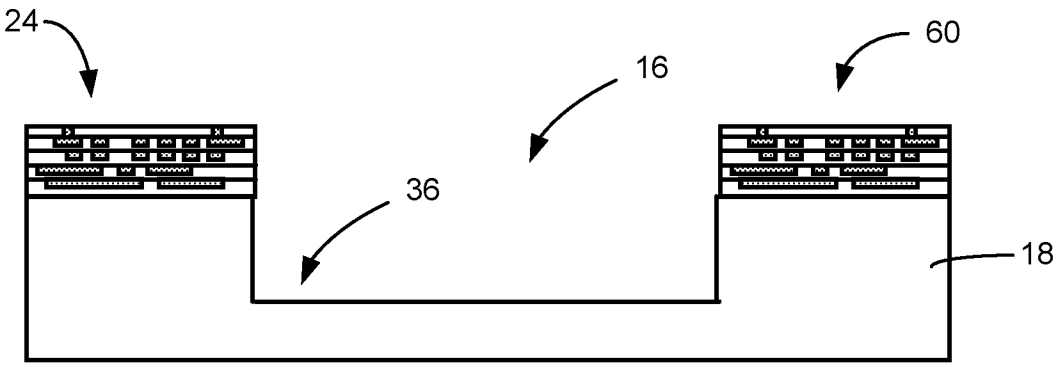


FIG. 5C

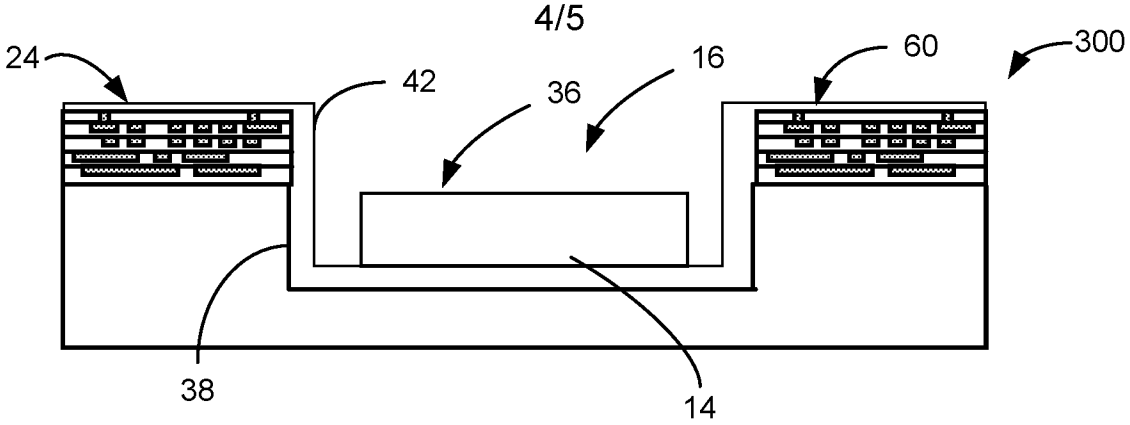


FIG. 5D

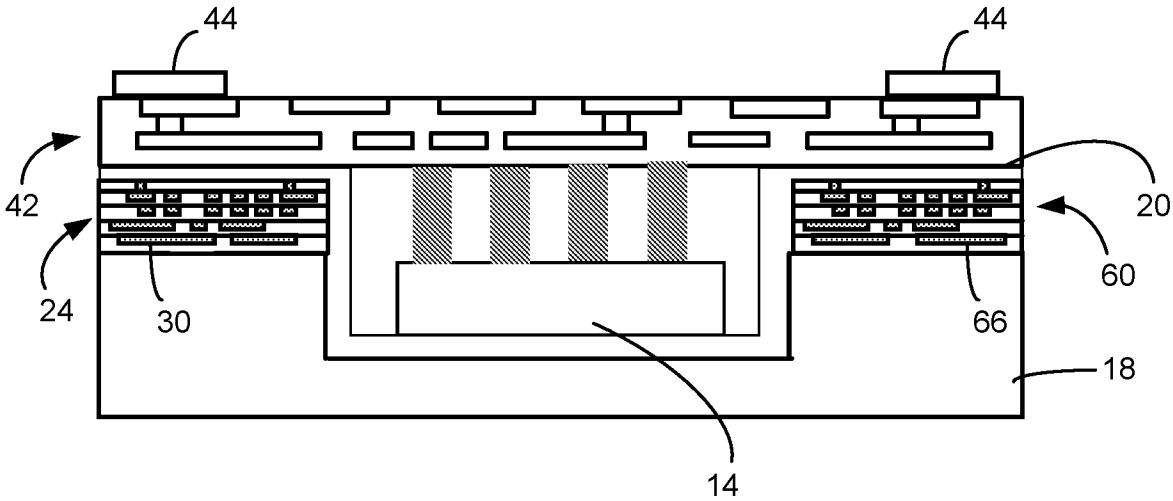


FIG. 5E

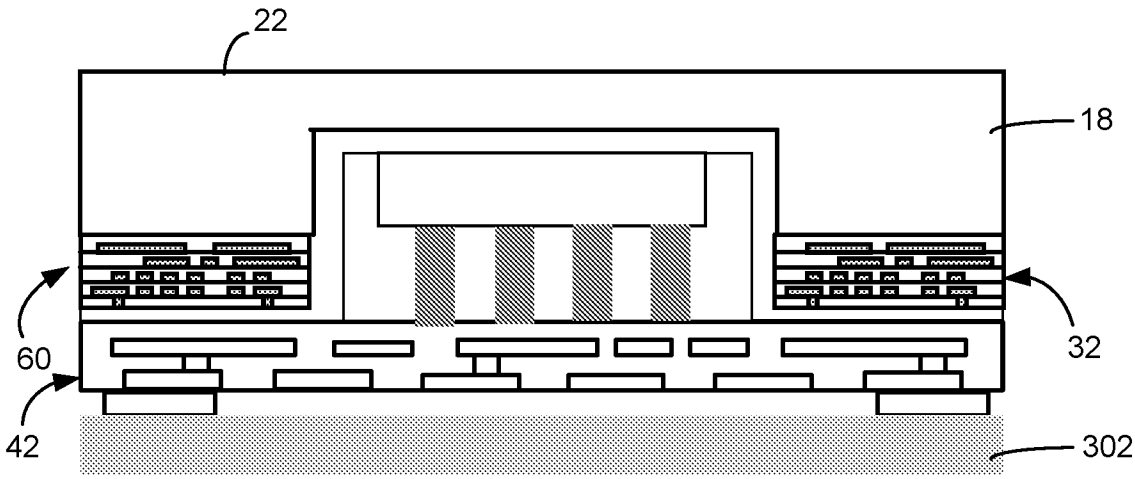


FIG. 5F

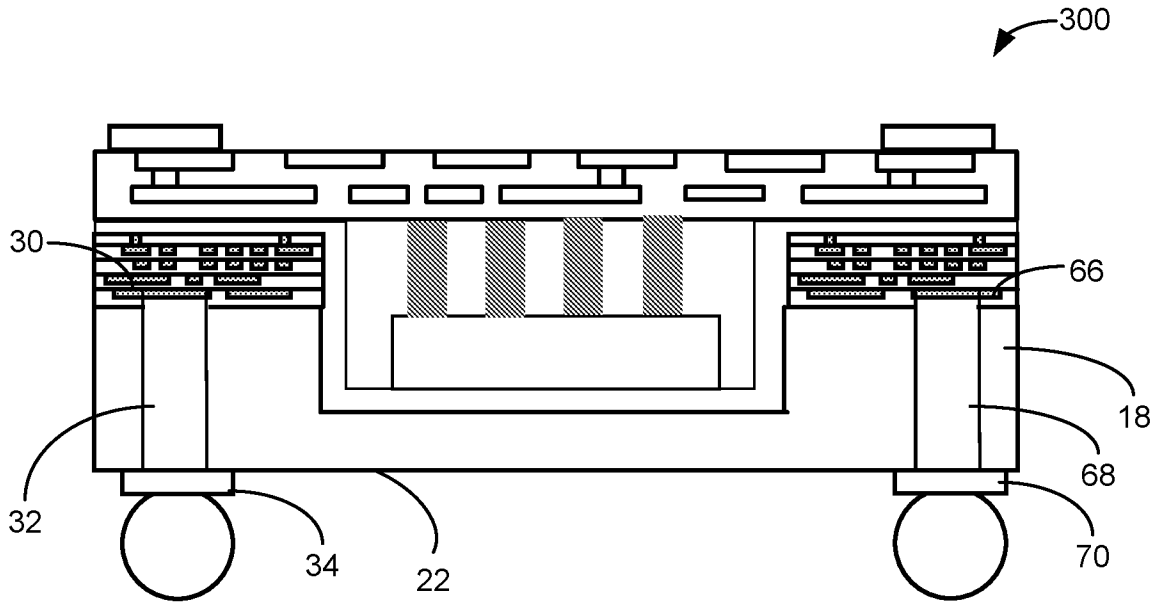


FIG. 5G

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2024/056337

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L23/538 H01L23/498 H01L23/13 H01L23/14
ADD. H01L23/48

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/162308 A1 (KRAFT JOCHEN [AT] ET AL) 11 June 2015 (2015-06-11) paragraph [0038] - paragraph [0039] paragraph [0042] - paragraph [0046] figures 1-5 -----	1-15
X	US 2023/061861 A1 (CHANG JEN-YUAN [TW]) 2 March 2023 (2023-03-02) paragraph [0016] paragraph [0027] - paragraph [0028] paragraph [0057] paragraph [0059] paragraph [0064] - paragraph [0073] figures 1, 3B -----	1-12,14, 15
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[x] Further documents are listed in the continuation of Box C.

[x] See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 September 2024	22/10/2024

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Rodríguez San S., H

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2024/056337

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2022/077085 A1 (HENSCHEL MARK E [US] ET AL) 10 March 2022 (2022-03-10) paragraph [0102] figure 5 -----	15
A	US 2020/058567 A1 (KIM CHUNHO [US] ET AL) 20 February 2020 (2020-02-20) paragraph [0072] figure 4 -----	15

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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		WO 2020036902 A1	20-02-2020