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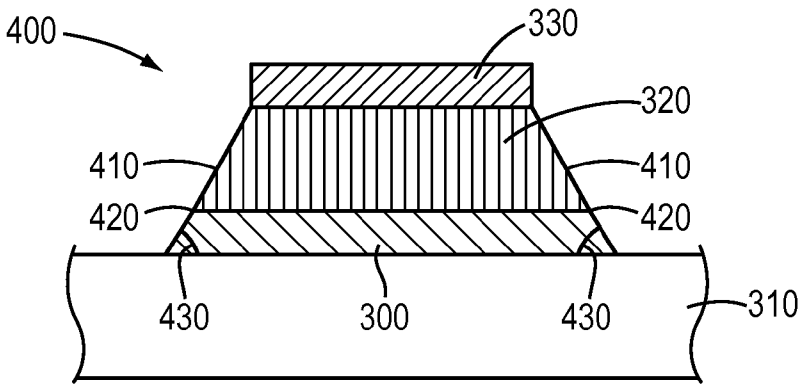

FIG. 4

(57) Abstract: In various embodiments, electronic devices such as thin-film transistors and/or touch-panel displays incorporate electrodes and/or interconnects featuring a conductor layer and, disposed above or below the conductor layer, a capping layer and/or a barrier layer comprising an alloy of Cu and one or more refractory metal elements selected from the group consisting of Ta, Nb, Mo, W, Zr, Hf, Re, Os, Ru, Rh, Ti, V, Cr, and Ni.

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COPPER-ALLOY BARRIER LAYERS AND CAPPING LAYERS FOR METALLIZATION IN ELECTRONIC DEVICES

Related Application

This application claims the benefit of and priority to U.S. Provisional Patent Application No. 61/831,865, filed June 6, 2013, the entire disclosure of which is hereby incorporated herein by reference.

Technical Field

[0001] In various embodiments, the present invention relates to the metallization of electronic devices such as flat panel displays and touch panel displays, in particular to capping and barrier layers for such metallization.

Background

[0002] Flat panel displays have rapidly become ubiquitous in various markets, and are now commonly utilized in a variety of appliances, televisions, computers, cellular phones, and other electronic devices. One example of a commonly used flat panel display is the thin film transistor (TFT) liquid crystal display (LCD), or TFT-LCD. A typical TFT-LCD contains an array of TFTs each controlling the emission of light from a pixel or sub-pixel of an LCD. Figure 1A depicts the cross-section of a conventional TFT 100 as might be found in a TFT-LCD. As shown, the TFT 100 includes a gate electrode 105 formed on a glass substrate 110. A gate insulator 115 electrically insulates the gate electrode 105 from overlying conductive structures. An active layer 120, typically composed of amorphous silicon, conducts charge between a source electrode 125 and a drain electrode 130, under the electrical control of gate

electrode 105, and the conducted charge controls the operation of the pixel or sub-pixel connected thereto (not shown). A source/drain insulator 132 electrically isolates the source electrode 125 from the drain electrode 130 and protectively seals the TFT 100. As shown, each of the gate electrode 105, source electrode 125, and drain electrode 130 typically include a barrier metal layer 135 and a metal conductor layer 140 thereover. The barrier 135 provides good adhesion between the conductor 140 and the underlying glass and/or silicon and reduces or prevents diffusion therebetween.

[0003] Over time, LCD panel sizes have increased and TFT-based pixel sizes have decreased, placing increasingly high demands on the conductors within the TFT-LCD structure. In order to decrease the resistance in the conductors and thereby increase electrical signal propagation speeds in the TFT-LCD, manufacturers are now utilizing low-resistivity metals such as copper (Cu) for the conductors 140 within the display. Metals such as molybdenum (Mo), titanium (Ti), or molybdenum-titanium alloys (Mo-Ti) have been utilized for barriers 135 underlying Cu conductors 140; however, these metals suffer from one or more deficiencies that limit the performance of the TFT-LCD and/or present difficulties in the fabrication process for the TFT-LCD. For example, some conventional barriers 135 have relatively high resistivity and therefore compromise the overall conductivity of the electrodes. Furthermore, as shown in Figure 1B, during the etching of electrodes such as gate electrodes 105, either a residue 145 (of one or both electrode materials) or etch discontinuities 150, e.g., stepped or nonlinear profiles (caused by non-uniform etch rates of the two different electrode materials), may result.

[0004] Similarly, touch-panel displays are becoming more common in electronic devices, and they may even be utilized in tandem with TFT-LCDs. A typical touch-panel display includes an array of sensors arranged in rows and columns and that sense a touch (or close proximity) of, e.g., a finger, via capacitive coupling. Figure 2A schematically depicts an exemplary sensor array 200 for a touch-panel display that includes multiple conductive column sensors 210 that are interconnected to form

columns 220, as well as multiple conductive row sensors 230 that are interconnected to form rows 240. The sensors 210, 230 are formed over a substrate 250 and are electrically coupled to a processor 260 that both senses the changes in capacitive coupling that represent "touches" and provides these signals to other electronic components within a device (e.g., a computer or mobile computing device that incorporates a touch screen). The sensors 210, 230 may be formed of a transparent conductor such as indium tin oxide (ITO), and the substrate 250 may be glass or any other suitably rigid (and/or transparent) support material.

[0005] Figure 2B depicts a magnified perspective view of a point within the sensor array 200 where the interconnected column sensors 210 intersect the interconnected row sensors 230. In order to avoid electrical shorting between the columns 220 and the rows 240 (see Figure 2A), the interconnections between column sensors 210 are isolated from the underlying or overlying row sensors 230. For example, as shown in Figure 2B, an insulator layer 270 is disposed between the column 220 of column sensors 210 and a conductive interconnect (or "bridge") 280 that electrically connects the row sensors 230 within a row 240. As shown in Figure 2C, the interconnects 280 are typically composed of an Al conductive layer 290 with an overlying barrier or capping layer 295 that is typically composed of Mo, Ti, or Mo-Ti. The capping layer 295 helps to prevent diffusion from the conductive layers 290 and protects conductive layers 290 from corrosion during processing and product use. The capping layer 295 may also improve adhesion to overlying layers. However, as described above for TFT-LCDs, the metals conventionally used for the capping layer 295 metals from one or more deficiencies that limit performance and/or present difficulties in the fabrication process. For example, the capping layers 295 may have relatively high resistivity and therefore compromise the overall conductivity of the interconnects 280, degrading electrical performance. Furthermore, as shown in Figure 2D, during the etching of the interconnects 280, either a residue 296 (of one or both of conductive layer 290 or capping layer 295) or etch discontinuities 297, e.g., stepped or

nonlinear profiles (caused by non-uniform etch rates of the two different materials), may result.

[0006] In view of the foregoing, there is a need for barrier and/or capping metal layers for electronic devices such as TFT-LCDs and touch-panel displays that provide excellent adhesion to underlying substrates, prevent diffusion of the conductor metal into nearby layers, protect the conductor metal from corrosion, and are uniformly etched with the underlying or overlying conductor metals during fabrication.

Summary

[0007] In accordance with various embodiments of the present invention, electronic devices such as TFT-LCDs and touch-panel displays, and the metallic interconnects and electrodes therein, are fabricated utilizing capping and/or barrier layers including or consisting essentially of an alloy of Cu and one or more refractory metal elements such as tantalum (Ta), niobium (Nb), Mo, tungsten (W), zirconium (Zr), hafnium (Hf), rhenium (Re), osmium (Os), ruthenium (Ru), rhodium (Rh), Ti, vanadium (V), chromium (Cr), or nickel (Ni). The one or more refractory elements may be present in the alloy at weight concentrations of 1-50 percent. In an exemplary implementation, alloy barrier layers are formed directly on substrate layers such as glass and/or silicon-based layers, and conductor layers including or consisting essentially of highly conductive metals such as Cu, silver (Ag), aluminum (Al), or gold (Au) are formed thereover to form the various electrodes in a TFT structure. In another exemplary implementation, highly conductive metals such as Cu, Ag, Al, and/or Au are utilized as conductive interconnects in a touch-panel display and are capped with protecting capping layers that include or consist essentially of an alloy of Cu and one or more refractory metal elements such as Ta, Nb, Mo, W, Zr, Hf, Re, Os, Ru, Rh, Ti, V, Cr, or Ni. The one or more refractory elements may be present in the alloy at weight concentrations of 1-50 percent (hereafter weight %).

[0008] Surprisingly, even though the barrier and capping layers are predominantly Cu, the presence of the refractory-metal alloying element(s) discourages or even prevents the diffusion of Cu into nearby layers, e.g., an underlying silicon layer, approximately as well as pure Mo barrier layers when utilized with Cu conductor layers. While not wishing to be bound by any particular theory or mechanism for this phenomenon, the refractory-metal alloying element may react with atoms of the silicon layer to form silicide regions that occupy grain boundaries in the barrier or capping metal and thereby prevent diffusion of Cu into the substrate (or other adjoining layer) along the grain boundaries, which would otherwise be fast diffusion paths.

[0009] In various embodiments, the barrier and/or capping layer includes or consists essentially of an alloy of Cu with (i) Ta and Cr, (ii) Ta and Ti, or (iii) Nb and Cr. For example, the barrier and/or capping layer may include (i) 1 weight % - 12 weight % Ta (preferably approximately 5 weight % Ta) and 1 weight % - 5 weight % Cr (preferably approximately 2 weight % Cr), (ii) 1 weight % - 12 weight % Ta (preferably approximately 5 weight % Ta) and 1 weight % - 5 weight % Ti (preferably approximately 2 weight % Ti), or (iii) 1 weight % - 10 weight % Nb (preferably approximately 5 weight % Nb) and 1 weight % - 5 weight % Cr (preferably approximately 2 weight % Cr). Furthermore, when utilized in conjunction with highly conductive conductor layers such as Cu to form electrodes and/or interconnects, the barrier and/or capping layer and the conductor layer exhibit substantially identical etch rates in preferred etchants such as a PAN etch, i.e., a mixture of phosphoric acid, acetic acid, and nitric acid, which may be mixed with water and may be heated to elevated temperatures. Thus, etch-related residue and discontinuities are minimized or eliminated via use of the barrier and/or capping layers in accordance with preferred embodiments of the present invention.

[0010] In an aspect, embodiments of the invention feature a thin-film transistor that includes or consists essentially of a substrate and an electrode. The substrate may include or consist essentially of silicon and/or glass. The electrode includes or consists

essentially of (i) disposed over or on the substrate, a barrier layer that includes, consists essentially of, or consists of an alloy of Cu and one or more refractory metal elements selected from the list consisting of Ta, Nb, Mo, W, Zr, Hf, Re, Os, Ru, Rh, Ti, V, Cr, and Ni, and (ii) disposed over or on the barrier layer, a conductor layer that includes, consists essentially of, or consists of Cu, Ag, Al, and/or Au.

[0011] Embodiments of the invention may include one or more of the following in any of a variety of different combinations. The substrate may include, consist essentially of, or consist of glass. The substrate may include, consist essentially of, or consist of silicon, e.g., amorphous silicon. The barrier layer may include, consist essentially of, or consist of an alloy of Cu, Ta, and Cr. The barrier layer may include, consist essentially of, or consist of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Cr, and the balance Cu. The barrier layer may include, consist essentially of, or consist of approximately 5 weight % Ta, approximately 2 weight % Cr, and the balance Cu. The barrier layer may include, consist essentially of, or consist of 5 weight % Ta, 2 weight % Cr, and the balance Cu. The barrier layer may include, consist essentially of, or consist of approximately 2 weight % Ta, approximately 1 weight % Cr, and the balance Cu. The barrier layer may include, consist essentially of, or consist of 2 weight % Ta, 1 weight % Cr, and the balance Cu.

[0012] The barrier layer may include, consist essentially of, or consist of an alloy of Cu, Ta, and Ti. The barrier layer may include, consist essentially of, or consist of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Ti, and the balance Cu. The barrier layer may include, consist essentially of, or consist of approximately 5 weight % Ta, approximately 2 weight % Ti, and the balance Cu. The barrier layer may include, consist essentially of, or consist of 5 weight % Ta, 2 weight % Ti, and the balance Cu.

[0013] The barrier layer may include, consist essentially of, or consist of an alloy of Cu, Nb, and Cr. The barrier layer may include, consist essentially of, or consist of 1 weight % - 10 weight % Nb, 1 weight % - 5 weight % Cr, and the balance Cu. The

barrier layer may include, consist essentially of, or consist of approximately 5 weight % Nb, approximately 2 weight % Cr, and the balance Cu. The barrier layer may include, consist essentially of, or consist of 5 weight % Nb, 2 weight % Cr, and the balance Cu.

[0014] The electrode may include a sidewall including, consisting essentially of, or consisting of (a) an exposed portion of the barrier layer, (b) an exposed portion of the conductor layer, and (c) an interface between the exposed portion of the barrier layer and the exposed portion of the conductor layer. The sidewall of the electrode may be substantially, or even entirely, free of discontinuities notwithstanding the interface. The substrate may be substantially, or even entirely, free of Cu diffusion from the barrier layer. The barrier layer may include, consist essentially of, or consist of a plurality of crystalline grains separated by grain boundaries. At least one of the grain boundaries may include a particulate therein. The particulate may include, consist essentially of, or consist of a reaction product of silicon and at least one of the refractory metal elements.

[0015] In another aspect, embodiments of the invention feature a method of forming an electrode of a thin-film transistor. A substrate is provided. The substrate may include, consist essentially of, or consist of silicon and/or glass. A barrier layer is deposited over the substrate, and a conductor layer is deposited over the barrier layer. The barrier layer includes, consists essentially of, or consists of an alloy of Cu and one or more refractory metal elements selected from the group consisting of Ta, Nb, Mo, W, Zr, Hf, Re, Os, Ru, Rh, Ti, V, Cr, and Ni. The conductor layer includes, consists essentially of, or consists of Cu, Ag, Al, and/or Au. A mask layer is formed over the barrier layer, and the mask layer is patterned to reveal a portion of the conductor layer. A remaining portion of the mask layer may at least partially define a shape of the electrode. An etchant is applied to remove portions of the conductor layer and the barrier layer not masked by the patterned mask layer, thereby forming a sidewall of the electrode. The sidewall includes, consists essentially of, or consists of (a) an exposed portion of the barrier layer, (b) an exposed portion of the conductor layer, and (c) an interface between the exposed portion of the barrier layer and the exposed portion of the

conductor layer. The sidewall is substantially, or even entirely, free of discontinuities notwithstanding the interface.

[0016] Embodiments of the invention may include one or more of the following in any of a variety of different combinations. The mask layer may include, consist essentially of, or consist of photoresist. The etchant may include, consist essentially of, or consist of a mixture of phosphoric acid, acetic acid, nitric acid, and water. The etchant may include, consist essentially of, or consist of 50-60 weight % phosphoric acid, 15-25 weight % acetic acid, 3-5 weight % nitric acid, and the balance water. The etchant may include, consist essentially of, or consist of 50 weight % phosphoric acid, 25 weight % acetic acid, 3 weight % nitric acid, and the balance water. The remaining portion of the patterned mask layer may be removed, e.g., after the etchant is applied. The barrier layer may include, consist essentially of, or consist of a plurality of crystalline grains separated by grain boundaries. The substrate may include, consist essentially of, or consist of silicon. The electrode may be annealed at a temperature sufficient to form a particulate within at least one of the grain boundaries (e.g., between 200 °C and 700 °C, or between 300 °C and 500 °C). The particulate may include, consist essentially of, or consist of a reaction product of silicon and at least one of the refractory metal elements (e.g., a refractory metal silicide). The substrate may include, consist essentially of, or consist of glass or amorphous silicon.

[0017] The barrier layer may include, consist essentially of, or consist of an alloy of Cu, Ta, and Cr. The barrier layer may include, consist essentially of, or consist of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Cr, and the balance Cu. The barrier layer may include, consist essentially of, or consist of approximately 5 weight % Ta, approximately 2 weight % Cr, and the balance Cu. The barrier layer may include, consist essentially of, or consist of 5 weight % Ta, 2 weight % Cr, and the balance Cu. The barrier layer may include, consist essentially of, or consist of approximately 2 weight % Ta, approximately 1 weight % Cr, and the balance Cu. The barrier layer may include, consist essentially of, or consist of 2 weight % Ta, 1 weight % Cr, and the

balance Cu.

[0018] The barrier layer may include, consist essentially of, or consist of an alloy of Cu, Ta, and Ti. The barrier layer may include, consist essentially of, or consist of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Ti, and the balance Cu. The barrier layer may include, consist essentially of, or consist of approximately 5 weight % Ta, approximately 2 weight % Ti, and the balance Cu. The barrier layer may include, consist essentially of, or consist of 5 weight % Ta, 2 weight % Ti, and the balance Cu.

[0019] The barrier layer may include, consist essentially of, or consist of an alloy of Cu, Nb, and Cr. The barrier layer may include, consist essentially of, or consist of 1 weight % - 10 weight % Nb, 1 weight % - 5 weight % Cr, and the balance Cu. The barrier layer may include, consist essentially of, or consist of approximately 5 weight % Nb, approximately 2 weight % Cr, and the balance Cu. The barrier layer may include, consist essentially of, or consist of 5 weight % Nb, 2 weight % Cr, and the balance Cu.

[0020] In yet another aspect, embodiments of the invention feature a touch-panel display that includes or consists essentially of a substrate, a plurality of conductive touch-panel row sensors, a plurality of conductive touch-panel column sensors, and an interconnect. The row sensors are disposed over the substrate and arranged in lines extending along a first direction. The column sensors are disposed over the substrate and arranged in lines extending along a second direction and intersecting the lines of the row sensors. The interconnect is disposed at a point of intersection between a line of row sensors and a line of column sensors, and the interconnect electrically connects two column sensors or two row sensors. The interconnect includes, consists essentially of, or consists of (i) a conductor layer that includes, consists essentially of, or consists of Cu, Ag, Al, and/or Au, and (ii) disposed over or on the conductor layer, a capping layer that includes, consists essentially of, or consists of an alloy of Cu and one or more refractory metal elements selected from the list consisting of Ta, Nb, Mo, W, Zr, Hf, Re, Os, Ru, Rh, Ti, V, Cr, and Ni.

[0021] Embodiments of the invention may include one or more of the following in any of a variety of different combinations. The interconnect may extend over or under a row sensor and electrically connect two column sensors. An insulating layer may be disposed between the interconnect and the row sensor and may electrically insulate the interconnect and the row sensor. The interconnect may extend over or under a column sensor and electrically connect two row sensors. An insulating layer may be disposed between the interconnect and the column sensor and may electrically insulate the interconnect and the column sensor. The substrate may include, consist essentially of, or consist of an insulating material, e.g., glass. The row sensors and/or the column sensors may include, consist essentially of, or consist of a substantially transparent conductive material, e.g., indium tin oxide.

[0022] The capping layer may include, consist essentially of, or consist of an alloy of Cu, Ta, and Cr. The capping layer may include, consist essentially of, or consist of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Cr, and the balance Cu. The capping layer may include, consist essentially of, or consist of approximately 5 weight % Ta, approximately 2 weight % Cr, and the balance Cu. The capping layer may include, consist essentially of, or consist of 5 weight % Ta, 2 weight % Cr, and the balance Cu. The capping layer may include, consist essentially of, or consist of approximately 2 weight % Ta, approximately 1 weight % Cr, and the balance Cu. The capping layer may include, consist essentially of, or consist of 2 weight % Ta, 1 weight % Cr, and the balance Cu.

[0023] The capping layer may include, consist essentially of, or consist of an alloy of Cu, Ta, and Ti. The capping layer may include, consist essentially of, or consist of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Ti, and the balance Cu. The capping layer may include, consist essentially of, or consist of approximately 5 weight % Ta, approximately 2 weight % Ti, and the balance Cu. The capping layer may include, consist essentially of, or consist of 5 weight % Ta, 2 weight % Ti, and the balance Cu.

[0024] The capping layer may include, consist essentially of, or consist of an alloy of Cu, Nb, and Cr. The capping layer may include, consist essentially of, or consist of 1 weight % - 10 weight % Nb, 1 weight % - 5 weight % Cr, and the balance Cu. The capping layer may include, consist essentially of, or consist of approximately 5 weight % Nb, approximately 2 weight % Cr, and the balance Cu. The capping layer may include, consist essentially of, or consist of 5 weight % Nb, 2 weight % Cr, and the balance Cu.

[0025] The interconnect may include a sidewall that includes, consists essentially of, or consists of (a) an exposed portion of the capping layer, (b) an exposed portion of the conductor layer, and (c) an interface between the exposed portion of the capping layer and the exposed portion of the conductor layer. The sidewall of the electrode may be substantially, or even entirely free of discontinuities notwithstanding the interface. The capping layer may include, consist essentially of, or consist of a plurality of crystalline grains separated by grain boundaries. At least one of the grain boundaries may include a particulate therein. The particulate may include, consist essentially of, or consist of an agglomeration (e.g., an aggregation of atoms coming together via diffusion) of one or more of the refractory metal elements. One or more of the grain boundaries may contain a larger concentration of the refractory metal element(s) than the bulk volumes of the grains of the capping layer.

[0026] In another aspect, embodiments of the invention feature a method of forming an interconnect of a touch-panel display. A structure including or consisting essentially of a substrate, a plurality of conductive touch-panel row sensors, and a plurality of conductive touch-panel column sensors is provided. The row sensors are disposed over the substrate and arranged in lines extending along a first direction. The column sensors are disposed over the substrate and arranged in lines extending along a second direction and intersecting the lines of the row sensors. An insulator layer is deposited at least at a point of intersection between a line of row sensors and a line of column sensors. A conductor layer is deposited over the insulator layer, and a capping

layer is deposited over or on the conductor layer. The conductor layer includes, consists essentially of, or consists of Cu, Ag, Al, and/or Au. The capping layer includes, consists essentially of, or consists of an alloy of Cu and one or more refractory metal elements selected from the group consisting of Ta, Nb, Mo, W, Zr, Hf, Re, Os, Ru, Rh, Ti, V, Cr, and Ni. A mask layer is formed over the capping layer. The mask layer is patterned to reveal a portion of the capping layer. A remaining portion of the mask layer may at least partially define a shape of the interconnect. An etchant is applied to remove portions of the capping layer and the conductor layer not masked by the patterned mask layer, thereby forming a sidewall of the interconnect. The sidewall includes, consists essentially of, or consists of (a) an exposed portion of the capping layer, (b) an exposed portion of the conductor layer, and (c) an interface between the exposed portion of the capping layer and the exposed portion of the conductor layer. The sidewall is substantially, or even entirely, free of discontinuities notwithstanding the interface.

[0027] Embodiments of the invention may include one or more of the following in any of a variety of different combinations. The mask layer may include, consist essentially of, or consist of photoresist. The etchant may include, consist essentially of, or consist of a mixture of phosphoric acid, acetic acid, nitric acid, and water. The etchant may include, consist essentially of, or consist of 50-60 weight % phosphoric acid, 15-25 weight % acetic acid, 3-5 weight % nitric acid, and the balance water. The etchant may include, consist essentially of, or consist of 50 weight % phosphoric acid, 25 weight % acetic acid, 3 weight % nitric acid, and the balance water. Any remaining portion of the patterned mask layer may be removed. The capping layer may include, consist essentially of, or consist of a plurality of crystalline grains separated by grain boundaries. The interconnect may be annealed at a temperature sufficient to form a particulate within at least one of the grain boundaries (e.g., between 200 °C and 700 °C, or between 300 °C and 500 °C). The particulate may include, consist essentially of, or consist of an agglomeration of at least one of the refractory metal elements. The substrate may include, consist essentially of, or consist of an insulating material, e.g.,

glass. The row sensors and column sensors may include, consist essentially of, or consist of a substantially transparent conductive material, e.g., indium tin oxide.

[0028] The capping layer may include, consist essentially of, or consist of an alloy of Cu, Ta, and Cr. The capping layer may include, consist essentially of, or consist of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Cr, and the balance Cu. The capping layer may include, consist essentially of, or consist of approximately 5 weight % Ta, approximately 2 weight % Cr, and the balance Cu. The capping layer may include, consist essentially of, or consist of 5 weight % Ta, 2 weight % Cr, and the balance Cu. The capping layer may include, consist essentially of, or consist of approximately 2 weight % Ta, approximately 1 weight % Cr, and the balance Cu. The capping layer may include, consist essentially of, or consist of 2 weight % Ta, 1 weight % Cr, and the balance Cu.

[0029] The capping layer may include, consist essentially of, or consist of an alloy of Cu, Ta, and Ti. The capping layer may include, consist essentially of, or consist of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Ti, and the balance Cu. The capping layer may include, consist essentially of, or consist of approximately 5 weight % Ta, approximately 2 weight % Ti, and the balance Cu. The capping layer may include, consist essentially of, or consist of 5 weight % Ta, 2 weight % Ti, and the balance Cu.

[0030] The capping layer may include, consist essentially of, or consist of an alloy of Cu, Nb, and Cr. The capping layer may include, consist essentially of, or consist of 1 weight % - 10 weight % Nb, 1 weight % - 5 weight % Cr, and the balance Cu. The capping layer may include, consist essentially of, or consist of approximately 5 weight % Nb, approximately 2 weight % Cr, and the balance Cu. The capping layer may include, consist essentially of, or consist of 5 weight % Nb, 2 weight % Cr, and the balance Cu.

[0031] These and other objects, along with advantages and features of the present

invention herein disclosed, will become more apparent through reference to the following description, the accompanying drawings, and the claims. Furthermore, it is to be understood that the features of the various embodiments described herein are not mutually exclusive and may exist in various combinations and permutations. As used herein, the terms "approximately" and "substantially" mean ±10%, and in some embodiments, ±5%. The term "consists essentially of" means excluding other materials that contribute to function, unless otherwise defined herein. Nonetheless, such other materials may be present, collectively or individually, in trace amounts. For example, a structure consisting essentially of multiple metals will generally include only those metals and only unintentional impurities (which may be metallic or non-metallic) that may be detectable via chemical analysis but do not contribute to function. As used herein, "consisting essentially of at least one metal" refers to a metal or a mixture of two or more metals but not compounds between a metal and a non-metallic element or chemical species such as oxygen or nitrogen (e.g., metal nitrides or metal oxides); such non-metallic elements or chemical species may be present, collectively or individually, in trace amounts, e.g., as impurities. As used herein, "columns" and "rows" refer to elements arranged in different directions (and that may intersect), and are otherwise arbitrary unless otherwise noted; i.e., an arrangement of elements may be a row or a column, regardless of its orientation in space or within a device. As used herein, "substrate" or "base layer" refers to a support member (e.g., a semiconductor substrate such as silicon, GaAs, GaN, SiC, sapphire, or InP, or a platform including or consisting essentially of another material, e.g., an insulating material such as glass) with or without one or more additional layers disposed thereon, or to the one or more additional layers themselves.

Brief Description of the Drawings

[0032] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the

invention. In the following description, various embodiments of the present invention are described with reference to the following drawings, in which:

Figure 1A is a schematic cross-section of a thin-film transistor for a liquid crystal display;

Figure 1B is a schematic cross-section of an etched conventional TFT electrode;

Figure 2A is a plan-view schematic of the sensor array of a touch-panel display;

Figure 2B is a magnified perspective view of a portion of the sensor array of Figure 2A;

Figure 2C is a schematic cross-section of the sensor-array portion of Figure 2B;

Figure 2D is a schematic cross-section, along a plane perpendicular to that of Figure 2C, of the sensor-array portion of Figure 2B depicting an etched conventional interconnect;

Figures 3 and 4 are schematic cross-sections of a TFT electrode during fabrication in accordance with various embodiments of the invention;

Figures 5 and 6 are schematic cross-section of an interconnect for a touch-panel display in accordance with various embodiments of the invention;

Figures 7A and 7B are Auger spectra graphs of mutual diffusion of Cu and Si without a diffusion barrier therebetween;

Figures 8A and 8B are Auger spectra graphs of mutual diffusion of Cu and Si between a Si layer and a Cu-alloy capping or barrier layer in accordance with various embodiments of the invention;

Figures 9A – 9C are plan-view micrographs of the surface of a Cu-alloy capping or barrier layer as deposited (Figure 9A), after annealing at 300 ºC (Figure 9B), and after annealing at 500 ºC (Figure 9C), in accordance with various embodiments of the invention;

Figures 10A and 10B are plan-view micrographs taken via scanning electron microscopy (Figure 10A) and transmission electron microscopy (Figure 10B) of an annealed Cu-alloy capping or barrier layer on Si, in accordance with various embodiments of the invention; and

Figure 11 depicts corrosion levels after environmental corrosion testing of samples of pure Mo, pure Cu, CuTaCr alloy, and CuNbCr alloy in accordance with various embodiments of the invention.

Detailed Description

[0033] Figure 3 depicts an initial step in the fabrication of a TFT gate electrode in accordance with embodiments of the present invention. As shown, a barrier layer 300 is deposited on a substrate 310 (e.g., a glass or silicon substrate) by, e.g., sputtering or other physical deposition process. A conductor layer 320 is subsequently deposited on the barrier layer 300 by, e.g., sputtering or other physical deposition process. Typically the thickness of the barrier layer 300 will be between approximately 5% and approximately 25% (e.g., approximately 10%) of the thickness of conductor layer 320. For example, the thickness of the barrier layer 300 may be approximately 50 nm, and the thickness of the conductor layer 320 may be approximately 500 nm. A mask layer 330 (e.g., photoresist) is formed over the conductor layer 320 and patterned by conventional photolithography.

[0034] As shown in Figure 4, a gate electrode 400 is then fabricated by etching the portions of the conductor layer 320 and barrier layer 300 not covered by the mask layer 330, preferably in a single-step wet etch. A wet etchant (e.g., a PAN etch) is utilized to etch away the metal layers at substantially the same rates, resulting in sidewalls 410 that are substantially smooth and/or linear and that are substantially free of any discontinuity (e.g., a stepped or nonlinear profile) at an interface 420 between the conductor layer 320 and barrier layer 300. The wet etchant may include or consist essentially of, for example, a PAN etch including or consisting essentially of 50-60

weight % phosphoric acid, 15-25 weight % acetic acid, 3-5 weight % nitric acid, and the balance DI water. Some specific examples are provided in the table below. In one preferred embodiment, the wet etchant includes or consists essentially of 50 weight % phosphoric acid, 25 weight % acetic acid, 3 weight % nitric acid, and the balance (22 weight %) DI water.

	phosphoric acid, H3PO4 (wt%)	nitric acid, HNO3 (wt%)	acetic acid, CH3COOH (wt%)	DI water, balance (wt%)
etchant 1	50	5	15	30
etchant 2	60	5	20	15
etchant 3	50	3	25	22

[0035] After etching, the substrate 310 (as well as the electrode 400) is preferably substantially free of etch residue of one or both of the conductor layer 320 and the barrier layer 300 in regions proximate the gate electrode 400. In accordance with various embodiments of the invention, the wet-etching process is performed at room temperature. The wet etchant may be sprayed on the substrate 310, or the substrate 310 may be partially or completely immersed in the wet etchant. The wet-etching process may be performed as a batch (i.e., multiple-substrate) process or as a single-substrate process. In preferred embodiments, after etching the sidewalls 410 form an angle 430 with the surface of the underling substrate 310 of between approximately 50° and approximately 70°, e.g., approximately 60°. After etching, the mask layer 330 may be removed by conventional means, e.g., acetone, a commercial photoresist stripping agent, and/or exposure to an oxygen plasma.

[0036] Figure 5 depicts an initial step in the fabrication of a touch-panel sensor interconnect in accordance with embodiments of the present invention. As shown, a conductive layer 500 is deposited over a sensor 510 (e.g., a row or column sensor that may be composed of a transparent conductor such as ITO) on a substrate 520 (e.g., a glass or silicon substrate) by, e.g., sputtering or other physical deposition process. A capping layer 530 is subsequently deposited on the conductive layer 500 by, e.g., sputtering or other physical deposition process. Typically the thickness of the capping layer 530 will be between approximately 5% and approximately 25% (e.g.,

approximately 10%) of the thickness of conductive layer 500. For example, the thickness of the capping layer 530 may be approximately 50 nm, and the thickness of the conductive layer 500 may be approximately 500 nm. A mask layer 540 (e.g., photoresist) is formed over the capping layer 530 and patterned by conventional photolithography.

[0037] As shown in Figure 6, an interconnect 600 is then fabricated by etching the portions of the capping layer 530 and conductive layer 500 not covered by the mask layer 540, preferably in a single-step wet etch. A wet etchant (e.g., a PAN etch) is utilized to etch away the metal layers at substantially the same rates, resulting in sidewalls 610 that are substantially smooth and/or linear and that are substantially free of any discontinuity (e.g., a stepped or nonlinear profile) at an interface 620 between the capping layer 530 and conductive layer 500. The wet etchant may include or consist essentially of, for example, a PAN etch including or consisting essentially of 50-60 weight % phosphoric acid, 15-25 weight % acetic acid, 3-5 weight % nitric acid, and the balance DI water. In one preferred embodiment, the wet etchant includes or consists essentially of 50 weight % phosphoric acid, 25 weight % acetic acid, 3 weight % nitric acid, and the balance (22 weight %) DI water.

[0038] After etching, the substrate 520 and electrode 510 (as well as the interconnect 600) are preferably substantially free of etch residue of one or both of the capping layer 530 and the conductive layer 500 in regions proximate the interconnect 600. In accordance with various embodiments of the invention, the wet-etching process is performed at room temperature. The wet etchant may be sprayed on the substrate 520, or the substrate 520 may be partially or completely immersed in the wet etchant. The wet-etching process may be performed as a batch (i.e., multiple-substrate) process or as a single-substrate process. In preferred embodiments, after etching the sidewalls 610 form an angle 630 with the surface of the underling substrate 520 of between approximately 50° and approximately 70°, e.g., approximately 60°. After etching, the mask layer 330 may be removed by conventional means, e.g., acetone, a commercial

photoresist stripping agent, and/or exposure to an oxygen plasma.

[0039] Barrier layers 300 and capping layers 530 in accordance with various embodiments of the invention also serve as effective diffusion barriers for metallic layers that include or consist essentially of, e.g., Cu, Ag, Al, or Au. Specifically, the alloying element(s) within the barrier layer 300 and/or capping layer 530 substantially prevent diffusion of a conductor layer material (e.g., Cu) into an underlying silicon substrate or an adjoining layer even after exposure to elevated temperatures (e.g., up to approximately 200 ºC, up to approximately 350 ºC, up to approximately 500 ºC, or even higher) for times of, e.g., up to 2 hours. Figures 7A and 7B show the concentrations of Cu and silicon across a Cu/silicon interface (i.e., one without a barrier layer between the Cu and silicon) as measured with Auger electron spectroscopy (AES) as fabricated (no anneal) and after anneals of 200 ºC – 500 ºC. As shown, mutual diffusion of the Cu and silicon occurs at temperatures as low as (or even lower than) 200 ºC, and the interface is severely diffused after an anneal at 500 ºC. Additionally, the Cu layer exhibits poor adhesion to silicon in the absence of a barrier layer between the Cu and silicon.

[0040] Figures 8A and 8B show the concentrations of Cu and silicon across an interface between silicon and a barrier layer 300 or capping layer 530 that includes or consists essentially of CuTaCr as measured with AES after no anneal and anneals of 200 ºC – 500 ºC. In the illustrated embodiment, the barrier layer 300 or capping layer 530 is composed of 2 weight % Ta, 1 weight % Cr, and the balance Cu. (In another embodiment exhibiting similar behavior, the barrier layer 300 or capping layer 530 includes or consists essentially of 5 weight % Ta, 2 weight % Cr, and the balance Cu.) In contrast to the results shown in Figures 7A and 7B, there is negligible diffusion of Cu or silicon across the interface, even after an anneal at 500 ºC for two hours. Figures 9A – 9C are a series of scanning electron microscopy (SEM) micrographs of the surface of the barrier layer 300 or capping layer 530 as deposited (Figure 9A), after an anneal of 300 ºC for one hour (Figure 9B), and after an anneal of 500 ºC for one hour (Figure 9C). As shown, the grain structure and size of the barrier layer 300 or capping layer 530 show

no appreciable change, and there is no evidence of the formation of different phases (e.g., copper silicide phases) even after a heat treatment of 500 ºC. These results were confirmed by x-ray diffraction (XRD) scans of annealed structures, in which no silicide phases were detected even after anneals of 500 ºC for two hours. In contrast, copper silicide phases are clearly evident in SEM and XRD performed on samples of pure Cu layers on Si that have been annealed at 500 ºC for two hours.

[0041] Figures 10A and 10B show, respectively, SEM and transmission electron microscopy (TEM) images of a barrier layer 300 or capping layer 530 that is disposed in contact with silicon (e.g., a silicon substrate and/or a silicon overlayer) and that has been annealed at 350 ºC for 30 minutes. Precipitates 1000 are evident within the Cu grain boundaries 1010 of the barrier layer 300 or capping layer 530. In various embodiments the precipitates include or consist essentially of a silicide of one or more of the refractory metal alloying elements of the barrier layer 300 or capping layer 530, and such precipitates reduce or substantially eliminate Cu diffusion along the grain boundaries into the adjoining silicon.

[0042] Similarly, in various embodiments of the invention, the refractory-metal dopants of barrier layers 300 and/or capping layers 530 tend to segregate to the Cu grain boundaries and provide beneficial effects even in the absence of reaction with silicon to form silicides. For example, the Cu grain boundaries may be occupied, and partially or substantially completely "blocked" with the refractory-metal dopants and thereby retard or substantially prevent oxygen diffusion along the Cu grain boundaries. In this manner, corrosion of the barrier layer 300, capping layer 530, and/or the conductive layer in contact therewith is decreased or substantially prevented. Thus, in various embodiments of the present invention, a barrier layer 300 or capping layer 530 may include or consist essentially of a polycrystalline Cu matrix doped with one or more refractory metal elements, where the grain boundaries of the layer between the doped Cu grains contain a higher concentration of the refractory metal dopant(s) that the concentration within the grains themselves. For example, the refractory metal concentration within the grain

boundaries may be larger than that within the grains by a factor of 5, a factor of 10, or even a factor of 100.

[0043] Figure 11 depicts images of four different metallic samples after an environmental corrosion test conducted at 60 ºC and 80% humidity for a period of 260 hours. As shown, the samples of pure Cu and pure Mo experienced much more severe corrosion that did the Cu-alloy samples in accordance with embodiments of the present invention. The two Cu-alloy samples were (1) Cu with 10 weight % Ta and 2 weight % Cr (labeled in Figure 11 as CuTaCr), and (2) Cu with 5 weight % Nb and 2 weight % Cr (labeled in Figure 11 as CuNbCr). The table below provides data regarding the amount of exposed surface area corroded during the environmental corrosion test for each of the samples. As indicated, the Cu-alloy samples in accordance with embodiments of the present invention experienced much less corrosion than the pure Cu and Mo samples, demonstrating the benefits of such alloys over conventional Mo diffusion barriers and capping layers, as well as over pure Cu.

Sample	Corroded Surface Area (%)
Mo	6.78
Cu	3.84
CuTaCr	1.75
CuNbCr	0.83

[0044] In preferred embodiments of the invention, the barrier layers 300 or capping layers 530 have low resistivity, e.g., below 10 microOhm-cm, or even below 5 microOhm-cm, even after anneals of up to 500 ºC, up to 600 ºC, or even higher temperatures. Moreover, in preferred embodiments the barrier layers 300 or capping layers 530 exhibit good adhesion to glass as measured by, e.g., an ASTM standard tape test. Embodiments of the invention also include electronic devices (or portions thereof)

in which a highly conductive material (e.g., Cu, Ag, Al, and/or Au) is utilized to form all or a portion of a conductor or electrode and has both a barrier layer 300 below it and a capping layer 530 above it.

[0045] The terms and expressions employed herein are used as terms and expressions of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding any equivalents of the features shown and described or portions thereof. In addition, having described certain embodiments of the invention, it will be apparent to those of ordinary skill in the art that other embodiments incorporating the concepts disclosed herein may be used without departing from the spirit and scope of the invention. Accordingly, the described embodiments are to be considered in all respects as only illustrative and not restrictive.

What is claimed is:

1. A thin-film transistor comprising:

a substrate comprising at least one of silicon or glass; and

an electrode comprising:

(i) disposed on the substrate, a barrier layer comprising an alloy of Cu and one or more refractory metal elements selected from the list consisting of Ta, Nb, Mo, W, Zr, Hf, Re, Os, Ru, Rh, Ti, V, Cr, and Ni, and

(ii) disposed on the barrier layer, a conductor layer comprising at least one of Cu, Ag, Al, or Au.

2. The thin-film transistor of claim 1, wherein the substrate comprises glass.

3. The thin-film transistor of claim 1, wherein the substrate comprises silicon.

4. The thin-film transistor of claim 3, wherein the substrate comprises amorphous silicon.

5. The thin-film transistor of claim 1, wherein the barrier layer comprises an alloy of Cu, Ta, and Cr.

6. The thin-film transistor of claim 5, wherein the barrier layer consists essentially of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Cr, and the balance Cu.

7. The thin-film transistor of claim 5, wherein the barrier layer consists essentially of approximately 5 weight % Ta, approximately 2 weight % Cr, and the balance Cu.

8. The thin-film transistor of claim 5, wherein the barrier layer consists essentially of approximately 2 weight % Ta, approximately 1 weight % Cr, and the balance Cu.

9. The thin-film transistor of claim 1, wherein the barrier layer comprises an alloy of Cu, Ta, and Ti.

10. The thin-film transistor of claim 9, wherein the barrier layer consists essentially of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Ti, and the balance Cu.

11. The thin-film transistor of claim 9, wherein the barrier layer consists essentially of approximately 5 weight % Ta, approximately 2 weight % Ti, and the balance Cu.

12. The thin-film transistor of claim 1, wherein the barrier layer comprises an alloy of Cu, Nb, and Cr.

13. The thin-film transistor of claim 12, wherein the barrier layer consists essentially of 1 weight % - 10 weight % Nb, 1 weight % - 5 weight % Cr, and the balance Cu.

14. The thin-film transistor of claim 12, wherein the barrier layer consists essentially of approximately 5 weight % Nb, approximately 2 weight % Cr, and the balance Cu.

15. The thin-film transistor of claim 1, wherein (i) the electrode comprises a sidewall comprising (a) an exposed portion of the barrier layer, (b) an exposed portion of the conductor layer, and (c) an interface between the exposed portion of the barrier layer and the exposed portion of the conductor layer, and (ii) the sidewall of the electrode is substantially free of discontinuities notwithstanding the interface.

16. The thin-film transistor of claim 1, wherein the substrate is substantially free of Cu diffusion from the barrier layer.

17. The thin-film transistor of claim 1, wherein (i) the barrier layer comprises a plurality of crystalline grains separated by grain boundaries, (ii) at least one of the grain boundaries comprises a particulate therein, and (iii) the particulate comprises a reaction product of silicon and at least one of the refractory metal elements.

18. A method of forming an electrode of a thin-film transistor, the method comprising:

providing a substrate comprising at least one of silicon or glass;

depositing over the substrate a barrier layer comprising an alloy of Cu and one or more refractory metal elements selected from the group consisting of Ta, Nb, Mo, W, Zr, Hf, Re, Os, Ru, Rh, Ti, V, Cr, and Ni;

depositing over the barrier layer a conductor layer comprising at least one of Cu, Ag, Al, or Au;

forming a mask layer over the barrier layer;

patterning the mask layer to reveal a portion of the conductor layer, a remaining portion of the mask layer at least partially defining a shape of the electrode; and

thereafter, applying an etchant to remove portions of the conductor layer and the barrier layer not masked by the patterned mask layer, thereby forming a sidewall of the electrode:

comprising (i) an exposed portion of the barrier layer, (ii) an exposed portion of the conductor layer, and (iii) an interface between the exposed portion of the barrier layer and the exposed portion of the conductor layer, and

substantially free of discontinuities notwithstanding the interface.

19. The method of claim 18, wherein the mask layer comprises photoresist.

20. The method of claim 18, wherein the etchant comprises a mixture of phosphoric acid, acetic acid, nitric acid, and water.

21. The method of claim 18, wherein the etchant consists essentially of 50-60 weight % phosphoric acid, 15-25 weight % acetic acid, 3-5 weight % nitric acid, and the balance water.

22. The method of claim 18, wherein the etchant consists essentially of 50 weight % phosphoric acid, 25 weight % acetic acid, 3 weight % nitric acid, and the balance water.

23. The method of claim 18, further comprising removing the remaining portion of the patterned mask layer.

24. The method of claim 18, wherein (i) the barrier layer comprises a plurality of crystalline grains separated by grain boundaries, and (ii) the substrate comprises silicon.

25. The method of claim 24, further comprising annealing the electrode at a temperature sufficient to form a particulate within at least one of the grain boundaries, the particulate comprising a reaction product of silicon and at least one of the refractory metal elements.

26. The method of claim 18, wherein the substrate comprises glass.

27. The method of claim 18, wherein the substrate comprises silicon.

28. The method of claim 27, wherein the substrate comprises amorphous silicon.

29. The method of claim 18, wherein the barrier layer comprises an alloy of Cu, Ta, and Cr.

30. The method of claim 29, wherein the barrier layer consists essentially of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Cr, and the balance Cu.

31. The method of claim 29, wherein the barrier layer consists essentially of approximately 5 weight % Ta, approximately 2 weight % Cr, and the balance Cu.

32. The method of claim 29, wherein the barrier layer consists essentially of approximately 2 weight % Ta, approximately 1 weight % Cr, and the balance Cu.

33. The method of claim 18, wherein the barrier layer comprises an alloy of Cu, Ta, and Ti.

34. The method of claim 33, wherein the barrier layer consists essentially of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Ti, and the balance Cu.

35. The method of claim 33, wherein the barrier layer consists essentially of approximately 5 weight % Ta, approximately 2 weight % Ti, and the balance Cu.

36. The method of claim 18, wherein the barrier layer comprises an alloy of Cu, Nb, and Cr.

37. The method of claim 36, wherein the barrier layer consists essentially of 1 weight % - 10 weight % Nb, 1 weight % - 5 weight % Cr, and the balance Cu.

38. The method of claim 36, wherein the barrier layer consists essentially of approximately 5 weight % Nb, approximately 2 weight % Cr, and the balance Cu.

39. A touch-panel display comprising:

a substrate;

a plurality of conductive touch-panel row sensors (i) arranged in lines extending along a first direction and (ii) disposed over the substrate;

a plurality of conductive touch-panel column sensors (i) arranged in lines extending along a second direction and intersecting the lines of the row sensors and (ii) disposed over the substrate; and

an interconnect (i) disposed at a point of intersection between a line of row sensors and a line of column sensors, and (ii) electrically connecting two column sensors or two row sensors,

wherein the interconnect comprises:

(i) a conductor layer comprising at least one of Cu, Ag, Al, or Au, and

(ii) disposed on the conductor layer, a capping layer comprising an alloy of Cu and one or more refractory metal elements selected from the list consisting of Ta, Nb, Mo, W, Zr, Hf, Re, Os, Ru, Rh, Ti, V, Cr, and Ni.

40. The touch-panel display of claim 39, wherein the interconnect extends over or under a row sensor and electrically connects two column sensors, and further comprising

an insulating layer disposed between the interconnect and the row sensor and electrically insulating the interconnect and the row sensor.

41. The touch-panel display of claim 39, wherein the interconnect extends over or under a column sensor and electrically connects two row sensors, and further comprising an insulating layer disposed between the interconnect and the column sensor and electrically insulating the interconnect and the column sensor.

42. The touch-panel display of claim 39, wherein the substrate comprises an insulating material.

43. The touch-panel display of claim 39, wherein the substrate comprises glass.

44. The touch-panel display of claim 39, wherein the row sensors and column sensors comprise a substantially transparent conductive material.

45. The touch-panel display of claim 39, wherein the row sensors and column sensors comprise indium tin oxide.

46. The touch-panel display of claim 39, wherein the capping layer comprises an alloy of Cu, Ta, and Cr.

47. The touch-panel display of claim 46, wherein the capping layer consists essentially of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Cr, and the balance Cu.

48. The touch-panel display of claim 46, wherein the capping layer consists essentially of approximately 5 weight % Ta, approximately 2 weight % Cr, and the balance Cu.

49. The touch-panel display of claim 46, wherein the capping layer consists essentially of approximately 2 weight % Ta, approximately 1 weight % Cr, and the balance Cu.

50. The touch-panel display of claim 39, wherein the capping layer comprises an alloy of Cu, Ta, and Ti.

51. The touch-panel display of claim 50, wherein the capping layer consists essentially of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Ti, and the balance Cu.

52. The touch-panel display of claim 50, wherein the capping layer consists essentially of approximately 5 weight % Ta, approximately 2 weight % Ti, and the balance Cu.

53. The touch-panel display of claim 39, wherein the capping layer comprises an alloy of Cu, Nb, and Cr.

54. The touch-panel display of claim 53, wherein the capping layer consists essentially of 1 weight % - 10 weight % Nb, 1 weight % - 5 weight % Cr, and the balance Cu.

55. The touch-panel display of claim 53, wherein the capping layer consists essentially of approximately 5 weight % Nb, approximately 2 weight % Cr, and the balance Cu.

56. The touch-panel display of claim 39, wherein (i) the interconnect comprises a sidewall comprising (a) an exposed portion of the capping layer, (b) an exposed portion of the conductor layer, and (c) an interface between the exposed portion of the capping layer and the exposed portion of the conductor layer, and (ii) the sidewall of the electrode is substantially free of discontinuities notwithstanding the interface.

57. The touch-panel display of claim 39, wherein (i) the capping layer comprises a plurality of crystalline grains separated by grain boundaries, (ii) at least one of the grain boundaries comprises a particulate therein, and (iii) the particulate comprises an agglomeration of at least one of the refractory metal elements.

58. A method of forming an interconnect of a touch-panel display, the method comprising:

providing a structure comprising (i) a substrate, (ii) a plurality of conductive touch-panel row sensors (a) arranged in lines extending along a first direction and (b) disposed over the substrate, and (iii) a plurality of conductive touch-panel column sensors (a) arranged in lines extending along a second direction and intersecting the lines of the row sensors and (b) disposed over the substrate;

depositing an insulator layer at least at a point of intersection between a line of row sensors and a line of column sensors;

depositing over the insulator layer a conductor layer comprising at least one of Cu, Ag, Al, or Au;

depositing over the conductor layer a capping layer comprising an alloy of Cu and one or more refractory metal elements selected from the group consisting of Ta, Nb, Mo, W, Zr, Hf, Re, Os, Ru, Rh, Ti, V, Cr, and Ni;

forming a mask layer over the capping layer;

patterning the mask layer to reveal a portion of the capping layer, a remaining portion of the mask layer at least partially defining a shape of the interconnect; and

thereafter, applying an etchant to remove portions of the capping layer and the conductor layer not masked by the patterned mask layer, thereby forming a sidewall of the interconnect:

comprising (i) an exposed portion of the capping layer, (ii) an exposed portion of the conductor layer, and (iii) an interface between the exposed portion of the capping layer and the exposed portion of the conductor layer, and

substantially free of discontinuities notwithstanding the interface.

59. The method of claim 58, wherein the mask layer comprises photoresist.

60. The method of claim 58, wherein the etchant comprises a mixture of phosphoric acid, acetic acid, nitric acid, and water.

61. The method of claim 58, wherein the etchant consists essentially of 50-60 weight % phosphoric acid, 15-25 weight % acetic acid, 3-5 weight % nitric acid, and the balance water.

62. The method of claim 58, wherein the etchant consists essentially of 50 weight % phosphoric acid, 25 weight % acetic acid, 3 weight % nitric acid, and the balance water.

63. The method of claim 58, further comprising removing the remaining portion of the patterned mask layer.

64. The method of claim 58, wherein the capping layer comprises a plurality of crystalline grains separated by grain boundaries.

65. The method of claim 64, further comprising annealing the interconnect at a temperature sufficient to form a particulate within at least one of the grain boundaries, the particulate comprising an agglomeration of at least one of the refractory metal elements.

66. The method of claim 58, wherein the substrate comprises an insulating material.

67. The method of claim 58, wherein the substrate comprises glass.

68. The method of claim 58, wherein the row sensors and column sensors comprise a substantially transparent conductive material.

69. The method of claim 58, wherein the row sensors and column sensors comprise indium tin oxide.

70. The method of claim 58, wherein the capping layer comprises an alloy of Cu, Ta, and Cr.

71. The method of claim 70, wherein the capping layer consists essentially of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Cr, and the balance Cu.

72. The method of claim 70, wherein the capping layer consists essentially of approximately 5 weight % Ta, approximately 2 weight % Cr, and the balance Cu.

73. The method of claim 70, wherein the capping layer consists essentially of approximately 2 weight % Ta, approximately 1 weight % Cr, and the balance Cu.

74. The method of claim 58, wherein the capping layer comprises an alloy of Cu, Ta, and Ti.

75. The method of claim 74, wherein the capping layer consists essentially of 1 weight % - 12 weight % Ta, 1 weight % - 5 weight % Ti, and the balance Cu.

76. The method of claim 74, wherein the capping layer consists essentially of approximately 5 weight % Ta, approximately 2 weight % Ti, and the balance Cu.

77. The method of claim 58, wherein the capping layer comprises an alloy of Cu, Nb, and Cr.

78. The method of claim 77, wherein the capping layer consists essentially of 1 weight % - 10 weight % Nb, 1 weight % - 5 weight % Cr, and the balance Cu.

79. The method of claim 77, wherein the capping layer consists essentially of approximately 5 weight % Nb, approximately 2 weight % Cr, and the balance Cu.

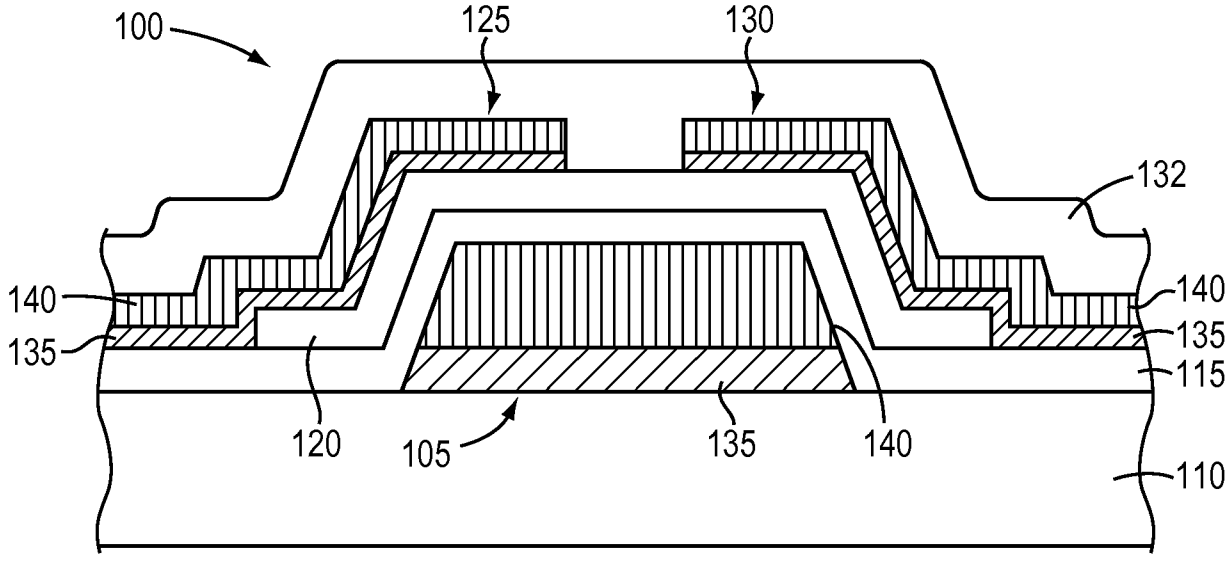


FIG. 1A
PRIOR ART

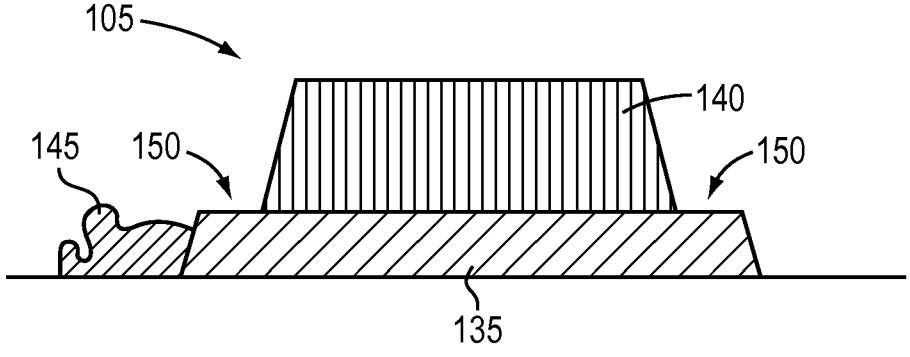


FIG. 1B
PRIOR ART

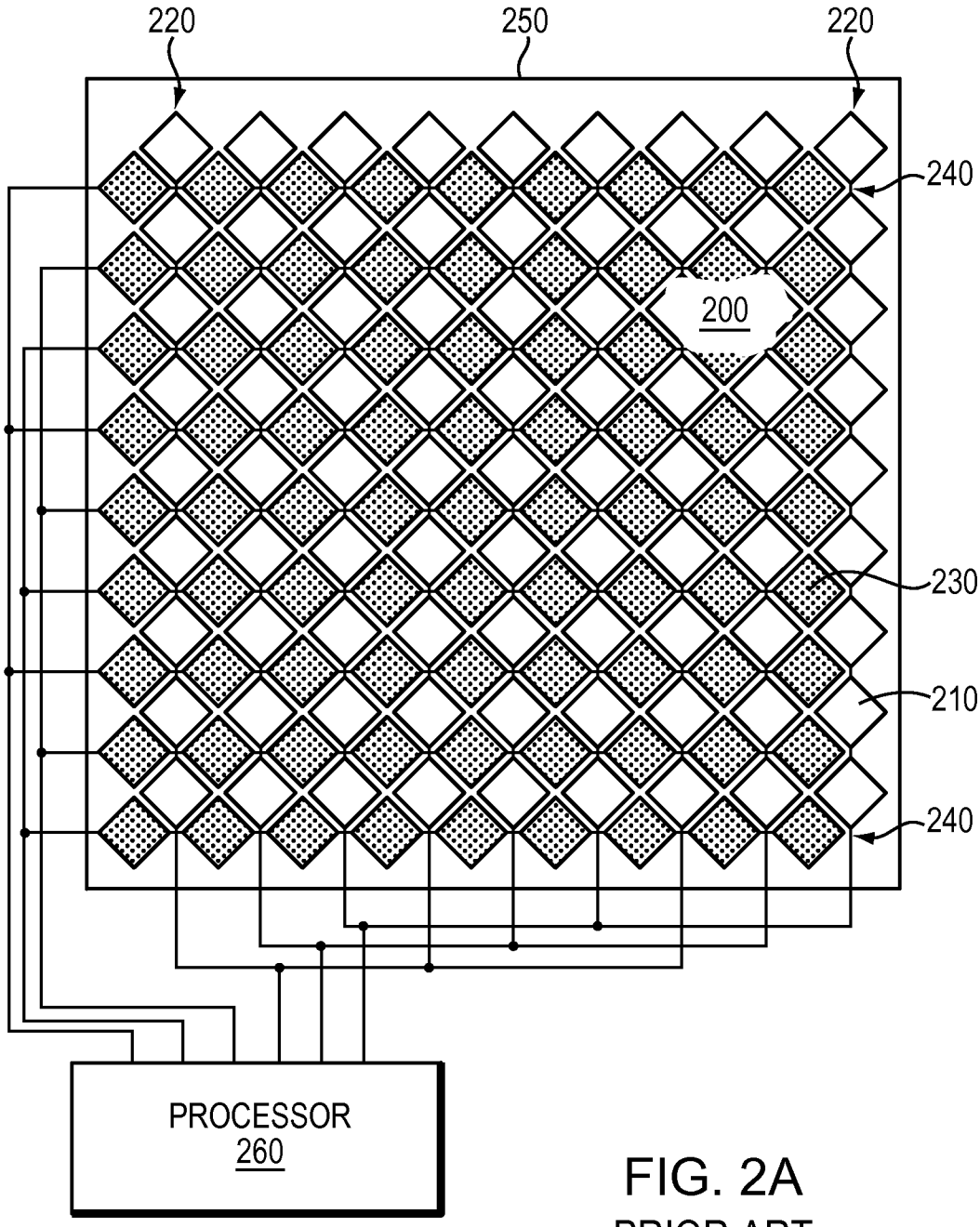


FIG. 2A
PRIOR ART

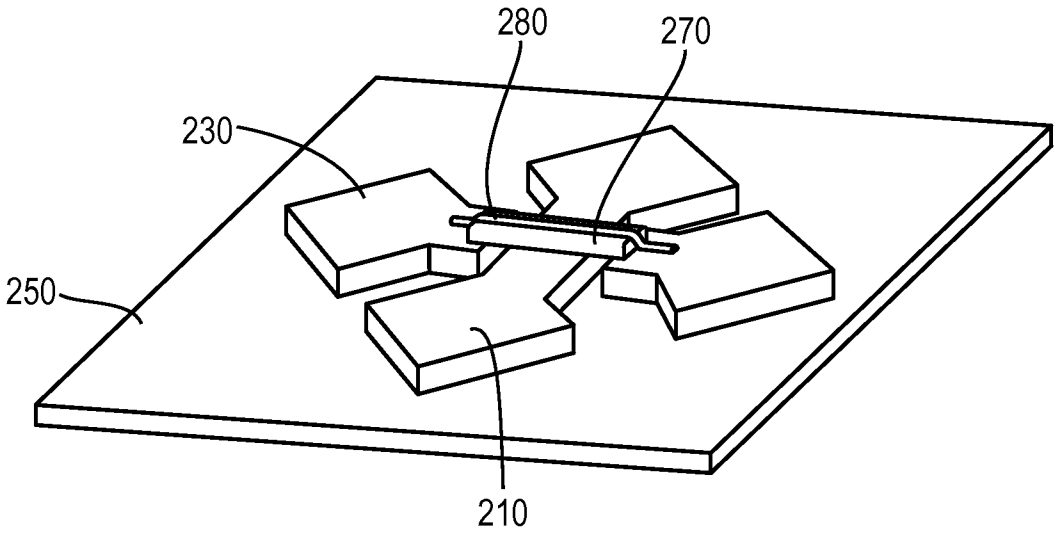


FIG. 2B
PRIOR ART

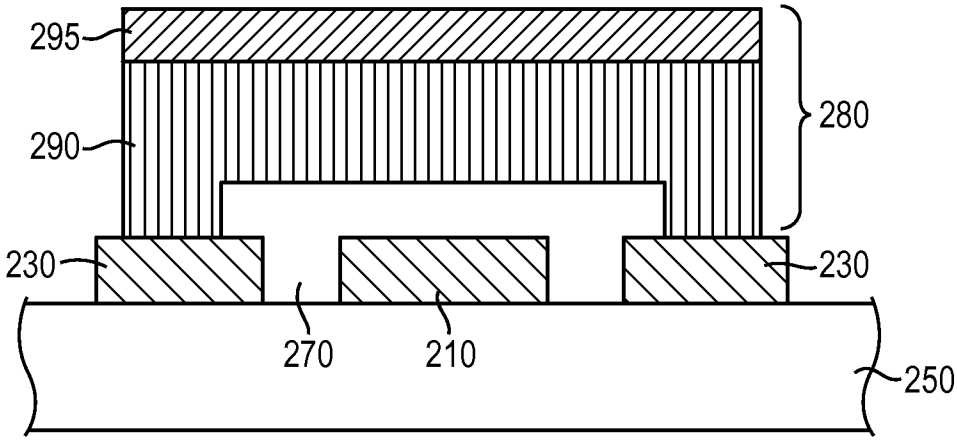


FIG. 2C
PRIOR ART

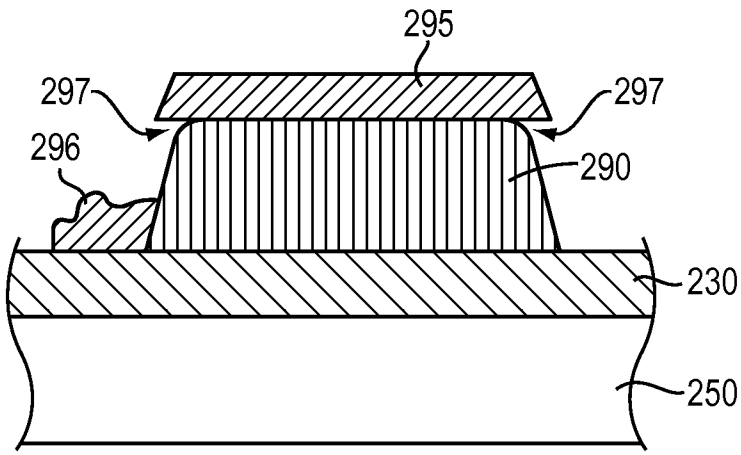


FIG. 2D
PRIOR ART

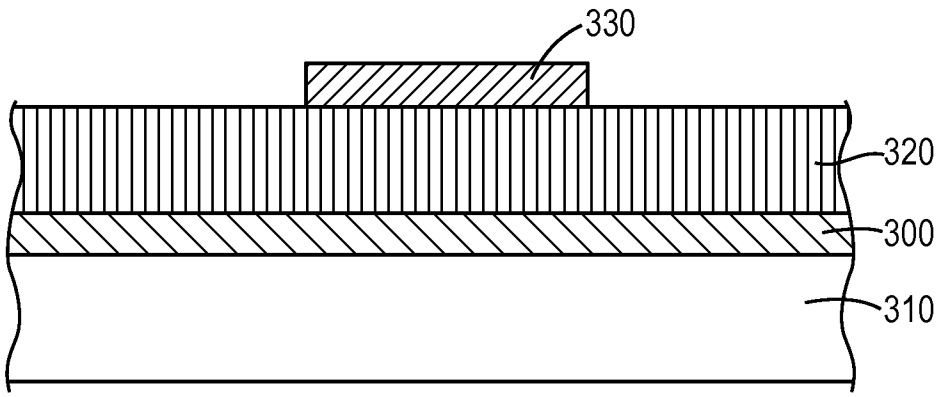


FIG. 3

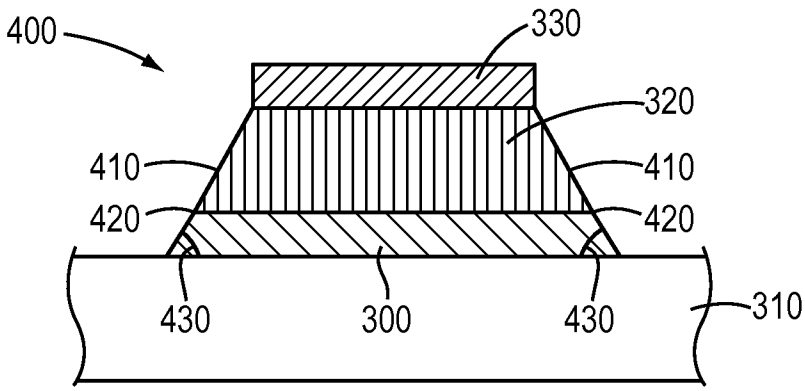


FIG. 4

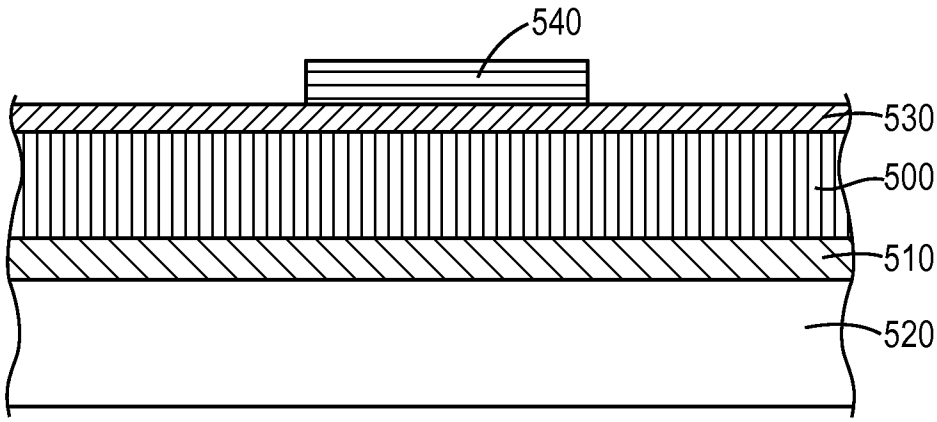


FIG. 5

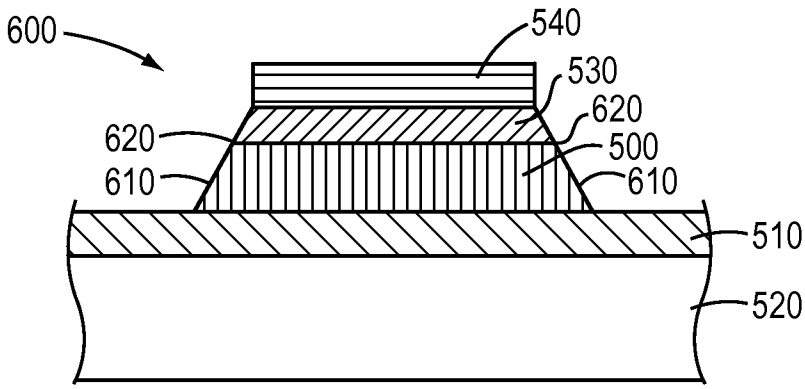


FIG. 6

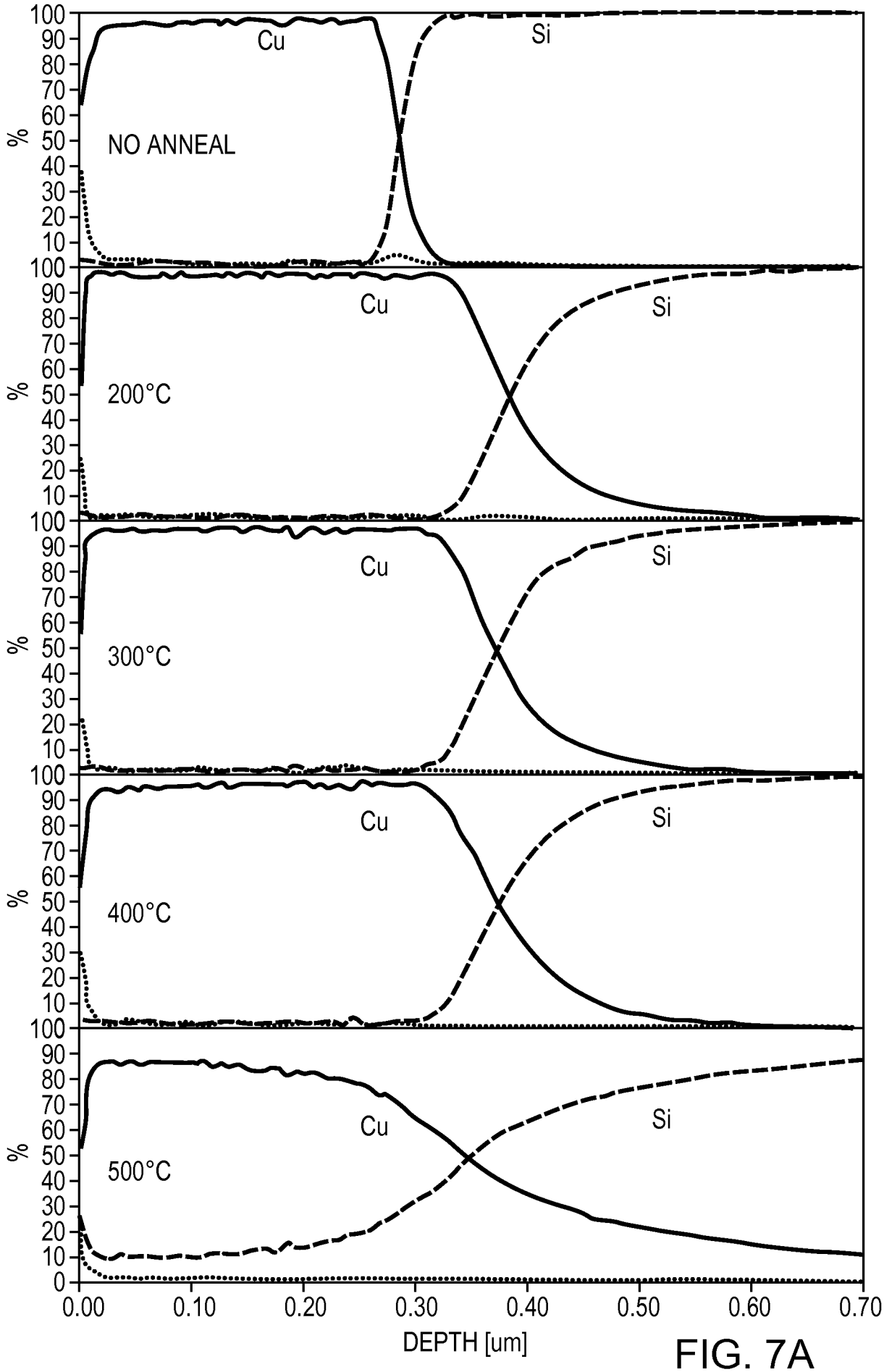

NO ANNEAL
200°C
300°C
400°C
500°C
Cu
Si
%
DEPTH [um]
0.00
0.10
0.20
0.30
0.40
0.50
0.60
0.70

FIG. 7A

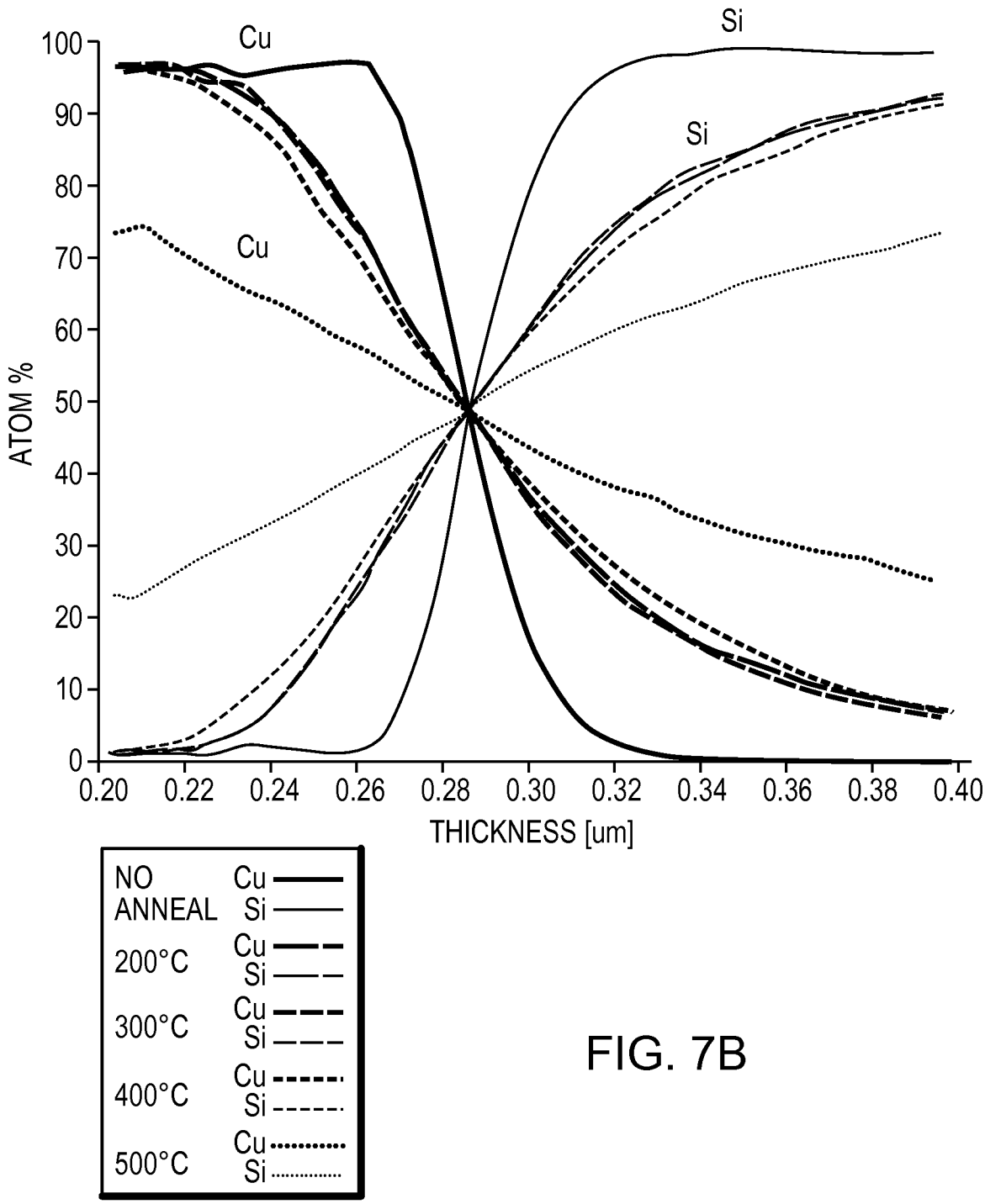

Cu
Si
Si
Cu
100
90
80
70
60
50
40
30
20
10
0
ATOM %
0.20
0.22
0.24
0.26
0.28
0.30
0.32
0.34
0.36
0.38
0.40
THICKNESS [um]
NO ANNEAL
Cu
Si
200°C
Cu
Si
300°C
Cu
Si
400°C
Cu
Si
500°C
Cu
Si

FIG. 7B

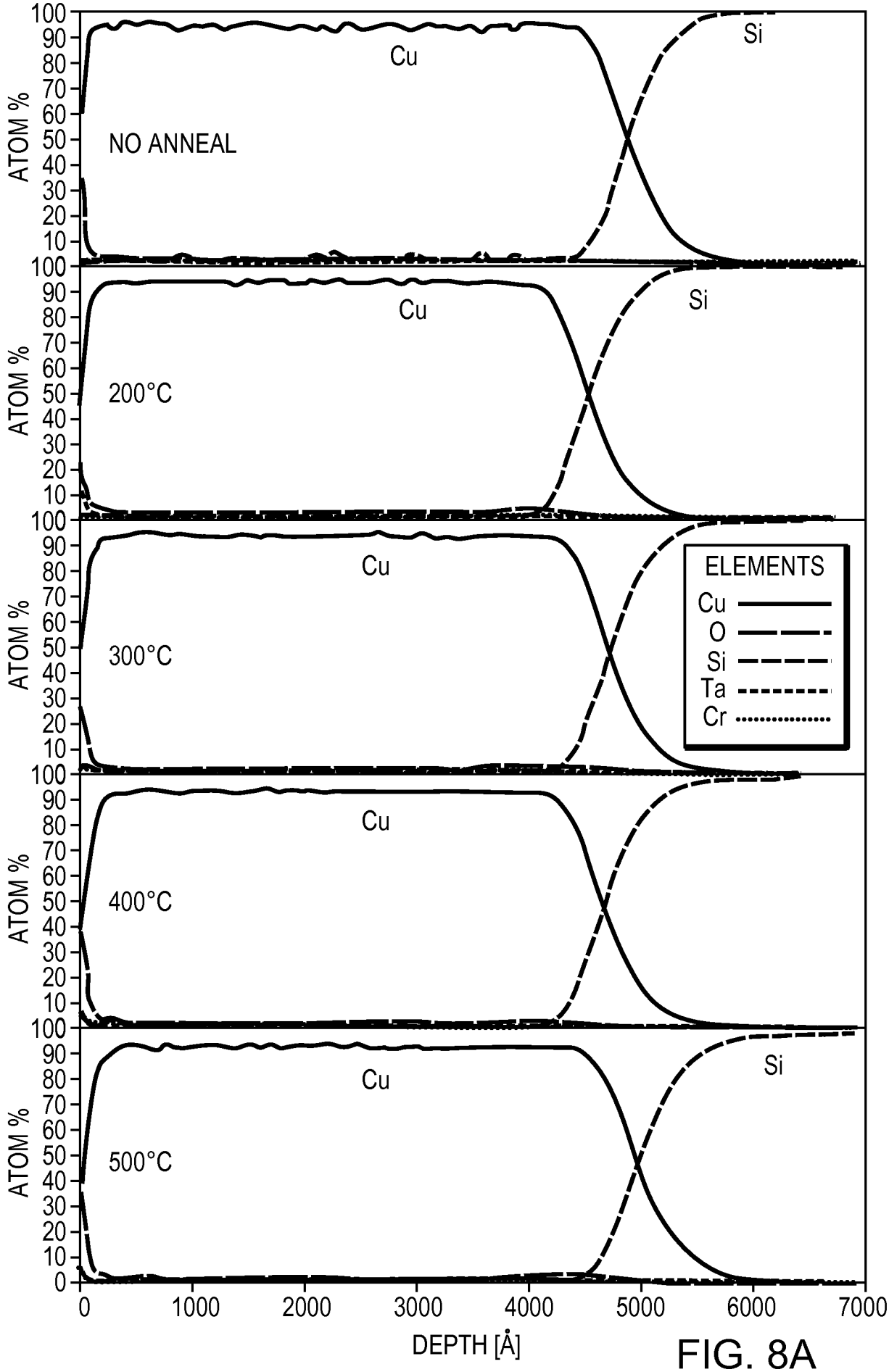

ATOM %
NO ANNEAL
Cu
Si
200°C
300°C
400°C
500°C
ELEMENTS
Cu
O
Si
Ta
Cr
0
1000
2000
3000
4000
5000
6000
7000
DEPTH [Å]

FIG. 8A

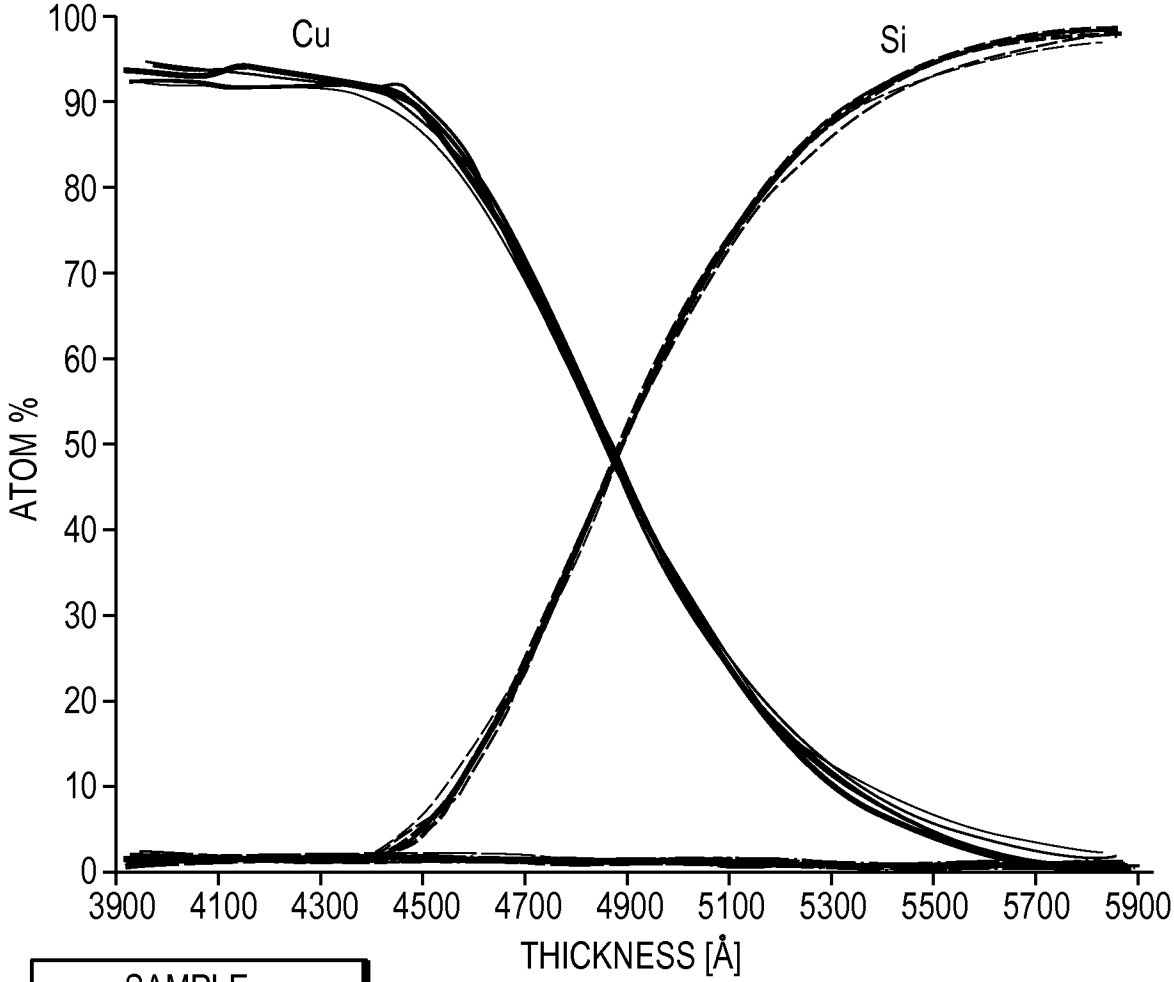
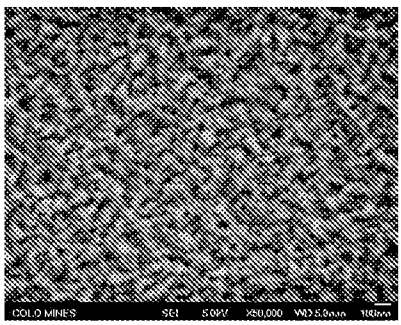
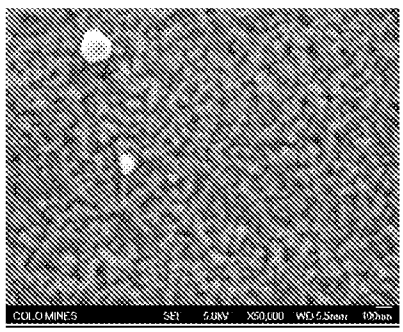

Cu
Si
100
90
80
70
60
50
40
30
20
10
0
ATOM %
3900
4100
4300
4500
4700
4900
5100
5300
5500
5700
5900
THICKNESS [Å]
SAMPLE
NO ANNEAL
Cu
Si
Ta
Cr
200°C
300°C
400°C
500°C

FIG. 8B



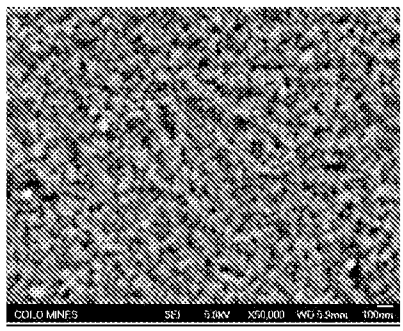
AS DEPOSITED

FIG. 9A



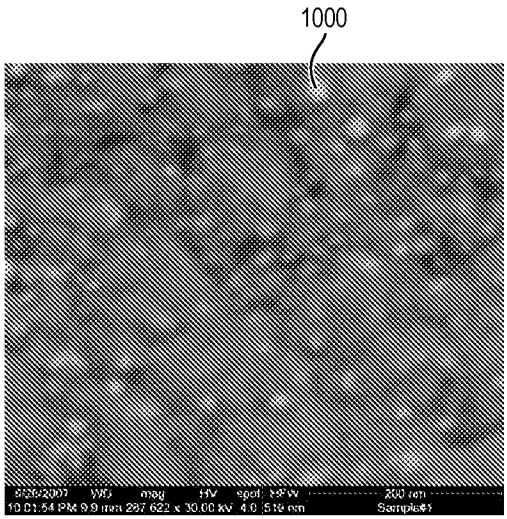
300°C/1h

FIG. 9B



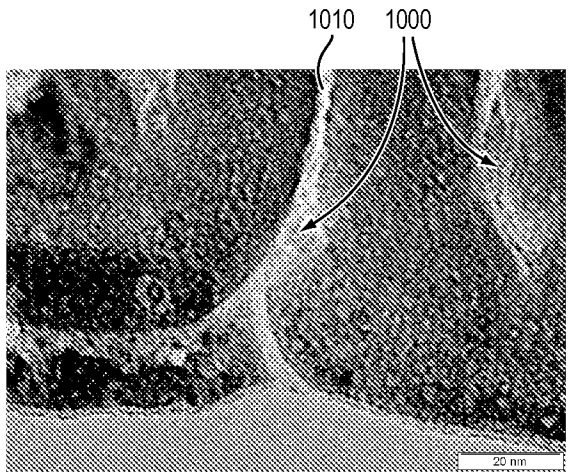
500°C/1h

FIG. 9C



SEM

FIG. 10A



TEM

FIG. 10B

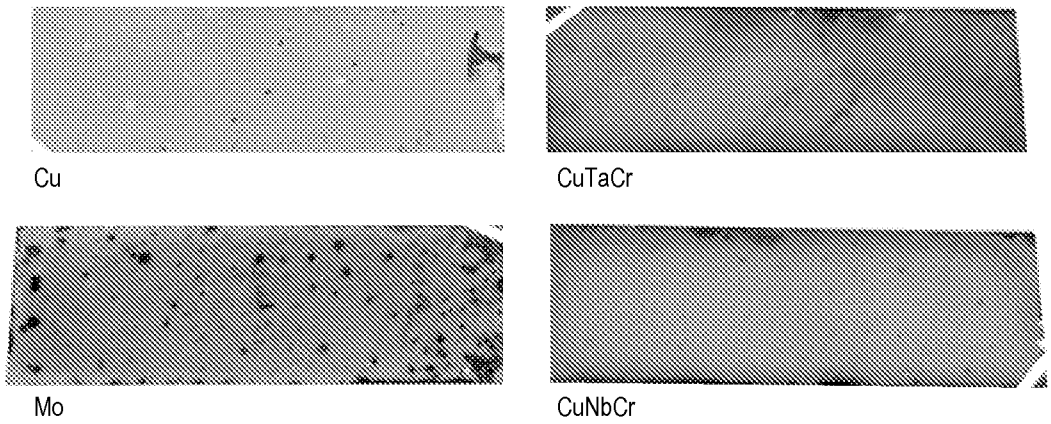


FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/041026

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/786(2006.01)i, H01L 21/335(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/786; C22C 19/05; H01L 21/331; H01L 21/20; H01L 33/00; B32B 5/02; G06F 3/041; H01L 21/335

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: thin-film transistor, barrier layer, touch-panel, interconnect, capping layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2010-013636 A1 (ULVAC INC. et al.) 04 February 2010 See abstract, paragraphs [0014]-[0063] and figures 1-3(d).	1-4,15-19,23-28
Y		5-14,20-22,29-38,56,58-79
A		39-55,57
Y	US 2013-0032793 A1 (DO-HYUN KIM et al.) 07 February 2013 See abstract, paragraphs [0047]-[0094] and figures 1-13.	5-14,29-38,46-55,70-79
Y	KR 10-2000-0056517 A (LG DISPLAY CO., LTD.) 15 September 2000 See abstract, pages 2-3 and figures 2a-2c.	20-22,60-62
X	US 2013-0135224 A1 (YUH-WEN LEE et al.) 30 May 2013 See abstract, paragraphs [0015]-[0023] and figures 1A-2.	39-45,57
Y		46-56,58-79
A	US 2009-0166640 A1 (GYU WON HAN et al.) 02 July 2009 See abstract, paragraphs [0038]-[0090] and figures 2A-6B.	1-79

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 October 2014 (16.10.2014)	**16 October 2014 (16.10.2014)**

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Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2014/041026

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		JP 2013-033927 A	14/02/2013
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		TW M434258 U	21/07/2012
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		CN 101471327 B	11/07/2012
		KR 10-1296654 B1	14/08/2013
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		US 8178973 B2	15/05/2012