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— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

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(54) Title: DATA PROCESSING CIRCUIT WITH RUN-TIME DIAGNOSTIC MONITOR CIRCUIT

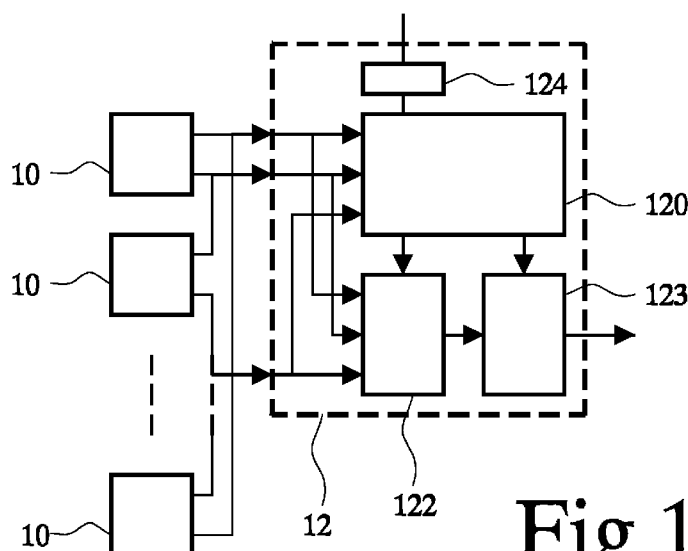


Fig.1

(57) Abstract: Operation of logic circuitry (10) is monitored using a content addressable memory (120) with content addressing inputs coupled to the logic circuitry (10). Signal patterns are stored in the content addressable memory (120). When the logic circuitry (10) is activated, output signals of the content addressable memory (120) in response to signals from the logic circuitry (10) are used to control diagnostic actions. In addition an arithmetic circuit may be added, to perform arithmetic operations on multi-bit signals from the logic circuitry. The type of arithmetic operation may be controlled by an output of the content addressable memory. Furthermore a feedback loop from the output of the content addressable memory to its input may be used to detect complex time dependent signal configurations.



— *as to the applicant's entitlement to claim the priority of
the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

DATA PROCESSING CIRCUIT WITH RUN-TIME DIAGNOSTIC MONITOR CIRCUIT

FIELD OF THE INVENTION

The invention relates to a data processing circuit that comprises a run-time diagnostic monitor circuit.

5 BACKGROUND OF THE INVENTION

US patent 5,867,644 describes a data processing circuit with diagnostic hardware. A programmable state machine is used that can be programmed to look for signal patterns presented by selected input sources and to respond to the occurrence of a defined pattern by driving certain control information onto a state machine output bus. US 5,867,644 describes that patterns are detected by means of user configurable comparators, with storage elements wherein data values are stored for comparison with signals from the selected input sources.

However, in this way it is not easy to test for signal patterns that satisfy complex conditions on the interrelations between the signals, such as a condition that the signal values in such a group have the same, arbitrary value, or a logic function of the group of signal values has a predetermined value. Use of circuits especially designed to verify such conditions would make diagnostic monitoring inflexible, or involve excessive circuit overhead, whereas sequential testing would make diagnostics painfully slow.

20 SUMMARY OF THE INVENTION

Among others, it is an object to provide for a data processing circuit with a diagnostic circuit that makes it possible to respond quickly and with little overhead to the occurrence of complex signal conditions.

A data processing circuit according to claim 1 is provided. Herein signals from the logic circuitry that is monitored by a diagnostic monitor are used as content addressing input of a content addressable memory. The output of the content addressable memory is used to control diagnostic actions such as for example trigger logging of data and/or to trigger diagnostic action and/or to trigger suspension of operation dependent on the output of

the content addressable memory. The use of the content addressable memory for this purpose makes it possible to provide a quick monitor response dependent on whether a complex condition on the signals from the monitored logic circuitry is satisfied.

In an embodiment the diagnostic monitor additionally comprises a computation circuit, which makes it possible to respond quickly when a conditions is satisfied that is based on an arithmetic relation. In a further embodiment the type of computation performed by the computation circuit is selected dependent on the output of the content addressable memory. This makes it possible to use flexible signal configuration dependent arithmetic tests quickly during monitoring. A multiplexing circuit may be used to select the operands of the arithmetic operation. In a further embodiment selection by the multiplexer may be controlled dependent on the output of the content addressable memory. This makes the possible complex tests even more flexible.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and advantageous aspects will become apparent from a description of exemplary embodiments, using the following Figures

Fig. 1 shows a data processing circuit wit a diagnostic monitor

Fig. 2 shows a content addressable memory

Fig. 3 shows a diagnostic monitor

Figs. 4, 4a show data processing circuits

Fig. 5 shows a computation circuit of a diagnostic monitor

Fig. 6 shows data processing circuits

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Fig. 1 shows a data processing interconnected circuit comprising circuit modules 10 and a diagnostic monitor 12. Circuit modules 10 comprise logic circuits that produce logic signals. Diagnostic monitor 12 comprises a content addressable memory 120, a computation circuit 122, a handler circuit 123 and a programming circuit 124. Diagnostic monitor 12 is provided to provide for optional programmable monitoring of operation of circuit modules 10, without having any function in the normal operation of the circuit.

Content addressable memory 120 has content based addressing inputs coupled to outputs of circuit modules 10 and outputs coupled to a computation circuit 122 and handler circuit 123. Although separate outputs are shown, it should be appreciated that these can be regarded as different parts of a single output of content addressable memory 120, or that the

same output may be coupled to both computation circuit 122 and handler circuit 123

Although an example has been shown wherein only communication lines between circuit modules 10 are coupled to content addressable memory 120 and computation circuit 122, it should be appreciated that alternatively (test) outputs of circuit modules 10 may be used that are not involved in communication between circuit modules 10.

Computation circuit 122 has inputs coupled to circuit modules 10 and an output coupled to handler circuit 123. Handler circuit 123 may have outputs coupled to circuit modules 10. Programming circuit 124 has an output coupled to programming inputs of content addressable memory 120.

Fig. 2 shows an example of a content addressable memory, comprising an array of associative memory cells 20, content lines 22, match lines 24, data lines 26, a selection circuit 28 and a programming circuit 29. As used herein “lines” refer to conductors, typically conductive tracks in an integrated circuit that preferably run in parallel to each other. Cells 20 are connected in parallel to content lines 22 and to data lines 26. Although only three cells 20 of the array are shown, it should be appreciated that a far larger number of cells may be present in the array, say at least a hundred and twenty eight. Each cell is coupled to a respective one of the match lines 24. Match lines 24 are coupled to selection circuit 28, which has selection outputs coupled to cells 20. In an embodiment selection circuit 28 may be implemented as respective connections, each between the match line 24 and a selection input of a respective one of cells 20. This suffices for example if it is ensured that that content of all cells is different.

Programming circuit 29 is coupled to content lines 22 and to data lines 26 and to selection circuit 28.

In operation a content addressing signal is applied to content lines 22 and each cell 20 of the array compares the content addressing signal with a content that is stored in the cell 20. All cells 20 do so in parallel. Each cell 20 controls the signal on its match line 24 dependent on the result of the comparison. When the content addressing signal matches the stored content, the cell 20 causes the signal on its match line 24 to have one value. Otherwise the cell 20 causes the signal on its match line 24 to have another value. In response to the signals on the match lines 24 selection circuit 28 selects stored data for one of the cells 20, if any, that indicates a match. The selected data is supplied to data lines 26 and output from the content addressable memory. Although a specific implementation of a content addressable memory has been shown, it should be appreciated that many variations are possible. For example, instead of storing output data in the cells and using that data as output signal, the

memory may be configured to output an address of the cell 20 that has detected a match. Furthermore, instead of binary matching a more refined type of matching may be used, that allows selectable bits to be masked out of the comparison in all or part of the cells. Although a content addressable memory with one array has been shown, it should be appreciated that the content addressable memory may comprise a plurality of similar arrays.

Returning to Fig. 1, content addressable memory 120 receives combinations of signals generated by modules 10 and supplies selected information in response to these combinations if the combination matches the content of a cell 20 of content addressable memory 120. Content addressable memory 120 supplies the information to computation circuit 122 and/or handler circuit 123, where it acts as an instruction to control diagnostic operation. As used herein “diagnostic” refers to operations that may be omitted without substantially affecting the main function of the circuit, for use to gather meta-information that is descriptive of one or more aspects of the operation.

The use of content addressable memory 120 makes it possible to define a large collection of combinations of signal values that may all be used to trigger a response and optionally to adapt the response to the data pattern. In a typical example such combinations of signal values may correspond to a signal pattern with a group of signals that must have the same value, although the value is arbitrary. In more advanced patterns there may be a plurality of such groups, each with its own shared signal value. In other examples a signal pattern may be defined by a logical function of a group of bits that must have a certain value, and there may be a plurality of such groups. Normally, testing for the presence of this type of pattern can involve successive comparison with different possible signal combinations that satisfy the pattern, but this may make testing extremely slow. Alternatively, one could provide dedicated hardware, using exclusive or gates for example to test for equality of signals, but this makes testing inflexible and/or it requires excessive circuit overhead.

The use of content addressable memory 120 makes it possible to program fast detection of arbitrary signal patterns. A content addressable memory with at least two hundred and fifty six cells may be used for example. The resulting parallel comparison of many different patterns from content addressable memory 120 with the signals from circuit modules 10 yields a detection result quickly.

Programming circuit 124 may be used to set content and/or data values in content addressable memory 120. Programming circuit 124, content addressable memory 120 and circuit modules 10 may be incorporated in the same integrated circuit. In this case, programming circuit 124 may have an interface to terminals of the integrated circuit to enable

supply of programming information from outside the integrated circuit. A scan test interface may be used for example. In addition programming circuit 124 may be used to set control values for other aspects of the diagnostic monitor.

Fig. 3 shows an example of a diagnostic circuit wherein the computation circuit comprises a control circuit 30 and a first and second ALU 32, 34 (Arithmetic and Logic Unit). The handler circuit is implemented as a trigger generator 36. Control circuit 30 has a command input coupled to the output of content addressable memory 120 and outputs coupled to operation selection inputs of first and second ALU 32, 34 and to trigger generator 36. First and second ALU 32, 34 have operand inputs coupled to the circuit modules (not shown) and result outputs coupled to trigger generator 36. Trigger generator 36 has a trigger signal output, which may be coupled to an input of a circuit module for example.

In operation, control circuit 30 translates the output signal of content addressable memory 120 to operation selection signals for first and second ALU 32, 34. These selection signals may select for example whether an addition or a subtraction is to be applied to operands received from circuit modules 10, or another operation. First and second ALU 32, 34 apply the selected operation to the operands and supply the results to trigger generator 36. Trigger generator 36 determines whether the results satisfy a trigger condition and if so it generates a trigger signal. The trigger signal may be used as an interrupt signal for example, or as a signal to a logging memory (not shown) to store current data from circuit modules 10, or as an external signal supplied to a terminal of an integrated circuit in which the entire circuit is located.

The use of first and second ALU 32, 34 enables a further speed up of pattern detection for aspects of the signal pattern that can be defined in arithmetical or bit-parallel logic terms. Thus for example patterns defined in terms of conditions on address values can be verified using first and second ALU 32, 34. An address distance can be determined by subtracting address values from circuit modules 10 when a certain pattern is detected, or an absolute address can be computed from a base address and an offset received from circuit modules 10.

Trigger generator 36 may be programmed to compare the results from the first and second ALU 32, 34 with reference values, or to combine conditions detected by the first and second ALU 32, 34. Furthermore trigger generator 36 may be configured to select between different courses of action, for example between just logging data from circuit modules 10 or suspending operation of circuit modules 10.

Although an embodiment has been shown with two ALUs, with all operand inputs coupled to circuit modules 10, it should be appreciated that alternatively one ALU may be used or more than two and that ALUs may be used that have an operand input coupled to a register (not shown) for supplying a programmable reference value. Thus for example, two ALUs, each with one operand input coupled to one or more of circuit modules 10 and one coupled to a respective register, may be used to test whether an address is within a predetermined range. A multiplexer circuit (not shown) may be used to select input signals for the ALUs from signals from circuit modules 10 and/or registers with test values. Furthermore, although an embodiment with ALUs has been shown, it should be appreciated that one or more of the ALUs may be replaced by an arithmetic circuit with a smaller number of functions or a logic circuit.

Although an embodiment has been shown wherein computation circuit 122 and handler circuit 123 are controlled by signals from content addressable memory it should be appreciated that their operation may also be controlled by static control information, set by programming circuit 124 for example. This control information may be used in addition to information from content addressable memory 120.

Furthermore, in another embodiment the control connection between content addressable memory 120 and computation circuit 122 may be omitted, and content addressable memory 120 may be used to control only handler circuit 123 dependent on signal patterns. In this case, the function of computation circuit 122 may be programmed independent of the current signal pattern. However, control of the computation dependent on the signal pattern, at least partly under control of information from content addressable memory 120 provides for detection of a wider range of patterns without increasing circuit complexity. Thus for example computation circuit 122 may be made to perform computations for a test whether an address distance is in a specified range when content addressable memory supplies one output signal and computations for a test whether a sum of a base address and an offset has a certain value when content addressable memory supplies another output signal.

Fig. 4 shows an embodiment wherein buffers 40 and enable circuits 42 have been added successively between circuit modules 10 and content addressable memory 120 and handler circuit 123. In addition enable signal registers 44 are provided coupled to enable circuits 42. Buffers 40 serve to minimize the load on circuit modules 10. Buffers 40 are optional. Buffers 40 may comprise registers (not shown) to sample and hold signal values from circuit modules 10. Buffers 40 may also comprise pipelines of registers, i.e. shift

registers (not shown) to hold signal values from circuit modules 10 obtained in respective successive clock cycles and to supply these from different clock cycles in parallel to content addressable memory 120 and/or computation circuit 122. Thus, configurations of signals in different clock cycles can be detected. Optionally, such shift registers may be used without enable circuits 42 and enable signal registers 44. Further registers may be added en route from circuit modules 10 to content addressable memory 120 and handler circuit 123.

Registers 44 are programmable. In operation they store enable signals for respective bits or bit groups from circuit modules 10. Enable circuits 42 are configured to pass the signals from circuit modules 10, optionally received via buffers 40, to content addressable memory 120 and handler circuit 123 for those bits or bit groups from circuit modules 10 for which this is indicated by the enable signals from enable signal registers 44. For other bits or bit groups enable circuits 42 pass a default value, independent of the signals from circuit modules 10.

Fig. 4a shows an embodiment wherein feedback registers 46 are added in a feedback path from content addressable memory 120 to enable circuits 42. This allows for a reduction of the number of signals needed to detect configurations of signal patterns distributed over different clock cycles. In operation, content addressable memory 120 may be used to generate signals indicating that a part of a configuration has been detected and to combine these signals with later signals from circuit modules in subsequent detections. Thus there is no need to combine all signals directly from circuit modules 10 in a single time slot in order to detect a signal configuration. Feedback registers 46 may comprise shift registers that output output signals from content addressable memory 120 for different clock cycles in parallel from the feedback loop. Thus configurations can be detected that extend over a longer period of time.

Fig. 4a furthermore shows further feedback registers 46 in a further feedback path from arithmetic circuit 122 to enable circuits 42, from where they may be applied to content addressable memory 120 and/or arithmetic circuit 122. This similarly allows for a reduction the number of signals needed to detect configurations of signal patterns distributed over different clock cycles. In operation, results from arithmetic operations (e.g. comparison results, or computed differences or sums) from computation circuit 122 may be combined with later signals from circuit modules in subsequent detections. Thus there is no need to combine all signals directly from circuit modules 10 in a single time slot in order to detect a signal configuration. Further feedback registers 48 may comprise shift registers that output output signals from computation circuit 122 for different clock cycles in parallel from the

feedback loop. Thus configurations can be detected that extend over a longer period of time. The feedback loop and the further feedback loop may be provided in combination, as shown, or individually, with or without enable circuits 42.

In an embodiment programming circuit 124 is configured to set signal values in enable signal registers 44. In a further embodiment the enable signals for the signals that are passed to computation circuit 122 may be controlled from the output of content addressable memory 120.

Although an embodiment has been shown wherein enable circuits 42 are used before both addressable memory 120 and handler circuit 123, it should be appreciated that instead enable circuits may be used only in front of one of addressable memory 120 and handler circuit 123, or only before part of the inputs of addressable memory 120 and handler circuit 123. Instead of buffers 40, or in addition to these buffers a multiplexing circuit may be used that makes it possible to select which signals from circuit modules 10 will be coupled to content addressable memory 120 and or handler circuit 123. A fixed programmable selection may be used. In another embodiment part or all of the selection of the multiplexers may be controlled from the output of content addressable memory 120.

Fig. 5 shows an embodiment of the computation circuit wherein multiplexers 50 are used in front first ALU 32. Multiplexers 50 have inputs coupled to various outputs of circuit modules 10 (not shown) optionally via shift registers in the buffers (not shown) and optionally to a feedback from content addressable memory 120. Although three such inputs are shown for each multiplexer 50, it should be appreciated that other numbers of inputs may be used, typically many more. Furthermore, the Figure shows registers 52 coupled to inputs of multiplexers 50.

Each multiplexer 50 has an output for supplying a multi-bit signal to a respective operand input of ALU 32. Although not shown a further ALU or other circuits may be present, and these may also have inputs coupled to the circuit modules and/or registers via multiplexers 50. Multiplexers 50 have control inputs (not shown) coupled to programming circuit 124 (not shown) to control which of the inputs will be coupled to the operand input. Similarly, registers 52 may be coupled to programming circuit 124 (not shown) for setting the content of registers 52. In this way the selection of input signals to ALU 32 may be controlled. In a further embodiment, the control input of multiplexers 50 is at least partly controlled from the output of content addressable memory 120 (not shown). In this way the input selection can be made dependent on signal configurations.

In an embodiment one or more multiplexers with corresponding control registers may be used to select input signals for content addressable memory 120. Thus, a selection may be made between different signals from circuit modules 10 and optionally between different feedback signals from content addressable memory 120 itself.

5 Fig. 6 shows an embodiment wherein diagnostic monitor 12 comprises a clock counter 60 coupled to content addressable memory 120 and/or computation circuit 122 via enable circuit 42. This makes it possible to use clock count values in the detection of signal configurations. Thus for example, it may be determined whether an event occurs within a predetermined number of clock cycles from another event. In an embodiment content
10 addressable memory 120 has an output coupled to a reset input of clock counter 60 (not shown). This makes it possible to reset the clock count value in clock counter 60 when a first event is detected, for use in the detection of a second event. The embodiment of Fig. 6 may be combined with one or more of the feedback loops of the embodiment of Fig. 4a.

Although an embodiment has been shown with a computation circuit 122, it should be
15 appreciated that in another embodiment this circuit may be omitted. In this case handler circuit 123 may be controlled only by the content addressable memory, or alternatively signals from circuit modules 10 may be coupled to handler circuit directly. However, the use of a computation circuit has the advantage that a wider range of signal patterns can be detected, including signal patterns that involve the presence of numerical relations between
20 parts of the signals.

Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims. In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a
25 plurality. A single processor or other unit may fulfill the functions of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage. A computer program may be stored/distributed on a suitable medium, such as an optical storage medium or a solid-state medium supplied together with or as part of other hardware, but may
30 also be distributed in other forms, such as via the Internet or other wired or wireless telecommunication systems. Any reference signs in the claims should not be construed as limiting the scope.

CLAIMS:

1. A data processing circuit comprising logic circuitry (10) and a diagnostic monitor (12), the diagnostic monitor (12) comprising:

- a programmable content addressable memory (120) with a content addressing input coupled to the logic circuitry (10);

5 - a diagnostic handling circuit (123) with a control input coupled to an output of the content addressable memory (120), configured to control a diagnostic action dependent on the output of the content addressable memory (120).

2. A data processing circuit according to claim 1, wherein the diagnostic
10 handling circuit (123) is configured to trigger logging of data and/or to trigger diagnostic action and/or to trigger suspension of operation dependent on the output of the content addressable memory (120).

3. A data processing circuit according to claim 1, comprising a computation
15 circuit (122) configured to perform a computation applied to at least one operand constructed from signals from the logic circuitry (10), the computation circuit (122) having an output coupled to the diagnostic handling circuit (123), the diagnostic handling circuit (123) being configured to control the diagnostic action additionally dependent on a result of the computation.

20

4. A data processing circuit according to claim 3, wherein the output of the content addressable memory (120) is further coupled to a control input of the computation circuit (122), the computation circuit (122) being configured to select a computation type of the computation dependent on the output of the content addressable memory (120).

25

5. A data processing circuit according to claim 1, wherein the diagnostic monitor (12) comprises a multiplexing circuit coupled between the logic circuitry (10) and the content addressable memory (122).

6. A data processing circuit according to claim 3, wherein the diagnostic monitor (12) comprises a multiplexing circuit (50) coupled between the logic circuitry (10) and the computation circuit (122).

5 7. A data processing circuit according to claim 1 comprising a buffer (40) coupled between the logic circuitry (10) and the content addressable memory (120).

8. A data processing circuit according to claim 7, wherein the buffer (40) comprises a register for supplying captured signal values from the logic circuitry (10) to the
10 content addressable memory (120).

9. A data processing circuit according to claim 8, wherein the register is a shift register configured to provide differently delayed signal values in parallel to the content addressable memory (120).
15

10. A data processing circuit according to claim 1, wherein the diagnostic monitor (12) comprises an enable circuit (42) coupled between the logic circuitry (10) and the content addressable memory (120) and configured to selectively enable the signals from the logic circuitry (10) for passing to the content addressable memory (120).
20

11. A data processing circuit according to claim 1 comprising a feedback loop from an output of the content addressable memory to its input, the feedback loop comprising a feedback register (46) for holding feedback signals.

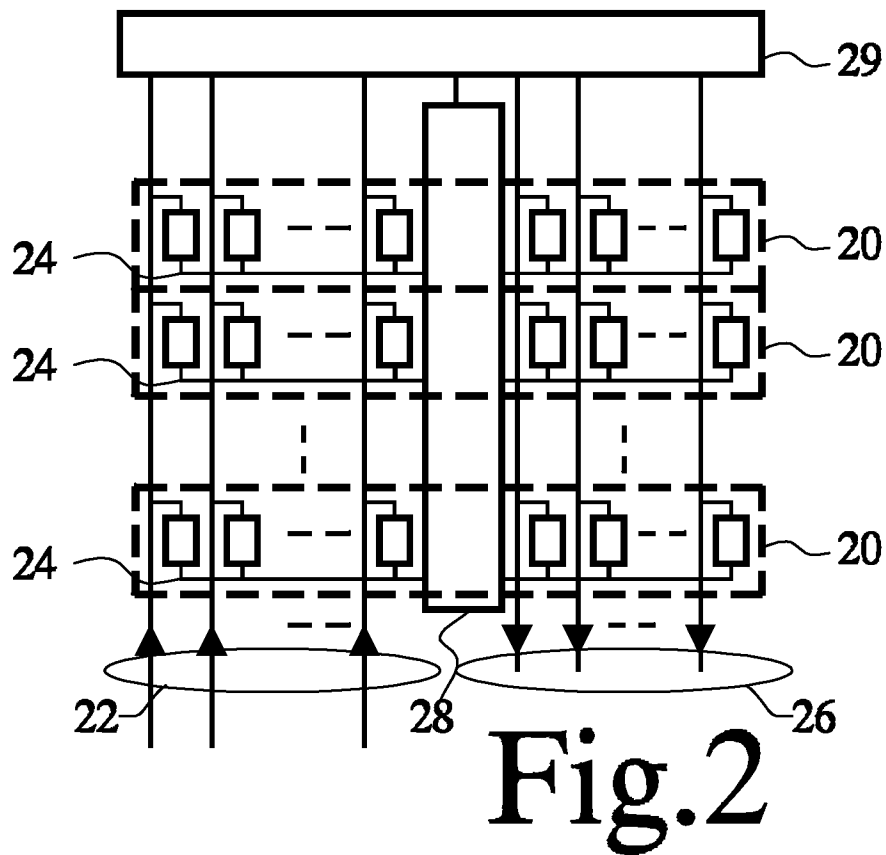
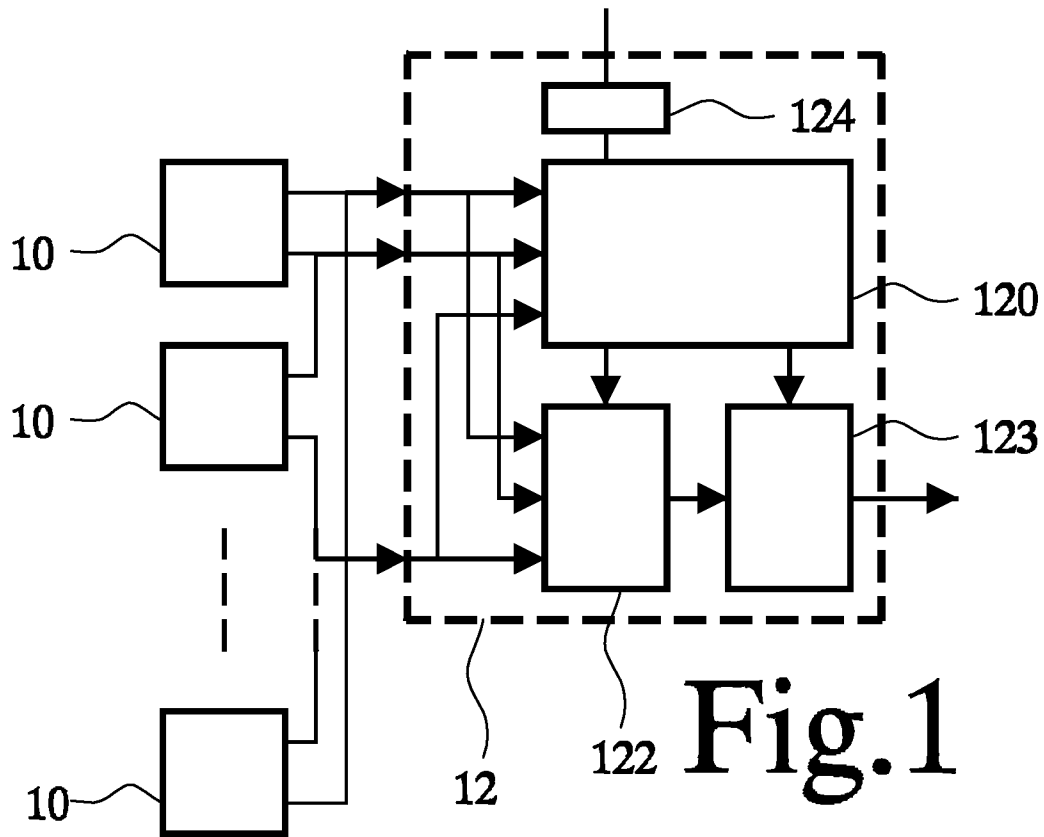
25 12. A data processing circuit according to claim 3 wherein the diagnostic monitor (12) comprises a feedback loop from an output of the computation circuit (122) to an input of the content addressable memory (120) and/or the computation circuit, the feedback loop comprising a feedback register (48) for holding feedback signals.

30 13. A data processing circuit according to claim 1, wherein the content addressable memory (120) comprises an array of associative memory cells (20) and a plurality of parallel content lines (22) each coupled in parallel to the associative memory cells (20).

14. A data processing circuit according to claim 3, wherein the diagnostic monitor (12) comprises a clock counter (60) with an output coupled to an input of the content addressable memory (120) and/or the computation circuit (122).

- 5 15. A method of monitoring operation of logic circuitry (10), the method comprising:
- providing a content addressable memory (120) with content addressing inputs coupled to the logic circuitry (10);
 - programming a plurality of signal patterns into the content addressable
 - 10 memory (120);
 - activating the logic circuitry (10);
 - using outputs of the content addressable memory (120) in response to signals from the logic circuitry (10) to control diagnostic actions.

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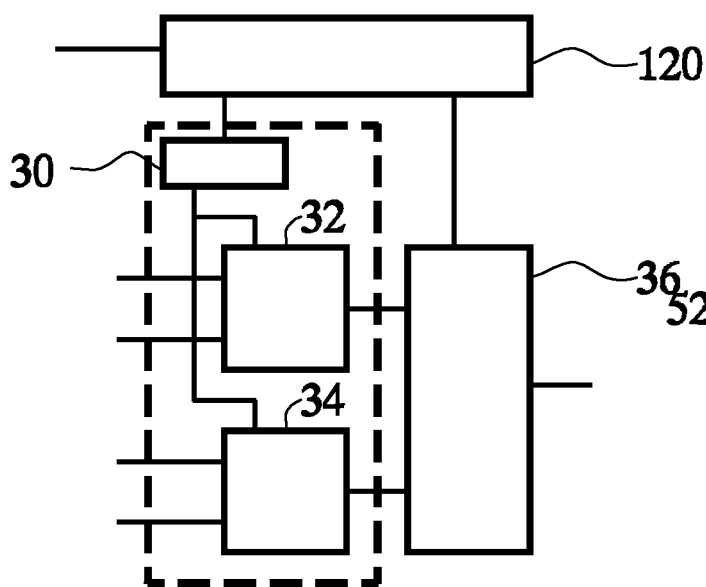


Fig.3

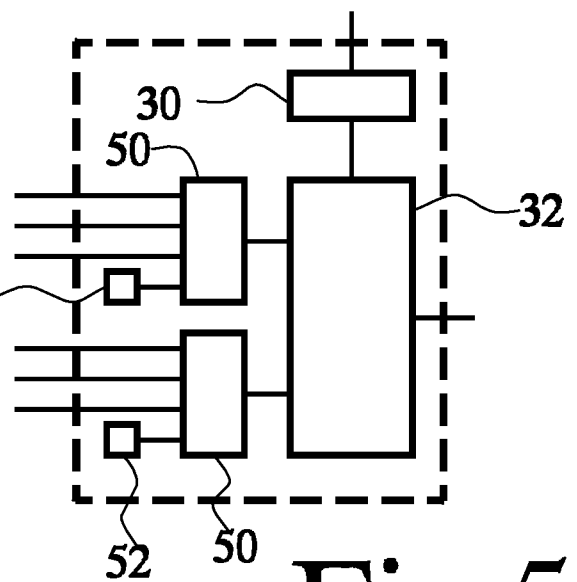


Fig.5

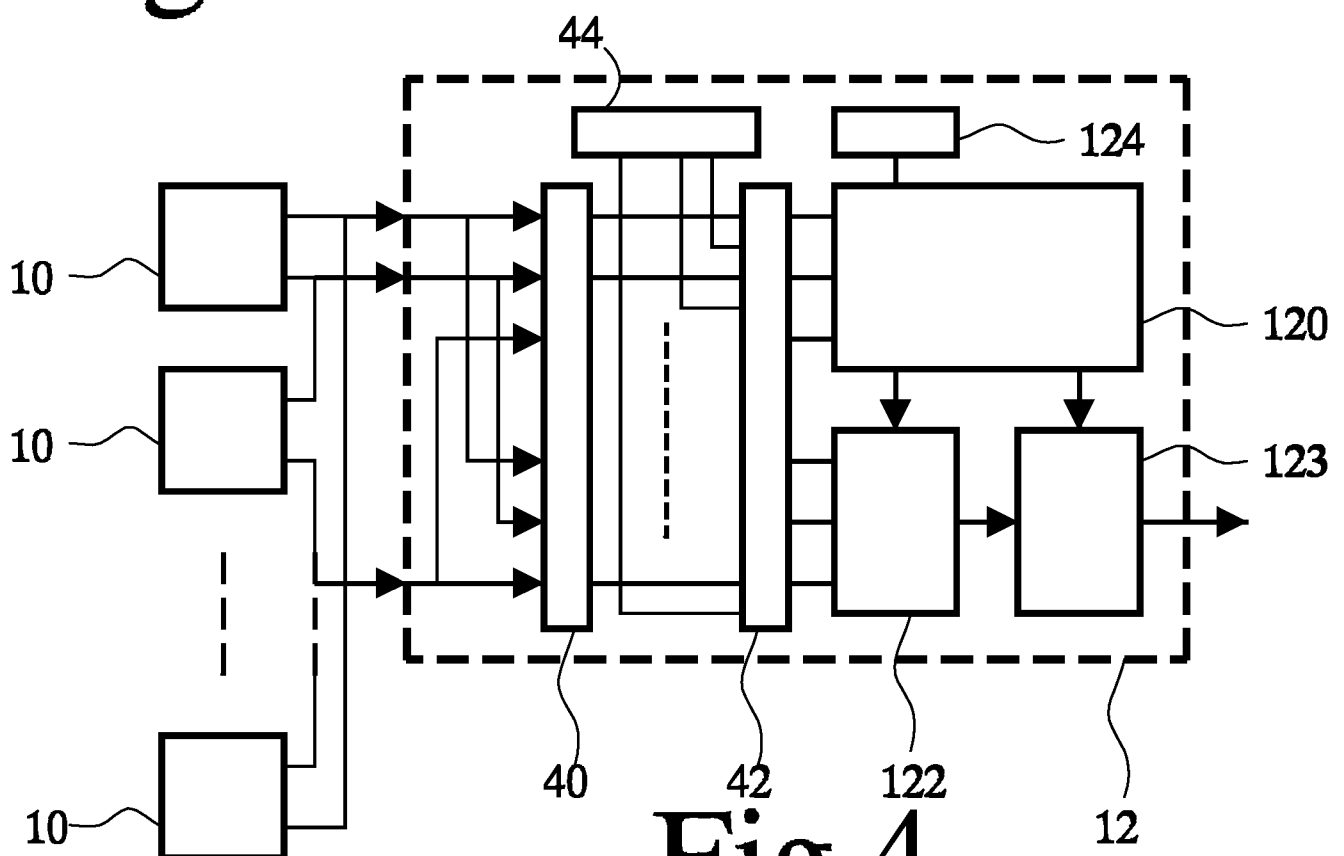


Fig.4

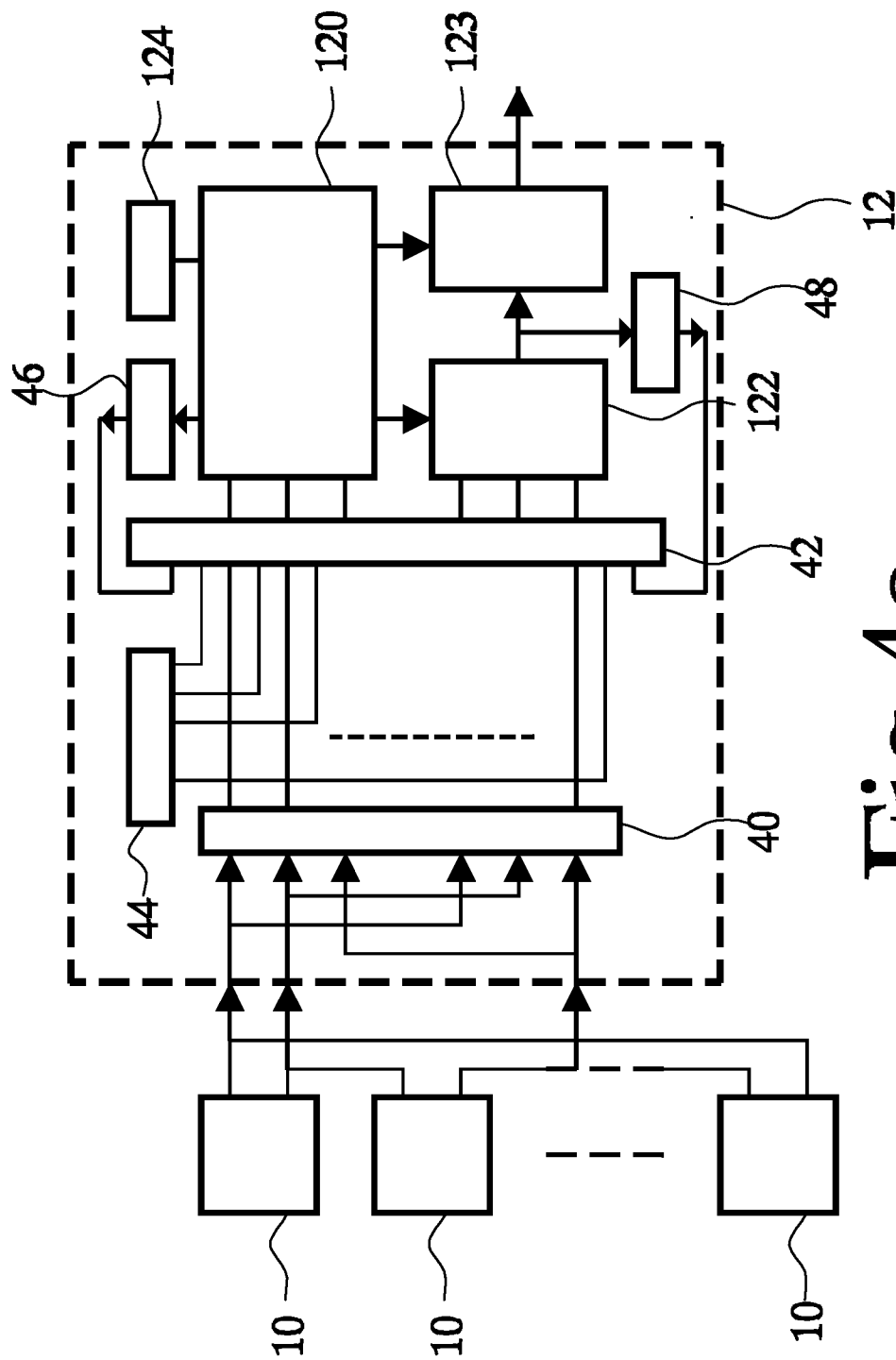


Fig. 4a

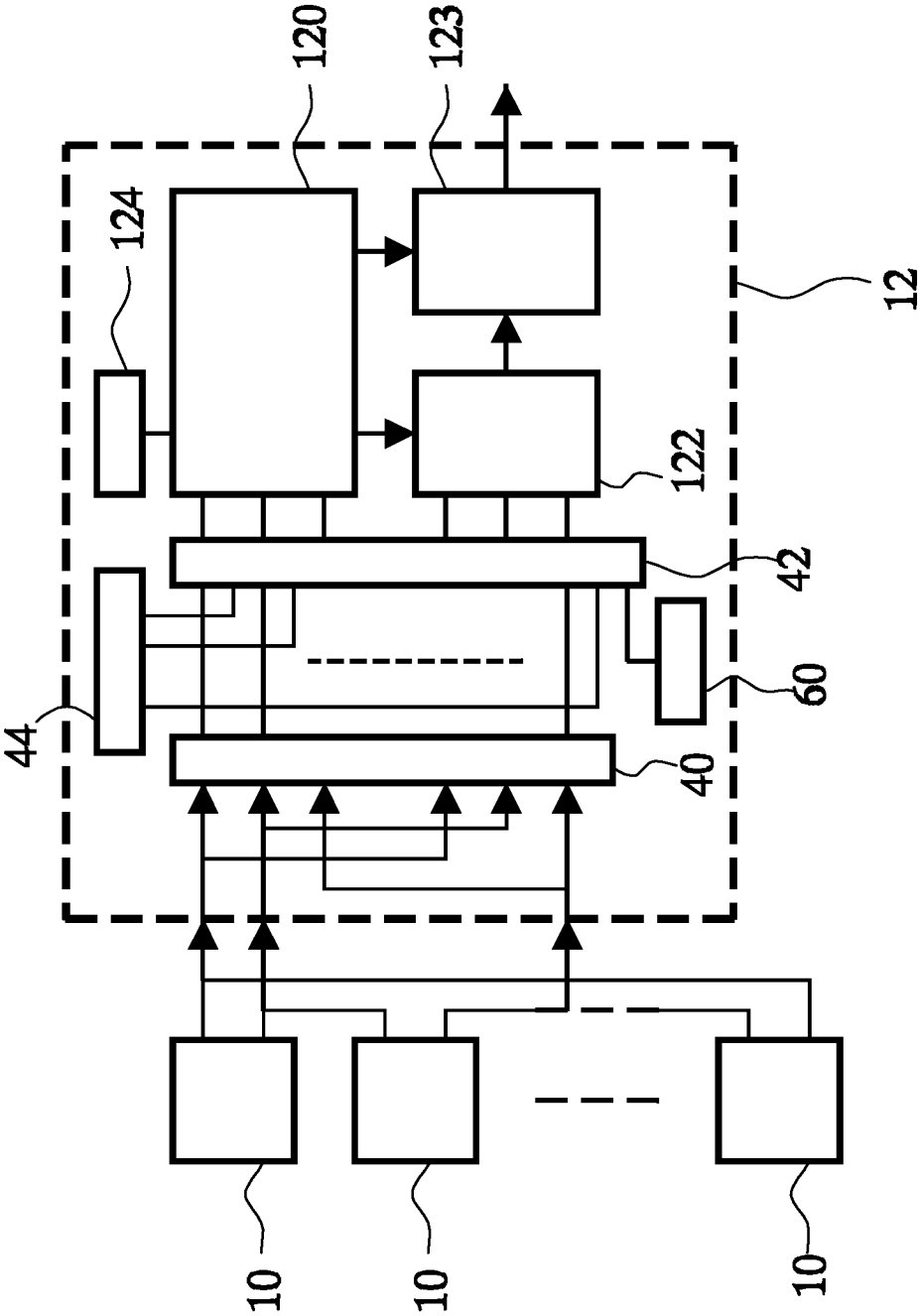


Fig. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/054958

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F11/22

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 674 089 A (PORET MARK [US] ET AL) 16 June 1987 (1987-06-16) abstract figures 1-4 column 2, line 35 - column 9, line 43	1-15
X	EP 0 455 946 A (IBM [US]) 13 November 1991 (1991-11-13) abstract figures 1,2 column 3, line 11 - column 6, line 30 ----- -/--	1,2,5, 7-10,13, 15

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search

19 January 2010

Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2009/054958

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 456 994 A (SEGARRA GERARD [FR]) 26 June 1984 (1984-06-26) abstract figures 1,2 column 3, line 42 - column 5, line 57 -----	1,2,5, 7-10,13, 15
A	US 5 125 098 A (BURROWS JAMES L [US]) 23 June 1992 (1992-06-23) the whole document -----	11

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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Patent document cited in search report		Publication date		Patent family member(s)	Publication date
US 4674089	A	16-06-1987	JP	61241841 A	28-10-1986
EP 0455946	A	13-11-1991	JP	4229340 A	18-08-1992
US 4456994	A	26-06-1984	DE	3001557 A1	14-08-1980
			FR	2448190 A1	29-08-1980
			GB	2040520 A	28-08-1980
			JP	55102056 A	04-08-1980
US 5125098	A	23-06-1992	NONE		