(54) Title: A VITERBI DETECTOR

(57) Abstract

A detector circuit for detecting a data sequence from an input sequence of data. The detector circuit includes a branch metric unit for computing a plurality of values, the values corresponding to the squared errors between input values to the circuit and all possible noiseless responses. The detector circuit also includes a Viterbi circuit responsive to the branch metric unit, the Viterbi circuit for computing the data sequence.
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STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH
This invention was made with government support under NSF Grant No. ECD8907068. The government may have certain rights in the invention.

BACKGROUND OF THE INVENTION

Field of the Invention
The present invention is directed generally to Viterbi detectors, and, more particularly, to a detector circuit that determines squared errors.

Description of the Background
In magnetic recording devices, digital data is converted into a signal that is recorded by a write head on a magnetic medium, such as a computer disk or a magnetic-coated tape. When the data is read from the magnetic medium by a read head, the data is distorted due to the presence of additive white Gaussian noise, jitter, and intersymbol interference (ISI). These distortions may also be present in a waveform that is transmitted through a communication channel for demodulation, equalization and detection by a receiver.

A reproduction equalizer is typically employed in magnetic recording systems and communication channels to shape the received waveform such that the effects of distortion due to noise and ISI are minimized. In addition, equalization can be used to shape the overall channel response to have a controlled nonzero ISI. A
common type of detector used for decoding the transmitted symbols after they are corrupted by a controlled ISI pattern and noise is a Viterbi detector. A Viterbi detector employs the Viterbi Algorithm, which was first proposed as an algorithm for decoding convolutional codes in A. J. Viterbi, "Error Bounds for Convolutional Codes and an Asymptotically Optimum Decoding Algorithm", IEEE Trans. Inform. Theory, Vol. IT-13, No. 2, pp. 260-69, April 1967.


After equalization, the overall magnetic recording channel functions like a convolutional coder. One common equalization target for the controlled ISI is called partial response ("PR") coding. PR coding is a type of convolutional coding in which one of a number of output signals is chosen in response to each bit of input data. The choice is made based on the current state of the encoder and the input bit. Thus, the input data is distributed over a greater number of symbols when encoded. A Viterbi detector must be able to determine whether the data sequence that is received is the same as the sequence that was encoded by the PR encoder.

A common Viterbi detection routine, termed "maximum likelihood" ("ML") detection, uses a trellis arrangement to compare a received sequence of data with all possible permitted outcomes of the data by examining the distances along paths in the trellis of the values of the reproduced signals assuming no noise (target values) with respect to the actual received sequence. The trellis is arranged such that a traversal of the nodes and edges of the trellis represents one or more responses of the PR encoder to a sequence of input data. The distance traversed is defined as the minimum sum of the squared differences between sequences of signals assuming no noise (target values) and
the actual received sequence. The minimum sum of the
squared differences results from two paths that diverge
from a common state on a trellis and converge to a common
state.

5 A Viterbi detector uses the maximum likelihood trellis
arrangement by projecting the possible states of the
encoder onto the trellis. The detector traverses the paths
through the trellis and selects the paths with the smallest
cumulative distance, which are the most likely, or
probable, paths. The paths that are less likely are
discarded.

10 It is typical for a Viterbi detector to select a
short, noiseless PR target of length N and to equalize the
data storage channel to match the target because the number
of trellis nodes is $2^{N-1}$. To eliminate the squaring, the
target is usually chosen to have values of 0, +1, -1, +2,
or -2. If the noiseless values are from the set {-2, -1,
0, 1, 2}, then a simplification for computing and comparing
squared errors can be realized by removing the input signal
squared term common to all squared errors at a given sample
time. In this way, the squaring of the difference is
reduced to a shift and an add or a subtract. In that case
each trellis node requires only an add/compare/select
("ACS") unit. Because of the simplicity of the targets,
25 they can be built into the ACS unit of the Viterbi detector
with little or no penalty in speed or die area. However,
there is a penalty in terms of error rate that is caused by
using a linear equalizer to force the binary data storage
channel response to fit into the target response. The use
30 of generalized target values for the trellis requires a
large number of computations, including multiplications, by
the detector circuit such that it is difficult to operate
such detectors in real time.

Therefore, there is a need for a detector circuit that
35 uses generalized target values for the trellis and can thus
adapt to the natural response of the actual binary data
storage channel with little or no penalty in speed or die
area. It would even be desirable to have these generalized response values be a nonlinear function of the N transmitted symbols. Such a detector circuit will require less equalization and result in a lower error rate.

5 SUMMARY OF THE INVENTION

The present invention is directed to a detector circuit for detecting a data sequence from an input sequence of data. The detector circuit includes a branch metric unit for computing a plurality of values, the values corresponding to the squared errors between input values to the circuit and all possible noiseless responses. The detector circuit also includes a Viterbi circuit responsive to the branch metric unit, the Viterbi circuit for computing the data sequence.

15 The present invention represents a substantial advance over prior detector circuits. Because the present invention determines the squared errors for generalized target values, the present invention has the advantage that it can adapt to the natural response of the actual binary channel. The present invention has the further advantage that it can use generalized target values that are closer to the natural response of the actual binary channel with little or no penalty in speed or die area. The present invention also has the advantage that the generation of a branch metric or the use of a look-up table with stored squared errors can compensate for non-linear intersymbol interference. The present invention also contemplates use of a pipelined implementation so that the delay time associated with the branch metric unit or with the look-up table is not part of the delay of the Viterbi ACS unit.

30 Those advantages and benefits of the present invention, and others, will become apparent from the Detailed Description of the Invention hereinbelow.

BRIEF DESCRIPTION OF THE DRAWINGS

35 For the present invention to be clearly understood and
readily practiced, the present invention will be described in conjunction with the following figures, wherein:

FIG. 1A illustrates an example of a portion of a prior art binary storage channel;
5 FIGS. 1B and 1C illustrate pulse responses before and after the forward equalizer, respectively;
FIG. 2A illustrates a preferred embodiment of a portion of a binary storage channel of the present invention;
10 FIGS. 2B and 2C illustrate pulse responses before and after the forward equalizer, respectively;
FIG. 3A illustrates a preferred embodiment of a portion of a binary storage channel of the present invention;
15 FIGS. 3B and 3C illustrate pulse responses before and after the forward equalizer, respectively;
FIG. 4A illustrates a preferred embodiment of a portion of a binary storage channel of the present invention;
20 FIG. 4B illustrates a pulse response after the continuous time equalizer;
FIG. 5 illustrates a preferred embodiment of a detector circuit of the present invention;
FIG. 6 illustrates another preferred embodiment of a detector circuit of the present invention;
25 FIG. 7 illustrates a magnetic recording channel system in which the detector circuit of the present invention may be used;
FIG. 8 illustrates another preferred embodiment of the detector circuit of the present invention;
30 FIG. 9 illustrates a preferred embodiment of the branch metric unit of FIG. 8;
FIG. 10 illustrates another preferred embodiment of the branch metric unit of FIG. 8;
35 FIG. 11 shows the Euclidean distance branch metric approximated by three lines of slope $2^n$, where $n = -1, 1, \text{ and } 2$;
FIGS. 12 and 13 illustrate the performance of the linear branch metric approximation using data collected from a spin stand; and

FIG. 14 illustrates an embodiment of a portion of the branch metric unit 202.

DETAILED DESCRIPTION OF THE INVENTION

It is to be understood that the figures and descriptions of the present invention have been simplified to illustrate elements that are relevant for a clear understanding of the present invention, while eliminating, for purposes of clarity, many other elements found in a typical detector circuit. Those of ordinary skill in the art will recognize that other elements are desirable and/or required to implement the present invention. However, because such elements are well known in the art, and because they do not facilitate a better understanding of the present invention, a discussion of such elements is not provided herein.

FIG. 1A illustrates an example of a portion of a prior art binary storage channel 10. An analog signal \( r(t) \) is input to the channel 10. The signal \( r(t) \) is generated by, for example, a disk drive read head followed by a preamplifier. The signal \( r(t) \) is input to a continuous time low pass filter 12. The filter 12 is typically an anti-aliasing filter that produces a filtered signal \( s(t) \).

The signal \( s(t) \) is sampled by a sampling device 14 to produce a sampled pulse signal \( s_n \).

The noiseless pulse response 16 of the sampled signal \( s_n \) is illustrated in FIG. 1B as a function of the symbol sample times. The sampled signal \( s_n \) is input to a forward equalizer 18 to produce a pulse signal \( r_n \). The equalizer 18 can be, for example, an IIR filter or an FIR filter. The equalizer 18 shapes the signal \( r_n \) to "slim" it, i.e., to \( r_n \) to decrease the extent of the intersymbol interference of the signal and to force the nonzero values to selected target noiseless values. The noiseless pulse response 20
of the signal \( r_n \) is illustrated in FIG. 1C as a function of the symbol sample times. In a typical equalizer, the noiseless targets, as shown in FIG. 1C, are chosen to have values of -1, +1, and 0. The pulse signal \( r_n \) is input to a detector circuit 22, which typically includes a circuit that uses a variation of the Viterbi Algorithm. The circuit which uses the Viterbi Algorithm typically has the noiseless targets built into the add/compare/select circuits.

FIG. 2A illustrates a preferred embodiment of a portion of a binary channel 24 of the present invention. As in FIG. 1A, an analog signal \( r(t) \) is input to the channel 24. The signal \( r(t) \) is input to a continuous time low pass filter 26. The filter 26 can be, for example, an anti-aliasing filter that produces a filtered signal \( s(t) \). The signal \( s(t) \) is sampled by a sampling device 28 to produce a sampled pulse signal \( s_n \).

The noiseless pulse response 30 of the sampled signal \( s_n \), as illustrated in FIG. 2B as a function of the symbol sample times, is identical to the pulse response in FIG. 1B. The sampled signal \( s_n \) is input to a forward equalizer 32 to produce a pulse signal \( r_n \). The equalizer 32 can be, for example, an IIR filter or an FIR filter. As in FIG. 1A, the equalizer 32 limits the number of nonzero ISI samples of the pulse signal \( r_n \). The noiseless pulse response 34 of the signal \( r_n \) is illustrated in FIG. 2C as a function of the symbol sample times. As can be seen in FIG. 2C, the noiseless targets have a better match to the actual channel than the match shown in FIG. 1C. The better match results in a simpler circuit structure for the equalizer 32. The better match also results in less noise gain, resulting in a lower error rate by a detector circuit 36.

FIG. 3A illustrates a preferred embodiment of the present invention. A binary channel 38 is constructed similarly to the binary channel 24 of FIG. 2A. However, an equalizer 40 provides a further refined match of the target
to the $r_n$ signal by extending to more nonzero ISI samples, which results in a lower error rate by the detector circuit 36. The noiseless response 42 can be seen in FIG. 3C.

FIG. 4A illustrates another preferred embodiment of the present invention. A binary channel 44 is constructed similarly to the binary channel 24 of FIG. 2A and the binary channel 38 of FIG. 3A. However, due to the reduced requirements of generating the target noiseless pulse responses, the forward equalizer is greatly simplified and may be merged with the function of the low pass filter. Thus, a continuous time equalizer 46 filters the analog signal $r(t)$ and shortens the extent of the ISI before sampling by the sampling device 28. In operation, the noiseless pulse response 48, as seen in FIG. 4B, is similar to that of FIG. 3C.

If the signal $r_n$ of FIGS. 2A, 3A, and 4A was input to a conventional detector circuit, the detector circuit would have to perform complex mathematical calculations, including multiplications, on the signal $r_n$, and the detector circuit's implementation would be different. The detector circuit would require complex circuitry that would consume large amounts of integrated circuit die area and power. Thus, the detector 36, in a preferred embodiment of the present invention, is capable of operating on the signal $r_n$ with little or no performance penalty. Also, the detector 36, in a preferred embodiment, is constructed such that a small amount of additional die area is consumed by the added circuitry.

FIG. 5 illustrates a preferred embodiment of the detector circuit 36. The detector circuit 36 could be used in the binary channel as illustrated in FIGS. 2A, 3A, or 4A, or in a prior art binary channel, such as that illustrated in FIG. 1A. An M-bit binary number, which is input to the circuit 36, is generated by an analog to digital (A/D) converter 52 directly. However, it can be understood by those skilled in the art that the M-bit binary number may also be the output of an equalizer which
has a digital filter circuit. In such an arrangement, the 
A/D converter 52 would convert the signal before the 
digital equalizer.

The input signal is converted to an M-bit number. M 
is typically on the order of 5 to 6 bits. The M-bit number 
is latched into latches 54. The outputs of the latches 54 
are connected to an error output circuit 56 and a decoder 
circuit 58. The decoder circuit 58 decodes the M-bit 
number into 2^M signals, only one of which is high. The high 
signal corresponds to the binary number indicated by the M- 
bit number. The outputs of the decoder circuit 58 are 
connected to latches 60. The latches 60 operate to 
pipeline the decoding operation and thus remove the delay 
due to the decoding operation from subsequent operations.

However, the latches 60 may be omitted if it is desired 
that the decoding operation not be pipelined.

The decoded 2^M signals at the output of the latches 60 
are available as inputs to a storage device 62. The 
storage device 62 operates as a look-up table in which the 
resulting squared error computations between all possible 
input values, of which there are 2^M possible values, and all 
possible noiseless responses, of which there are 2^N possible 
values, where N is the number of non-zero ISI terms 
remaining at the input to the detector circuit, are stored.

For example, for a detector circuit that is constructed 
for an ISI pattern that is 4 symbols in length, there will 
be 16 possible noiseless values.

The squared errors are stored as P-bit numbers in the 
storage device 62. Typical values for P are 4 to 6 bits.

The values in the storage device 62 are arranged in rows 
and columns such that the signals from the decoder circuit 
58 are used as addresses to determine a row of values to be 
read from the storage device. Each row contains the 
squared error between the storage device 62 input value, or 
address, and every one of 2^M possible noiseless outputs.

Thus, there is one column for each noiseless value, or, in 
Viterbi Algorithm terminology, for each branch of a Viterbi
trellis. $P^2$ bits are therefore simultaneously read out of the storage device 62 for each input symbol.

The storage device 62 may be any type of conventional memory device known in the art. For example, the storage device 62 may be a random access memory (RAM), a read only memory (ROM), or a magnetic disk or tape device. In a preferred embodiment, the storage device 62 is a RAM with a write port and a read port. The input value is used to address the RAM through the read port and the write port can be used simultaneously or when the channel is idle, to update the values of the squared errors which are stored in the storage device 62. The stored values can be updated as necessary using the write port. For example, the stored values can be updated for each head, for each access to different zones of the magnetic recording medium from which the data is being read, etc.

The outputs of the storage device 62 are connected to a Viterbi circuit 64. The Viterbi circuit 64 can be of any type of circuit that implements any of a number of variations of the Viterbi Algorithm. A preferred embodiment of the Viterbi circuit 64, as shown in FIG. 5, is described hereinbelow.

The outputs of the storage device 62 are connected to a set of latches 66. The latches 66 act as a pipeline register. Thus, all of the squared error calculations have taken place in a pipelined manner and, other than an increase in the overall latency of the detector circuit 36 by 1 or 2 clock ticks, there is no adverse impact on the maximum clocking speed of the detector circuit 36. The latches 66 may be omitted from the Viterbi circuit 64 if it is desired that the Viterbi operation not be pipelined.

The outputs of the latches 66 are connected to a Viterbi add/compare/select ("ACS") circuit 68. In the preferred embodiment shown in FIG. 5, the ACS circuit 68 has an array of $2^{n-1}$ add/compare/select ("ACS") units. Each ACS unit is connected to and operates on the two squared errors associated with a node in the Viterbi trellis. The
internal structure of the ACS circuit 68 must be such that accumulated path costs may be passed between the appropriate trellis nodes. The ACS decisions computed by the ACS circuit 68 are stored in a set of latches 70. The latches 70 may be omitted from the Viterbi circuit 64 if it is desired that the Viterbi operation not be pipelined.

The outputs of the latches 70, which correspond to the ACS decisions, are connected to a Viterbi path trace-back circuit 72. The Viterbi path trace-back circuit 72 traces back through the Viterbi trellis and computes a final decision of the value that was input to the storage device 62. The final decision is output from the Viterbi path trace-back circuit after R clock ticks, where R is the number of stages in the circuit 72. The number of stages in the circuit 72 is dependent on the decision depth of the Viterbi trellis. A typical value for R could range from 10 to 16. The final decision is latched into latch 74. The latch 74 may be omitted from the Viterbi circuit 64 if it is desired that the Viterbi operation not be pipelined.

The final decision output appears at the output of the detector circuit 36 after R + 3 clock ticks from the time the input value is presented to the storage device 62 in the embodiment shown in FIG. 5, in which the set of latches 66, the set of latches 70, and the latch 74 act as pipeline registers.

The error output circuit 56 operates to determine the error between the noiseless ideal input and the actual observed input to the detector. The error output signal from the error output circuit 56 is important for decision-directed timing circuits, decision-directed amplitude control circuits, decision-directed DC offset control, and least mean squares ("LMS") adaption of filter coefficients and noiseless values. It can be understood by those skilled in the art that the error output circuit 56 can be implemented using any type of error calculation circuit. However, a preferred embodiment, as illustrated in FIG. 5, is described hereinbelow.
A delay circuit 76 delays the input M-bit word by the appropriate number of clock ticks, which is \( R + 3 \) in the pipelined implementation illustrated in FIG. 5, such that the current binary decision output bit corresponds to the appropriate input sample. An N-stage shift register 78 stores the current binary decision output and the previous \( N - 1 \) binary decision output bits. Because the number of terms in the ISI is \( N \), all that is needed is a block of \( N \) binary decision outputs to determine the noiseless value that should have been observed at the input to the detector.

The output of the shift register 78 indicates which noiseless value to subtract from the input value to determine the error output. The noiseless values are stored in a storage device 80. The storage device 80 stores the noiseless values as an array, which consists of one M-bit entry for every possible output pattern of depth \( N \). The output of the shift register 78 acts as an address which determines which M-bit noiseless value appears at the output of the storage device 80. The contents of the storage device 80 should correspond to the squared error look-up table which is stored in the storage device 62.

The storage device 80 may be any type of conventional memory device. For example, the storage device 80 may be a random access memory (RAM), a read only memory (ROM), or a magnetic disk or tape device. In a preferred embodiment, the storage device 80 is a RAM with a write port and a read port. The M-bit value from the shift register 78 outputs is used to address the RAM through the read port and the write port can be used to update the values of the noiseless values to correspond to the values in the squared error look-up table that is stored in the storage device 62.

The noiseless value that is output from the storage device 80 is stored in a latch 82. The output of the latch 82 is connected to an adder circuit 84. The adder circuit 84 subtracts the noiseless value from the observed value to
generate the error output signal. An alternative arrangement of the error output circuit 56 can be constructed such that the storage device 80 would store all errors that correspond to the input signal and the last N decision bits. Such an arrangement would require the elimination of the adder circuit 82 but would necessitate a larger storage device 80.

FIG. 6 illustrates another preferred embodiment of a detector circuit 86. The detector circuit 86 could be used in place of the detector circuit 36 in FIGS. 2A, 3A, and 4A, or could be used in a prior art binary channel. A flash analog to digital ("A/D") converter circuit 88 accepts the analog input signal. The signals input to the A/D converter circuit 88 are converted to "thermometer" code, in which the signals that are below a threshold level are converted to "1's", and the signals that are above the threshold level are converted to "0's". The A/D converter circuit 88 converts the "1's" and "0's" into a one of 2^n signal in which the only line that is a "1" is at the point where the "thermometer" code transitions from a "1" to a "0". The outputs of the A/D converter circuit 88 are connected to a set of latches 90. The 2^n outputs of the A/D converter circuit 88 correspond to the outputs of the decoder circuit 58 of the preferred embodiment shown in FIG. 5. Thus, there is no need for a decoder circuit in the embodiment shown in FIG. 6. However, an encoder circuit 92 is needed to compress the 2^n outputs of the latches 90 to M signals for use in the error output circuit 56. In the implementation of the preferred embodiment shown in FIG. 6, the error output circuit 56, the storage device 62, and the Viterbi circuit 64 are constructed in an identical manner to those illustrated in FIG. 5.

FIG. 7 illustrates a magnetic recording channel system 94 in which the detector circuit of the present invention may be used. The system 94 includes a write circuit 96, a read circuit 98, and a head/disk assembly 100. The disk may be any type of magnetic recording medium that is known
in the art, such as a hard disk or a tape with a magnetic coating. The head/disk assembly 100 may include a read/write head or may contain separate read and write heads.

The write circuit 96 functions to convert a sequence of data bits that are to be written onto a recording medium in the head/disk assembly 100. The sequence of bits that are to be written on the medium is input to an error correction code ("ECC") circuit 102. The outputs of the ECC circuit 102 represent data blocks and ECC blocks, which are input to a coder circuit 104. The coder circuit 104 outputs the data blocks and ECC blocks as coded symbols, such as, for example, symbols selected from the set of \{+1,-1\}. The symbols are input to a write pre-compress circuit 106, which time shifts the symbols. A current waveform circuit outputs a current waveform to the head/disk assembly, which is written by the head onto the magnetic medium.

The read circuit 98 operates to process information that is read from the head/disk assembly 100 and convert the information into a sequence of data bits that was originally input to the magnetic recording system 94. A preamplifier 110 operates similarly to the low pass filters 12 and 26 as shown in FIGS. 1A, 2A, and 3A to filter all but the channel response, any nonlinearities, any media noise, and any white noise from the signal that is read from the head/disk assembly 100. An equalizer 112 operates similarly to the equalizers 18 and 32 of FIGS. 1A, 2A, and 3A to limit the white noise bandwidth of the signal from the preamplifier 110 and to "slim" the pulse signal from the preamplifier 100 to decrease the intersymbol interference of the signal. A narrow target response pulse is generated by the equalizer 112.

A detector circuit 114, which is constructed as illustrated by the detector circuit 36 of FIG. 5 or the detector circuit 86 of FIG. 6, produces a binary decision output that is coded in symbols as a result of the coding
operation of the coder circuit 104. A decoder circuit 116 decodes the symbols to produce binary data blocks and ECC blocks. An ECC decoding circuit 118 ensures that the ECC blocks indicate that no errors are present in the data bits. The binary bits that were originally input to the system 94 are available at the output of the ECC decoding circuit 118.

FIG. 8 illustrates another embodiment of the detector circuit 36. In this embodiment, the input to the detector circuit 36 is generated directly by the analog to digital (A/D) converter 52. The converter 52 can be, for example, a flash A/D converter or an equalizer with a digital filter circuit.

The input signal is an M-bit number, where M can be, for example, 6 bits for data storage channels. The M-bit number is latched into the latches 54. The outputs of the latches 54 are connected to an error output circuit 200 and a branch metric unit 202. Inputs to the branch metric unit 202 include the outputs from the latches 54 and the latches 204. The latches 204 hold $2^N$ noiseless target values, where N is the number of non-zero ISI terms remaining at the input to the detector circuit 36. The noiseless target values are M-bit numbers.

The branch metric unit 202 computes the squared distance between the M-bit digital input and all possible $2^N$ M-bit noiseless target values. Because the digital input and the noiseless target values are each M-bit numbers, 2M bits are needed to represent the squared difference without introducing truncation errors.

The outputs of the branch metric unit 202 are connected to the Viterbi circuit 64. The Viterbi circuit 64 of FIG. 8 functions as described hereinabove in conjunction with FIGS. 5 and 6.

The error output circuit 200 of FIG. 8 functions substantially the same as the error output circuit 56 of FIGS. 5 and 6. However, a multiplexer 206 is used to select one of $2^N$ noiseless target values to be output to the
latch 82. The inputs to the multiplexer 206 are the $2^N$
noiseless target values output from the latches 204 and the
output from the N-stage shift register 78.

FIG. 9 illustrates an embodiment of the branch metric
unit 202 which utilizes $2^N$ full adders 208, $2^N$ half adders
210, $2^N$ multiplexers 212, and $2^N$ logic circuits 214 to
determine the value of each branch metric. Each of the $2^N$
full adders 208 is connected in parallel with the
complement of the M-bit digital input. The other inputs to
the full adders 208 are the $2^N$ target noise values. The $2^N$
full adders 208 are used for subtraction by inverting the
digital input and holding the carry-in bit high.

In operation, the output of the left-most full adder
208 is an M+1 bit signed 2's complement of the difference
between the input and the left-most target noise value. The
2's complement output of the left-most full adder 208 is
input into the left-most half adder 210. The other input
to the left-most half adder 210 is held high. The carry-out
bit of the left-most full adder 208, the output of the
left-most full adder 208, and the output of the left-most
half adder 210, are input into the left-most of $2^N$
multiplexers 212. If the carry-out bit of the left-most
full adder 208 is a logical 0, the left-most multiplexer
212 passes on the input generated by the output of the
left-most full adder 208. If the carry-out bit of the
left-most full adder 208 is a logical 1, the left-most
multiplexer 212 passes on the input generated by the output
of the left-most half adder 210. The output of the left-
most multiplexer 212 is a 6-bit number which represents the
magnitude of the difference between the digital input to
branch metric unit 202 and the left-most target noises
value input to branch metric unit 202.

Once the magnitude of the difference is determined,
the logic circuit 214 is utilized to square the magnitude
of the difference. The number of logic circuits 214
required for this operation is related to the number of
output bits desired. A ROM storage device may also be used
to look up the squared value of a given input instead of
the logic circuit 214. The operation described above is
repeated $2^N$ times to determine the squared difference for
each $2^N$ target noise value. The branch metrics determined
by the branch metric unit 202 are output to the latches 66.

The square of an $M$-bit number is a $2M$ bit number.
Although the above embodiment passes on the full $2M$ bit
number as the branch metric, extensive simulations have
shown that passing on fewer retaining P-bits for the
squared error only marginally decreases the bit error rate.

FIG. 10 illustrates another preferred embodiment of
the branch metric unit 202 in which fewer P-bits are
retained and the squared error computation is performed for
the case of $M=6$ and $P=5$. Extensive simulations have
determined that retaining P-bits (e.g. $P=5$, the $7^{th}$ bit
through the $3^{rd}$ bit for the case of $M=6$) for the squared
error provides a sufficiently accurate bit error rate. In
operation, the modulus of the difference between the input
and the left-most noiseless target value is first obtained
as described above in conjunction with FIG. 9. This value
is then compared with the number 11 at a comparator 213.
If the modulus exceeds 11, then the square will exceed 121,
where 121 can be represented by the 7-bit number 1111001.
Ignoring the two least significant bits, the branch metric
is saturated at 30, which can be represented by the 5-bit
number 11110. If the modulus of the difference is greater
than 11, the left-most of $2^N$ multiplexers 216 passes on the
saturated branch metric of 30.

However, if the modulus of the difference is less than
the number 11, the square of that difference is determined
by the logic circuits 214. When the modulus of the
difference is not greater than 11, the left-most of $2^N$
multiplexers 216 passes on the squared difference
determined by the logic circuits 214 as the branch metric.

The above described operation is repeated $2^N$ times, one
for each target noise value. Once all of the branch
metrics are determined, the $2^N$ P-bit branch metrics are
latched in latches 217 and are output to the latches 66.

The Euclidean distance branch metric can be
approximated by a series of linear functions in the branch
metric unit 202. Approximating the Euclidean distance in
this manner reduces the cost associated with any
multiplication requirements in computing branch metric
values. The linear approximation only requires digital
left/right bit shifts and add operations to realize the
branch metric. Simulations have shown that a three line
branch metric approximation yields error rate performance
that is essentially equivalent to the Euclidean distance
branch metric.

FIG. 11 shows the Euclidean distance branch metric
approximated by three lines of slope $2^n$, where $n = -1, 1,$
and 2. Because the slopes are powers of two, each branch
metric is computed by appropriately left or right bit
shifting the digital representation of the error between
the input and the target noiseless value, then adding a
constant term. The above described computation avoids the
expense associated with multiplication.

FIGS. 12 and 13 illustrate the performance of the
linear branch metric approximation using data collected
from a spin stand. The recording head and medium were
taken from a portable IBM product released in 1998. A
write gap length of 0.25 μm and a spin valve head with read
gap 0.20μm were employed in combination with a medium whose
$H_c, MrT$ and $S^*$ were 3070 Oe, 0.54 memu/cm$^2$ and 0.79,
respectively. Data was encoded using a rate $8/9(0,4/4)$ RLL
code and write precompensation was applied. Oversampled
data was collected using a high-speed digitizing
oscilloscope. The linear velocity of the medium was 443.2
inches / second (1125.7 cm/second).

Traces labeled with the suffixes L3, L2 and L1 denote
three-line, two-line and single-line approximations,
respectively, to the Euclidean distance branch metrics in
the VA. The three-line approximation (L3) used is that
depicted in FIG. 11. Two two-line approximations (L2) were
invoked. One approximation was the lines expressed by
0.51x_k-a_k1 and 2.01x_k-a_k1 - 0.9. This approximation very
closely matches the Euclidean distance metric for low
values of lx_k-a_k1 (see FIG. 11). Since lx_k-a_k1 is, in some
sense, a measure of the noise in the channel (i.e. if noise
variance is low, low values of lx_k-a_k1 are expected), it is
expected that this approximation will perform well at
higher SNR (lower lx_k-a_k1). For this reason it was invoked
at the higher SANRs of 28 dB and 29.5 dB. The other two-
line approximation invoked was that consisting of the lines
lx_k-a_k1 and 4.01x_k-a_k1 - 3.6. This approximation is a better
match to the Euclidean distance metric over a wider range
of lx_k-a_k1. This is required at lower SNR, where the noise
variance is large and values of lx_k-a_k1 can vary widely.
For this reason this approximation was invoked at the lower
SANRs of 22 dB, 24 dB and 26 dB. Finally, the single-line
approximation (L1) invoked at all SANRs was lx_k-a_k1.

FIGS. 12 and 13 reveal that the three-line
approximation yields error rate performance that is
essentially equivalent to the Euclidean distance branch
metric. In addition, the two line approximations in
conjunction with the adapted length-4 monic GPR target
yield performance exceeding that of the Euclidean distance
metric applied to the class IV PR target of EPR4. The
improvement, in terms of SNR, is between 1 dB and 2 dB for
both PWS50/T=3.25 and PWS50/T=3.50 channels. The single-line
approximation, however, lags behind EPR4 in the lower-
density channel at higher SANRs but exceeds EPR4 in the
higher-density channel.

The effective SNR gain provided by the GPR targets is
gradually offset by the mischaracterization of the noise
implied by the linear metric approximation. The Euclidean-
distance metric VA is the maximum likelihood receiver for
uncorrelated Gaussian noise. By employing a linear
approximation in place of the Euclidean distance branch
metric, the noise is effectively characterized as having a
probability density function (pdf) that is something other than Gaussian. For example, the single-line branch metric approximation given by the line $|x_k - a_k|$ would be optimal if the pdf of the noise was exponential. Assuming the noise is truly Gaussian, the most valid linear branch metric approximations will imply noise pdfs that approach Gaussian pdfs.

FIG. 14 illustrates an embodiment of a portion of the branch metric unit 202 of FIG. 8. The branch metric unit 202 computes the branch metric using the techniques described hereinabove in conjunction with FIGS. 11-13. The portion of the branch metric unit includes adders 220, multiplexers 222, inverters 224, and gate 226.

While the present invention has been described in conjunction with preferred embodiments thereof, many modifications and variations will be apparent to those of ordinary skill in the art. The foregoing description and the following claims are intended to cover all such modifications and variations.
CLAIMS
What is claimed is:

1. A detector circuit for detecting a data sequence from an input sequence of data, comprising:
   a branch metric unit for computing a plurality of values, the values corresponding to the squared errors between input values to the circuit and all possible noiseless responses; and
   a Viterbi circuit responsive to the branch metric unit, the Viterbi circuit for computing the data sequence.

2. The circuit of claim 1 wherein the Viterbi circuit comprises:
   a Viterbi add/compare/select circuit responsive to the branch metric unit, the add/compare/select circuit for computing a plurality of acs decisions; and
   a Viterbi trace-back circuit responsive to the Viterbi add/compare/select circuit, the Viterbi trace-back circuit for computing the data sequence.

3. The circuit of claim 1 further comprising an error output circuit, the error output circuit responsive to the input sequence of data and the Viterbi circuit, the circuit for producing an error output value.

4. The circuit of claim 3 wherein the error output circuit comprises:
   a multiplexer responsive to the noiseless responses and the Viterbi circuit;
   a delay circuit for producing a delayed input value from the input sequence of data; and
   a circuit responsive to the multiplexer and the delay circuit, the circuit for subtracting the delayed input value from a noiseless value selected by the multiplexer to produce an error output.

5. The circuit of claim 4 further comprising:
   a shift register responsive to the Viterbi circuit, the output of the shift register connected to the multiplexer; and
a latch responsive to the multiplexer, the output of the latch connected to the circuit.

6. The circuit of claim 2 further comprising a plurality of latches responsive to the branch metric unit, the output of the latches connected to the Viterbi add/compare/select circuit, the latches for pipelining the squared errors to the Viterbi add/compare/select circuit.

7. The circuit of claim 6 further comprising a second plurality of latches responsive to the Viterbi add/compare/select circuit, the output of the second latches connected to the Viterbi trace-back circuit.

8. The circuit of claim 7 further comprising a latch, the latch responsive to the Viterbi trace-back circuit.

9. The circuit of claim 1 further comprising:
   an analog to digital converter circuit responsive to the input data sequence; and
   a plurality of latches responsive to the analog to digital converter circuit, the outputs of the latches connected to the branch metric unit.

10. A combination, comprising:
    a filter for filtering an analog input signal to produce a filtered signal;
    a sampling circuit responsive to the filter, the sampling circuit for producing a sampled signal from the filtered signal;
    a forward equalizer responsive to the sampling circuit, the forward equalizer for producing a target response signal from the sampled signal; and
    a detector circuit responsive to the forward equalizer, the detector circuit comprising:
        a branch metric unit for computing a plurality of values, the values corresponding to the squared errors between input values to the circuit and all possible noiseless responses; and
a Viterbi circuit responsive to the branch metric unit, the Viterbi circuit for computing a binary decision output.

11. The combination of claim 10 wherein the detector circuit further comprises an error output circuit, the error output circuit responsive to the input sequence of data and the Viterbi circuit, the circuit for producing an error output value.

12. The combination of claim 11 wherein the error output circuit comprises:
   a multiplexer responsive to the noiseless responses and the Viterbi circuit;
   a delay circuit for producing a delayed input value from the input sequence of data; and
   a circuit responsive to the multiplexer and the delay circuit, the circuit for subtracting the delayed input value from a noiseless value selected by the multiplexer to produce an error output.

13. A combination, comprising;
   a continuous time equalizer for filtering an input analog signal and generating a target response signal;
   a sampling circuit responsive to the continuous time equalizer, the sampling circuit for producing a sampled signal from the target response signal; and
   a detector circuit responsive to the sampling circuit, the detector circuit comprising:
   a branch metric unit for computing a plurality of values, the values corresponding to the squared errors between input values to the circuit and all possible noiseless responses; and
   a Viterbi circuit responsive to the branch metric unit, the Viterbi circuit for computing a binary decision output.

14. The combination of claim 13 wherein the detector circuit further comprises an error output circuit, the error output circuit responsive to the input sequence of
data and the Viterbi circuit, the circuit for producing an
error output value.

15. The combination of claim 14 wherein the error
output circuit comprises:

5 a multiplexer responsive to the noiseless
responses and the Viterbi circuit;

a delay circuit for producing a delayed input
value from the input sequence of data; and

a circuit responsive to the multiplexer and the
delay circuit, the circuit for subtracting the delayed
input value from a noiseless value selected by the
multiplexer to produce an error output.

16. A magnetic data recording system having a
head/disk assembly, comprising:

15 a write circuit for converting a sequence of data
bits that are to be written onto a recording medium in the
head/disk assembly to a recording signal;

a preamplifier for filtering a signal that is
read from the recording medium;

an equalizer responsive to the preamplifier, the
equalizer for producing a target response signal from the
filtered signal;

a detector circuit responsive to the equalizer,
the detector circuit comprising:

25 a branch metric unit for computing a
plurality of values, the values corresponding to the
squared errors between input values to the circuit and
all possible noiseless responses; and

a Viterbi circuit responsive to the branch
metric unit, the Viterbi circuit for computing a
binary decision output;

a decoder circuit responsive to the detector
circuit, the decoder circuit for decoding the binary
decision output to produce binary data blocks and
error correction code data blocks; and

an error correction code decoding circuit
responsive to the decoder circuit.
17. A method for detecting a data sequence from an input sequence of data, comprising the steps of: 

computing a plurality of values in response to the input sequence of data, the values corresponding to the squared errors computed between the input values and all possible noiseless responses; and 

detecting the data sequence using a Viterbi Algorithm in response to the plurality of retrieved values.

18. The method of claim 17, wherein computing a plurality of values includes approximating a Euclidean branch metric with a series of linear functions.
FIG. 9
Target Valves

COut  1  224
      break 1

COut  226

1/2n  "0"  1/2n-1

222

220

1  224
offset 1

1  224
offset 2

"0"  1/2n-1  222

Branch Metric

Σ

FIG. 14

SUBSTITUTE SHEET (RULE 26)
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11B20/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03M G11B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, COMPENDEX, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Date of the actual completion of the international search
22 August 2000

Date of mailing of the international search report
06/09/2000

Name and mailing address of the ISA
European Patent Office, P.B. 5816 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo.nl, Fax (+31-70) 340-3016

Authorized officer
Berbain, F

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